Mini Analog Baseband Power Management IC

General Description

The RT8966H is an analog subsystem which includes a linear charger, 4 LDOs, a 4-CH current source, and a multiplexer for USB, UART, microphone, stereo and audio on a single mini/micro USB connector.

The RT8966H adopts an I^2C bus for control and uses an internal method to determine the connected device.

The USB input provides high speed USB connection. The audio inputs feature negative rail signal operation to realize simple DC coupled headset speakers. The RT8966H provides an internal device detection method by using the USB ID signal pin and the VBUS voltage. The resistor values and VBUS voltage determine the unique detection method of each accessory. The host microprocessor adopts I^2C to control the switch position and read the results of the accessory detection. The RT8966H can also detect USB chargers, including dedicated chargers (D+/D– shorted) and high, power, host/hub chargers.

The RT8966H has a linear charger with maximum 1A current capability. The charging current and end of charge current can be controlled by I^2C interface. It also provides a 50mA LDO to support the power of the peripheral circuit. In factory mode, the RT8966H provides 4.35V/2.3A power to support system operation.

The RT8966H is available in a thin WQFN-32L 4x4 package.

Ordering Information

RT8966H □□

- Package Type
  QW : WQFN-32L 4x4 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

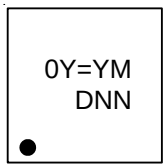
Features

- **Hi-Speed USB Operation**
- **Interrupt for Device Insertion and Removal**
- **Interrupt for SEND/END Button Detection**
- **Interrupt for Protection Function**
- **Low Power Microphone Standby Mode**
- **Default Startup Mode for Factory Support**
- **Negative Rail Audio Signal Paths**
- **Internal LDO for Low Noise Microphone Bias**
- **28V Maximum Rating for DC Adapter**
- **Internal Integrated Power MOSFETs of Charger**
- **Support 4.35V/2.3A Factory Mode**
- **I^2C Controlled Interface**
- **4 Current Sources with 32-Steps Current Setting**
- **4 LDOs with Programmable Output Voltage**
- **Thin 32-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Cellular Phone
- Smart Handheld Device

Marking Information

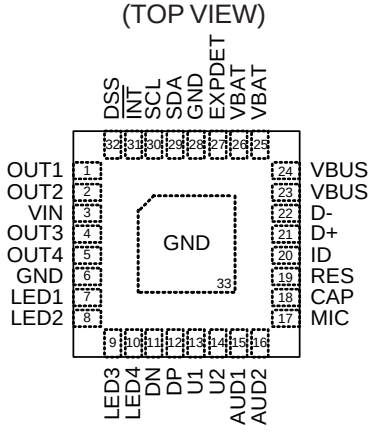


0Y= : Product Code

YMDNN : Date Code

Pin Configurations

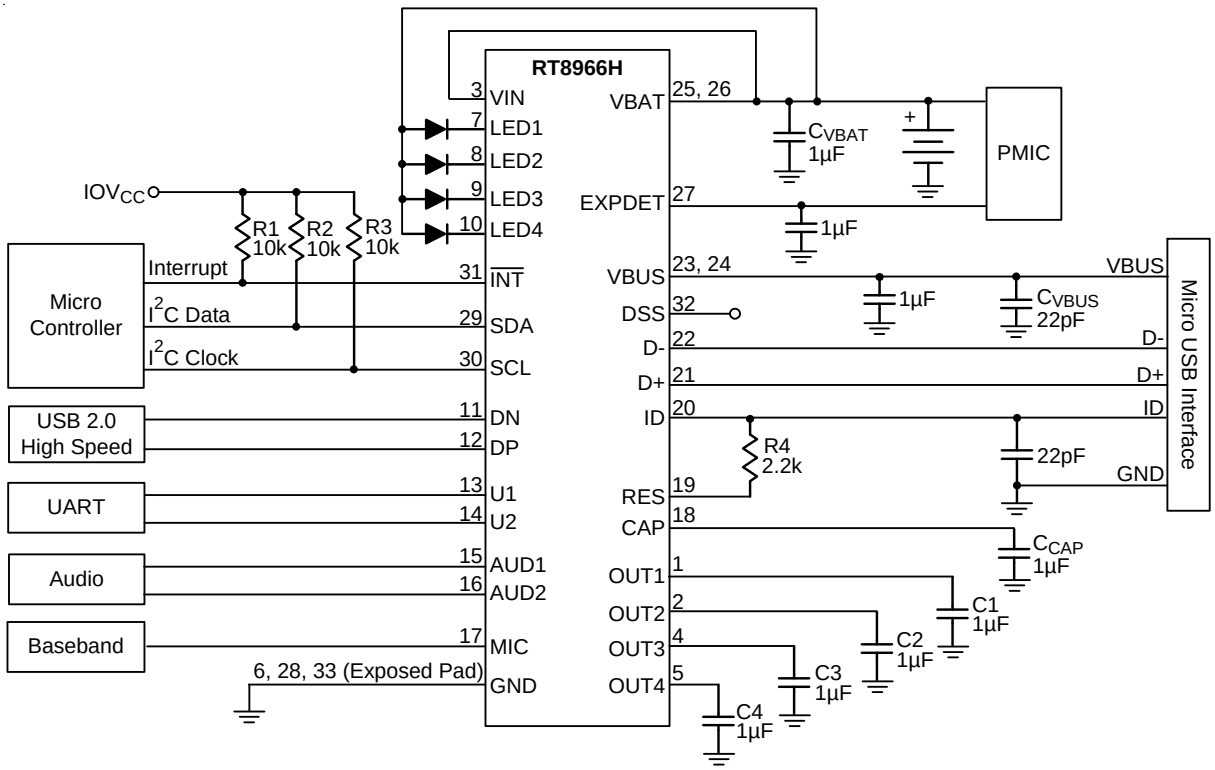
(TOP VIEW)



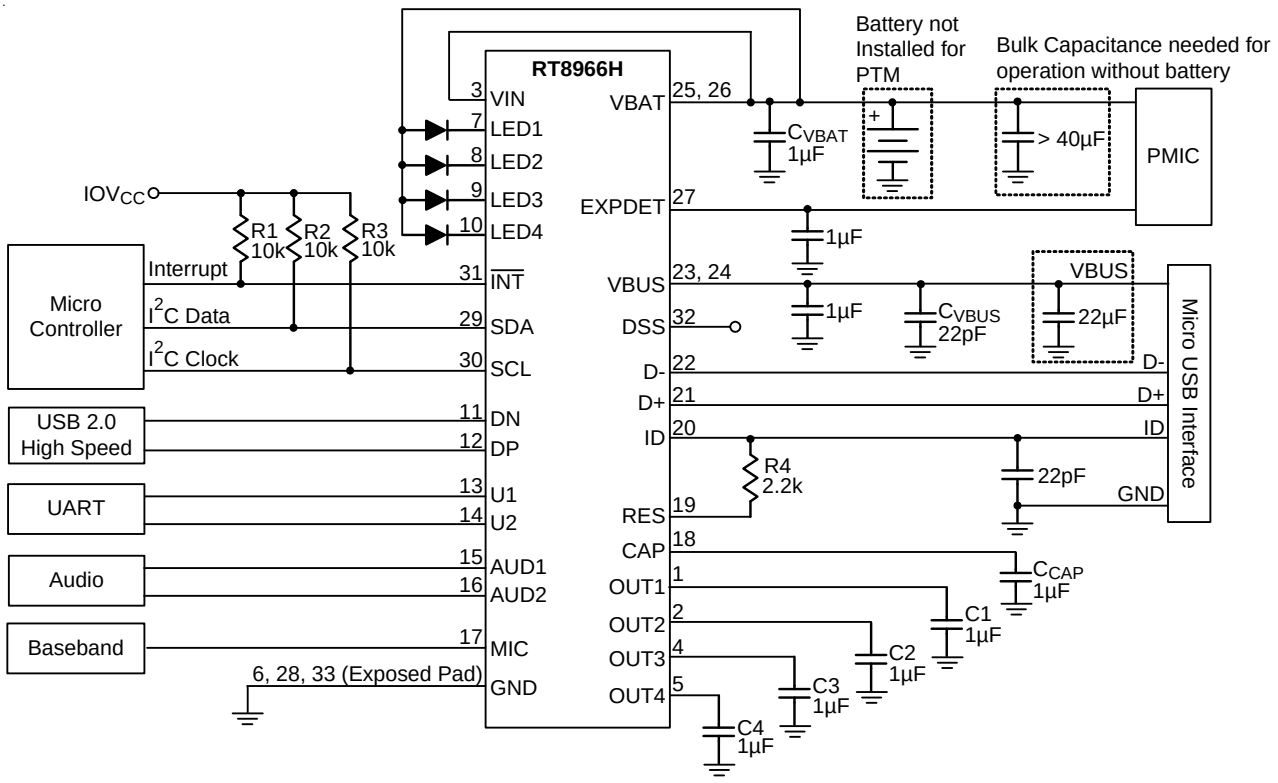
WQFN-32L 4x4

Typical Application Circuit

Typical Application Circuit with Battery Installed :



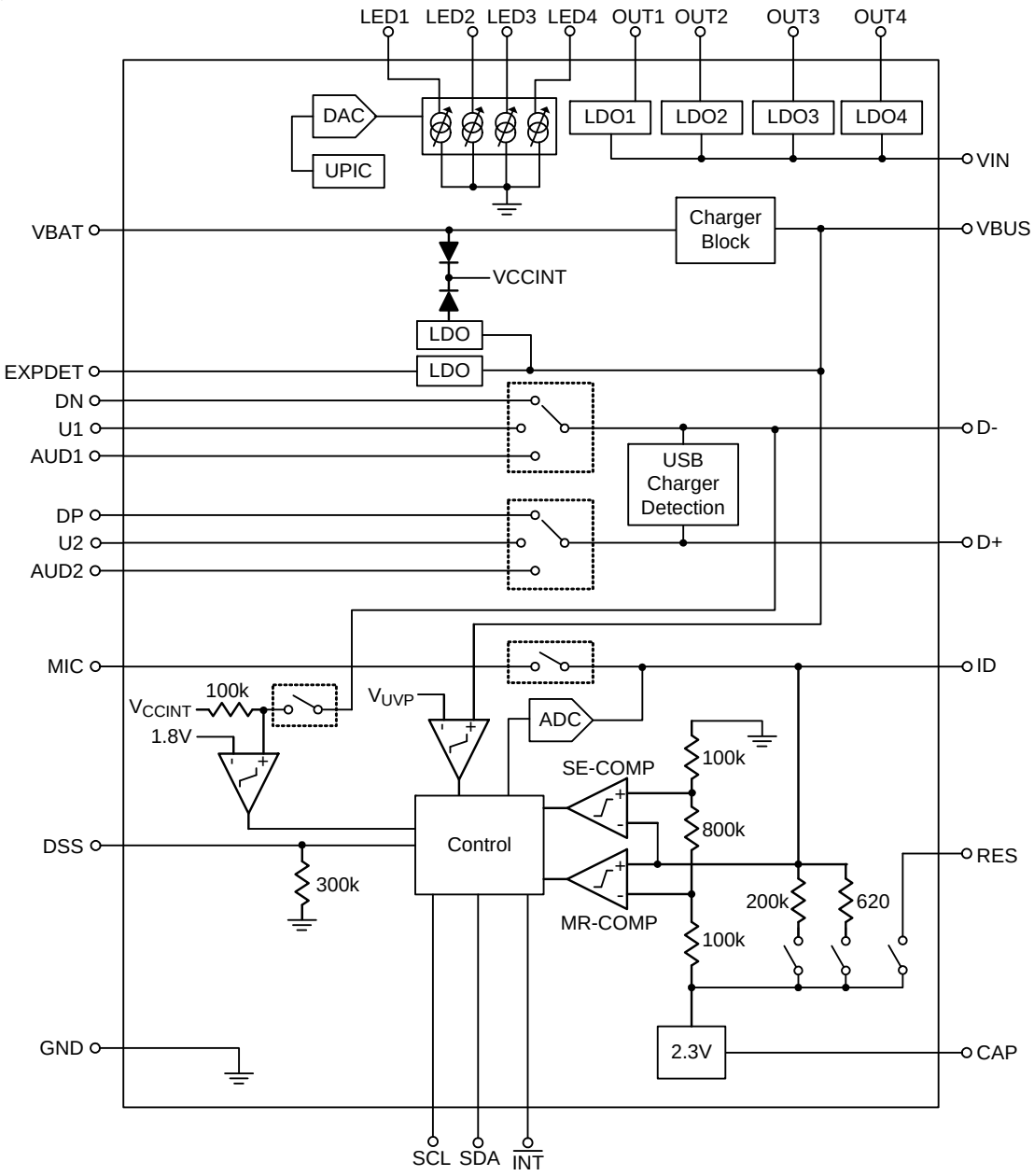
Typical Application Circuit for Factory Mode with no Battery Installed :



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	OUT1	LDO1 Output Voltage.
2	OUT2	LDO2 Output Voltage.
3	VIN	LDO Input Power Supply.
4	OUT3	LDO3 Output Voltage.
5	OUT4	LDO4 Output Voltage.
6, 28, 33 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
7	LED1	LED1 Current Source Output.
8	LED2	LED2 Current Source Output.
9	LED3	LED3 Current Source Output.
10	LED4	LED4 Current Source Output.
11	DN	USB Inout1 for D−.
12	DP	USB Input2 for D+.
13	U1	UART/USB Full Speed Input1.
14	U2	UART/USB Full Speed Input2.
15	AUD1	Stereo Audio Input1. (Negative rail capable).
16	AUD2	Stereo Audio Input2. (Negative rail capable).
17	MIC	Microphone Input.
18	CAP	Internal LDO Output. Connect a 1μF ceramic (X5R, X7R or better) capacitor between CAP and GND. Do not use CAP to power other circuitry.
19	RES	External Microphone Bias Resistor. Connect a resistor (typical 2.2kΩ) between RES and UlD line.
20	ID	USB lD Input. Connect to lD on mini/micro USB connector.
21	D+	Common Output2.Connect to D+ on min/micro USB connector.
22	D-	Common Output1.connect to D- on mini/micro USB connector.
23, 24	VBUS	USB VBUS Input. Provides power for internal circuitry in the case $V_{BAT} < V_{BUS}$ and used to sense presence of voltage on USB VBUS.
25, 26	VBAT	Power Supply Input. Connect to Li-ion battery or other voltage source.
27	EXPDET	LDO Output (4.9V). This pin provides 50mA output current.
29	SDA	I^2C Serial Data Input/Output. Connect to an external pull up resistor.
30	SCL	I^2C Serial Clock Input. Connect to an external pull up resistor.
31	$\overline{INT}$	Interrupt Output-Open Drain. Connect to an external pull up resistor.
32	DSS	Multiple Use Pin. Used to set Default Startup mode based on dc voltage when power is applied.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- VBUS ---------- –0.3V to 28V
- All Other Inputs ---------- –0.3V to (V_{IN} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-32L 4x4 ---------- 3.59W
- Package Thermal Resistance (Note 2)
  WQFN-32L 4x4, θ_{JA} ---------- 27.8°C/W
  WQFN-32L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Battery Supply Voltage Range, VBAT ---------- 2.8V to 5.5V
- USB Supply Voltage Range, VBUS ---------- 4.3V to 6.7V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{BAT} = 3.7V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
DC Characteristics							
VBUS OVP Threshold Voltage	V_{OVP}			6.7	6.9	7.1	V
VBUS UVP Threshold Voltage	V_{UVP}			3.5	3.7	3.9	V
OTP		(Note 5)		--	135	--	°C
OTP Hysteresis		(Note 5)		--	10	--	°C
Internal Switch Supplies	V_{SWPOS}	(Note 5)		--	3.4	--	V
	V_{SWNEG}	(Note 5)		--	–1.9	--	
VBAT UVLO	V_{UVLO_BAT}			2.1	2.5	2.8	V
ID LDO Voltage	V_{LDO}	V_{BAT} = 3.5V	I^2C bit : V_{LDO} = 0	2.5	2.6	2.7	V
			I^2C bit : V_{LDO} = 1	2.2	2.3	2.4	
ID LDO PSRR	$PSRR_{LDO}$	VLDO = 1, V_{BAT} = 3.3 ± 0.2V, f = 217Hz, I_{ID} = 100μA (Note 5)		--	90	--	dB
ID LDO Noise	N_{LDO}	ID_2P2 = 1, MICLP = 0, f = 400Hz to 4kHz, I_{LOAD} = 100μA (Note 5)		--	5	--	μV_{RMS}
VBAT Supply PSRR	$PSRR_{VBAT}$	Noise from V_{BAT} to D-, D+, or ID, R_L = 50Ω; f = 10kHz, V_{BAT} = 3.5 ± 0.2V (Note 5)		--	80	--	dB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBAT Leakage Current	I_{VBAT_L}	V_{BAT} = 4.5V, V_{BUS} = 0V, CP_EN = 0, ADCEN = 0, SEMREN = 0; ID_200 = 0, ID_620 = 0, ID_2P2 = 0, CHG_OFF = 1, CHG_EN = 0, SCL = 0, SDA = 0	--	10	15	μA
VBAT Supply Current	I_{VBAT_S}	V_{BAT} = 4.5V, V_{BUS} = 0V, V_{ID} = 0V, CP_EN = 1 and either ADCEN = 1 or SEMREN = 1, ID_620 = 0, ID_2P2 = 0, ID_200 = 0, CHG_OFF = 1, CHG_EN = 0	--	44	--	μA
VBUS Supply Current	I_{VBUS}	V_{BUS} = 5V, V_{BAT} = 4.5V, V_{ID} = 0V, CP_EN = 1, either ADCEN = 1 or SEMREN = 1, ID_2P2 = 0, ID_620 = 0 CHG_OFF = 1, CHG_EN = 0, ID_200 = 0	--	168	211	μA
D- Pull up Resistor	R_{D-DET}	V_{D-} = 0V	63	106	332	kΩ
D- Comparator Threshold	V_{D-DET}		0.86	1.8	2.83	V
Default Startup Switch Position Comparator Threshold	V_{DSP}	Measured at IC	--	1	--	V
Default Startup Switch Position Pull down Resistor	R_{DSP}	Measured at IC	130	273	660	kΩ
Microphone Removal Threshold	V_{MRCOMP}	In Percent of LDO voltage	85	--	95	%
SEND/END Threshold	V_{SECOMP}	In Percent of LDO voltage	5	--	15	%
VDAT_SRC Voltage	V_{DAT_SRC}	With IDAT_SRC = 0 to 200μA	0.5	--	0.7	V
VDAT_REF Voltage	V_{DAT_REF}		0.25	--	0.4	V
VLGC Voltage	V_{LGC}		0.8	--	2	V
IDATA_SINK Current	I_{DAT_SINK}	May be a resistance if desired	50	--	150	μA
IDPU1 Resistance	R_{IDPU1}		--	200	--	kΩ
IDPU2 Resistance	R_{IDPU2}		--	620	--	Ω
RCD Resistance	R_{CD}		200	--	600	kΩ
ADC Detection Resistors	R_{ADC}	GND	--	--	5	kΩ
		R1	--	24	--	
		R2	--	56	--	
		R3	--	100	--	
		R4	--	130	--	
		R5	--	180	--	
		R6	--	240	--	
		R7	--	330	--	
		R8	--	430	--	
		R9	--	620	--	
		R10	--	910	--	
		Open	1600	--	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
USB Analog Switch (DN1, DP2)						
Analog Signal Range	V_{DN1}, V_{DP2}	CP_EN = 0	0	--	V_{CCINT}	V
		CP_EN = 1	V_{SWNEG}	--	V_{SWPOS}	
On-Resistance	$R_{DS(ON)\_USB}$	V_{BAT} = 3V, CP_EN = 1, I_{COMx} = 10mA, V_{COMx} = 0V to 3V	--	3	--	Ω
On-Resistance Match Between Channels	$\Delta R_{DS(ON)\_USB}$	V_{BAT} = 3V, CP_EN = 1, I_{COMx} = 10mA, V_{COMx} = 400mV	--	0.5	--	Ω
Off Leakage Current	I_{USB_Off}	V_{BAT} = 4.35V, Switch open, V_{DN1} or V_{DP2} = 0.3V, 2.5V, V_{COMx} = 2.5V, 0.3V	–360	--	360	nA
On Leakage Current	I_{USB_On}	V_{BAT} = 4.35V, Switch closed, V_{DN1} or V_{DP2} = 0.3V, 2.5V	–360	--	360	nA
UART/USB Analog Switch (U1, U2)						
Analog Signal Range	V_{U1}, V_{U2}	CP_EN = 0	0	--	V_{CCINT}	V
		CP_EN = 1	V_{SWNEG}	--	V_{SWPOS}	
On-Resistance	$R_{DS(ON)\_UART}$	V_{BAT} = 3V, CP_EN = 1, I_{COMx} = 10mA, V_{COMx} = 0V to 3V	--	12	--	Ω
On-Resistance Match Between Channels	$\Delta R_{DS(ON)\_UART}$	V_{BAT} = 3V, CP_EN = 1, I_{COMx} = 10mA, V_{COMx} = 1.5V	--	5	--	Ω
Off Leakage Current	I_{UART_Off}	V_{BAT} = 4.35V, Switch open, V_{U1} or V_{U2} = 0.3V, 2.5V, V_{COMx} = 2.5V, 0.3V	–360	--	360	nA
On Leakage Current	I_{UART_On}	V_{BAT} = 4.35V, Switch closed, V_{U1} or V_{U2} = 0.3V, 2.5V	–360	--	360	nA
MIC Analog Switch (MIC)						
Analog Signal Range	V_{MIC}	CP_EN = 0	0		V_{CCINT}	V
		CP_EN = 1	V_{SWNEG}		V_{SWPOS}	
On-Resistance	$R_{DS(ON)\_M}$	V_{BAT} = 3V, CP_EN = 1, I_{MIC} = 10mA, V_{MIC} = 0V to 3V	--	3.4	10	Ω
On-Resistance Flatness	R_{FLATM}	V_{BAT} = 3V, CP_EN = 1, I_{MIC} = 10mA, V_{MIC} = 0V to 3V (Note 5)	--	0.1	--	Ω
Off Leakage Current	I_{LM_Off}	V_{BAT} = 4.35V, Switch open, V_{MIC} = 0.3V, 2.5V, V_{ID} = 2.5V, 0.3V	–360	--	360	nA
On Leakage Current	I_{LM_On}	V_{BAT} = 4.35V, Switch closed, V_{MIC} = 0.3V, 2.5V	–360	--	360	nA
Audio Analog Switch (AUD1, AUD2)						
Analog Signal Range	V_{AUDIO}	CP_EN = 0	0	--	V_{CCINT}	V
		CP_EN = 1	V_{SWNEG}	--	V_{SWPOS}	
On-Resistance	$R_{DS(ON)\_A}$	V_{BAT} = 3V, CP_EN = 1, I_{COMx} = 10mA, V_{COMx} = –2V to 3V	--	4	--	Ω
On-Resistance Match Between Channels	$\Delta R_{DS(ON)\_A}$	V_{BAT} = 3V, CP_EN = 1, I_{COMx} = 10mA, V_{COMx} = 0V	--	0.2	--	Ω
On-Resistance Flatness	R_{FLATA}	V_{BAT} = 3V, CP_EN = 1, I_{COMx} = 10mA, V_{COMx} = –0.5 to 0.5V (Note 5)	--	1	--	Ω

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
Off Leakage Current		$I_{LA\_(OFF)}$	V_{BAT} = 4.35V, Switch Open, V_{AUDx} = –0.5V to 0.5V, V_{COMx} = –0.5V to 0.5V		–360	--	360	nA
On Leakage Current		$I_{LA\_(ON)}$	V_{BAT} = 4.35V, Switch Closed, V_{AUDx} = –0.5V, 2V		–360	--	360	nA
Shunt Resistor		R_{SHUNT}			30	100	200	Ω
Digital Signals (DSS, SCL, SDA)								
DSS, SCL, SDA Input Voltage Threshold	Logic-High	V_{IH}			1.4	--	--	V
	Logic-Low	V_{IL}			--	--	0.4	
Input Leakage Current		I_{INLEAK}			–1	--	1	μA
Open Drain Low		V_{ODOL}	I_{SINK} = 1mA		--	--	0.4	V
DYNAMIC								
I^2C Max Clock		f_{I2CCLK}			--	--	400	kHz
MIC_LP Detection Pulse Time		$t_{MICLPDP}$	MIC_LP = 1, SEMREN = 1		--	120	--	μs
MIC_LP Detection Period		t_{MICLPD}	MIC_LP = 1, SEMREN = 1		--	120	--	ms
CP_EN Delay Time		t_{CP_EN}	Not production tested		--	--	1	ms
Analog Switch Turn On Time		t_{ON}	I^2C Stop to Switch On; R_L = 50Ω		--	--	1	ms
Analog Switch Turn Off Time		t_{Off}	I^2C Stop to Switch Off; R_L = 50Ω		--	--	1	ms
Break-Before-Make Delay Time		t_D	R_L = 50Ω (Note 5)		>0	--	--	μs
Charger Debounce Time		$t_{CHGR\_DET\_DBNC}$			20	--	40	ms
VDAT_SRC ON Time		$t_{DP\_SRC\_ON}$			100	--	200	ms
VDAT_SRC OFF To ISET enable		$t_{DPSRC\_HICHRNT}$			40	--	80	ms
Debounce Time		t_{MDEB}	All Comparators		20	--	500	ms
Off-Isolation		V_{ISO}	R_L = 50Ω, f = 20kHz, V_{COMx} = 0.5Vp-p (Note 5)	DN1, DP2	--	–60	--	dB
				U1, U2	--	–60	--	
				AUD1, AUD2	--	–60	--	
				MIC	--	–60	--	
Cross-talk		V_{CT}	R_L = 50Ω, f = 20kHz, V_{COMx} = $1V_{RMS}$ (Note 5)		--	–115	--	dB
Total Harmonic Distortion		THD	f = 20Hz to 20kHz, V_{COMx} = 0.5Vp-p, R_L = 50Ω; DC bias=0 (Note 5)	MIC	--	0.05	--	%
				Audio	--	0.05	--	
Battery Charger								
VBUS-VBAT VOS Rising					--	75	150	mV
VBUS-VBAT VOS Falling					18	32	--	mV
DPM Regulation Voltage		V_{DPM}			3.9	3.95	4	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBAT Regulation Voltage		T_A = 0°C to 85°C	4.307	4.35	4.393	V
Thermal Regulation		(Note 5)	--	125	--	°C
Pre-Charge Threshold	V_{PRECH}	VBAT Rising	2.5	2.6	2.7	V
Pre-Charge Current Accuracy			--	10	--	mA
Fast-Charge Current Accuracy			--	5	--	%
Fast-Charge to Pre-Charge Deglitch Time			--	25	--	ms
VBUS Power FET $R_{DS(ON)}$		I_{BAT} = 1A	--	250	500	mV
LDO $R_{DS(ON)}$			--	3	6	Ω
LDO Output Voltage			4.75	4.9	5.05	V
LDO Maximum Output Current			60	120	180	mA
Factory Mode V_{OUT}		C_{VBUS} = 22μF, C_{VBAT} > 40μF	4.263	4.35	4.437	V
Factory Mode Maximum Output Current			2.3	--	--	A
Linear Regulator						
LDO Output Voltage		Setting OUTx = 3.3V	3.2	3.3	3.4	V
Output Current	$I_{OUT-LDO}$		300	--	--	mA
Drop Out Voltage	$I_{DROP-LDO}$	V_{IN} = OUTx – 100mV / I_{OUTx} = 100mA	--	0.13	--	V
Supply Current	I_{Q-LDO}	V_{IN} = 4.2V / I_{OUTx} = 0mA	--	20	--	μA
Power Supply Rejection Ratio	$PSRR_{LDO}$	(Note 5)	--	70	--	dB
LED Current Source						
LED Quiescent Current	I_{Q-LED}		--	100	--	μA
Maximum LED Current	$I_{LED(MAX)}$		--	30	--	mA
LED Current Accuracy	ΔI_{LED}	Setting I_{LED} = 20mA	--	5	--	%
LED Current Match			--	5	--	%

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

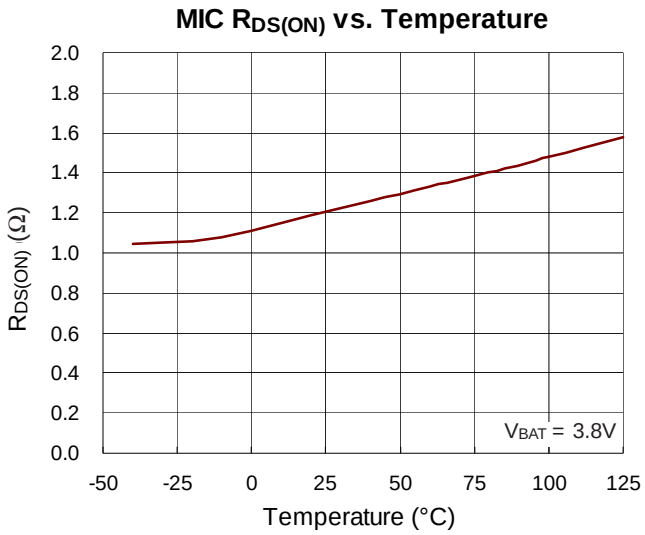
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

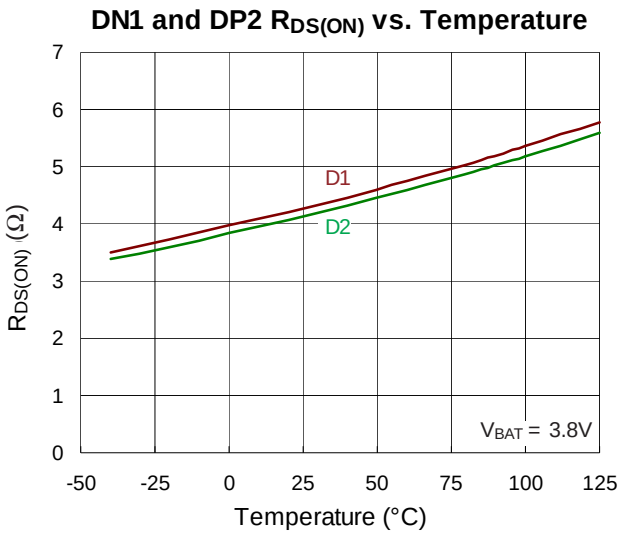
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

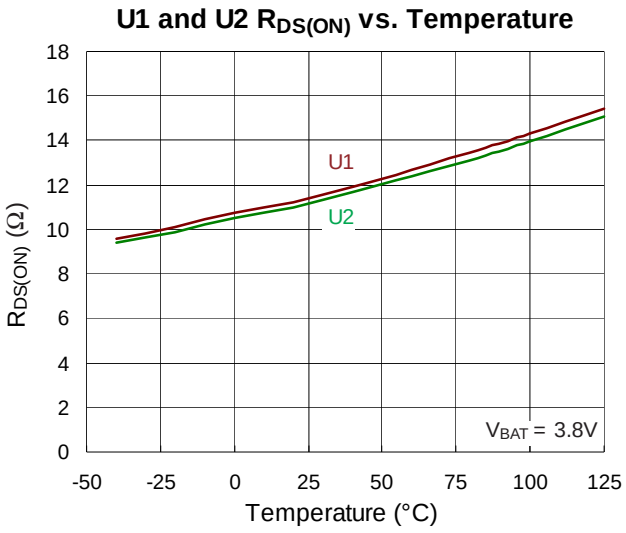
Note 4. The device is not guaranteed to function outside its operating conditions.

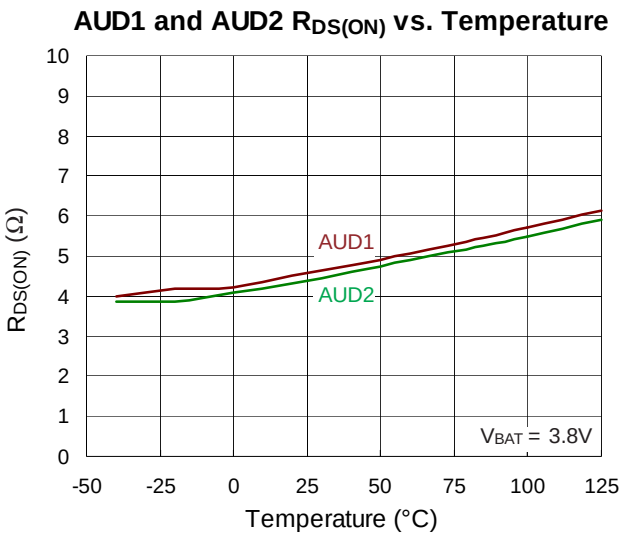
Note 5. Guaranteed by Design.

Typical Operating Characteristics









Application Information

Charger Description

The RT8966H integrates a single-cell Li-ion battery charger IC with pre-charge mode, a fast charge mode (constant current mode) or constant voltage mode. The charge current is programmable via the I^2C interface as shown in the control register address tables, CHG_Ctrl1 and CHG_Ctrl2. The CV mode voltage is fixed at 4.35V. The pre-charge threshold is fixed at 2.6V. If the battery voltage is below the pre-charge threshold, the RT8966H charges the battery with a trickle current until the battery voltage rises above the pre-charge threshold. The RT8966H is capable of being powered up from AC adapter and USB (Universal Serial Bus) port inputs. Moreover, the RT8966H includes a linear regulator (LDO 4.9V, 50mA) for supplying low power external circuitry.

Charger Over Voltage Protection

The input voltage is monitored by the internal comparator and the input over voltage protection threshold is set to 6.9V. However, input voltage over 28V will still cause damage to the RT8966H. When the input voltage exceeds the threshold, the comparator outputs a logic signal to turn off the power P-MOSFET to prevent high input voltage from damaging the electronics in the handheld system. When the input over voltage condition is removed, the comparator re-enables the output by running through soft-start.

Battery Charge Profile

Pre-Charge Mode :

Figure 1 shows the RT8966H charging state of the charging function. During a charge cycle, if the battery voltage is below the V_{PRECH} threshold (typical value is 2.6V), the charger enters pre-charge mode. This feature revives deeply discharged cells and protects battery life. The pre-charge current has a typical value of 50mA.

Constant Current Mode :

Once the battery voltage is higher than 2.6V, the charger enters the constant current stage. The constant current level can be programmed from 90mA to 1A via the I^2C compatible interface but the default value is 400mA.

Constant Voltage Mode :

Once the battery voltage level closes in at 4.35V, the charger enters constant voltage phase and the charging current begins to decrease. When the charging current becomes lower than I_{EOC} (end of charge current), the loop enters charge done mode.

The RT8966H will then send an interrupt and register CHG bit, as shown in Table 10. Finally, INT_STA2 becomes 0 to indicate that the RT8966H has completed the charging.

Recharge Phase :

When any loading or event causes V_{BAT} to drop or battery to discharge, the charger will automatically jump to the appropriate mode to recharge the battery.

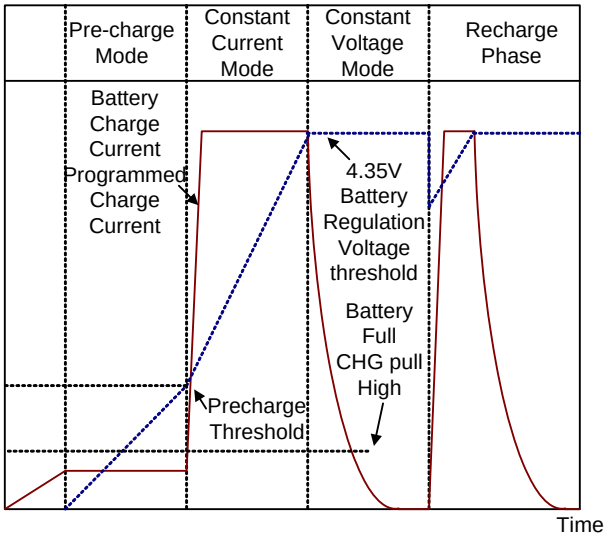


Figure 1. Charging State of the Charger Function

Charger for Factory Mode

The RT8966H provides factory mode for supplies up to 2.3A for powering external loads with no battery installed and V_{BAT} is regulated to 4.35V. The factory mode allows the user to supply system power with no battery connected. It is programmable by I^2C via the PTM bit, as shown in Table 13.

In factory mode, thermal regulation is disabled, but thermal protection (135°C) is still active. When using currents greater than 1.5A in factory mode, the user must limit the duty cycle at the maximum current to 20% with a maximum period of 10ms.

Charger Sleep Mode

The RT8966H enters sleep mode if the power is removed from the input. This feature prevents draining the battery during absence of input supply.

Charger Temperature Regulation and Thermal Protection

In order to maximize charge rate, the RT8966H features a junction temperature regulation loop. This allows the RT8966H to limit the charge current in order to maintain a junction temperature around the thermal regulation threshold (125°C). The RT8966H monitors the junction temperature, T_J, of the die and disconnects the battery from the input if T_J exceeds 125°C. This operation continues until junction temperature falls below thermal regulation threshold (125°C) by the hysteresis level. This feature prevents maximum power dissipation from exceeding typical design conditions.

Charger Input and Output Capacitors Selection

For most applications, a high frequency decoupling capacitor place near the input is usually sufficient. A 1μF ceramic capacitor, should work well. However, in other applications, depending on the power supply characteristics and cable length, it may be necessary to add an additional 10μF ceramic capacitor to the input.

The RT8966H also requires a small output capacitor for loop stability. A typical 1μF ceramic capacitor placed between the VBATT pin and GND is sufficient.

Input DPM Mode

When USB sources are selected, the input voltage, VBUS, is monitored. If VBUS falls to VDPM, the input current limit is reduced to prevent the input voltage from falling further. This prevents the IC from crashing poorly designed or incorrectly configured USB sourced.

EXPDET Linear Regulator

The RT8966H integrates one low dropout linear regulator (LDO) that supplies up to 50mA of output current. The LDO can be enabled by I^2C via the EXTPDET bit, as shown in Table 13. Note that the LDO current is independent and not monitored by the charge current limit.

Linear Regulator

There are four LDOs in the RT8966H. These LDOs can be programmed via I^2C in the following control registers Enable, OUT Set1, OUT Set2. These registers include each LDO's enable/disable control as well as its output voltage selection from 1V to 3.3V.

Linear Regulator Capacitor Selection

In order to maintain regulator stability and performance, better quality ceramic capacitor, such as X7R/X5R, should be selected.

Like any low-dropout regulator, the external capacitors used with the RT8966H must be carefully selected for regulator stability and performance. Use a capacitor with value larger than 1μF on the RT8966H input. The amount of capacitance can be increased without limit. The input capacitor should be located at a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. A capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet requirements for both minimum amount of capacitance and ESR in all LDOs application. The RT8966H is designed specifically to work with low ESR ceramic output capacitor for space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR > 30mΩ on the RT8966H output ensures stability. The RT8966H still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor with larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located at a distance of not more than 0.5 inch from the OUTx pin of the RT8966H and returned to a clean analog ground.

Current Source LED Driver

There are four current source LED drivers in the RT8966H. These current sources can be programmed via I^2C in the following control registers, Enable and LED Set. These registers include each driver's enable/disable control, source current control, and LED brightness dimming.

The RT8966H provides a constant current for the white LEDs. Each channel supports up to 30mA current and regulates a constant current for uniform intensity. In order to maintain LED constant current, the input voltage must provide the required LED forward voltage and current source dropout voltage. If the forward voltage of the white LEDs is 3.3V, the input voltage should be higher than 3.4V to provide enough voltage headroom for maintaining constant brightness.

I²C Control Interface

The RT8966H uses an I²C to be the control interface. The I²C interface allows the host microprocessor to control the switches and the accessory detection ADC. The status of the device detection may be sent through the I²C bus. The interrupt line may also be used to signal a status change to the host microprocessor. The I²C interface and interrupt output are compliant with 1.8V logic voltage levels. The SCL pin is only an input and the SDA pin is an input or open drain output. The interrupt line is only an open drain output.

I²C Device Address = 1000100x (where x is the read/write bit)

Switches

The RT8966H provides a multiple input multiplexer to support USB high Speed, UART, stereo audio, mono audio and a microphone. The output of the multiplexer is used to connect to a mini or micro USB connector. When the VBUS voltage is higher than the VB Detect threshold voltage, the RT8966H can turn on and turn off the paths of USB, UART and Audio. However, when the VBUS voltage is lower than the VB Detect threshold voltage, the RT8966H can then only turn on and turn off the paths of stereo audio and mono audio. The following table shows the switch status versus VBUS level.

	USB Switches	UART Switches	Audio Switches
VBUS = High	Allow	Allow	Allow
VBUS = Low	Not Allow	Not Allow	Allow

The default startup of the RT8966H can be set as USB or UART according to the voltage at the DSS pin. The voltage on the DSS pin will be sampled immediately once the first power supply is attached to the RT8966H through VB or BAT and is latched by the first rising voltage on the SCL pin. The DSS pin voltage controls the switch state during this period. If the voltage of the DSS pin rises or falls below 0.4V before the first rising edge on the SCL pin, the switch state will be changed between USB or UART positions.

When the DSS pin voltage is below 1V, the default startup will be USB. If the DSS pin voltage is greater than 1V, the UART will be set as the default startup. The DSS pin provides an internal 300kΩ pull down resistor for USB startup. The DSS pin can also be left unconnected or connected to GND. For UART startup, connect the DSS pin with an external 300kΩ resistor to BAT.

Multiplexer Inputs

DN/DP :

These two pins can support all speed ranges of the USB including USB high speed, full Speed, low speed and UART signals from 0V to 3.3V. In order to function, the CP_EN bit in the register must be set to 1 when signals pass through the switch. DN/DP channel of the RT8966H will be routed to the D–/D+ lines on a mini/micro USB connector.

U1/U2 :

These two pins can also support the speed range of the USB including USB full speed, low speed and UART signals from 0V to 3.3V. Similarly, the CP_EN bit must be set to 1 when signals pass through the switch. U1/U2 channel of the RT8966H will be routed to D–/D+ lines on a mini/micro USB connector.

Voice Audio : The RT8966H can support one mono microphone in which the signal is routed to the ID line. For routing to a headset, the microphone audio will be used with the stereo audio input. CP_EN must be 1 when signals pass through the switch.

Stereo Audio : The RT8966H supports a stereo audio amplifier connected with a mono microphone. The LEFT and RIGHT channel audio of the RT8966H is routed to the D+ and D– lines on the mini/micro USB connector, while the microphone is routed to the ID line on the mini/micro

USB connector. The RT8966H provides internal 100kΩ shunt resistors on the AUD1 and AUD2 speaker lines. Those resistors are used to reduce pops and clicks when the audio amplifier is switched on due to the ac coupling capacitors. If a Direct Drive audio amplifier is adopted, the 100kΩ switched shunt resistors can be removed. CP_EN must be 1 when signals pass through the switch.

Multiplexer Output with High Impedance Mode

The RT8966H provides an I^{2}C control to set the D-, D+ and ID pins in high impedance condition. CP_EN must be 1 when the multiplexer output is connected to high impedance. The D-, D+ and ID pin of the multiplexer outputs must always be connected to the D–,D+ and ID pin of the mini/micro USB connector respectively. This allows the D-, D+ and ID pins to maintain in a "safe" position when a headset is inserted. If the D-, D+ switches are left connected to one of the 4 inputs, it is possible that a dc voltage will be present to cause a pop in the speakers.

Enable Power Saving Mode

The RT8966H provides multiple power saving modes. The power saving mode is used to turn off the internal LDO, charge pump and comparator when not in use. The VB OVP will not be affected by any power saving mode. The RT8966H provides three I^{2}C bits for power saving operation.

CP_EN : CP_EN is used to control the charge pump to achieve proper operation of the analog switches. This bit must be set to 1 when a signal passes through a switch and also any time a negative rail signal is connected to an audio switch input (AUD1, AUD2). The charge pump provides low on-resistance for the switches when they are in conduction condition.

ADC_EN : ADC_EN is used to control the internal ADC and the ID LD0. When this bit is set to disable, the ADC bits will be 0000 and no interrupt signal will be generated. Any pending interrupt signals arising from the change in ADC value will not be cleared unless a READ is sent manually to the STATUS register.

SEMREN : This bit controls the internal comparators used for the SEND/END switch, microphone removal and the ID LDO. When this bit is set to disable, the SE_COMP and MR_COMP registers will be set to zero and no interrupt signal will be generated. Any pending interrupt signals arising from the change in the SE_COMP and MR_COMP comparators will not be cleared. It can only be cleared manually by sending a READ to the STATUS register. (ID LDO Enable = ADC_EN or SEMREN)

Microphone Power Saving Mode

The microphone can draw a large current due to the typical 2.2kΩ bias resistor when it is plugged in. This current will be dissipated even if the microphone is not used for audio input (not in a call or voice recorder not in use, etc.) This is done to allow for the SEND/END button detection's operation. The RT8966H provides a method to reduce the drawn current by turning off the 2.2kΩ pull up resistor. This resistor will be turned on only for short durations to check whether the SEND/END was being pressed. The detail of the microphone power saving circuit is shown in Figure 2. When the external 2.2kΩ resistor is turned off, the internal 200kΩ resistor will be turned on to immediately detect a microphone removal event once it occurs. When the register bit MIC_LP = 1, an interrupt signal will be generated for both a microphone removal (MR_COMP) event and a SEND/END button detection (SE_COMP).

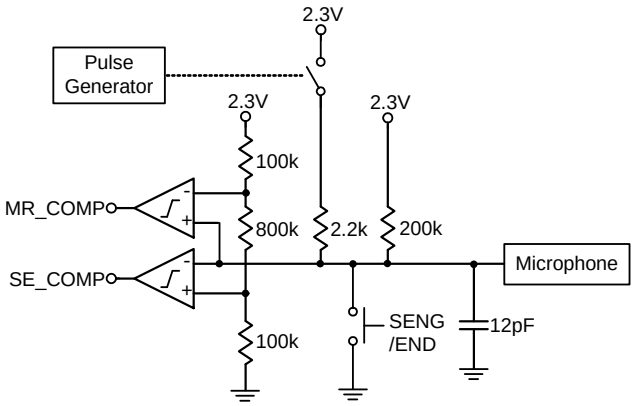


Figure 2. The Microphone Power Saving Circuit of the RT8966H

Event Detection and Interrupt Generation

When a specific event occurs, the RT8966H will be able to detect it and then will generate an interrupt signal. The above-mentioned specific events include CHGDET, MR_COMP, SE_COMP, VBUS and IDNO. For details of those specific events, please refer to Table 9, under

"INT_STA1 0x04". If the ADC reads and detects that there is a plugged device with an ID resistor or microphone present, an interrupt signal will be generated. If a device is removed and the ADC reads a high voltage on the ID line, an interrupt signal is generated. If the voltage on the VB pin rises above or drops below the VB detect threshold, V_{DET_VB} for the detection/removal of an USB cable, an interrupt signal will also be generated. Interrupt will also be generated once the status changes on the SE_OMP and MR_COMP comparators. The interrupt signal will be cleared by reading the STATUS register. The interrupt signal is triggered by different levels and the interrupt polarity can be set through the I^2C bus.

CHGDET : Charger Detection

The RT8966H is compliant with the USB Battery Charging Specification Revision 1. The RT8966H is capable of detecting dedicated chargers, host/hub chargers and standard USB port. The RT8966H USB detection function is off (USB_DET_DIS = 1) by default and requires an I^2C WRITE to enable the detection.

The RT8966H charger detection includes internal logic to allow valid charger detection (D+/D– shorted for host/hub charger) and an external open drain for automatic ISET signal generation. The charger detection sequence is started once VBUS rises above V_{DET_VB}. However, the charge detection will not be activated if the cable ID resistor value is 56kΩ since this value is already designated as the UART cable. Besides, it can only be started if the USB_DET_DIS bit is equal to 0. When V_{DAT_SRC} is applied to D+, the V_{DAT_SRC} voltage will also be applied to the D– line by the dedicated charger since D+ and D– are shorted. The dedicated charger detection is shown in Figure 3. As for the host/hub charger, D+ receives V_{DAT_SRC} and retransfers it on D–. Thus, it acts similarly to the dedicated charger. The host/hub charger detection is shown in Figure 4. However, when a standard USB port is inserted instead, the D– will not receive the VDAT_SRT after D+ sends out the VDAT_SRT signal. The standard USB port is shown in Figure 5. It is through such method that the RT8966H differentiates between a standard USB port and a charger port. (either dedicated charger or host/hub charger).

The distinction between a dedicated charger or a high current host/hub can be achieved by the manual operation started with an I^2C WRITE. After an interrupt signal is sent to the host, it reads the IN_STAT register which can be used to set the CHGDET and VBUS bits (USB high current host/hub or dedicated charger detected). The host will set the CHG_TYP bit to perform the type detection. The detection is achieved by connecting a high value pull up resistor (300k to 600k) to D+. If D– stays low (below 0.8V), a high current hub/host is detected. A dedicated charger will be detected if D– goes high. The output of this detection is two bits in the STATUS register. The CHGDET bit in INT_STAT rather than the interrupt signal is guaranteed by the register. After the charger type detection is completed, the CHG_TYP bit will automatically reset to 0.

The ISET pin of the RT8966H is an external open-drain connected to an external charger to indicate whether the inserted USB is a charger or not. When the inserted one is a standard USB port, the ISET pin will be high impedance. When the inserted one is a charger (dedicated charger or host/hub charger), the ISET pin will be pulled low. ISET controls the external battery charger current limit. If ISET is high impedance, the charger current will be limited at 100mA. If ISET is low, then the charger current is allowed to be drawn up to 1.5A.

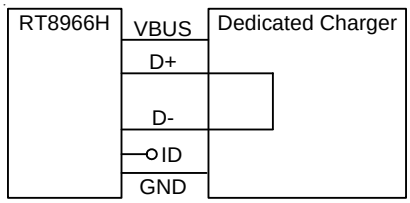


Figure 3. Dedicated Charger Detection

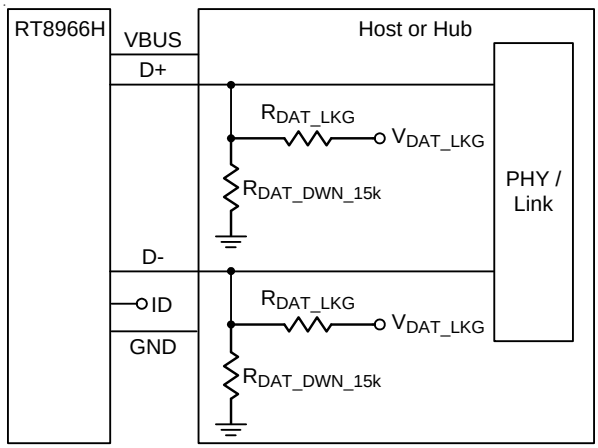


Figure 4. Host/Hub Charger Detection

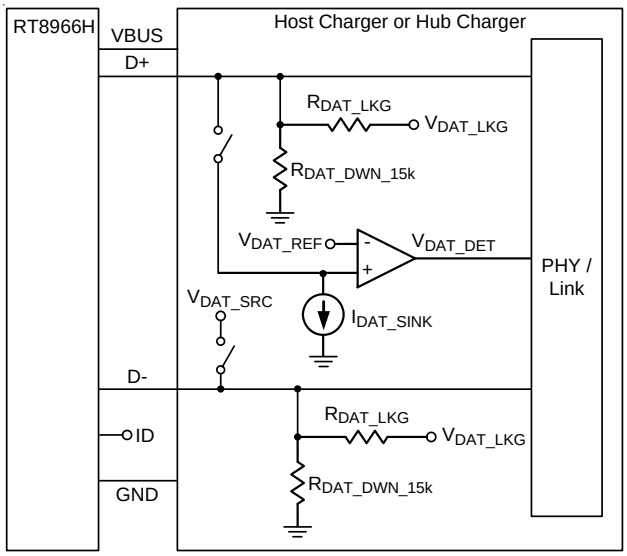


Figure 5. Standard USB Port

MR_COMP, SE_COMP : Microphone Removal Detection and Send/End Switch

The RT8966H provides MR_COMP for microphone removal detection and SE_COMP for Send/End switch detection by checking the voltage on ID when a microphone is detected on the ID pin. A bias resistor (typical 2.2k) should be connected between ID and a bias voltage source (typical 2.3V). When the microphone is not connected, the ID pin voltage will be pulled high to equal the bias voltage and the comparator will detect this voltage rise. The microphone removal threshold voltage will be 90% of the microphone bias voltage. There is a switch included in the headset which is connected between the ID line and ground to signal a SEND or END condition. The voltage drop of the ID line will be detected by an internal comparator with a typical threshold of 10% bias voltage source. If the voltage on the ID pin rises above the microphone removal threshold voltage or drops below the SEND/END threshold, the host microprocessor will read the status of these comparators across the I^2C bus. An ID voltage >90% means the microphone is removed, an ID voltage <10% means push, and an ID voltage between 10% to 90% means the microphone is plugged.

VBUS : VB Voltage Detection

When the VB voltage is lower than V_{DET_VB}, the VBUS bit will be equal to 0. If the VB voltage is higher than V_{DET_VB}, the VBUS bit will be equal to 1.

Device Identification

The RT8966H supports multiple accessories by detecting unique characteristics, such as VBUS voltage, ID resistor value and shorted USB data lines. These characteristics are shown in Tables 1 to 3. The detection of connected accessories is performed by using an internal 200kΩ pull up resistor.

Table 1. Detection Values With 200kΩ pull up

ADC Value	ADC Voltage	ID Resistor kΩ	D+ Condition	D– Condition	VBUS	Function
1011	100%	Open	15k to GND	15k to GND	5	USB Cable
1011	100%	Open	Shorted	Shorted	5	TA Charger
1010	81.90%	910	--	--	--	Reserved
1001	75.60%	620	--	--	--	Reserved
1000	68.20%	430	--	--	--	Reserved
0111	62.20%	330	--	--	--	Reserved
0110	54.50%	240	--	--	--	Reserved
0101	47.40%	180	Shorted	Shorted	5	LG Proprietary TA
0100	39.40%	130	--	--	--	UART Factory
0011	33.30%	100	--	--	--	Reserved
0010	21.90%	56	TX	RX	5	UART Cable
0001	10.70%	24	Audio	Audio	--	Video - no load
0000	0%	--	Speaker	Speaker	--	Microphone
0000	0%	GND	D+	D–	--	USB OTG
0000	0%	75Ω	Audio	Audio	--	Video - with load

Table 2. Detection Values With 2.2kΩ Pull Up

ADC Value	ADC Voltage	ID Resistor kΩ	D+ Condition	D– Condition	VBUS	Function
1011	100%	Open	--	--	--	--
1011	100%	Open	--	--	--	--
1010	81.90%	--	--	--	--	Microphone
1001	75.60%	--	--	--	--	Microphone
1000	68.20%	--	--	--	--	Microphone
0111	62.20%	--	--	--	--	Microphone
0110	54.50%	--	--	--	--	Microphone
0101	47.40%	--	--	--	--	Microphone
0100	39.40%	--	--	--	--	Microphone
0011	33.30%	--	--	--	--	Microphone
0010	21.90%	--	--	--	--	Microphone
0001	10.70%	--	--	--	--	Microphone
0000	0%	75Ω	Audio	Audio	--	Video - with load
0000	0%	GND	D+	D–	--	USB OTG

Table 3. Detection Values With 620Ω Pull Up

ADC Value	ADC Voltage	ID Resistor kΩ	D+ Condition	D– Condition	VBUS	Function
1011	100%	Open	--	--	--	--
1011	100%	--	--	--	--	--
1010	81.90%	--	--	--	--	--
1001	75.60%	--	--	--	--	--
1000	68.20%	--	--	--	--	--
0111	62.20%	--	--	--	--	--
0110	54.50%	--	--	--	--	--
0101	47.40%	--	--	--	--	--
0100	39.40%	--	--	--	--	--
0011	33.30%	--	--	--	--	--
0010	21.90%	--	--	--	--	--
0001	10.70%	75Ω	Audio	Audio	--	Video - with load
0000	0%	GND	D+	D–	--	USB OTG

I²C Register Information

Table 4. Address : 1000100x

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	Device ID	VENDOR_ID				CHIP_REV			
	Reset Value	0	0	1	0	0	0	0	1
	Read/Write	R	R	R	R	R	R	R	R
0x01	Control1	Reserved	ID_2P2	ID_620	ID_200	VLDO	SEMREN	ADC_EN	CP_EN
	Reset Value	0	0	0	0	0	0	0	1
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x02	Control2	INTPOL	INT_EN	MIC_LP	CP_AUD	Reserved	Reserved	CHG_TYP	USB_DET_DIS
	Reset Value	0	0	0	0	0	0	0	1
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x03	SW Control	Reserved	MIC_ON	DP2			DN1		
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x04	INT_STA1	CHGDET	MR_COMP	SEND/END	VBUS	INDO			
	Reset Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	Read/Write	R	R	R	R	R	R	R	R
0x05	INT_STA2	CHG	TSHD	TMD	OVLO	UVLO	Reserved	Reserved	Reserved
	Reset Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	Read/Write	R	R	R	R	R	R	R	R
0x06	STATUS1	DCPORT	CHPORT	CHG_STAT		Reserved	Reserved	Reserved	C1COMP
	Reset Value	0	0	0	0	0	0	0	1
	Read/Write	R	R	R	R	R	R	R	R
0x07	STATUS2	TMP_STAT			Reserved	Reserved	Reserved	Reserved	Reserved
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R	R	R	R	R	R	R	R
0x08	CHG_Ctrl1	CHG_EN	EXPDET	PTM	CHG_OFF	IPRE_CHG		Reserved	Reserved
	Reset Value	1	1	0	0	1	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x09	CHG_Ctrl2	CHG_SET				Reserved	IMIN_SET		
	Reset Value	0	0	1	0	0	0	0	1
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x0A	Enable	OUT1_EN	OUT2_EN	OUT3_EN	OUT4_EN	LED1_EN	LED2_EN	LED3_EN	LED4_EN
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x0B	OUT Set 1	OUT1_SET				OUT2_SET			
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset Value	0	0	0	0	0	0	0	0

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0C	OUT Set 2	OUT3_SET				OUT4_SET			
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x0D	OUT Set 2	LED_FS			LED_DIM				
	Reset Value	1	0	0	1	1	1	1	1
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x0E	TEST1	MUIC							
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x0F	TEST2	Charge / LED / LDO							
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 5. Device ID 0x00 – Read Only

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	Device ID	VENDOR_ID				CHIP_REV			
	Reset Value	0	0	1	0	0	0	0	1
	Read/Write	R	R	R	R	R	R	R	R
VENDOR_ID		Vendor Identification : Richtek : 1000b							
CHIP_REV		Chip Revision							

Table 6. Control1 0x01 – Read/Write

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x01	Control1	Reserved	ID_2P2	ID_620	ID_200	VLDO	SEMREN	ADC_EN	CP_EN
	Reset Value	0	0	0	0	0	0	0	1
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ID_2P2		Connects the internal ID LDO Output to the RES pin. Used to connect an external microphone bias resistor to USB ID. 0 : Disabled (Open) 1 : Enabled (Connect)							
ID_620		Connects an internal 620Ω resistor between the internal ID LDO Output and USB ID. 0 : No resistor (Open) 1 : Resistor connected							
ID_200		Connects an internal 200kΩ resistor between the internal ID LDO Output and USB ID. 0 : No resistor (Open) 1 : Resistor connected							
VLDO		Sets the voltage on the ID LDO . 0 : 2.6V 1 : 2.3V							
SEMREN		Enables the SEND/END, Microphone Removal comparators and the ID LDO . 0 : Disabled 1 : Enabled							
ADC_EN		Enables the internal ADC and ID LDO. 0 : Disabled 1 : Enabled							
CP_EN		Enables the charge pump required for analog switch operation. Set to 1 when any signal is passed through the switch. When set to disable, there must be no signal connected to an audio input which goes below ground. 0 : Disabled 1 : Enabled							

Table 7. Control2 0x02 – Read/Write

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	Control2	INTPOL	INT_EN	MIC_LP	CP_AUD	Reserved	Reserved	CHG_TYP	USB_DET_DIS
	Reset Value	0	0	0	0	0	0	0	1
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
INTPOL		This bit sets the interrupt polarity 0 : Active low 1 : Active High							
INT_EN		Enables interrupt generation. When set to disabled, all pending interrupts are cleared and the $\overline{INT}$ pin will de-assert. 0 : Disable Interrupt 1 : Enable Interrupt							
MIC_LP		Enables ID line pulsing for low power detection of the SEND/END key and microphone removal. This mode must only be enabled when a valid microphone has been detected and microphone audio is not required. 0 : Disabled 1 : Enabled							
CP_AUD		This bit sets the position of the click/pop resistor on both AUD1 and AUD2 0 : Disabled 1 : Enabled							
CHG_TYP		Enables Charger Type Detection. Set this bit to determine between Dedicated USB Charger and High Current Host/Hub Chargers. 0 : Disabled 1 : Enabled							
USB_DET_DIS		Disables the USB Charger Detection. This bit must be set to 0 for a USB detection sequence to be run when VBUS is applied. 0 : Enabled 1 : Disabled							

Table 8. SW Control 0x03 – Read/Write

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	SW Control	Reserved	MIC_ON	DP2			DN1		
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MIC_ON		This bit sets the position of the switch connecting MIC to ID 0 : Open 1 : ID Connected to MIC							
DP2		This bit sets the position of the mux switch connected to D+ 000 : D+ connected to DP 001 : D+ connected to U2 010 : D+ connected to AUD2 011 : Future Use 100 to 111 : High Impedance							
DN1		This bit sets the position of the mux switch connected to D- 000 : D- connected to DN 001 : D- connected to U1 010 : D- connected to AUD1 011 : D- connected to C1COMP 100 to 111 : High Impedance							

Table 9. INT_STA1 0x04 – Read Only

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x04	INT_STA1	CHGDET	MR_COMP	SEND/END	VBUS	INDO			
	Reset Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	Read/Write	R	R	R	R	R	R	R	R
CHGDET		Output of USB Charger Detection Comparator. This bit will be set to one if D+ > V_{DAT_REF} for longer than 20ms. Any change in this bit triggers an interrupt. 0 : D+ < V_{DAT_REF} or D+ > V_{LGC} (High current charger not detected) 1 : V_{LGC} > D+ > V_{DAT_REF} (High current charger detected)							
MR_COMP		Output from the Microphone Removal Comparator – only active for SEMREN = 1. Any change in this bit triggers an interrupt. 0 : ID voltage is less than $V_{MICRDET}$ or SEMREN = 0 1 : ID voltage is greater than $V_{MICRDET}$							
SEND/END		Output from the SEND/END Comparator – only active for SEMREN = 1. Any change in this bit triggers an interrupt. 0 : ID voltage is greater than $V_{MICSEDET}$ or SEMREN = 0 1 : ID voltage is less than $V_{MICSEDET}$							
VBUS		Any change in this bit triggers an interrupt. Active for ADC_EN = 1 or SEMREN = 1 0 : VBUS voltage is less than UVP or higher than OVP or ADC_EN = SEMREN = 0 1 : VBUS voltage is higher than UVP and lower than OVP							
INDO		ADC Output. Any change in these bits triggers an interrupt. Only active for ADC_EN = 1. 0000 : GND 0001 : 24 0010 : 56 0011 : 100 0100 : 130 0101 : 180 0110 : 240 0111 : 330 1000 : 430 1001 : 620 1010 : 910 1011 : open or ADC_EN = 0							

Table 10. INT_STA2 0x05 – Read Only

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x05	INT_STA2	CHG	TSHD	TMP	OVLO	UVLO	Reserved	Reserved	Reserved
	Reset Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	Read/Write	R	R	R	R	R	R	R	R
CHG		0 : Charging Current I_{CHG} < I_{EOC} or VBUS is absent. Once EOC occurs, CHG will be latched at “0” and can be reset to “1” by CHG_EN = 0 or CHG_OFF = 1. 1 : Charging Current I_{CHG} > I_{EOC} CHG is active High when CHG_EN = 1, CHG_OFF = 0 and VBUS > UVLO							
TSHD		Thermal Shutdown 0 : Chip Temperature is lower than Threshold temp 1 : Chip Temperature is higher than Threshold temp							
TMP		1 : TEMP_STAT < 2 : 0> change 0 : TEMP_STAT < 2 : 0> does not change							
OVLO		0 : VBUS Voltage is lower than OVP Threshold Voltage 1 : VBUS Voltage is Higher than OVP Threshold Voltage							
UVLO		0 : VBUS Voltage is Higher than UVP Threshold Voltage 1 : VBUS Voltage is Lower than UVP Threshold Voltage							

Table 11. STATUS1 0x06 – Read Only

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x06	STATUS1	DCPORT	CHPORT	CHG_STAT		Reserved	Reserved	Reserved	C1COMP
	Reset Value	0	0	0	0	0	0	0	1
	Read/Write	R	R	R	R	R	R	R	R
DCPORT		Indicates if a Dedicated USB Charger is Connected 0: No dedicated Charger 1: Dedicated Charger Detected							
CHPORT		Indicates if a High Current Host/Hub is Connected 0: No dedicated HCHH 1: HCHH Detected							
CHG_STAT		Charger Status 00: Charger is operating in Pre-charging status 01: Charger is operating in Fast-charging status 10: Charger is operating in CV Mode 11: Charging current is lower than EOC threshold							
C1COMP		Output from the D- Comparator 0: D- voltage is less than V_{D-DET} 1: D- voltage is greater than V_{D-DET}							

Table 12. STATUS2 0x07 – Read Only

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x07	STATUS2	TMP_STAT			Reserved	Reserved	Reserved	Reserved	Reserved
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R	R	R	R	R	R	R	R
TMP_STAT		Temperature detect and Alarm 000 : < 75°C 001 : 75 to 95°C 010 : 95 to 115°C 011 : 115 to 135°C 100 : > 135°C 101 to 111 : Reserved							

Table 13. CHG_Ctrl1 0x08 – Read/Write

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x08	CHG_Ctrl1	CHG_EN	EXPDET	PTM	CHG_OFF	IPRE_CHG		Reserved	Reserved
	Reset Value	1	1	0	0	1	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CHG_EN		0 : Disable Charging Path of Charger 1 : Enable Charging Path of Charger (CHG_OFF = 1 is not allow)							
EXPDET		0 : Disable LDO Output of Charger 1 : Enable LDO Output of Charger (CHG_OFF = 1 is not allow)							
PTM		Production Test Mode 0 : Disable Test Mode 1 : Enable Test Mode (CHG_OFF = 1 or CHG_EN = 0 is not allow)							
CHG_OFF		0 : Enable Charger Circuit 1 : Disable Charger Circuit and EXPDET and PTM mode							
IPRE_CHG		Setting of Pre-charging Current of Charger 00 : Pre-charging Current = 40mA 01 : Pre-charging Current = 60mA 10 : Pre-charging Current = 80mA 11 : Pre-charging Current = 100mA							

Table 14. CHG_Ctrl2 0x09 – Read/Write

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x09	CHG_Ctrl2	CHG_SET				Reserved	IMIN_SET		
	Reset Value	0	0	1	0	0	0	0	1
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CHG_SET		Setting of Fast Charging Current of Charger 0000 : 90mA 0001 : 100mA 0010 : 400mA 0011 : 450mA 0100 : 500mA 0101 : 600mA 0110 : 700mA 0111 : 800mA 1000 : 900mA 1001 : 1000mA 1010 to 1111 : Reserved (1000mA)							
IMIN_SET		Setting of End of Charge Current Ratio 000 : 5% 001 : 10% 010 : 16% 011 : 20% 100 : 25% 101 : 33% 110 : 50% 111 : Reserved (50%)							

Table 15. Enable 0x0A – Read/Write

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0A	Enable	OUT1_EN	OUT2_EN	OUT3_EN	OUT4_EN	LED1_EN	LED2_EN	LED3_EN	LED4_EN
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OUT1_EN		0 : Disable LDO1 1 : Enable LDO1							
OUT2_EN		0 : Disable LDO2 1 : Enable LDO2							
OUT3_EN		0 : Disable LDO3 1 : Enable LDO3							
OUT4_EN		0 : Disable LDO4 1 : Enable LDO4							
LED1_EN		0 : Disable LED1 1 : Enable LED1							
LED2_EN		0 : Disable LED2 1 : Enable LED2							
LED3_EN		0 : Disable LED3 1 : Enable LED3							
LED4_EN		0 : Disable LED4 1 : Enable LED4							

Table 16. OUT Set1 0x0B – Read/Write

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0B	OUT Set 1	OUT1_SET				OUT2_SET			
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OUT1_SET		Setting of LDO1 Output Voltage 0000 : 1.0V 0001 : 1.2V 0010 : 1.5V 0011 : 1.8V 0100 : 2.0V 0101 : 2.1V 0110 : 2.5V 0111 : 2.6V 1000 : 2.7V 1001 : 2.8V 1010 : 2.9V 1011 : 3.0V 1100 : 3.1V 1101 : 3.3V							
OUT2_SET		Setting of LDO2 Output Voltage 0000 : 1.0V 0001 : 1.2V 0010 : 1.5V 0011 : 1.8V 0100 : 2.0V 0101 : 2.1V 0110 : 2.5V 0111 : 2.6V 1000 : 2.7V 1001 : 2.8V 1010 : 2.9V 1011 : 3.0V 1100 : 3.1V 1101 : 3.3V							

Table 17. OUT Set2 0x0C – Read/Write

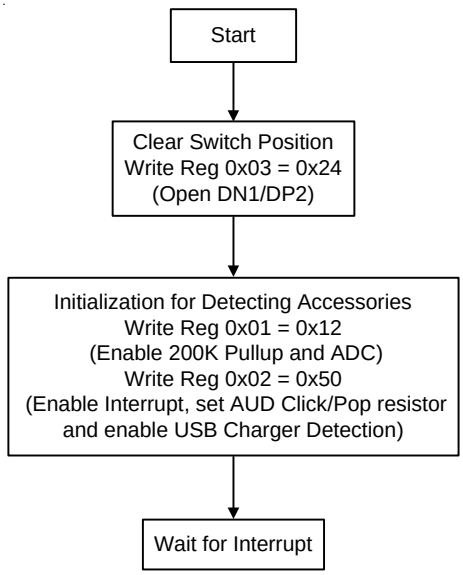
Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0C	OUT Set 2	OUT3_SET				OUT4_SET			
	Reset Value	0	0	0	0	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OUT3_SET		Setting of LDO3 Output Voltage 0000 : 1.0V 0001 : 1.2V 0010 : 1.5V 0011 : 1.8V 0100 : 2.0V 0101 : 2.1V 0110 : 2.5V 0111 : 2.6V 1000 : 2.7V 1001 : 2.8V 1010 : 2.9V 1011 : 3.0V 1100 : 3.1V 1101 : 3.3V							
OUT4_SET		Setting of LDO4 Output Voltage 0000 : 1.0V 0001 : 1.2V 0010 : 1.5V 0011 : 1.8V 0100 : 2.0V 0101 : 2.1V 0110 : 2.5V 0111 : 2.6V 1000 : 2.7V 1001 : 2.8V 1010 : 2.9V 1011 : 3.0V 1100 : 3.1V 1101 : 3.3V							

Table 18. LED Set 0x0D – Read/Write

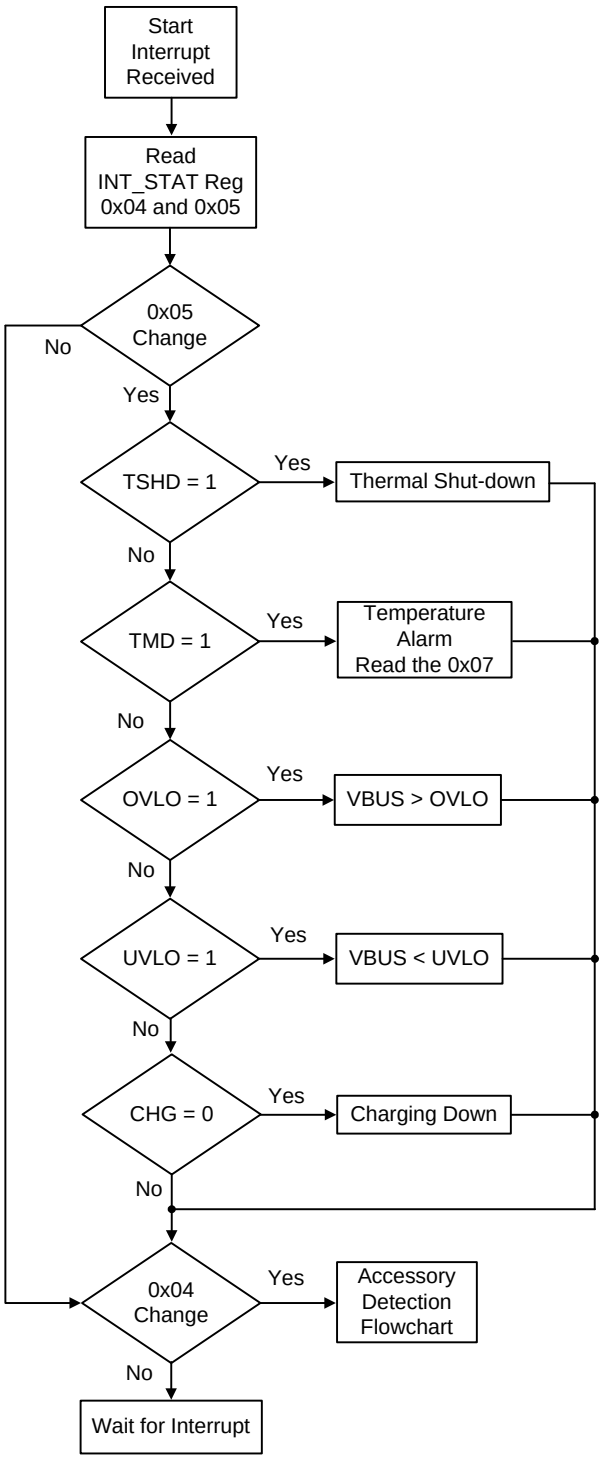
Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0D	LED Set	LED_FS			LED_DIM				
	Reset Value	1	0	0	1	1	1	1	1
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LED_FS		Setting of LED Full Scale Current 000 : 2.5mA 001 : 5mA 010 : 10mA 011 : 15mA 100 : 20mA (Default) 101 : 25mA 110 : 30mA 111 : Reserved (30mA)							
LED DIM		Setting of LED Full Scale Current 00000 : 32 steps (Maximum Brightness) 00000 : 31 steps : : 11111 : 0 steps (Default) (Minimum Brightness)							

Software Flowcharts

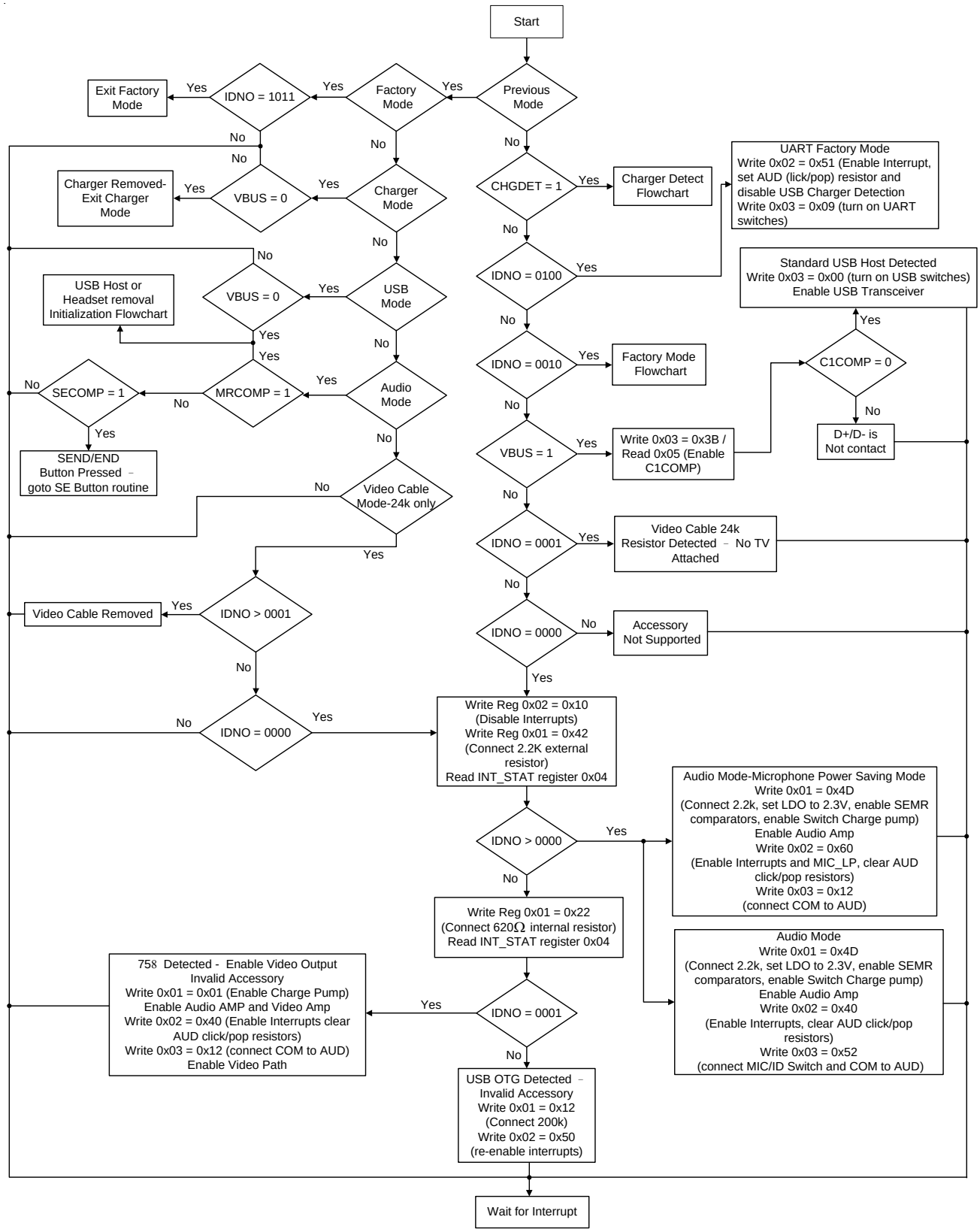
Initialization Flowchart :



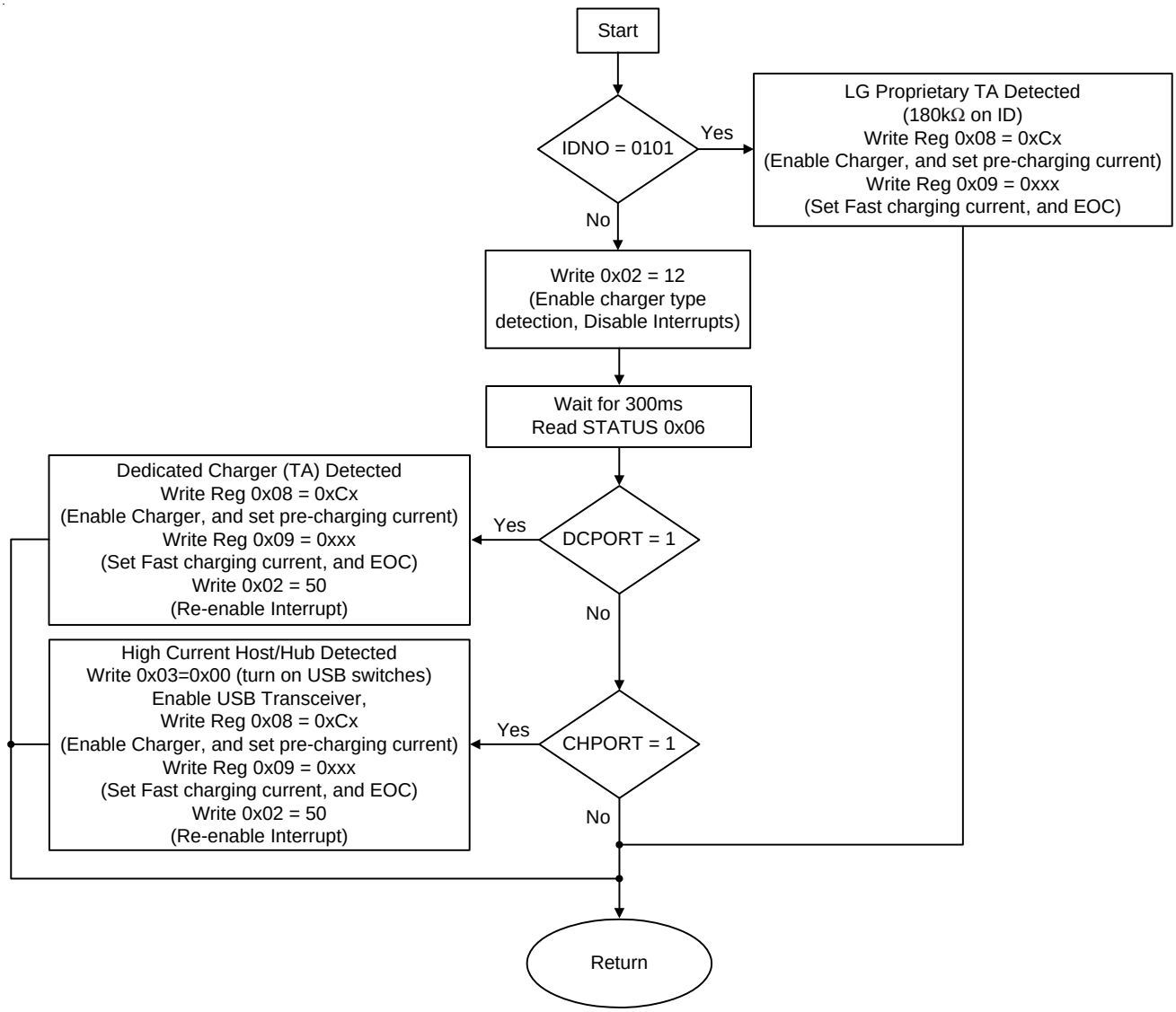
Alarm Flowchart :



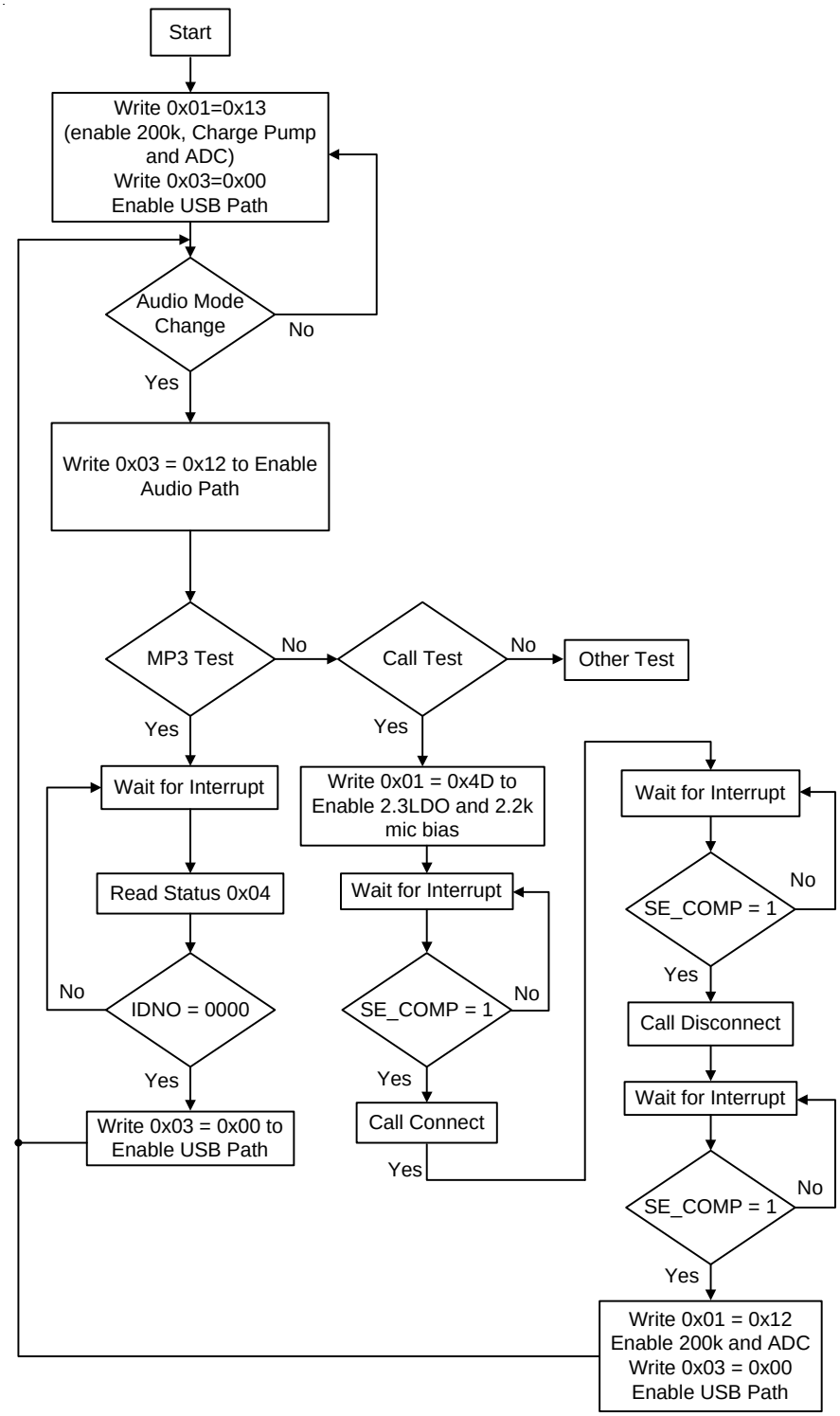
Accessory Detection Flowchart :



Charger Detection Flowchart :

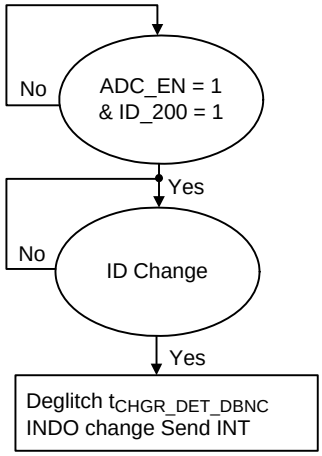


Factory Mode Flowchart :

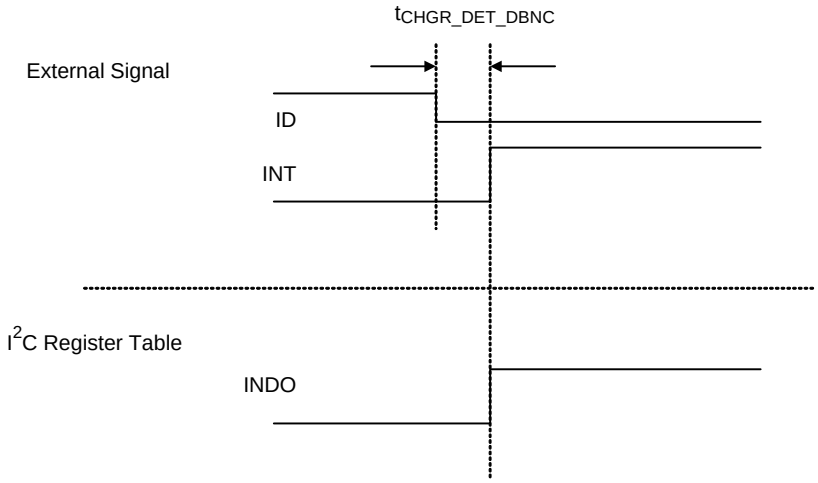


RT8966H Internal Logic Flowchart

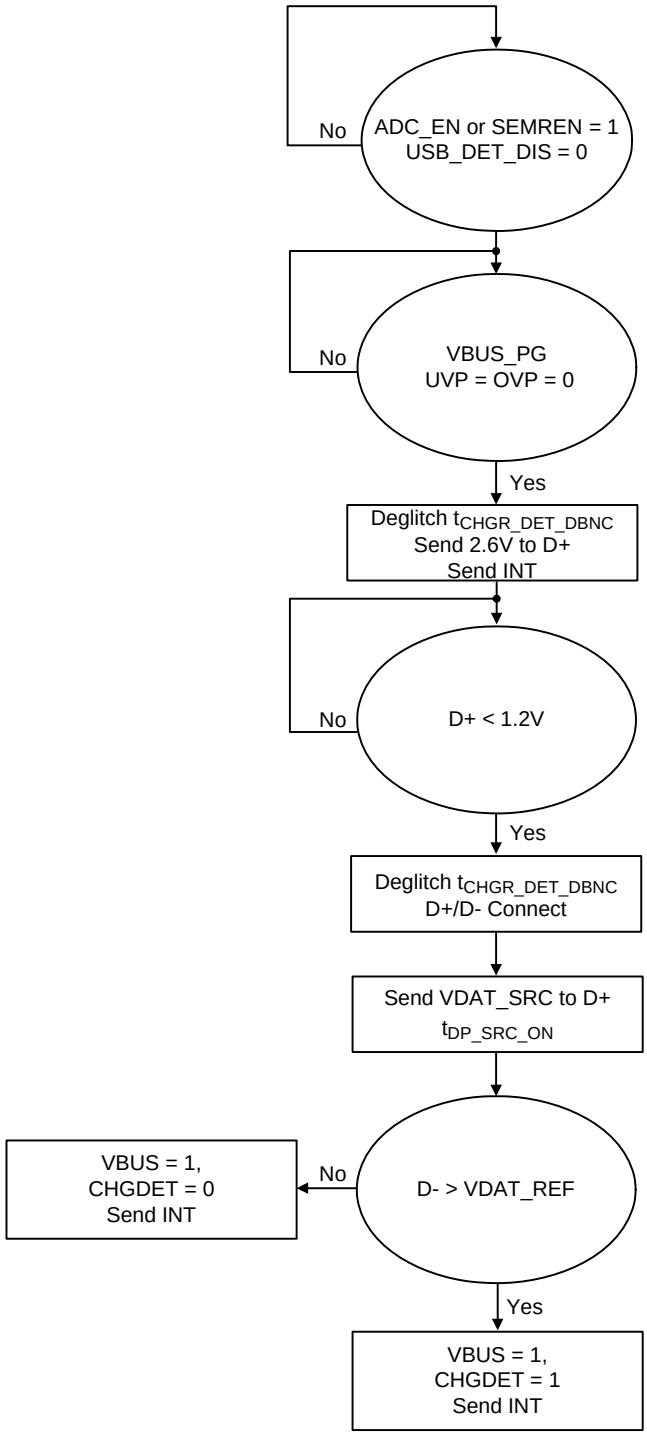
Case 1.1 Accessory without VBUS Flowchart :



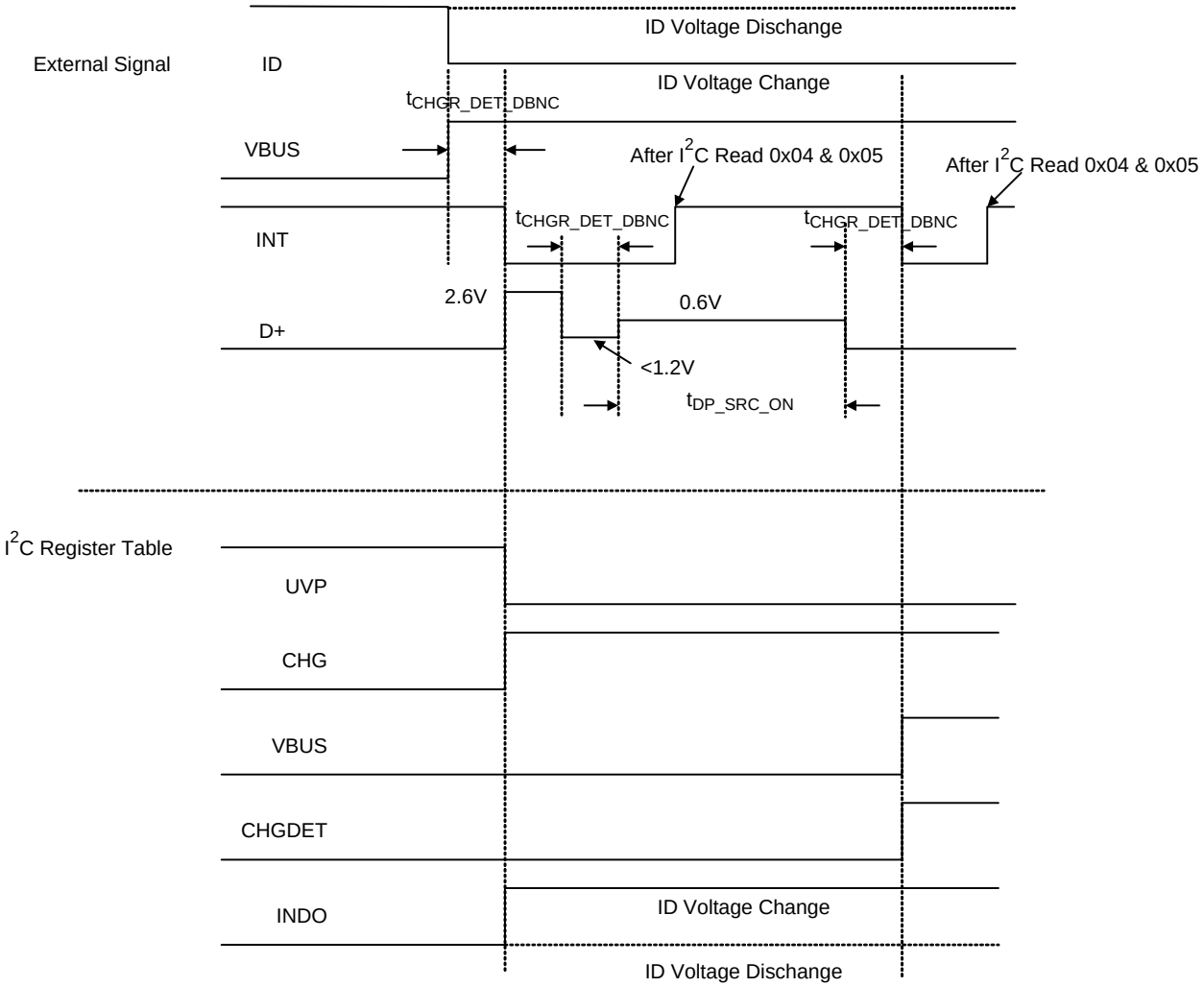
Case 1.2 Accessory without VBUS Signal Sequence :



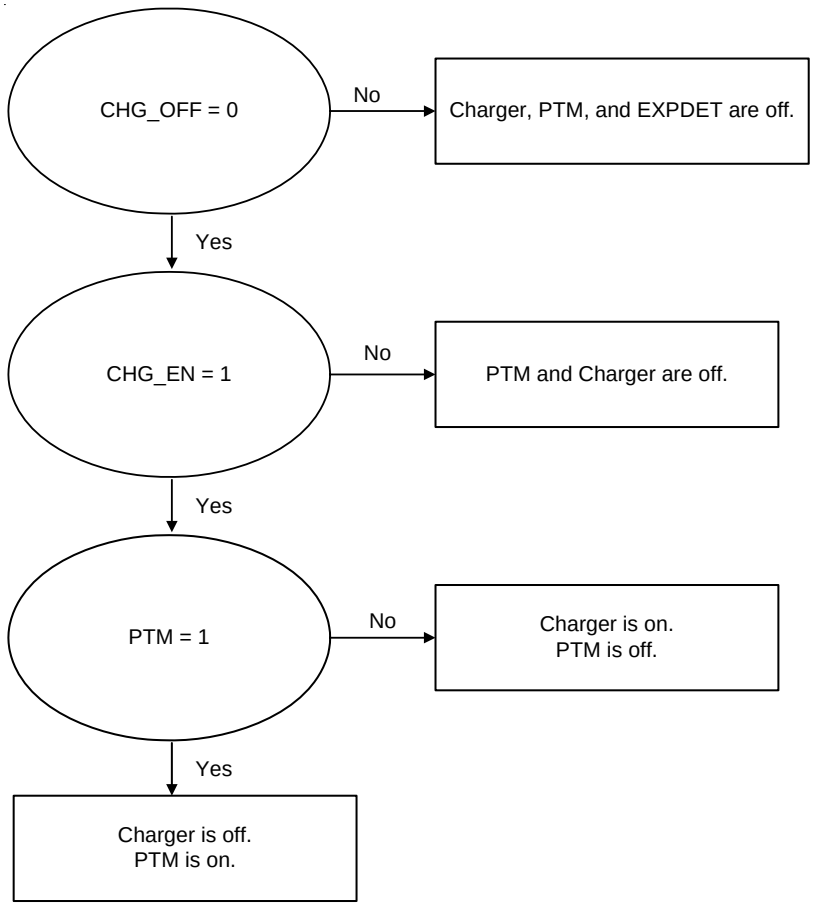
Case 2.1 Accessory with VBUS Flowchart :



Case 2.2 Accessory with VBUS Signal Sequence :



Charger Internal Logic Flowchart :



Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-32L 4x4 packages, the thermal resistance, θ_{JA}, is 27.8°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.8°C/W) = 3.59W for WQFN-32L 4x4 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

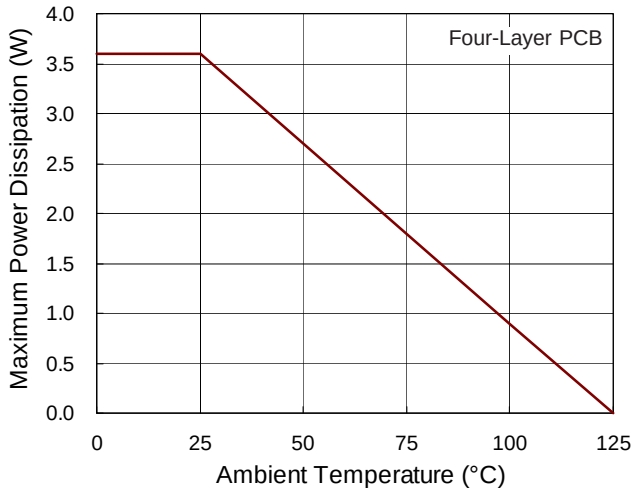
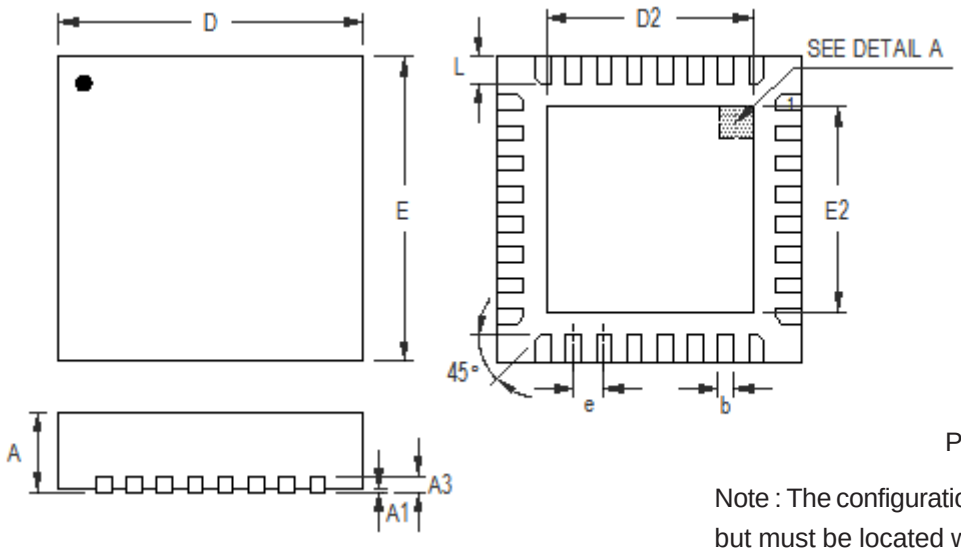
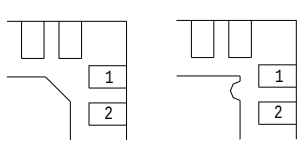


Figure 6. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
D2	2.650	2.750	0.104	0.108
E	3.900	4.100	0.154	0.161
E2	2.650	2.750	0.104	0.108
e	0.400		0.016	
L	0.300	0.400	0.012	0.016

W-Type 32L QFN 4x4 Package

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