15W Stereo Class-D Audio Power Amplifier

General Description

The RT9108NB is a 15W per channel, high efficiency Class D stereo audio amplifier for driving Bridge Tied Load (BTL) speakers. The RT9108NB can drive stereo speakers with load as low as 4Ω. Its high efficiency eliminates the need for an extra heat sink when playing music. The gain of the amplifier can be controlled by two gain select pins. The outputs are fully protected against shorts to GND, PV_{CC}, and output to output with an auto recovery feature and monitored output.

The RT9108NB is available in a TSSOP-28 (Exposed Pad) package.

Ordering Information

RT9108NB□□

- Package Type
  CP : TSSOP-28 (Exposed Pad-Option 3)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **8V to 26V Input Supply Range**
- **6W/CH for an 8Ω Load, 10V Supply at 10% THD +N**
- **15W/CH for an 8Ω Load, 16V Supply at 10% THD +N**
- **90% Efficiency Eliminates Need for Heat Sinks**
- **Four Selectable or Fixed Gain Settings**
- **Mute Function Amplifier**
- **Robust Pin-to-Pin Short Circuit Protection**
- **Thermal Protection with Auto Recovery Option**
- **Speaker Protection with Adjustable Power Limit**
- **Surface Mount TSSOP-28 (Exposed Pad) Package**
- **RoHS Compliant and Halogen Free**

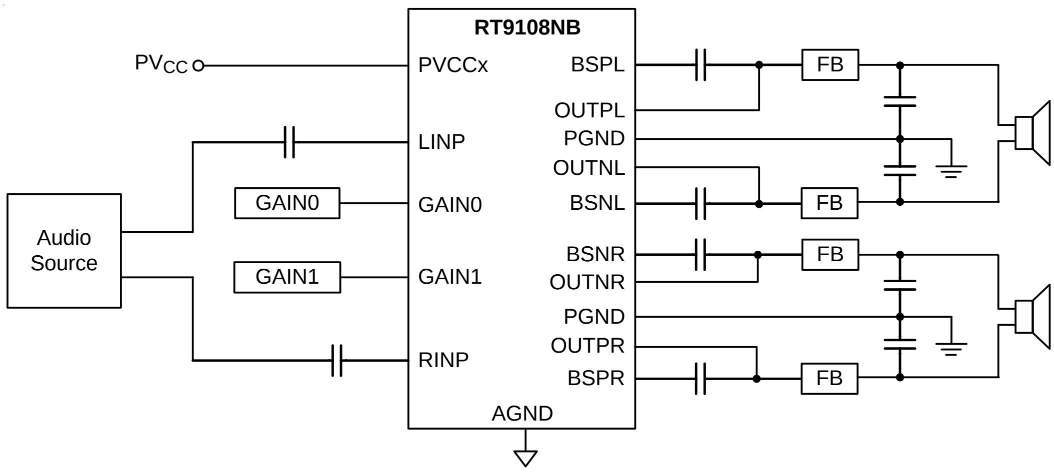
Applications

- LCD-TV
- Monitors
- DVD Players

Marking Information

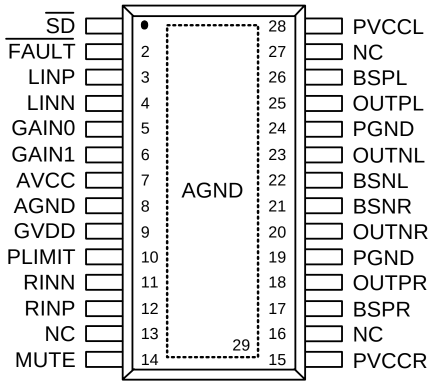
RT9108NB GCPYMDNN	RT9108NBGCP : Product Number YMDNN : Date Code

Simplified Application Circuit



Pin Configurations

(TOP VIEW)



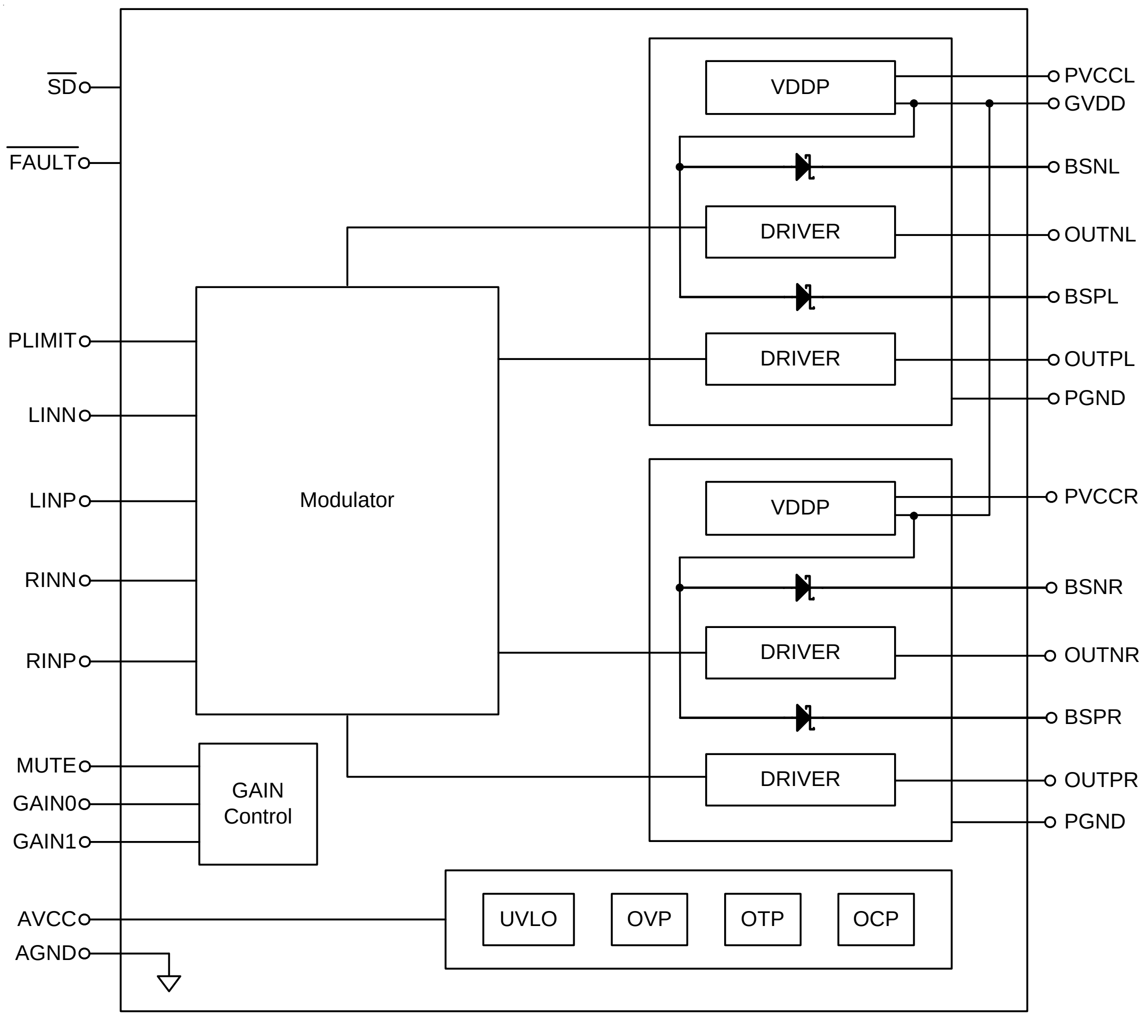
TSSOP-28 (Exposed Pad)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	$\overline{SD}$	Shutdown Logic Input for Audio Amp (High = outputs enabled). TTL logic levels with compliance to AVCC.
2	$\overline{FAULT}$	Open Drain Output for Short Circuit Fault Status. Short circuit faults can be set to auto recovery by connecting $\overline{FAULT}$ pin to $\overline{SD}$ pin.
3	LINP	Positive Audio Input for Left Channel. Biased at 2.3V.
4	LINN	Negative Audio Input for Left Channel. Biased at 2.3V.
5	GAIN0	Gain Select Least Significant Bit.
6	GAIN1	Gain Select Most Significant Bit.
7	AVCC	Analog Supply Input.
8, 29 (Exposed Pad)	AGND	Analog Ground. Connect to the thermal pad. The exposed pad must be soldered to a large PCB and connected to AGND for maximum power dissipation.
9	GVDD	High Side FET Gate Drive Supply. Nominal voltage is 5V.
10	PLIMIT	Power Limit Level Adjustment.
11	RINN	Negative Audio Input for Right Channel. Biased at 2.3V.
12	RINP	Positive Audio Input for Right Channel. Biased at 2.3V.
13, 16, 27	NC	No Internal Connection.
14	MUTE	Mute Logic Input for Audio Amp (Low = outputs enabled).
15	PVCCR	Power Supply Input for Right Channel H-Bridge. Right channel and left channel power supply inputs are connected internally.
17	BSPR	Bootstrap I/O for Right Channel, Positive High Side FET.
18	OUTPR	Class-D H-Bridge Positive Output for Right Channel.

Pin No.	Pin Name	Pin Function
19, 24	PGND	Power Ground for H-Bridges.
20	OUTNR	Class-D H-Bridge Negative Output for Right Channel.
21	BSNR	Bootstrap I/O for Right Channel, Negative High Side FET.
22	BSNL	Bootstrap I/O for Left Channel, Negative High Side FET.
23	OUTNL	Class-D H-Bridge Negative Output for Left Channel.
25	OUTPL	Class-D H-Bridge Positive Output for Left Channel.
26	BSPL	Bootstrap I/O for Left Channel, Positive High Side FET.
28	PVCCL	Power Supply Input for Left Channel H-Bridge. Right channel and left channel power supply inputs are connected internally.

Function Block Diagram



Operation

The RT9108NB is a 15W (per channel) efficient Class-D audio power amplifier for driving bridged-tied stereo speakers. The RT9108NB uses the three-level modulation scheme (BD model) that allows operation without the classic LC reconstruction filter when the amplifier drives is driving an inductive load. The internal close-loop modulator enables the negative error feedback, which improves the THD+N of output signal.

An adjustable power limiter is included in the modulator to protect the load speaker. The adjustable power limiter allows the user to set a "virtual" voltage rail lower than the chip supply to limit the amount of current through the speaker.

RT9108NB has protection from over current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported at the $\overline{\text{FAULT}}$ pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SD pin through the low state. If automatic recovery from the short circuit protection latch is desired, connect the $\overline{\text{FAULT}}$ pin directly to the $\overline{\text{SD}}$ pin. This allows the $\overline{\text{FAULT}}$ pin function to automatically drive the $\overline{\text{SD}}$ pin low which clears the short-circuit protection latch.

The RT9108NB can drive stereo speakers as low as 4Ω. The high efficiency of the RT9108NB, 90%, eliminates the need for an external heat sink when playing music.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, PVCCR, PVCCL, AVCC -- −0.3V to 30V
- Input Voltage, $\overline{\text{SD}}$, GAIN0, GAIN1, $\overline{\text{FAULT}}$ -- −0.3V to (AVCC + 0.3V)
- Output Voltage, OUTPR, OUTPL, OUTNR, OUTNL -- −0.3V to (PVCCx + 0.3V)
- Bootstrap Voltage, BSPR, BSPL, BSNR, BSNL --- −0.3V to (PVCCx + GVDD)
- Other Pins --- −0.3V to (GVDD + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  TSSOP-28 (Exposed pad) -- 3.44W
- Package Thermal Resistance (Note 2)
  TSSOP-28 (Exposed pad), θ_{JA} -- 29°C/W
  TSSOP-28 (Exposed pad), θ_{JC} -- 1.2°C/W
- Junction Temperature -- 150°C
- Lead Temperature (Soldering, 10 sec.) --- 260°C
- Storage Temperature Range --- −65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) -- 2kV
  MM (Machine Model) --- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, PVCCR = PVCCL -- 8V to 26V
- Junction Temperature Range --- −40°C to 125°C
- Ambient Temperature Range -- −40°C to 85°C

Electrical Characteristics

(PV_{CCx} = 12V, R_L = 8Ω, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
$\overline{\text{SD}}$, GAIN0, GAIN1, MUTE Input Voltage	Logic-High	V_{IH}			3	--	--	V
	Logic-Low	V_{IL}			--	--	0.8	V
Low Level Output Voltage		V_{OL}	$\overline{\text{FAULT}}$, $R_{PULL\text{-}UP}$ = 100kΩ		--	--	0.8	V
High Level Input Current		I_{IH}	$\overline{\text{SD}}$, GAIN0, GAIN1, MUTE, V_I = 3V,		--	--	50	μA
Low Level Input Current		I_{IL}	$\overline{\text{SD}}$, GAIN0, GAIN1, MUTE, V_I = 0.8V,		--	--	10	μA
Class-D Output Offset Voltage (measured differentially)		$\|V_{OS}\|$	V_I = 0V, Gain = 36dB		--	10	25	mV
Quiescent Supply Current		I_Q	$V_{\overline{SD}}$ = 3V, no load		--	20	35	mA
Quiescent Supply Current in Shutdown Mode		I_{Q_SHDN}	$V_{\overline{SD}}$ = 0.8V, no load		--	--	2	mA
Drain-Source On-State Resistance		$R_{DS(ON)}$	I_O = 500mA, T_J = 25°C	High Side	--	250	--	mΩ
				Low Side	--	200	--	
Gain		G	V_{GAIN1} = 0.8V	V_{GAIN0} = 0.8V	19	20	21	dB
				V_{GAIN0} = 3V	25	26	27	
			V_{GAIN1} = 3V	V_{GAIN0} = 0.8V	31	32	33	
				V_{GAIN0} = 3V	35	36	37	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Turn-On Time	t_{ON}	$V_{\overline{SD}}$ = 3V	--	14	--	ms
Turn-Off Time	t_{OFF}	$V_{\overline{SD}}$ = 0.8V	--	1	--	ms
Gate Drive Supply	V_{GVDD}	I_{GVDD} = 2mA	4.5	5	5.5	V
Power Supply Ripple Rejection	PSRR	200mVPP ripple at 1kHz, Gain = 20dB, Inputs ac-coupled to AGND	--	−70	--	dB
Continuous Output Power	P_O	THD + N = 10%, f_{IN} = 1kHz, PV_{CC} = 13V	--	10	--	W
Total Harmonic Distortion + Noise	THD + N	f_{IN} = 1kHz, P_O = 5W	--	0.1	--	%
Output Integrated Noise	V_N	20Hz to 22kHz, A-weighted filter, Gain = 20dB	--	100	--	μV
			--	–80	--	dBV
Crosstalk		V_O = $1V_{RMS}$, Gain = 20dB, f_{IN} = 1kHz	--	–80	--	dB
Signal-to-Noise Ratio	SNR	Maximum output at THD + N < 1%, f_{IN} = 1kHz, Gain = 20dB, A-weighted filter	--	98	--	dB
Oscillator Frequency	f_{OSC}		220	300	380	kHz

(PV_{CCx} = 24V, R_L = 8Ω, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
$\overline{SD}$, GAIN0, GAIN1, MUTE Input Voltage	Logic-High	V_{IH}		3	--	--	V
	Logic-Low	V_{IL}		--	--	0.8	V
Low Level Output Voltage		V_{OL}	$\overline{\text{FAULT}}$, $R_{PULL-UP}$ = 100kΩ	--	--	0.8	V
High Level Input Current		I_{IH}	$\overline{SD}$, GAIN0, GAIN1, MUTE, V_I = 3V	--	--	50	μA
Low Level Input Current		I_{IL}	$\overline{SD}$, GAIN0, GAIN1, MUTE, V_I = 0.8V	--	--	10	μA
Class-D Output Offset Voltage (measured differentially)		$\|V_{OS}\|$	V_I = 0V, Gain = 36dB	--	15	30	mV
Quiescent Supply Current		I_Q	$V_{\overline{SD}}$ = 3V, No Load	--	30	50	mA
Quiescent Supply Current in Shutdown Mode		I_{Q_SHDN}	$V_{\overline{SD}}$ = 0.8V, No Load	--	--	2	mA
Gain		G	V_{GAIN1} = 0.8V, V_{GAIN0} = 0.8V	19	20	21	dB
			V_{GAIN1} = 0.8V, V_{GAIN0} = 3V	25	26	27	dB
			V_{GAIN1} = 3V, V_{GAIN0} = 0.8V	31	32	33	dB
			V_{GAIN1} = 3V, V_{GAIN0} = 3V	35	36	37	dB
PVCC Over Voltage Lockout		OVP		--	30	--	V
Turn-On Time		t_{ON}	$V_{\overline{SD}}$ = 3V	--	14	--	ms
Turn-Off Time		t_{OFF}	$V_{\overline{SD}}$ = 0.8V	--	1	--	ms
Gate Drive Supply		V_{GVDD}	I_{GVDD} = 2mA	4.5	5	5.5	V
Power Supply Ripple Rejection		PSRR	200mVPP ripple at 1kHz, Gain = 20dB, Inputs ac-coupled to AGND	--	–70	--	dB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Continuous Output Power	P_O	THD + N = 10%, f_{IN} = 1kHz, PV_{CC} = 16V	--	15	--	W
Total Harmonic Distortion + Noise	THD + N	PV_{CC} = 16V, f_{IN} = 1kHz, P_O = 7.5W (half-power)	--	0.1	--	%
Output Integrated Noise	V_N	20Hz to 22kHz, A-weighted filter, Gain = 20dB	--	100	--	μV
			--	–80	--	dBV
Crosstalk		V_O = 1V_{RMS}, Gain = 20dB, f_{IN} = 1kHz	--	–80	--	dB
Signal-to-Noise Ratio	SNR	Maximum output at THD + N < 1%, f_{IN} = 1kHz, Gain = 20dB, A-weighted filter	--	98	--	dB
Oscillator Frequency	f_{OSC}		220	300	380	kHz
Thermal Trip Point	T_{SD}		--	170	--	°C
Thermal Hysteresis	ΔT_{SD}		--	15	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

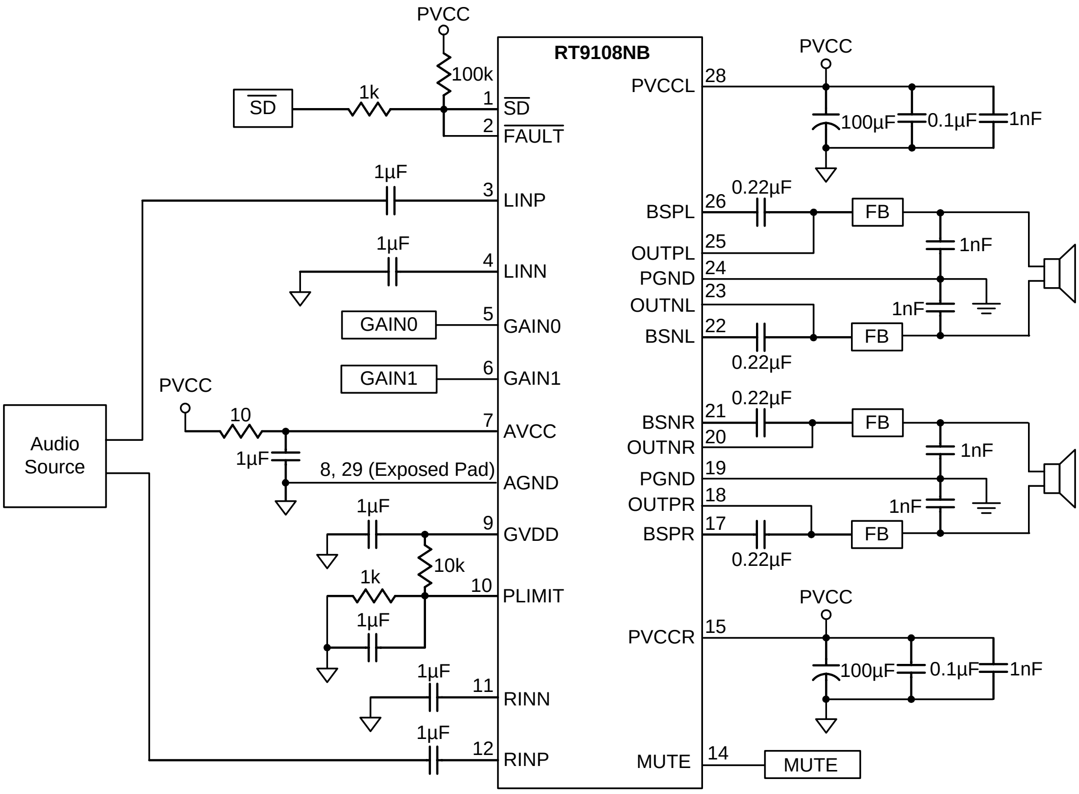


Figure 1. Typical Application Circuit

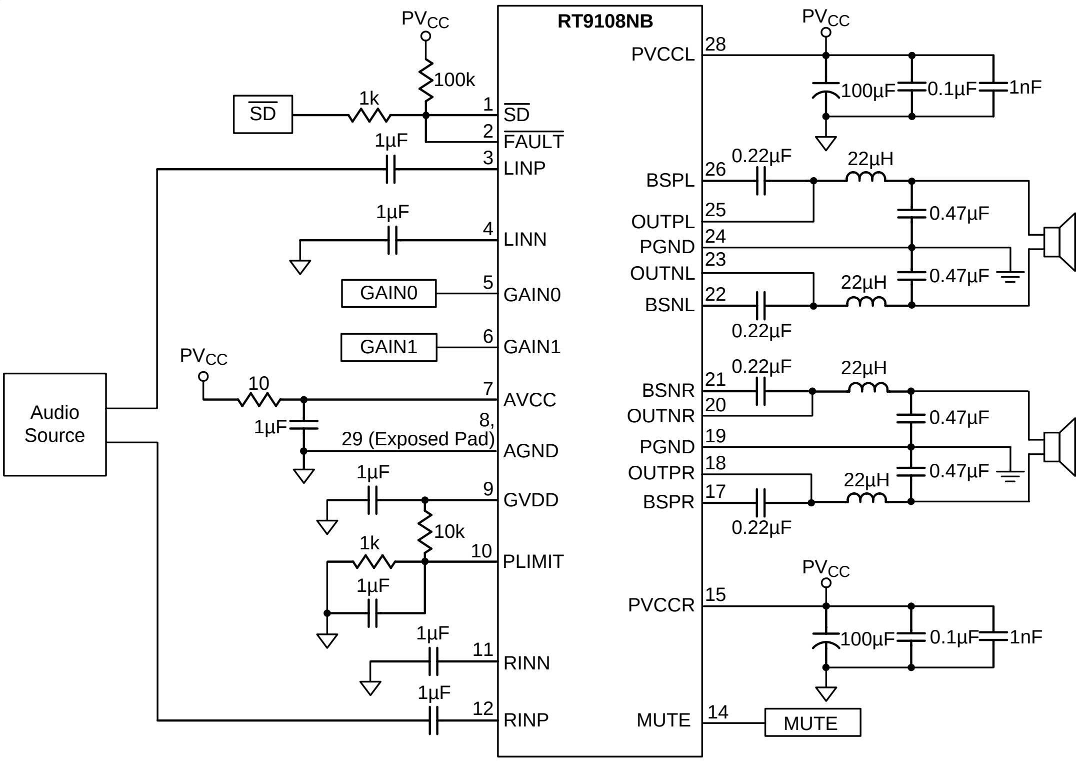
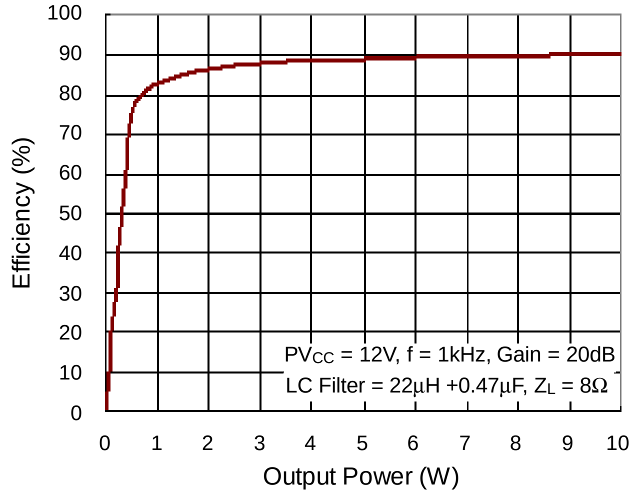


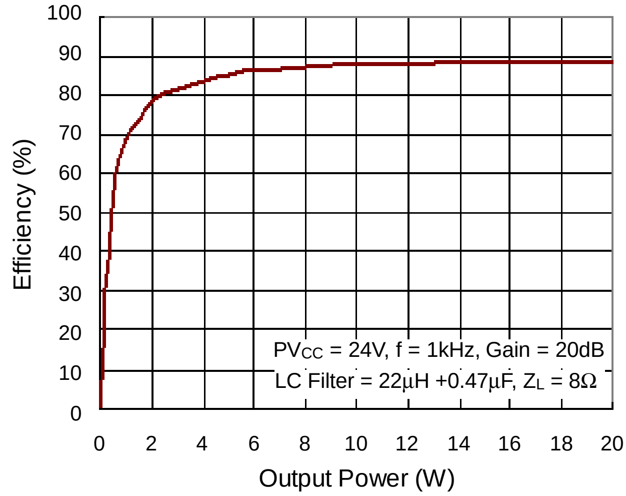
Figure 2. Typical LC Output Filter

Typical Operating Characteristics

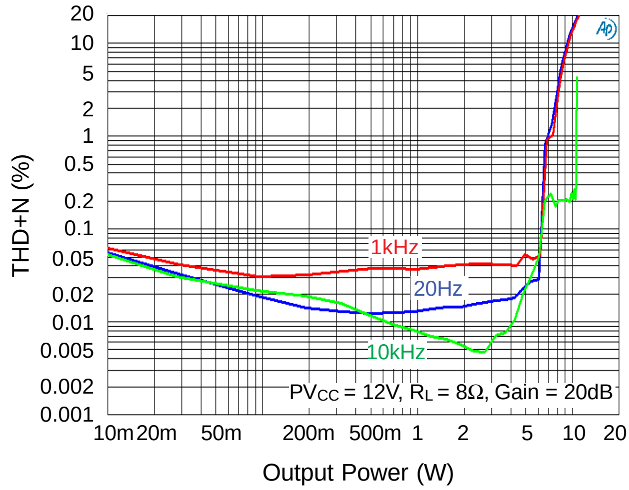
Efficiency vs. Output Power



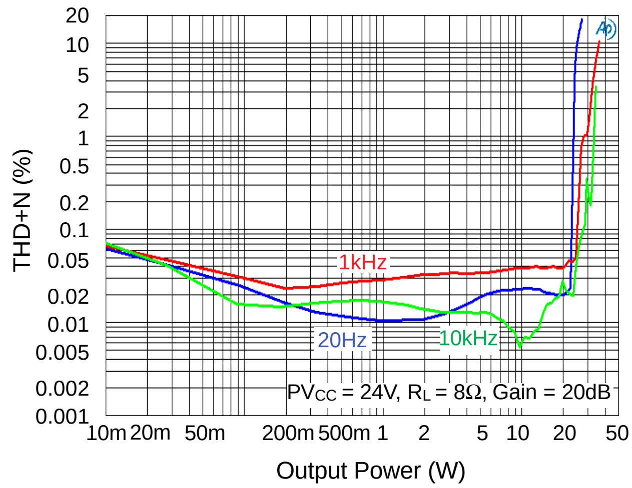
Efficiency vs. Output Power



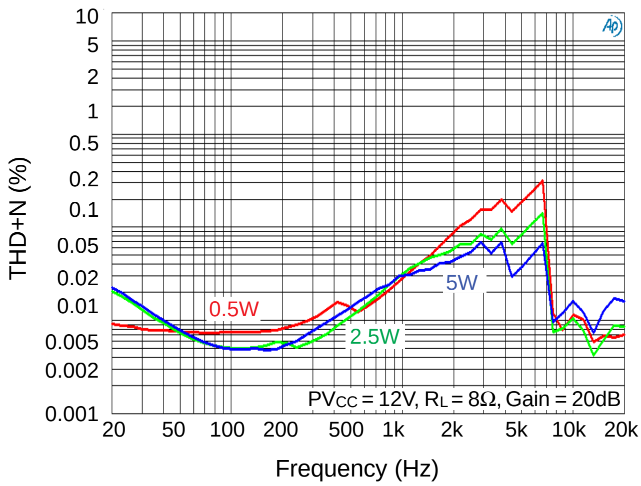
THD+N vs. Output Power



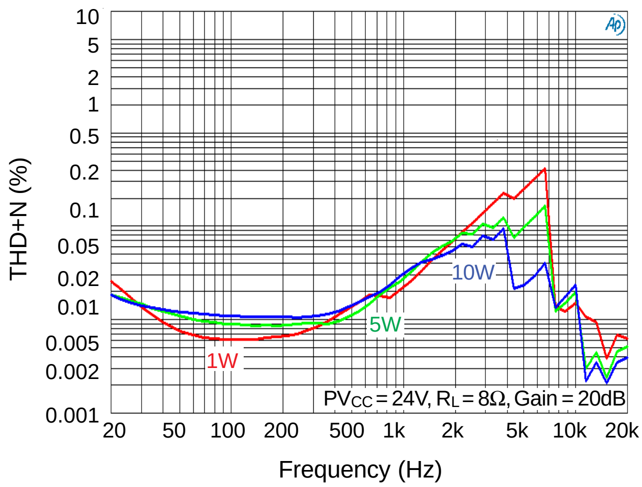
THD+N vs. Output Power



THD+N vs. Frequency



THD+N vs. Frequency



Application Information

Amplifier Gain Setting

The gain of the RT9108NB amplifier can be set by two input terminals, GAIN0 and GAIN1, shown as Table 1.

The gain setting is realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by the ratios of the resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

Table 1. Gain Setting

GAIN1	GAIN0	Amplifier GAIN (dB)	Input Impedance (kΩ)
		Typ	Typ
0	0	20	56
0	1	26	28
1	0	32	14
1	1	36	8.75

$\overline{SD}$ Operation

The RT9108NB employs a shutdown mode operation designed to reduce supply current (I_{CC}) to the absolute minimum level for power saving. The $\overline{SD}$ input terminal should be held high (see specification table for trip point) in normal operation. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low current state. Leaving $\overline{SD}$ floating will cause the amplifier operation to be unpredictable. Never leave $\overline{SD}$ pin unconnected!

For the best power-off pop performance, turn off the amplifier in the shutdown mode prior to removing the power supply voltage.

GVDD Supply

The GVDD is used to supply the Gate Drivers for the output full bridge transistors. Connect a 1μF capacitor from this pin to ground for good bypass. The typical GVDD output voltage is 5V.

Short Circuit Protection and Automatic Recovery

The RT9108NB has protection from over current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the $\overline{FAULT}$ pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. The latch can be cleared by cycling the $\overline{SD}$ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the $\overline{FAULT}$ pin directly to the $\overline{SD}$ pin. This allows the $\overline{FAULT}$ pin function to automatically drive the $\overline{SD}$ pin low which clears the short-circuit protection latch.

Thermal Protection

Thermal protection on the RT9108NB prevents damage to the device when the internal die temperature exceeds 170°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15°C. The device begins normal operation at this point with no external system interaction.

Thermal protection faults are NOT reported on the $\overline{FAULT}$ terminal.

Power Limit

The voltage at pin 10 can used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also add a 1uF capacitor from pin 10 to ground.

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. This "virtual" rail is 5 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power}$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and any resistance in the output filter.

R_L is the load resistance.

V_P is the peak amplitude of the output possible within the supply rail.

$V_P = 5 \times$ PLIMIT voltage if PLIMIT $< 5 \times V_P$

P_{OUT} (10%THD) = $1.25 \times P_{OUT}$ (unclipped)

PLIMIT Typical Operation with RT9108NB

Test Conditions ()	PLIMIT Voltage	Output Power (W)	Output Voltage Amplitude (V_{P-P})
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=26dB	GVDD	36.3 (thermally limited)	46
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=26dB	2.94	18.5	31.8
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=26dB	2.34	12.3	25.5
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=26dB	1.62	6.2	18.2
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=20dB	GVDD	11.6	29.6
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=20dB	3.00	10.4	26.6
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=20dB	1.86	5.2	17.3
PVCC=12V, Vin=1Vrms, RL=8Ω, Gain=20dB	GVDD	9.35	23.4
PVCC=12V, Vin=1Vrms, RL=8Ω, Gain=20dB	1.76	5	16.4

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For TSSOP-28 (Exposed Pad) packages, the thermal resistance, θ_{JA}, is 28°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (28°C/W) = 3.571W for TSSOP-28 (Exposed Pad) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J\ (MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

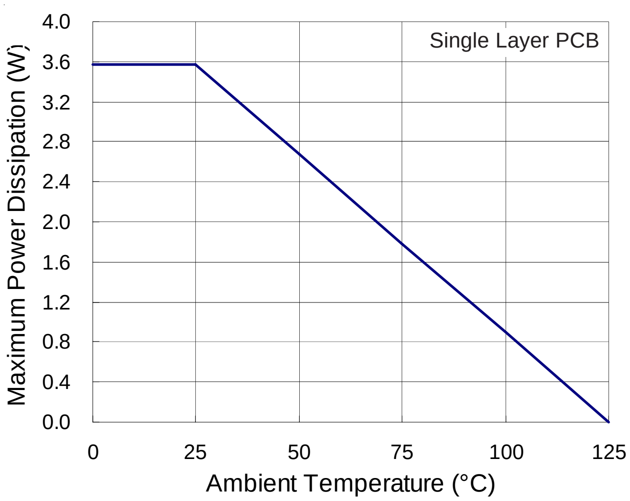


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

For the best performance of the RT9108NB, the below PCB Layout guidelines must be strictly followed.

- Place the decoupling capacitors as close as possible to the AVCC, PVCCL, PVCCR and GND pins. For achieving a good quality, consider adding a small, good performance low ESR ceramic capacitor between 220pF and 1000pF and a larger mid-frequency capacitor between 0.1μF and 1μF to the PVCC pins of the chip. Do not trace out the NC pins (Pin13, 16 and Pin27) to avoid the pin short issue.
- Keep the differential output traces as wide and short as possible.
- The traces of (LINP & LINN, RINP & RINN) and (OUTPL & OUTNL, OUTPR & OUTNR) should be kept equal width and length respectively.
- The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be larger for application. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB.

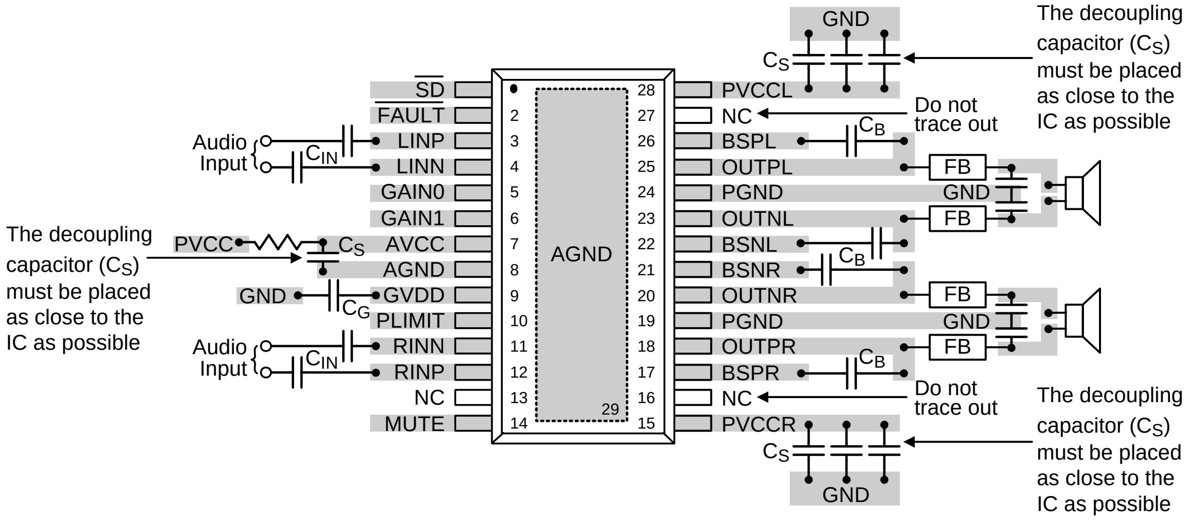
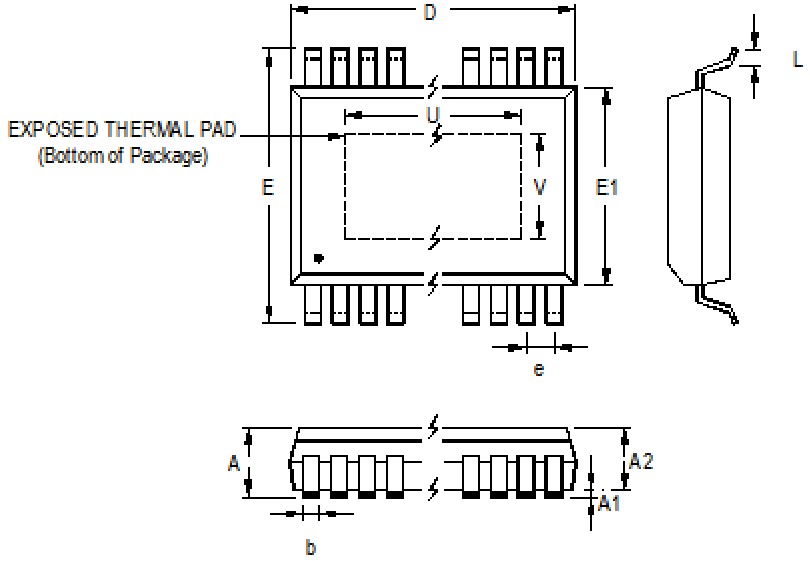


Figure 4. PCB Layout Guide

Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		1.000	1.200	0.039	0.047
A1		0.000	0.150	0.000	0.006
A2		0.800	1.050	0.031	0.041
b		0.190	0.300	0.007	0.012
D		9.600	9.800	0.378	0.386
e		0.650		0.026	
E		6.300	6.500	0.248	0.256
E1		4.300	4.500	0.169	0.177
L		0.450	0.750	0.018	0.030
Option 1	U	4.410	5.510	0.174	0.217
	V	2.400	3.000	0.094	0.118
Option 2	U	5.500	6.170	0.217	0.243
	V	1.600	2.210	0.063	0.087
Option 3	U	5.800	6.200	0.228	0.244
	V	2.600	3.000	0.102	0.118

28-Lead TSSOP (Exposed Pad) Plastic Package

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Datasheet Revision History

Version	Data	Page No.	Item	Description
P00	2012/9/27			first edition
P01	2013/4/19			datasheet modify