RICHTEK®

RT9123

3.2W Mono I^{2}S Input Class-D Audio Amplifier, Budget-Friendly, Effortless Boot, Ultra-Low Quiescent Current

1 General Description

The RT9123 is a mono Class-D amplifier that features high efficiency and performance. In addition to I^{2}C control, the RT9123 also features a "HW Control Mode" selection for the I^{2}S/TDM interface. This mode simplifies the amplifier driver, as it does not require I^{2}C commands to turn on or off the device. The digital audio interface supports various formats, including I^{2}S, left justified, right justified, and 8-channel time division multiplexed (TDM) formats.

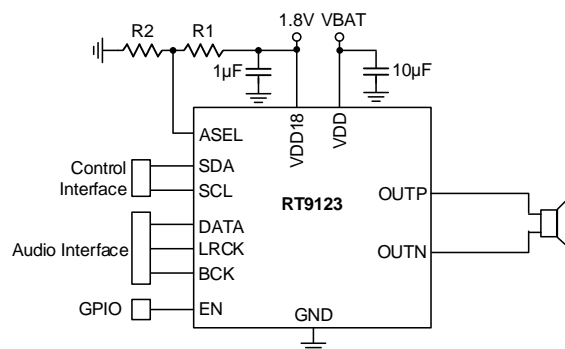The recommended junction temperature range is −40°C to 125°C, and the ambient temperature range is −40°C to 85°C.

2 Applications

- Smartphones, Tablets
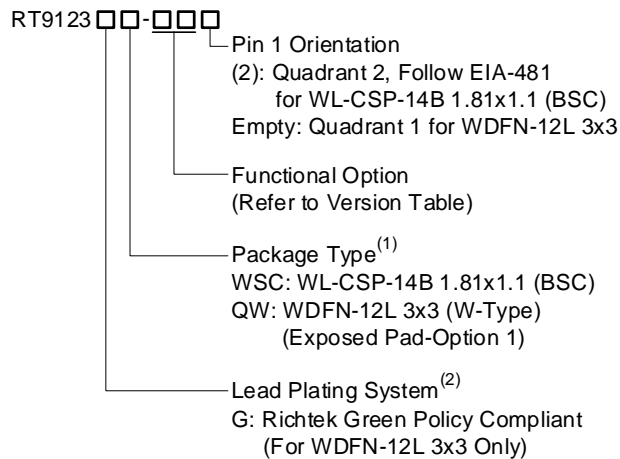- Personal Media Players/Portable TVs
- Game Players/Cameras

3 Features

- **Class-D Speaker AMP**
  - **3.2W Output Power @ 4Ω Load, THD < 10%**
  - **8μV Output Noise**
  - **Low Shutdown Current**
  - **Add DRE to Reduce Output Noise**
  - **Spread Spectrum Frequency**
  - **Fast Turn-On Time: 1ms**
  - **Support HW Control Mode without Driver and I^{2}C Controlled**
  - **Silence Data Detection**
  - **Beep Function**
- **Audio Interface**
  - **Digital Audio Interface Support I^{2}S, Left-Justified, Right-Justified, TDM**
  - **Support 8/16/20/24/32 Bit Data Length and 8kHz to 96kHz Sample Rate**
- **Digital**
  - **Volume Control**
  - **Clipping Reduce Gain Control**
- **Protection**
  - **OCP: Detects High Current Levels to Disable the Analog Blocks for 100ms**
  - **VDD UVP: Disables the Analog Blocks when the Battery Voltage Falls Below 2.2V**
  - **VDD18 UVP: Disables the Analog Blocks when the Battery Voltage Falls Below 1.4V**
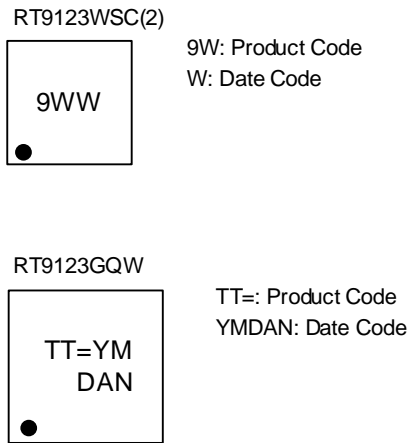 - **OTP: Disables the Analog Block when the IC Temperature Exceeds 150°C**

4 Simplified Application Circuit

5 Ordering Information

RT9123□□-□□□

└─ Pin 1 Orientation
(2): Quadrant 2, Follow EIA-481
for WL-CSP-14B 1.81x1.1 (BSC)
Empty: Quadrant 1 for WDFN-12L 3x3

└─ Functional Option
(Refer to Version Table)

└─ Package Type[1]
WSC: WL-CSP-14B 1.81x1.1 (BSC)
QW: WDFN-12L 3x3 (W-Type)
(Exposed Pad-Option 1)

└─ Lead Plating System[2]
G: Richtek Green Policy Compliant
(For WDFN-12L 3x3 Only)

Note 1.

● Marked with [1] indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.

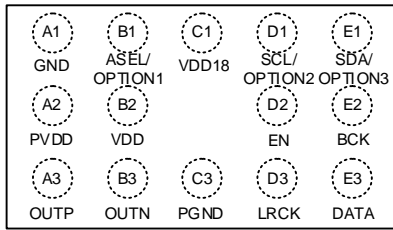● Marked with [2] indicated: Richtek products are Richtek Green Policy compliant.

6 Marking Information

RT9123WSC(2)

9WW

9W: Product Code
W: Date Code

RT9123GQW

TT=YM
DAN

TT=: Product Code
YMDAN: Date Code

7 RT9123 Version Table

RT9123 Current Release Version			RT9123 Customized Setting		
Part Number	Spread Spectrum	Volume Ramp	Clipping Automatic Gain Control	Audio Format (I^2S/Left-Justify)	Silence Detection
RT9123WSC-2C RT9123GQW-2C	ON	ON (5.3ms)	OFF	I^2S	ON
RT9123WSC-2E RT9123GQW-2E	ON	OFF (1ms)	OFF	I^2S	ON
RT9123WSC-A4 RT9123GQW-A4	OFF	ON (5.3ms)	OFF	I^2S	ON
RT9123WSC-A6 RT9123GQW-A6	OFF	OFF (1ms)	OFF	I^2S	ON

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8 Pin Configuration

(TOP VIEW)

WL-CSP-14B 1.81x1.1 (BSC)
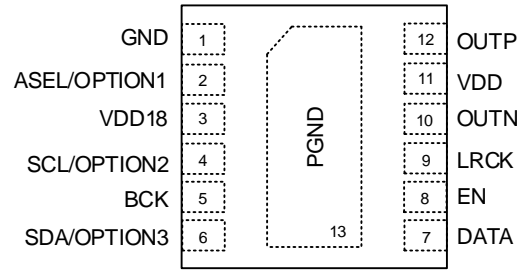
WDFN-12L 3x3

9 Functional Pin Description

Pin No.		Pin Name	Type	Pin Function
WL-CSP-14B 1.81x1.1 (BSC)	WDFN-12L 3x3			
A1	1	GND	G	Ground
A2	--	PVDD	P	Supply for the Class-D amplifier
A3	12	OUTP	O	Positive Class-D amplifier output
B1	2	ASEL/OPTION1	I	Address/gain selection (5 steps)
B2	11	VDD	P	Supply for analog power
B3	10	OUTN	O	Negative Class-D Amplifier output
C1	3	VDD18	P	Supply for IO power
C3	13	PGND	G	Power ground
D1	4	SCL/OPTION2	I	I^2C clock signal input/channel selection
D2	8	EN	I	Chip enable pin
D3	9	LRCK	I	I^2S date frame signal input
E1	6	SDA/OPTION3	I/O	I^2C data signal input/channel selection
E2	5	BCK	I	I^2S bit clock signal input
E3	7	DATA	I	I^2S data signal input

9.1 IO Type Definition

- P: Power Pin
- G: Ground Pin
- O: Output Pin
- I: Input Pin
- I/O: Input/Output Pin

10 Functional Block Diagram
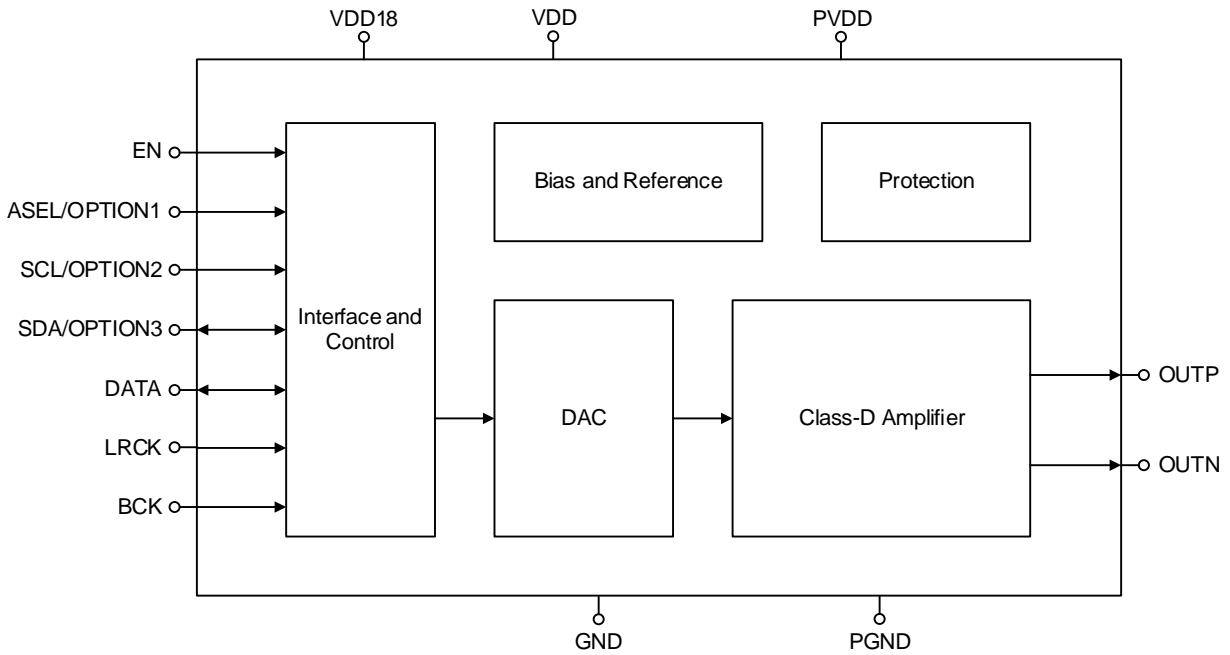
11 Absolute Maximum Ratings

(Note 2)

- VDD, PVDD--−0.3V to 6V
- OUTP, OUTN--−0.3V to 6V
- VDD18 --−0.3V to 2.5V
- LRCK, BCK, DATA, SCL/OPTION2, SDA/OPTION3, EN-------------------------------------−0.3V to 5V
- ASEL/OPTION1 ---−0.3V to 2.5V
- Power Dissipation, P_D @ T_A= 25°C

  WL-CSP-14B 1.81x1.1 (BSC)-- 3.89W

  WDFN-12L 3x3--- 3.24W
- Package Thermal Resistance   (Note 3)

  WL-CSP-14B 1.81x1.1 (BSC), θ_{JA}--- 25.7°C/W

  WDFN-12L 3x3, θ_{JA} -- 30.8°C/W

  WDFN-12L 3x3, θ_{JC} -- 5.4°C/W
- Junction Temperature --- 150°C
- Lead Temperature (Soldering, 10sec.)--260°C
- Storage Temperature Range --−65°C to 150°C
- ESD Susceptibility   (Note 4)

  HBM (Human Body Model) --- 2kV

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 5)

- Junction Temperature Range--−40°C to 125°C
- Ambient Temperature Range--−40°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

13 Electrical Characteristics

(VDD = 5V, VDD18 = 1.8V, load = 8Ω + 33μH, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System Performance						
Operating Condition	VDD		2.5	5.0	5.5	V
	VDD18		1.71	1.8	1.98	
Quiescent Current	I_VDD	BCK/LRCK on, DATA silence (Silence detection = disable)	--	1.78	2.83	mA
	I_VDD18	BCK/LRCK on, DATA silence (Silence detection = disable)	--	0.94	1.5	
Silence Mode Current	I_VDD silence	BCK/LRCK on, DATA silence (Silence detection = enable)	--	0.05	--	mA
	I_VDD18 silence	BCK/LRCK on, DATA silence (Silence detection = enable)	--	0.50	--	
SUSP Mode Current	I_VDD SUSP	BCK/LRCK/DATA at 0V	--	1	--	μA
	I_VDD18 SUSP	BCK/LRCK/DATA at 0V	--	10	--	
Shutdown Current	I_VDD SD	BCK/LRCK/DATA at 0V, EN = 0V	--	1	--	μA
	I_VDD18 SD	BCK/LRCK/DATA at 0V, EN = 0V	--	1	--	
Output Stage On-Resistance	R_{ON}	PMOS+NMOS	--	340	--	mΩ
Turn-On Time	t_{ON}	From SUSP to full gain output Sample rate = 48kHz	--	--	1	ms
Beep Sound_I^{2}C Control Mode	f_{SW_Beep}	ASEL/OPTION1 = 0V, Selection I	175	200	225	Hz
		ASEL/OPTION1 = 0V, Selection II (Default)	350	400	450	
		ASEL/OPTION1 = 0V, Selection III	700	800	900	
		ASEL/OPTION1 = 0V, Selection IV	850	1000	1150	
Beep Sound_HW Control Mode	f_{SW_Beep}	ASEL/OPTION1 = 0V	350	400	450	Hz
Analog Performance						
Output Power	P_{OUT}	THD + N < 10% @ 4Ω + 33μH	--	3.2	--	W
	P_{OUT}	THD + N < 10% @ 8Ω + 33μH	--	1.8	--	
Full-Scale Output Voltage		Gain = 0dB	0.94	1	1.06	Vrms
		Gain = 12dB (default) VDD/VDDP = 5.5V	3.6	--	3.85	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Gain	Gain	Analog (Class-D)	0	--	13.5	dB
		Step	--	1.5	--	
		Error	−0.5		0.5	
		Digital (Volume)	−103	--	24	
		Step	--	0.0625	--	
Signal to Noise Ratio	SNR	A-Weighting, THD + N Po = 1% Input: silence	--	120	--	dB
Dynamic Range	DR	A-Weighting @ THD + N Po = 1% Input: −60dBFs @ 8Ω + 33µH	--	112	--	dB
Total Harmonic Distortion + Noise	THD+N $_{1kHz}$	POUT = 1W @ 4Ω + 33µH	--	0.02	--	%
		POUT = 0.5W @ 8Ω + 33µH	--	0.02	--	
		POUT = 50mW @ 8Ω + 33µH	--	0.012	--	
Power Supply Rejection Ratio	PSRR$_{VDD}$	217Hz, VDD ripple = 200mVpp	--	85	--	dB
	PSRR$_{VDD}$	10kHz, VDD ripple = 200mVpp	--	82	--	
	PSRR$_{VDD18}$	217Hz, VDD18 ripple = 15mVpp	--	87	--	
Output Noise	V$_N$	A-weighted, 24/32-bit DATA	--	8	--	µV$_{rms}$
Output Offset Voltage	V$_{OS}$	DC offset	−1	--	1	mV
Class-D Switch Frequency	f$_{SW}$		--	--	450	kHz
Frequency Response	FR	20Hz to 20kHz	−0.5	--	0.5	dB
Efficiency	Eff	THD + N = 10% @ 8Ω + 33µH	--	92.5	--	%
Protect Performance						
Undervoltage Protection	UVP$_{VDD}$	VDD falling	2.1	2.2	2.3	V
		Hysteresis rising	--	0.15	--	V
	UVP$_{VDD18}$	VDD18 falling	1.3	1.4	1.5	V
		Hysteresis rising	--	0.15	--	V
Over-Temperature Protection	OTP	Temperature rising	--	150	--	°C
		Hysteresis falling	--	25	--	°C
Overcurrent Protection	OCP	VDD = 5V	--	2.8	--	A
		Auto-recovery time	--	100	--	ms
I^{2}C Interface Electrical Characteristics						
High-Level Input Voltage	V$_{IH}$		1.26	--	--	V
Low-Level Input Voltage	V$_{IL}$		--	--	0.54	V
Pull-Down Current	I$_{FO2}$		--	2	--	uA
Digital Output Low (SDA)	V$_{OL}$	I$_{PULL-UP}$ = 3mA	--	--	0.4	V
Clock Operating Frequency	f$_{SCL}$		--	--	400	kHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Bus Free Time Between Stop and Start Condition	t_{BUF}		1.3	--	--	μs
Hold Time After (Repeated) Start Condition	$t_{HD,STA}$		0.6	--	--	μs
Repeated Start Condition Setup Time	$t_{SU,STA}$		0.6	--	--	μs
Stop Condition Time	$t_{SU,STD}$		0.6	--	--	μs
Data Hold Time	$t_{HD,DAT}$ (OUT)		225	--	--	ns
Input Data Hold Time	$t_{HD,DAT}$ (IN)		0	--	900	ns
Data Setup Time	$t_{SU,DAT}$		100	--	--	ns
Clock Low Period	t_{LOW}		1.3	--	--	μs
Clock High Period	t_{HIGH}		0.6	--	--	μs
Clock Data Fall Time	t_F		20	--	300	ns
Clock Data Rise Time	t_R		20	--	300	ns
Spike Suppression Time	t_{SP}		--	--	50	ns
I²S / TDM Interface						
High-Level Input Voltage	V_{IH}		1.26	--	--	V
Low-Level Input Voltage	V_{IL}		--	--	0.54	V
Setup Time FS to BCK Rising Edge	t_{SU1}		10	--	--	ns
Hold Time FS from BCK Rising Edge	t_{SU1}		10	--	--	ns
Setup Time DATAI to BCK Rising Edge	t_{SU2}		10	--	--	ns
Hold Time DATAI from BCK Rising Edge	th2		10	--	--	ns
Rise Time for BCK/LRCLK	tr	10% - 90 % rise time	--	--	8	ns
Fall Time for BCK/LRCLK	tr	90% - 10 % fall time	--	--	8	ns
Sample Rate	fs	Sample rate	8	--	96	kHz
Bit Clock	BCK	Bit clock	0.256	--	24.576	MHz
Delay Time	DIN to BCLK Setup Time	Delay time	10	--	--	ns
Jitter Tolerance	BCK/LRCK	Jitter tolerance	--	12	--	ns
TDM Device Channel			--	8	--	CH

14 Typical Application Circuit

14.1 Mono Speaker with I²C Control Mode with Address 0x5E'h
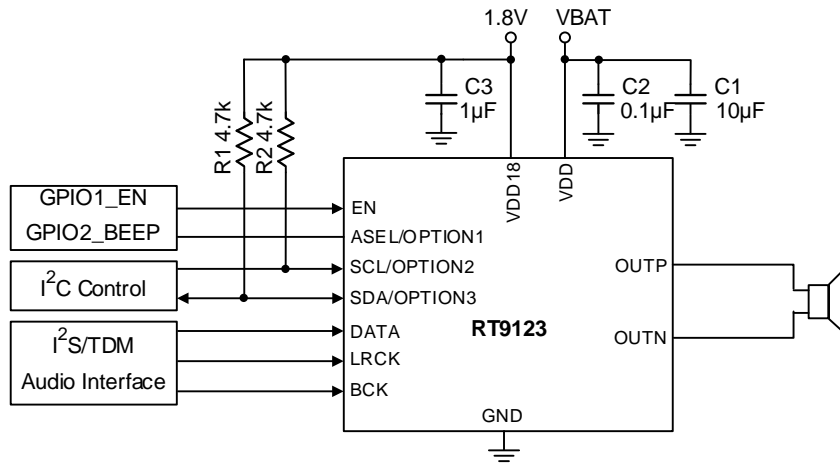
14.2 Stereo Speaker with I²C Control Mode with Address 0x5C'h and 0x5E'h
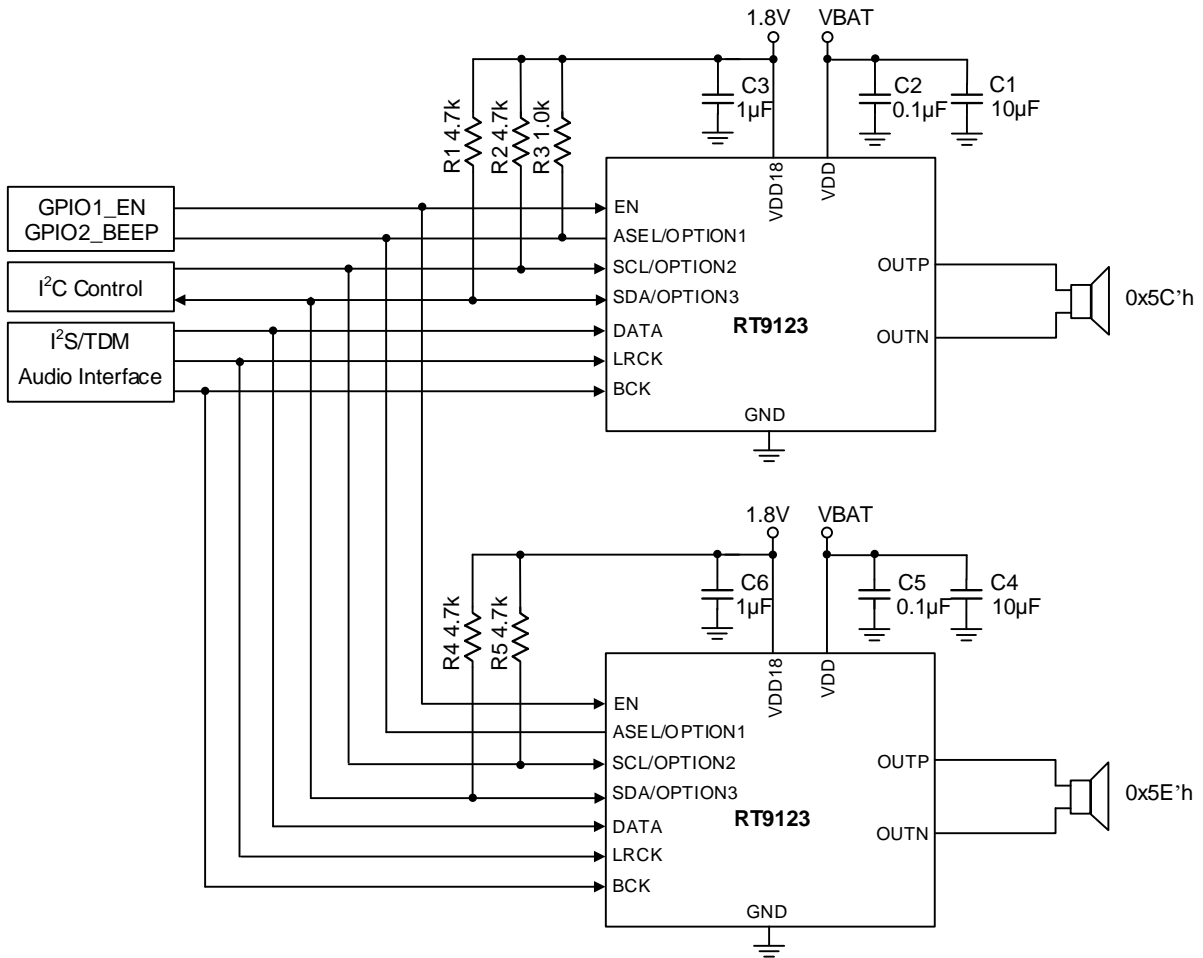
14.3 Mono Speaker with HW Control Mode (Gain = 12.0dB)
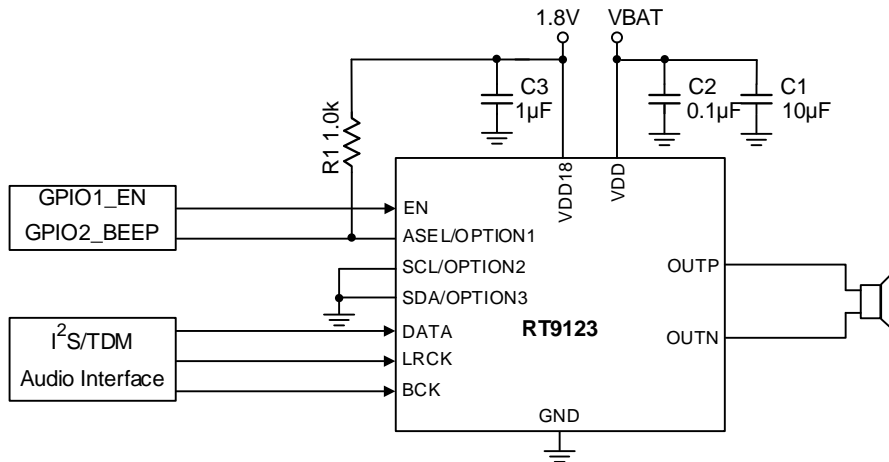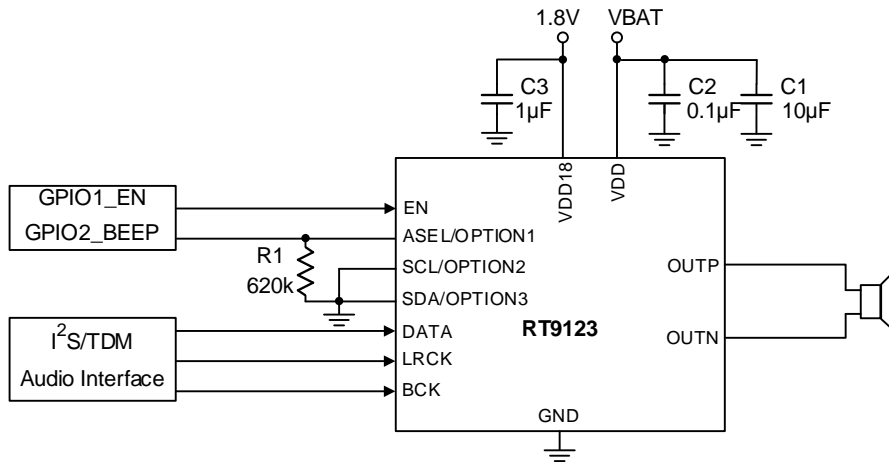

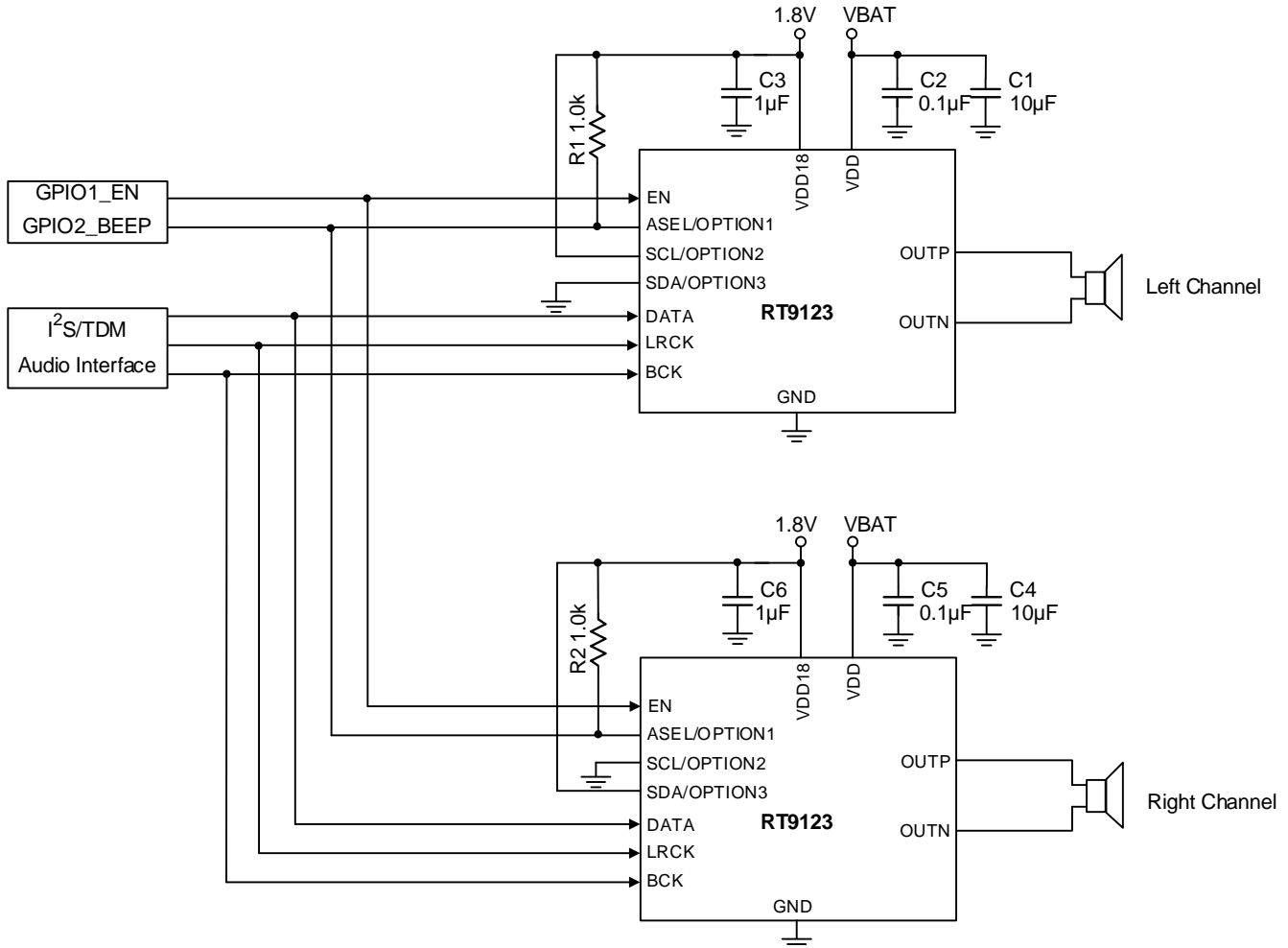### 14.4 Mono Speaker with HW Control Mode (Gain = 10.5dB)
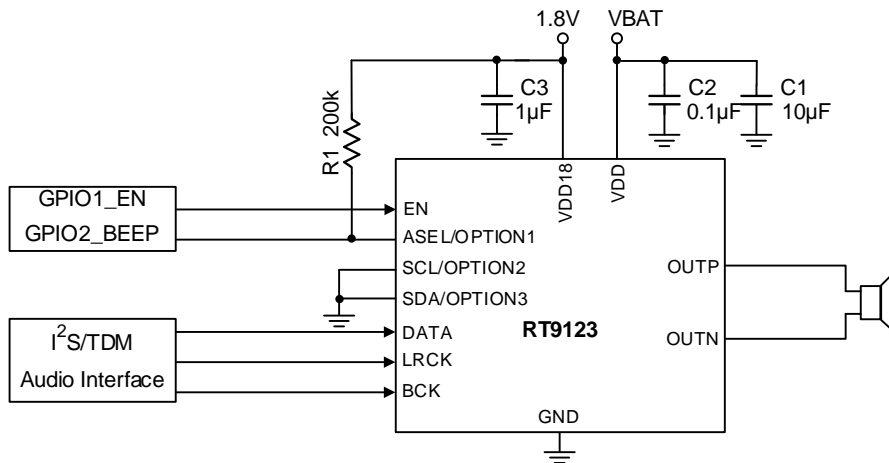
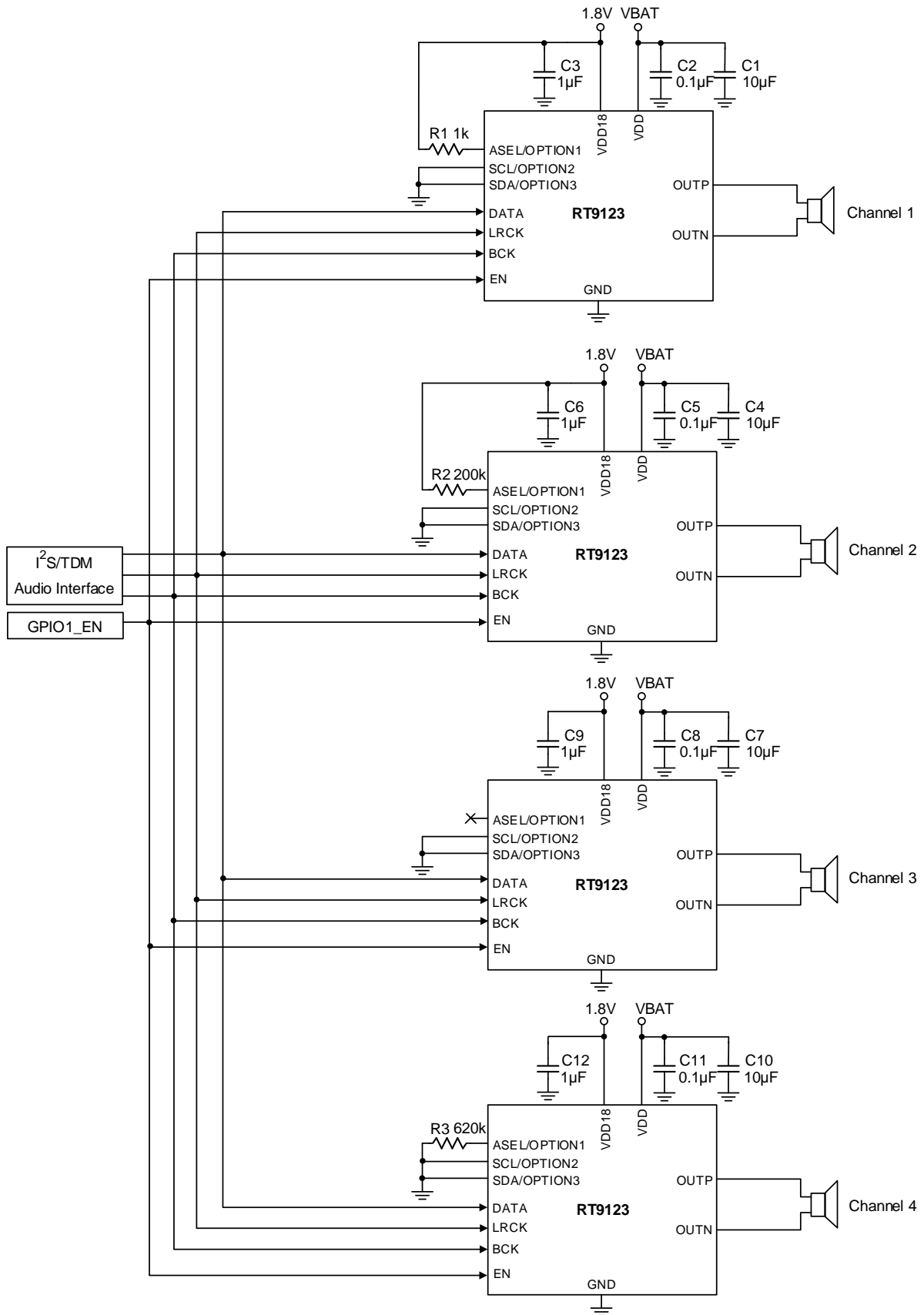### 14.5 Mono Speaker with HW Control Mode (Gain = 9.0dB)
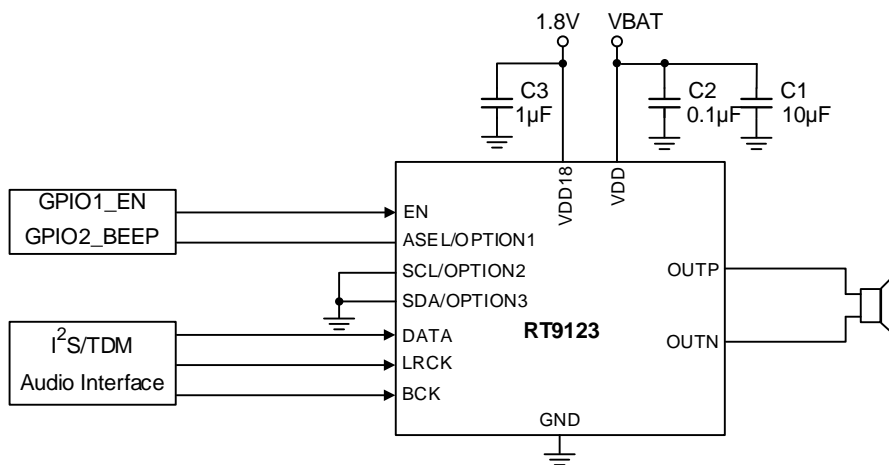
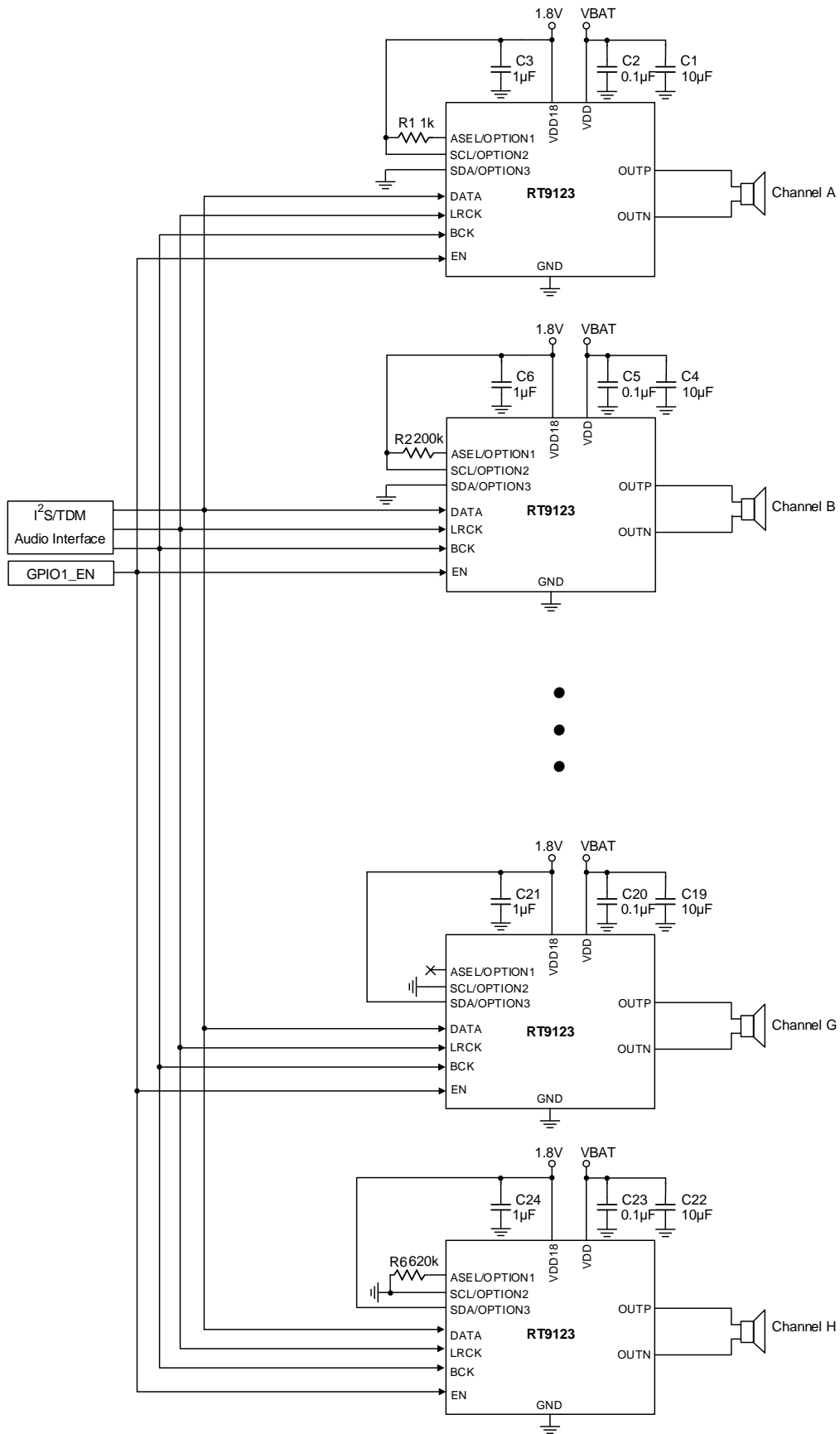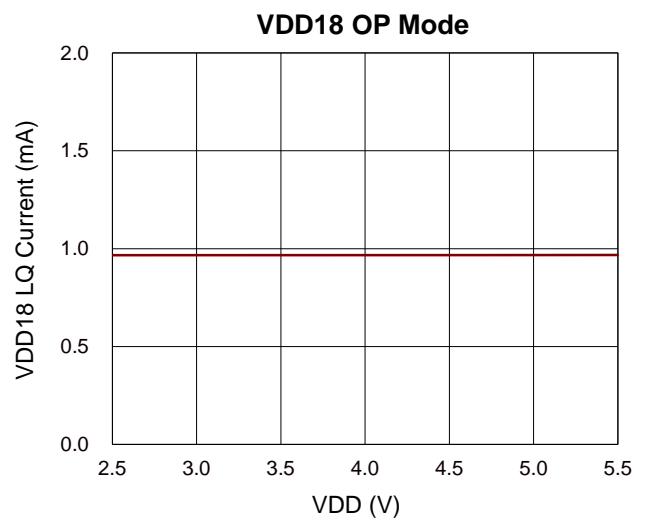## 14.6 Mono Speaker with HW Control Mode (Gain = 7.5dB)

14.7 Stereo Speaker with HW Control Mode (Gain = 12.0dB)
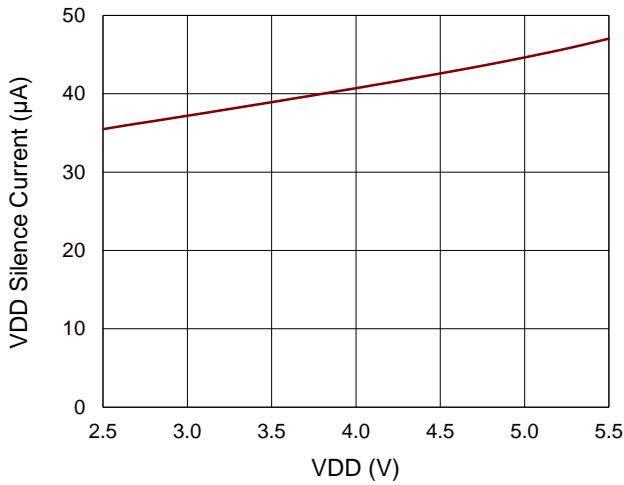
14.8 4-Channel TDM with HW Control Mode (Gain = 12.0dB)

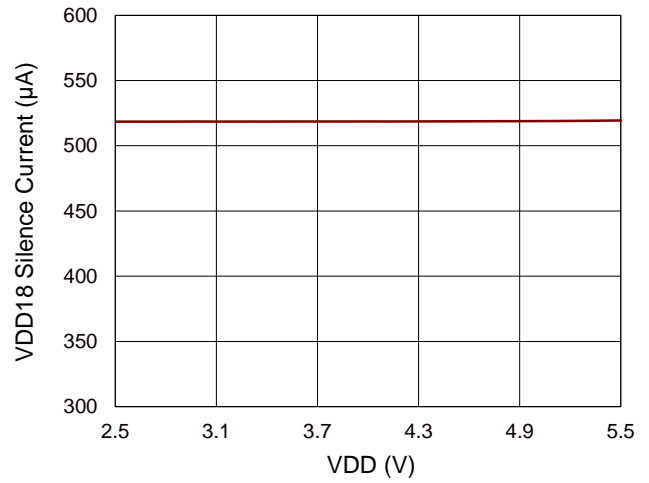## 14.9 8-Channel TDM with HW Control Mode (Gain = 12.0dB)
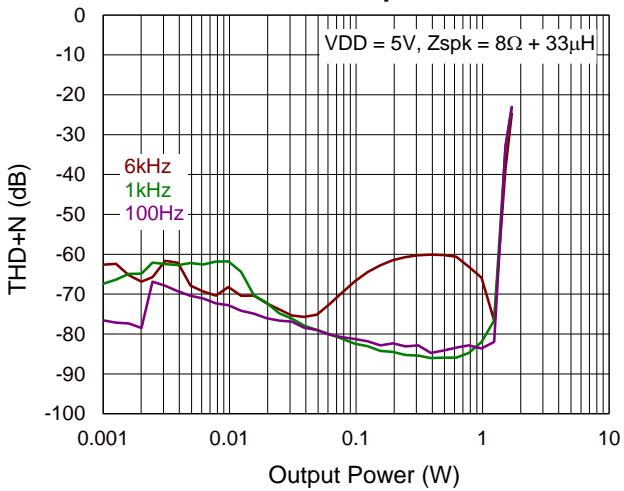
15 Typical Operating Characteristics

VDD SUSP Current vs. VDD

VDD18 SUSP Current vs. VDD

VDD SD Current vs. VDD

VDD18 SD Current vs. VDD

VDD OP Mode

VDD18 OP Mode
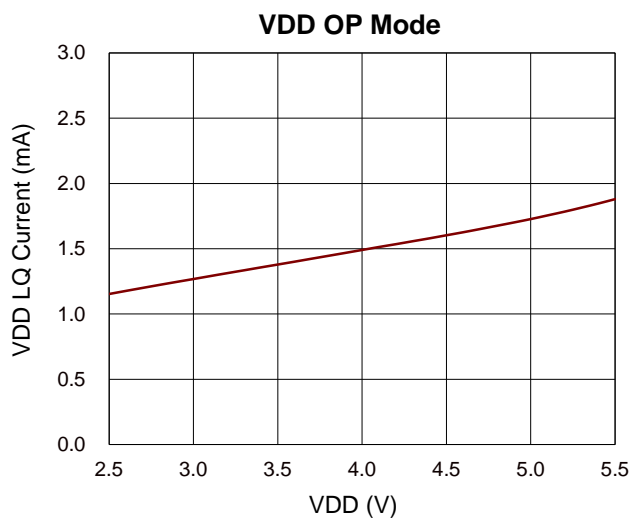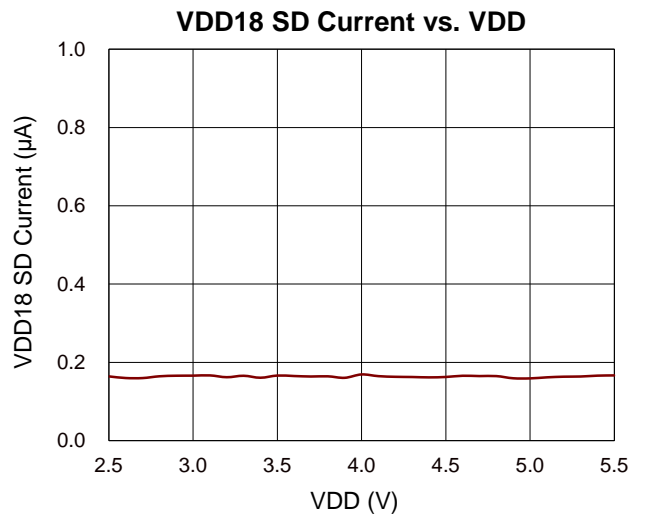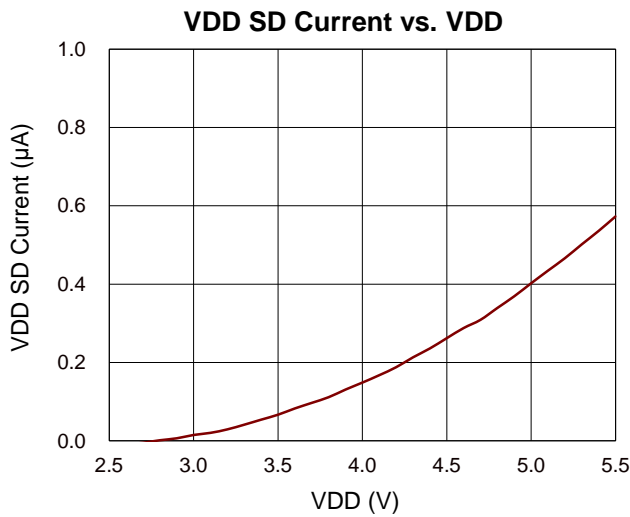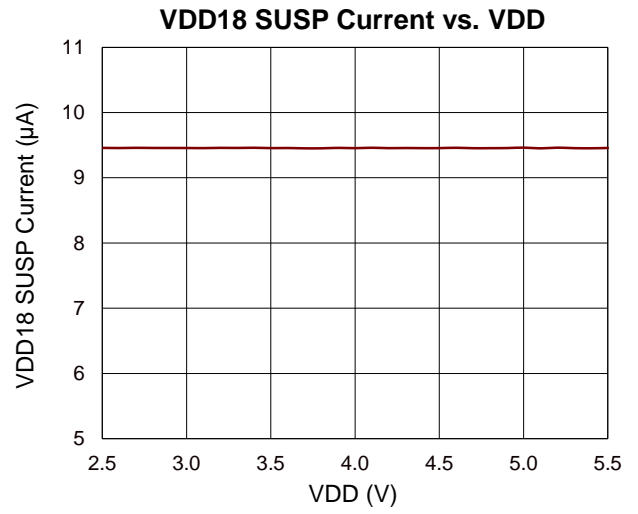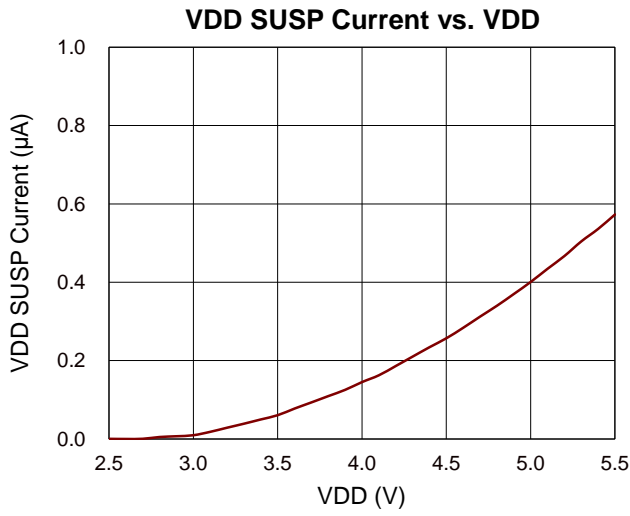
VDD Silence Current vs. VDD

VDD18 Silence Current vs. VDD

THD+N vs. Output Power

VDD = 5V, Zspk = 8Ω + 33µH

6kHz
1kHz
100Hz

THD+N vs. Output Power

VDD = 4.2V, Zspk = 8Ω + 33µH

6kHz
1kHz
100Hz

THD+N vs. Output Power

VDD = 3.7V, Zspk = 8Ω + 33µH

6kHz
1kHz
100Hz

THD+N vs. Output Power

VDD = 5V, Zspk = 4Ω + 33µH

6kHz
1kHz
100Hz

THD+N vs. Output Power

VDD = 4.2V, Zspk = 4Ω + 33μH

6kHz
1kHz
100Hz

THD+N (dB)

Output Power (W)

THD+N vs. Output Power

VDD = 3.7V, Zspk = 4Ω + 33μH

6kHz
1kHz
100Hz

THD+N (dB)

Output Power (W)

THD+N vs. Frequency

VDD = 5V, Zspk = 8Ω + 33μH

140mW
730mW

THD+N (dB)

Frequency (Hz)

THD+N vs. Frequency

VDD = 4.2V, Zspk = 8Ω + 33μH

100mW
510mW

THD+N (dB)

Frequency (Hz)

THD+N vs. Frequency

VDD = 3.7V, Zspk = 8Ω + 33μH

80mW
400mW

THD+N (dB)

Frequency (Hz)

THD+N vs. Frequency

VDD = 5V, Zspk = 4Ω + 33μH

1.3mW
260mW

THD+N (dB)

Frequency (Hz)

THD+N vs. Frequency

VDD = 4.2V, Zspk = 4Ω + 33μH

920mW
180mW

THD+N vs. Frequency

VDD = 3.7V, Zspk = 4Ω + 33μH

140mW
700mW

Normalized Gain vs. Frequency

48k
44.1k

Normalized Gain vs. Frequency

32k
24k
16k
8k

Efficiency vs. Output Power

PVDD = 5.5V
PVDD = 5V
PVDD = 4.2V

8Ω

Efficiency vs. Output Power

PVDD = 5.5V
PVDD = 5V
PVDD = 4.2V

8Ω

Efficiency vs. Output Power
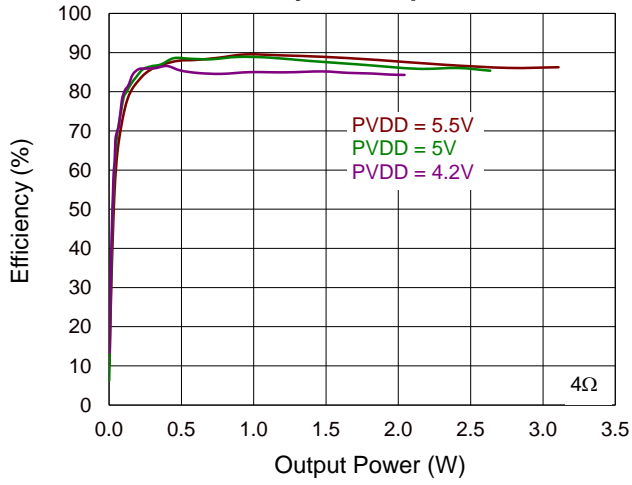
Efficiency vs. Output Power
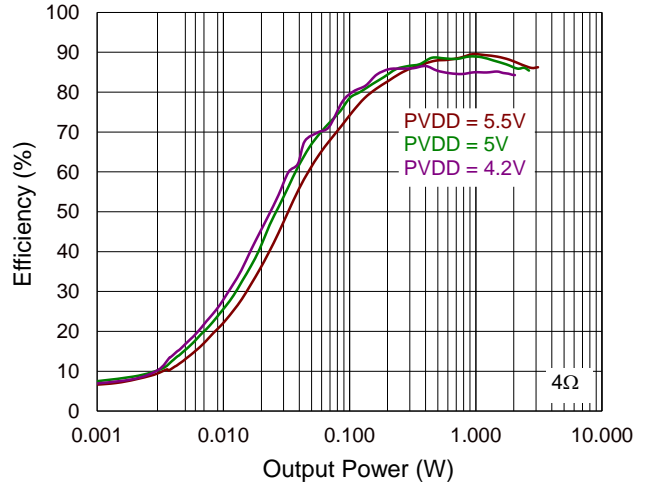
PSRR vs. Frequency

PSRR vs. Supply Power

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www.richtek.com
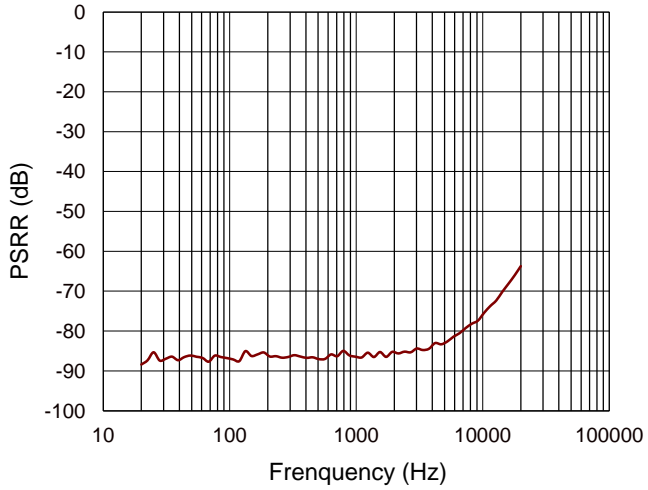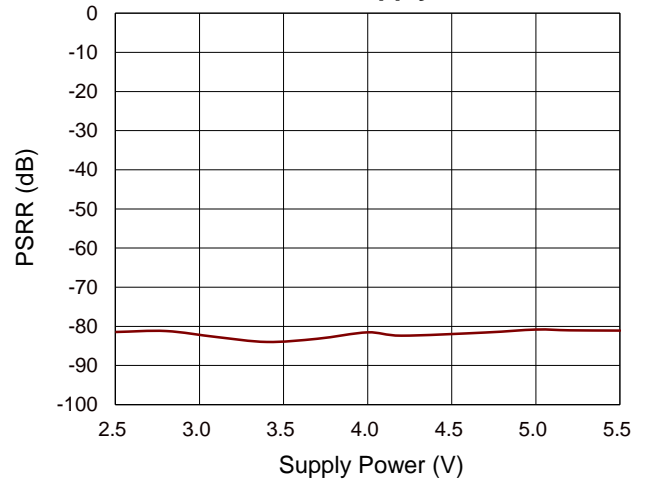
16 Application Information

([Note 6](#))

16.1 Operation Modes

The RT9123 operates in several modes, including operating, silence, suspend, power-down, and fault. The internal circuit block operational status in these different modes is depicted below.

Circuit Block \ Mode		OP	SILENCE	SUSP	FAULT	PWDN
I²C	SCL/SDA	○	○	○	○	✕
I²S	BCK/SR	○	○	✕	○	✕
I²S	DATA	○	✕	✕	○	✕
PLL	OSC_1MHz PLL	PLL	OSC_1MHz	✕	PLL	✕
AMP	Tri-Wav DAC/ADC	○	✕	✕	✕	✕
EN	EN	○	○	○	○	✕

○ : Normal operation

✕ : Power down

Table 1. Operation Mode

Mode	Condition	Description
Operating	SYS_STATUS [12] = 1 BCK/SR valid DATA valid EN = 1	1. The EN pin is asserted at a high level. 2. Enable AMP at SYS_STATUS register [12] = 1. 3. The DATA and BCK/SR paths of I²S are valid. 4. The I²C bus remains awake. 5. The PLL synchronizes to BCK. 6. The chip will enter operating mode.
Silence	SYS_STATUS [12] = 1 BCK/SR valid DATA invalid EN = 1	1. The EN pin is asserted at a high level. 2. Enable AMP at SYS_STATUS register [12] = 1. 3. The BCK/SR path of I²S is valid. 4. The DATA path of I²S is less than the threshold. 5. The I²C bus remains awake. 6. OSC_1MHz is used to monitor the I²S bus. 7. The chip will enter silence mode.
Suspend	SYS_STATUS [12] = 1 BCK/SR invalid DATA invalid EN = 1	1. The EN pin is asserted at a high level. 2. Enable AMP at SYS_STATUS register [12] = 1. 3. Most of the clock path of I²S are turned off. 4. The I²C bus remains awake. 5. Monitor the BCK/SR on the I²S bus to check if the format is correct. 6. The chip will enter suspend mode.

Mode	Condition	Description
Power-down	EN = 0	1. The EN pin is asserted at a low level. 2. The I²C bus is turned off. 3. The I²S path is disabled. 4. Power consumption is at a minimum. 5. The chip will enter power-down mode.
Fault	OTP = 1 OCP = 1 UVP18 = 1 UVP50 = 1 EN = 1	1. The chip enters fault mode when an error event from physical protection mechanisms occurs (OCP/UVP18/UVP50/OTP) 2. The AMP will be turned off. 3. The system exits Fault mode after the overcurrent protection event is released for a checking cycle of about 100ms. 4. The system exits Fault mode immediately after VDD18/UVP50/OTP are released.

16.2 Power-ON/OFF Sequence

16.2.1 I²C Control Mode
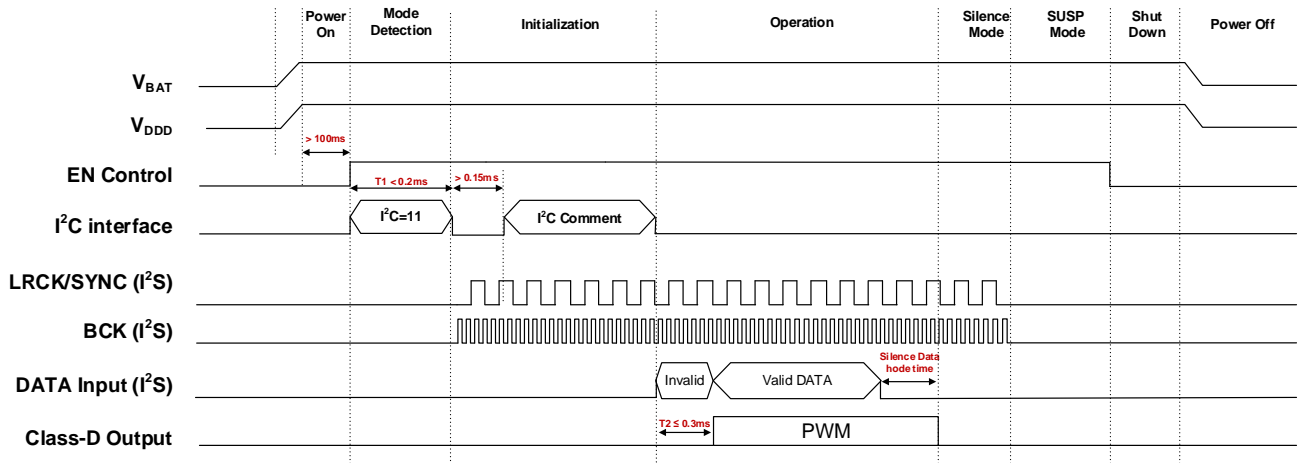
16.2.2 HW Control Mode
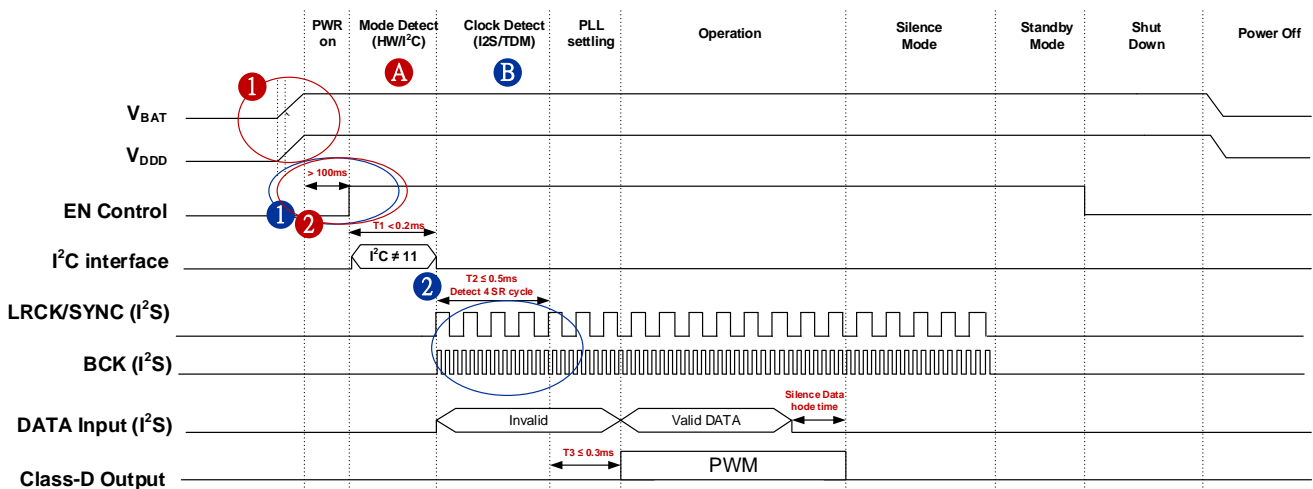
A. Mode Detect (HW/I2C) : 1st. Vbat & VDDD toggle (Low to High) 2st. "EN" toggle (Low to High)
B. Clock Detect (I2S/TDM) : 1st. EN" toggle (Low to High) 2nd. "BCK" Switch

16.3 Automatic Gain Control

The RT9123 is supported by an automatic gain control (AGC) function. This function can detect PWM cycles to determine if the output signal clipping at peak levels. When output clipping is detected, the AGC circuit will start to ramp down the output signal by reducing the gain. If the AGC detects that the output signal is not clipped, then it will release the gain to the default value.
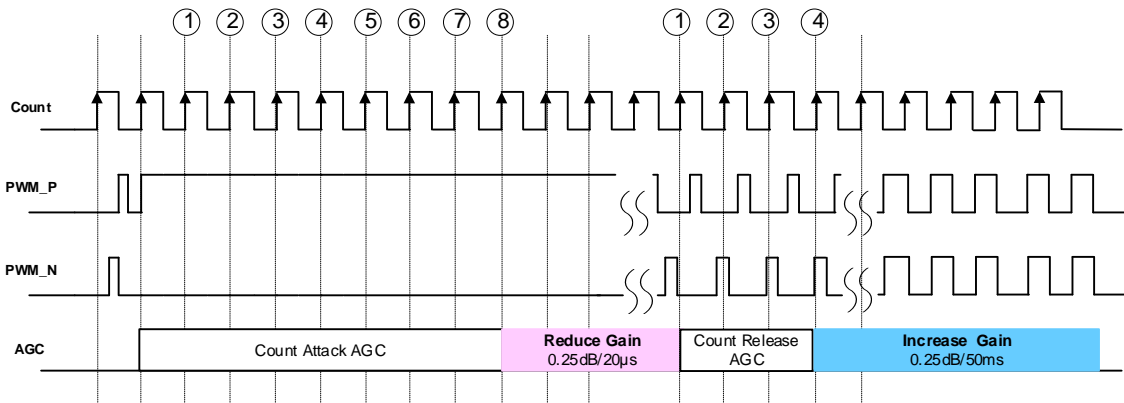
The count attack AGC and count release AGC can be adjusted by the register (CLIP_DET_SEL) in I^{2}C mode. Additionally, the registers (AGC_ATTACK_RATE) and (AGC_RELEASE_RATE) can be adjusted to set the attack and release times for reducing and increasing gain, respectively.

16.4 PIN Configuration for Detection

16.4.1 SCL/OPTION2 and SDA/OPTION3 PIN Configuration for Mode Selection

The RT9123 supports two operating modes that depend on SDA/OPTION2 and SCL/OPTION3 for situation determination.

When SDA/OPTION2 = 1 and SCL/OPTION3 = 1, the mode is defined as "I^{2}C Control Mode". It requires the host to initiate and control the on/off sequence of the amplifier via I^{2}C commands.
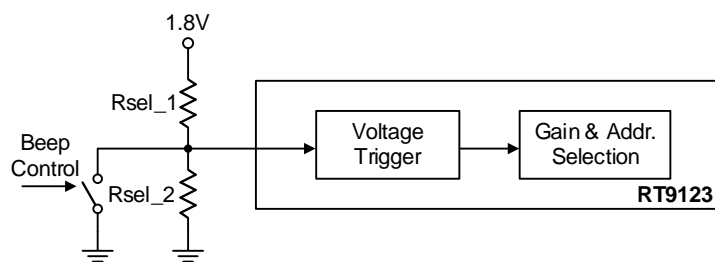
Mode	SCL/OPTION3	SDA/OPTION2	I^{2}S_BCK	ASEL	Device	Gain
I^{2}C Mode	1	1	N/A	R$_{sel\_1}$ (1k)	0x5C'h	12dB
				R$_{sel\_1}$ (200k)	0x5D'h	
				NC	0x5E'h	
				R$_{sel\_2}$ (620k)	0x5F'h	
				GND	BEEP	Beep sound

Except for the condition where SDA/OPTION2 = 1 and SCL/OPTION3 = 1, all other modes are defined as "HW Control Mode". This mode operates automatically and does not require initialization by an I^2C command.

Mode	SCL/OPTION3	SDA/OPTION2	I^2S_BCK	ASEL	Channel Selection	Gain
HW Mode (I^2S)	0	0	64fs 48fs 32fs	R_{sel_1} (1k)	(L+R)/2	12.0dB
				R_{sel_1} (200k)		10.5dB
				NC		9.0dB
				R_{sel_2} (620k)		7.5dB
				GND	BEEP	Beep sound
HW Mode (I^2S)	0	1	64fs 48fs 32fs	R_{sel_1} (1k)	R	12.0dB
				R_{sel_1} (200k)		10.5dB
				NC		9.0dB
				R_{sel_2} (620k)		7.5dB
				GND	BEEP	Beep sound
HW Mode (I^2S)	1	0	64fs 48fs 32fs	R_{sel_1} (1k)	L	12.0dB
				R_{sel_1} (200k)		10.5dB
				NC		9.0dB
				R_{sel_2} (620k)		7.5dB
				GND	BEEP	Beep sound
HW Mode (TDM)	0	0	128fs (32bit) 256fs (32bit) Fixed: 4-CH	R_{sel_1} (1k)	Channel 1	12dB
				R_{sel_1} (200k)	Channel 2	
				NC	Channel 3	
				R_{sel_2} (620k)	Channel 4	
				GND	BEEP	Beep sound
HW Mode (TDM)	1	0	128fs (16bit) 256fs (32bit) Fixed: 8-CH	R_{sel_1} (1k)	Channel A	12dB
				R_{sel_1} (200k)	Channel B	
				NC	Channel C	
				R_{sel_2} (620k)	Channel D	
				GND	BEEP	Beep sound
HW Mode (TDM)	0	1	128fs (16bit) 256fs (32bit) Fixed: 8-CH	R_{sel_1} (1k)	Channel E	12dB
				R_{sel_1} (200k)	Channel F	
				NC	Channel G	
				R_{sel_2} (620k)	Channel H	
				GND	BEEP	Beep sound

16.4.2 ASEL/OPTION1 Pin Configuration for Address/Device or Gain Selection

The ASEL/OPTION1 pin serves a multifunctional purpose in each mode.

Upon toggling the EN pin, the ASEL/OPTION1 pin can automatically detect the voltage threshold and enter different states. The voltage threshold can be set by connecting the pin to VDD18 using a 1kΩ (5%) resistor, connecting the pin to VDD18 using a 200kΩ (5%) resistor, connecting the pin to GND using a 620kΩ (5%) resistor, or leaving the pin unconnected.
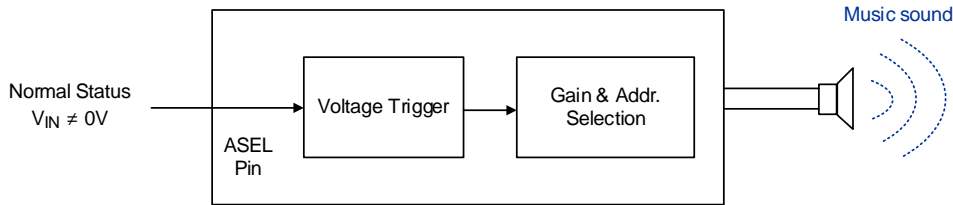
In I^{2}C Control Mode, there are four address selections: 0x5C, 0x5D, 0x5E, and 0x5F.

Mode	ASEL/OPTION1	Address
I^{2}C Control Mode	R$_{sel\_1}$ (1k)	0x5C'h
	R$_{sel\_1}$ (200k)	0x5D'h
	NC	0x5E'h
	R$_{sel\_2}$ (620k)	0x5F'h

In the I^{2}S format of HW Mode, there are four gain selections: 12.0dB, 10.5dB, 9.0dB, and 7.5dB.

Mode	ASEL/OPTION1	Gain
HW Control Mode (I^{2}S format)	R$_{sel\_1}$ (1k)	12.0dB
	R$_{sel\_1}$ (200k)	10.5dB
	NC	9.0dB
	R$_{sel\_2}$ (620k)	7.5dB

In the TDM format of HW Mode, there are 4 channels available for device selection.

Mode	ASEL/OPTION1	Device
HW Control Mode (TDM format)	R$_{sel\_1}$ (1k)	Channel 1
	R$_{sel\_1}$ (200k)	Channel 2
	NC	Channel 3
	R$_{sel\_2}$ (620k)	Channel 4

16.4.3 ASEL/OPTION1 Pin Configuration for Beep Sound

Whenever VDD/VDD18 power is on and the EN pin is asserted high, pulling the ASEL pin to 0V will trigger a Beep sound.
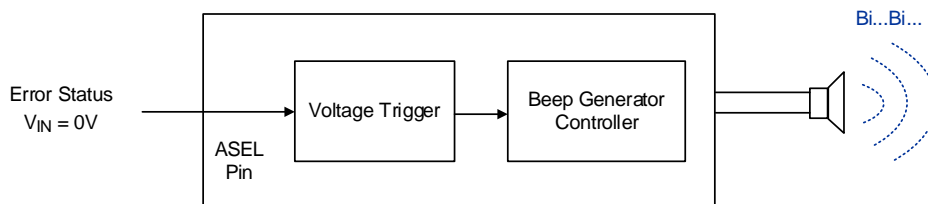
16.4.4 EN Pin Configuration for Shutdown mode

The audio chip enters Shutdown mode if the EN pin is asserted to a low level. All internal blocks are turned off in Shutdown mode, and the device consumes the minimum quiescent current from the VDD and VDD18 power supplies.

16.5 Audio Bits and Frame Widths

16.5.1 I^{2}C Control Mode

16.5.1.1 Data Format

The I^{2}S formats supported by the RT9123 are listed below:

| Interface	BCK Frequency	Data Format
I^{2}S Standard	32fs	up to 16-bit
I^{2}S Standard	48fs	up to 24-bit
I^{2}S Standard	64fs	up to 32-bit
Left-justified	32fs	up to 16-bit
Left-justified	48fs	up to 24-bit
Left-justified	64fs	up to 32-bit
Right-justified (16-bit)	32fs/48fs/64fs	16-bit
Right-justified (20-bit)	48fs/64fs	20-bit
Right-justified (24-bit)	48fs/64fs	24-bit
Right-justified (32-bit)	64fs	32-bit
TDM 8-slot	64fs	64-bit
TDM 16-slot	128fs	128-bit
TDM 32-slot	256fs	256-bit
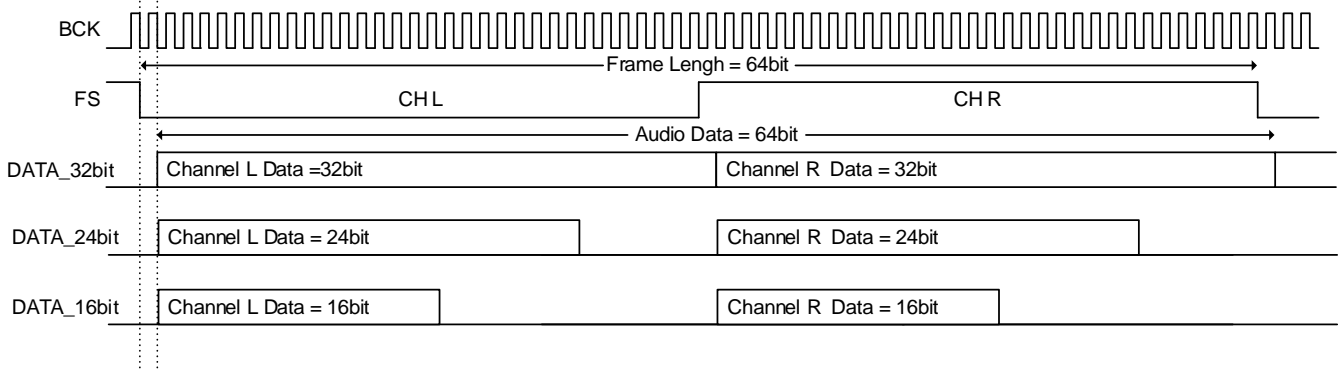
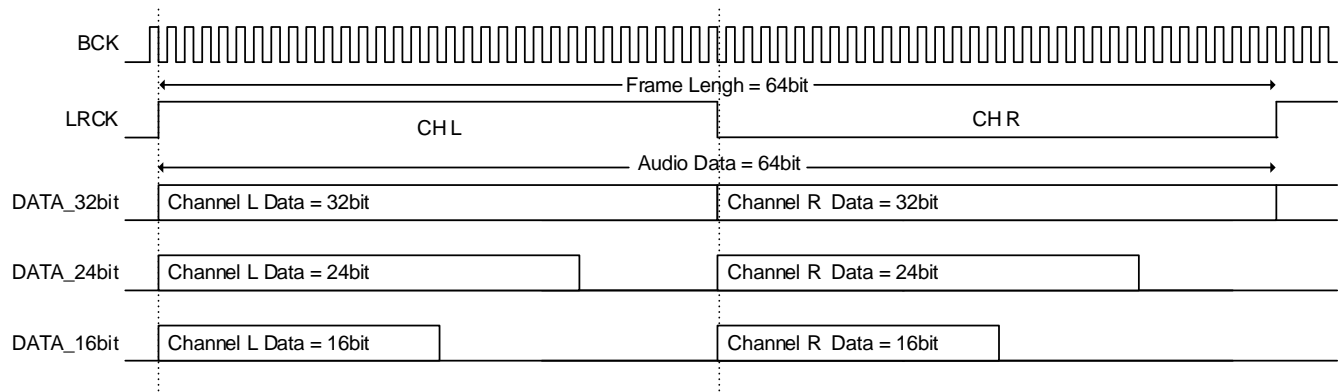Figure 1. I²S Format with I²C Control Mode

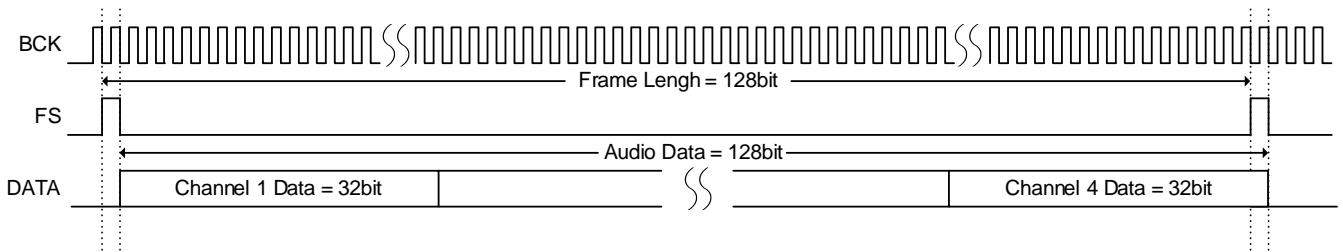Figure 2. Left-Justified Format with I²C Control Mode

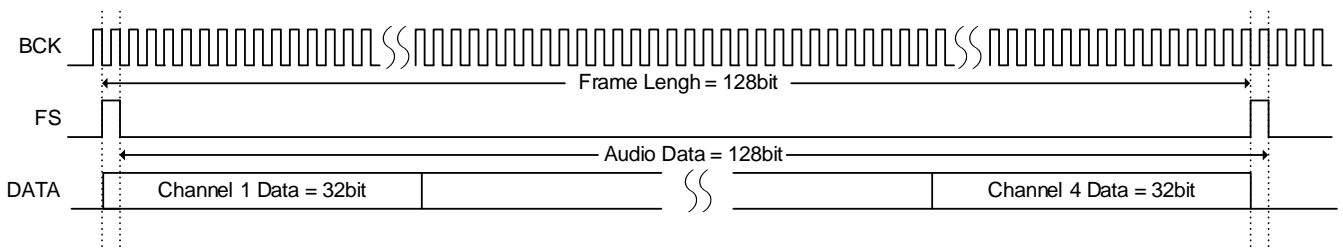Figure 3. TDM Standard Format (1bit offset) with I²C Control Mode

Figure 4. TDM Left-Justified Format with I²C Control Mode

16.5.2 I²S Sampling Rate

I²S can support rates of 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz, and 96kHz in 32fs/64fs/128fs/256fs.

I²S can support rates of 8kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz, and 96kHz in 48fs.

16.5.3 HW Control Mode

In the I²S/Left-Justify format of HW Mode, there are 2 channels per LRCK period, and the audio bits are 16bits per channel. Therefore, the audio bit of BCK periods per LRCK period in this mode is exactly 32fs.
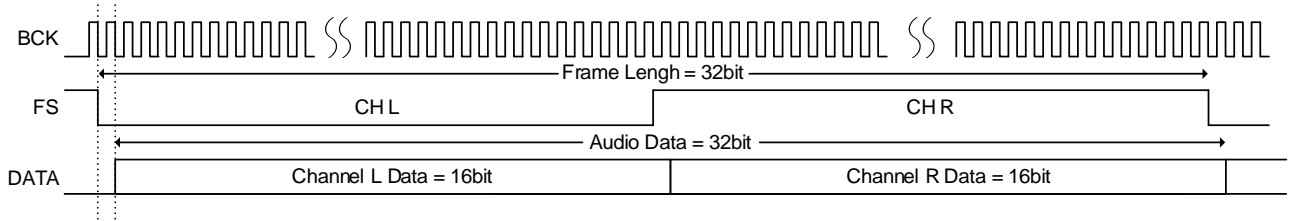
Figure 5. I²S format with HW Control Mode (BCK = 32fs)

According to this design concept, the audio bits are 24bits per channel and 32bits per channel, and the audio bit of BCK periods per LRCK period is exactly 48fs and 64fs, respectively.
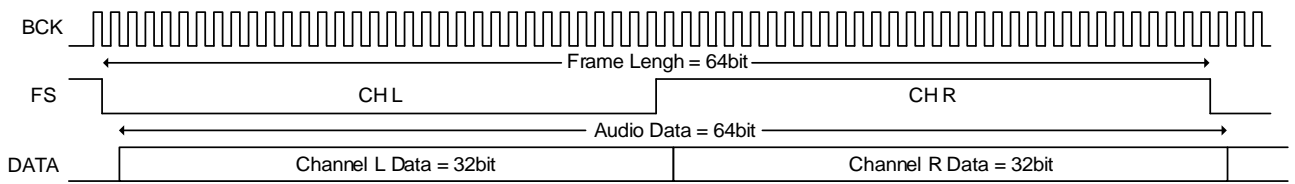
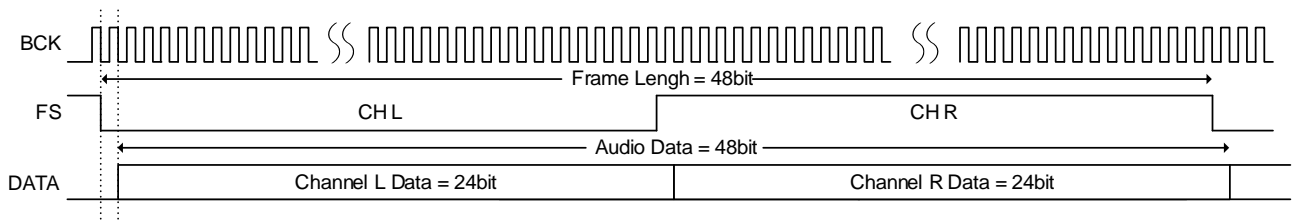Figure 6. I²S format with HW Control Mode (BCK = 64fs)

Figure 7. I²S format with HW Control Mode (BCK = 48fs)

In the 4-channel TDM format of HW Mode, there are 4 channels per LRCK period, and the audio bits are 32 bits per channel. The audio bit of BCK periods per LRCK period in this mode is exactly 128fs or 256fs.

Figure 8. 4-Channel TDM with HW Control Mode (BCK = 128fs)

Figure 9. 4-Channel TDM with HW Control Mode (BCK = 256fs)

In the 8-channel TDM format of HW Control Mode, there are 8 channels per LRCK period and the audio bits are 16 bits per channel. The audio bit of BCK periods per LRCK period in this mode is exactly 128fs. There are 8-channel per LRCK period and audio bits are 32 bits per channel. The audio bit of BCK periods per LRCK period in this mode is exactly 256fs.
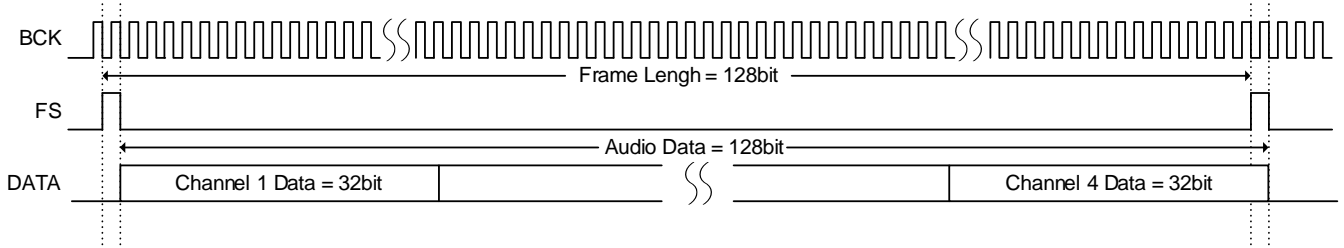

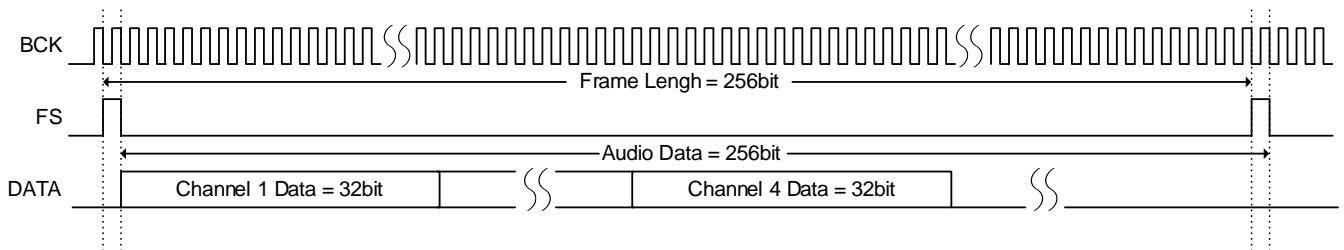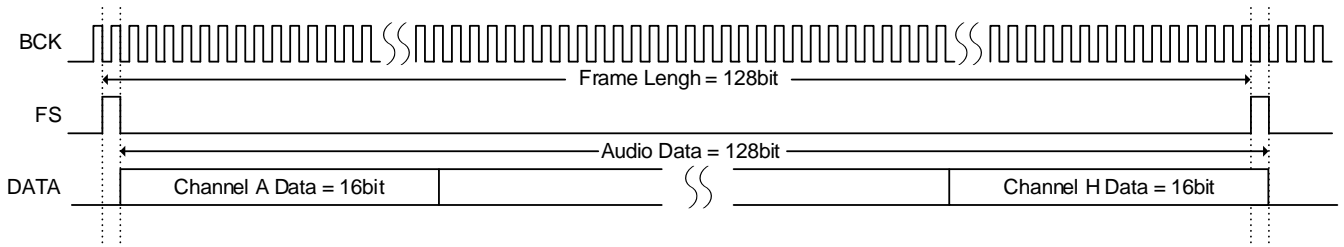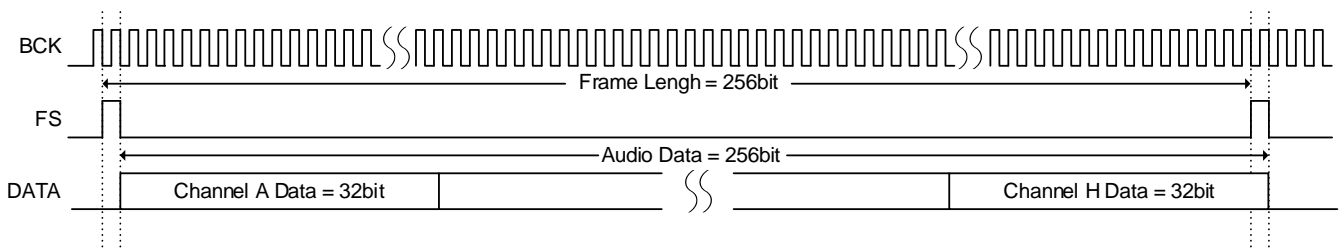Figure 10. 8-Channel TDM with HW Control Mode (BCK = 128fs)

Figure 11. 8-Channel TDM with HW Control Mode (BCK = 256fs)

Table 2. Valid Resolutions and Frame Widths

Audio Bits	BCK in I²S/Left-Justified	BCK in 4CH TDM Mode	BCK in 8CH TDM Mode
16	32fs	128fs/256fs	128fs
24	48fs	NOT VALID	NOT VALID
32	64fs	128fs/256fs	256fs

16.5.4 LRCK/BCK PIN Configuration for I²S or TDM Interface in HW Control mode

The RT9123 will automatically detect the bit clock rate and sample rate to determine audio source format after power-on. Valid sample rates are 8kHz, 16kHz, 24kHz, 44.1kHz, 48kHz, 88.2kHz, and 96kHz.

Table 3. Valid LRCK/BCK Frequencies (kHz)

BCK (MHz) / LRCK	I²S Mode			TDM Mode	
	32*fs	48*fs	64*fs	128*fs	256*fs
fs = 8kHz	0.256	0.384	0.512	1.024	2.048
fs = 16kHz	0.512	0.768	1.024	2.048	4.096
fs = 24kHz	0.768	1.152	1.536	3.072	6.144
fs = 32kHz	1.024	1.536	2.048	4.096	8.192
fs = 44.1kHz	1.411	2.117	2.822	5.645	11.290
fs = 48kHz	1.536	2.304	3.072	6.144	12.288
fs = 88.2kHz	2.822	4.234	5.645	11.290	22.579
fs = 96kHz	3.072	4.608	6.144	12.288	24.576

16.6 State Machine
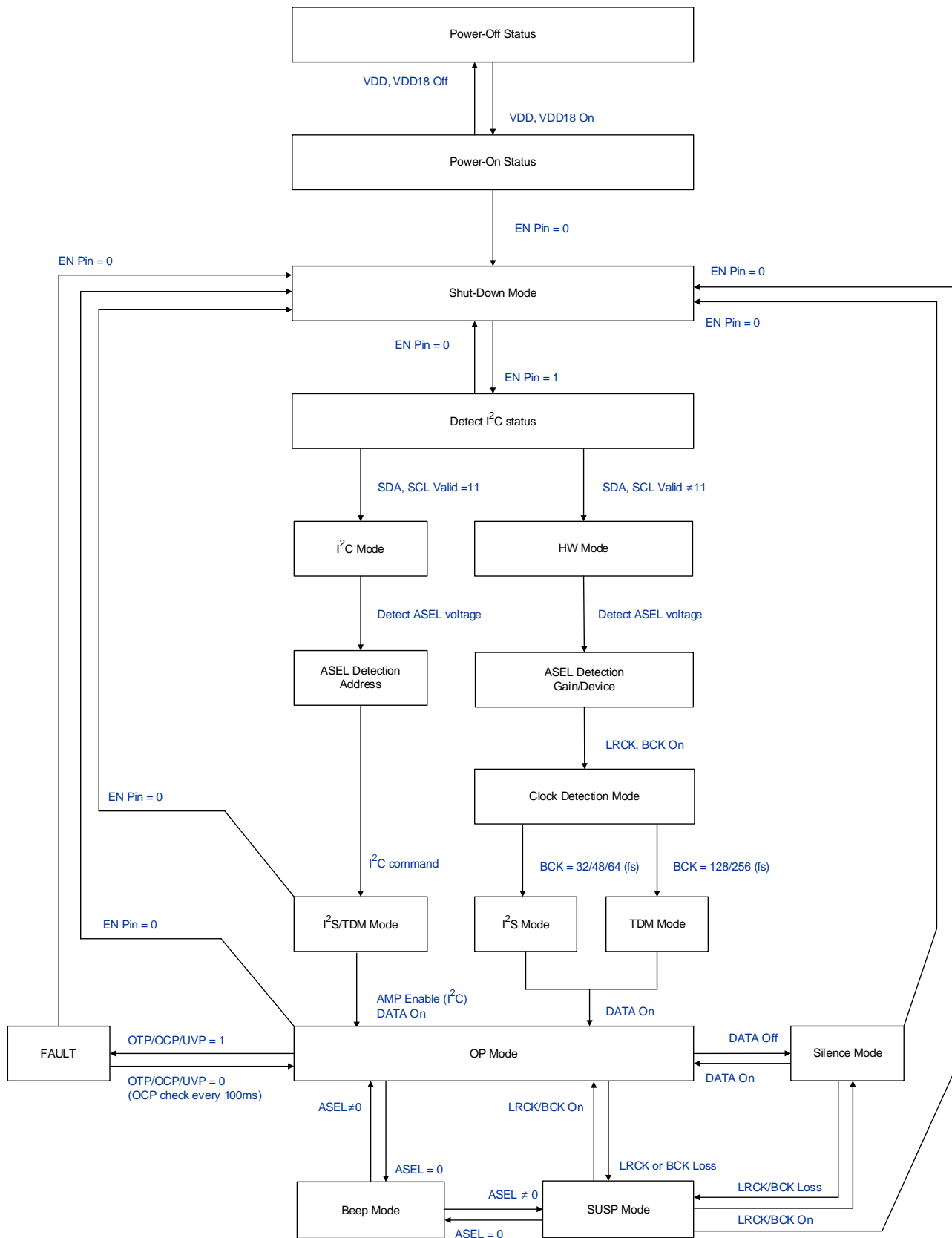
16.7 Protection

16.7.1 Undervoltage Protection (V_{DD})

The undervoltage protection can detect the undervoltage fault on the power supply V_{DD}. The UV flag is triggered when V_{DD} is lower than 2.2V, and then the digital control system disables the analog blocks. When V_{DD} is higher than the hysteresis UVP threshold 2.4V, the UV protection detects the voltage again to determine if the UV event is finished.

16.7.2 Undervoltage Protection (V_{DD18})

The undervoltage protection can detect the undervoltage fault on power supply V_{DD18}. When V_{DD18} is lower than 1.4V, the UV flag is triggered, and then the digital control system disables the analog blocks. When V_{DD18} is higher than the hysteresis UVP threshold 1.6V, the UV protection detects the voltage again to determine if the UV event is finished.

16.7.3 Over-Temperature Protection

The over-temperature protection can detect the over-temperature fault in the chip. The OT protection is triggered when the junction temperature is higher than 150°C, and then the digital control system disables the analog blocks. When the junction temperature is lower than the hysteresis threshold 150°C, the OT protection detects the temperature to determine if the OT event is finished.

16.7.4 Overcurrent Protection

The overcurrent protection can detect the overcurrent fault in the Class-D. The fault in the Class-D that causes a large current exceeding 2.80A triggers the OC flag to the digital control system and disables the analog blocks for 100ms. After a 100ms cooling period, the OC protection detects the current again to determine if the OC event is finished.

16.8 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the temperature difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to- ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-14B 1.81x1.1 (BSC) package, the thermal resistance, θ_{JA}, is 25.7°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a WDFN-12L 3x3 package, the thermal resistance, θ_{JA}, is 30.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (25.7°C/W) = 3.89W for a WL-CSP-14B 1.81x1.1 (BSC) package.

$P_{D(MAX)}$ = (125°C – 25°C) / (30.8°C/W) = 3.24W for a WDFN-12L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 12 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.
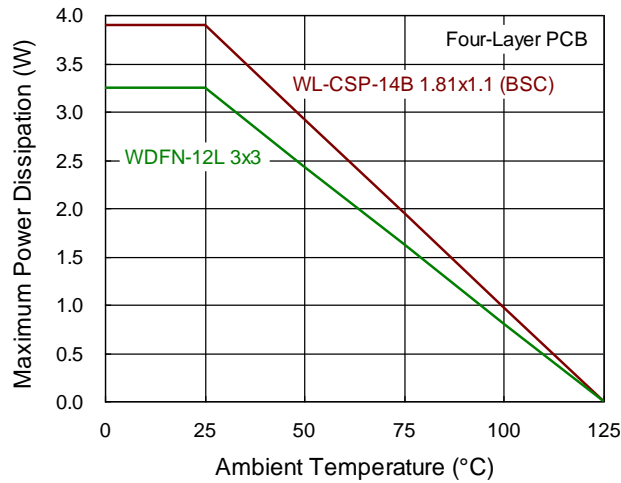

Figure 12. Derating Curve of Maximum Power Dissipation

16.9 Layout Considerations

1. For providing good grounding for the IC to ensure good audio quality and reduce the possibility of interference. Analog and digital signal paths should be separated as much as possible. Configure AGND and DGND separately during layout and ensure that digital signals are not affected by analog noise.
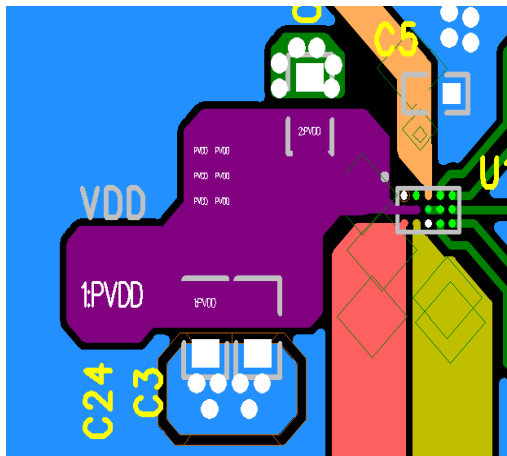
2. Keep the analog signal paths (VDD, outputP, outputN) as wide and short as possible. We recommend that each path has a minimum width of 1.5A to ensure sufficient current capacity. For example, on a 1oz copper thickness PCB, we recommend reserving at least 60mil width for the AVDD and output paths.
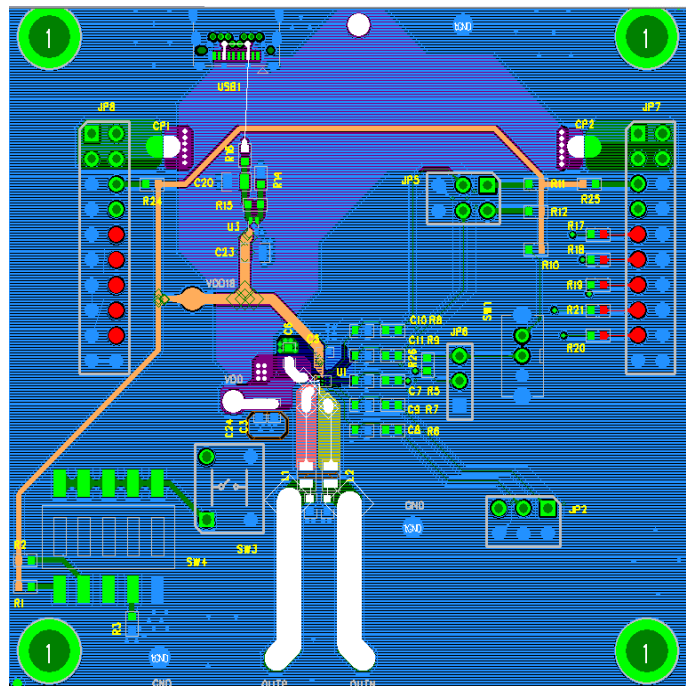
3. Place all decoupling capacitors as close to the RT9123 IC as possible to improve audio performance.
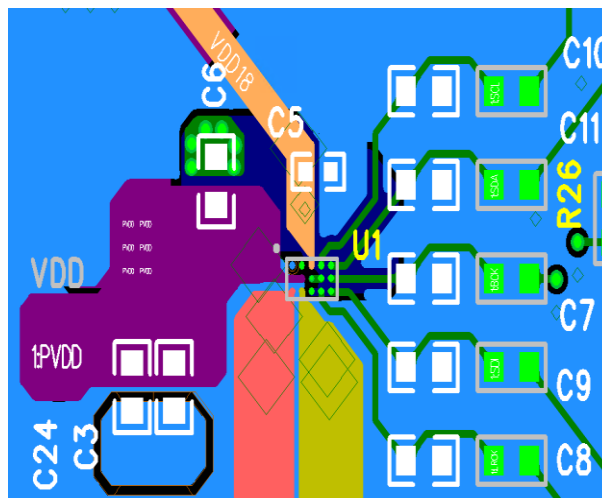
4. Ensure that I^{2}S and I^{2}C signal paths have a minimum bend angle should be over 90° to avoid the sharp bends that can cause antenna effects.

5. Ensure that both sides of each I^{2}S and I^{2}C signal path have grounding to prevent signal interference.
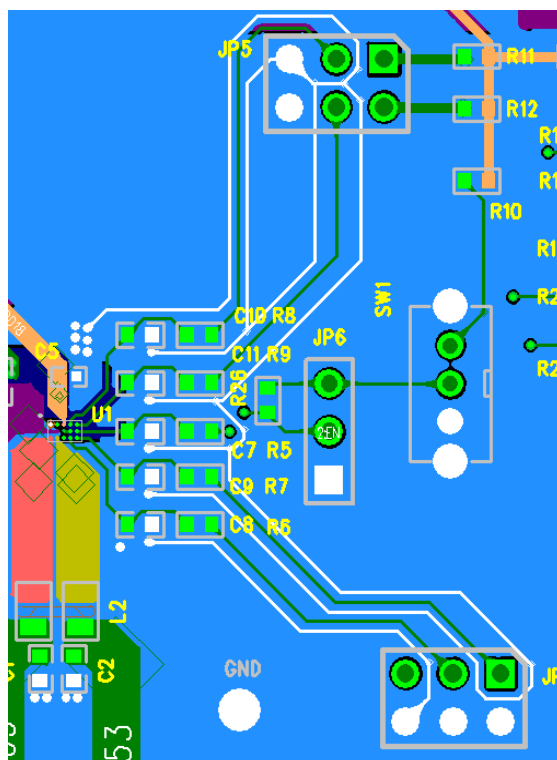
16.10   I^{2}C Interface

16.10.1   Read and Write Function

Read a single byte of data from Register
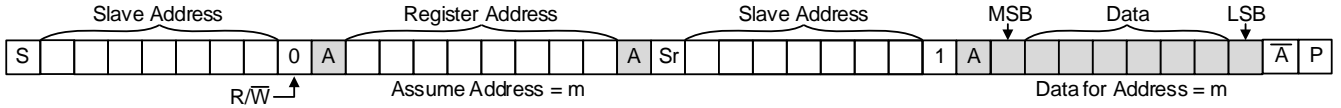
Read N bytes of data from Registers
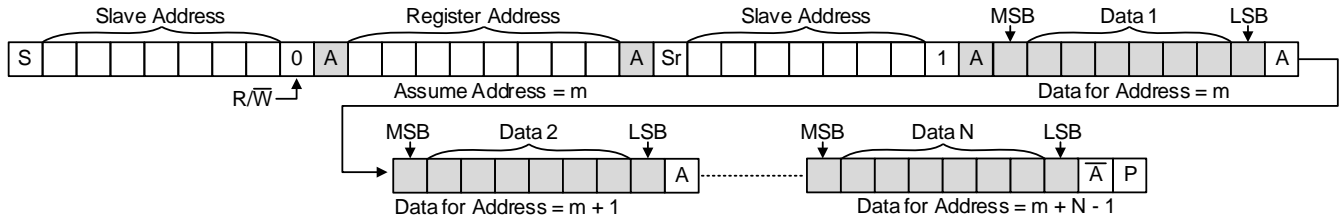
Write a single byte of data to Register
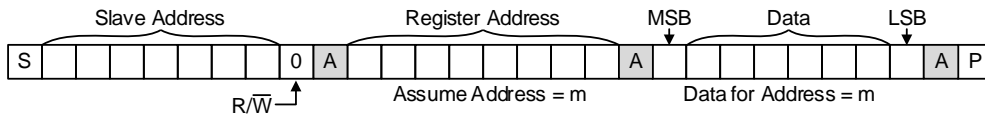
Write N bytes of data to Registers
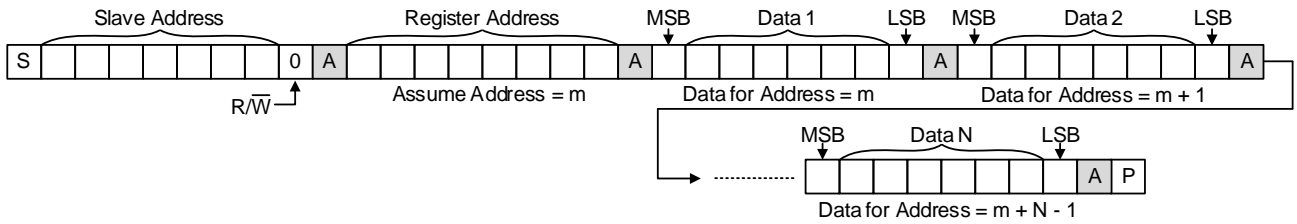
Driven by Master, Driven by Slave, P Stop, S Start, Sr Repeat Start

16.10.1.1   I^{2}C Waveform Information
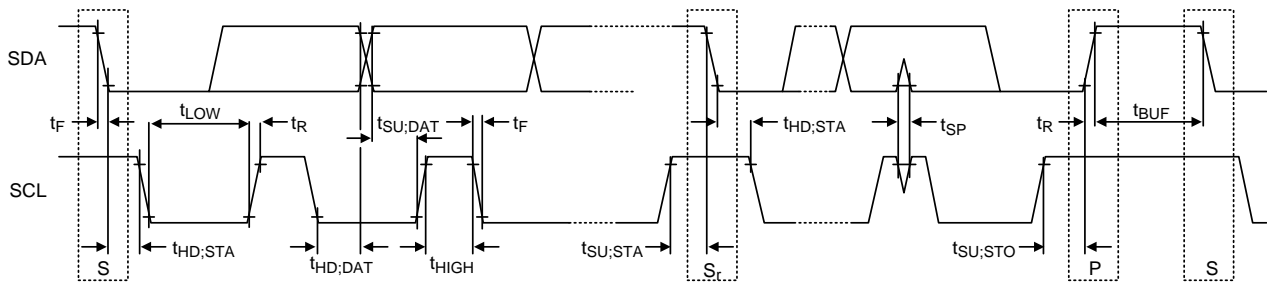
16.11 I²S Interface

16.11.1 I²S Waveform Information
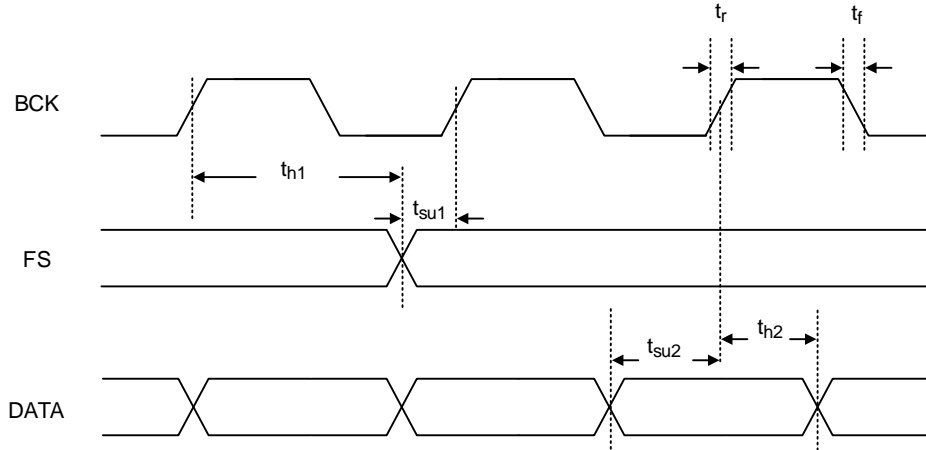
Note 6. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

17 Functional Register Description

Address	Byte	Bits	Bits Name	Default	Type	Description
0x00	2	15:10	Reserved	6'h0	RO	Reserved
		9:4	PROD_ID	000000'b	RO	Product ID
		3:0	VER_ID	0001'b	RO	Version ID
0x01	2	15	SF_RESET	0'b	WO	Write 1 to trigger a Software reset Need to wait for 10ms for reset completion
		14	MUTE	0'b	RW	0: Un-mute (default) 1: Soft mute
		13	Reserved	0'b	RO	Reserved
		12	AMP_ON	0'b	RW	Enable amp 0: Amp off (I²C mode default) (default) 1: Amp on (HW mode default)
		11	Reserved	0'b	RO	Reserved
		10:8	SYS_STATUS	000'b	RO	System status 000: Shutdown (default) 010: Suspend mode / Standby mode 011: Silence mode 100: Beep mode (1MHz clock) 110: Operation mode 111: Beep mode (BCK clock) Others: Reserved
		7:6	Reserved	00'b	RO	Reserved
		5:4	D_TRI_FREQ_SEL	10'b	RW	PWM frequency selection 00: 300kHz 01: 325kHz 10: 350kHz (default) 11: 375kHz
		3:0	SPK_GAIN	1001'b	RW	SPK RI (GAIN) selection 0000: −12dB (DRE-on) 0001: 0dB 0010:1.5dB 0011: 3dB 0100: 4.5dB 0101: 6dB 0110: 7.5dB 0111: 9dB 1000: 10.5dB 1001: 12dB (default) 1010: 14dB Others: Reserved

RICHTEK

Address	Byte	Bits	Bits Name	Default	Type	Description
0x02	2	15	SCLK_EDGE_SEL	0'b	RW	0: LRCK transition align with BCK falling (default) 1: LRCK transition align with BCK rising
		14:12	AUD_BITS	010'b	RW	000: 16 bits 001: 20 bits 010: 24 bits (default) 011: 32 bits 100: 8 bits Others: Reserved
		11	TDM_DSP_OFFSET	1'b	RW	TDM or DSPM offset selection 0: Without offset (DSPMB) 1: 1 bit clock offset (DSPMA) (default)
		10:8	AUD_FMT	000'b	RW	000: I^{2}S (default) 001: Left Justify 010: Right Justify 011: DSP mode 1xx: TDM mode
		7:6	Reserved	00'b	RO	Reserved
		5:4	I2S_CH_SEL	01'b	RW	I^{2}S channel selection 01: L channel (default) 10: R channel 00/11: (L+R) / 2
		3:2	Reserved	00'b	RO	Reserved
		1:0	BEEP_FREQ_SEL	01'b	RW	Beep frequency selection 00: 200Hz 01: 400Hz (default) 10: 800Hz 11: 1000Hz
0x03	2	15:5	Reserved	11'h0	RW	Reserved
		4:0	TDM_RX_LOC	00000'b	RW	TDM starts receiving location selection

Address	Byte	Bits	Bits Name	Default	Type	Description
0x04	2	15	Reserved	0'b	RW	Reserved
		14	SIL_DET_EN	0'b	RW	Silence detection enable 0: Disable (default) 1: Enable
		13:12	SIL_TH_SEL	11'b	RW	Silence mode detection threshold (in different AUD_BITS setting) Detect how much MSB swing between 0000… or FFFF… and don't care LSB toggled 00: 13MSB (16-bit)/17MSB (20-bit)/21MSB (24-bit)/25MSB (32-bit) 01: 14MSB (16-bit)/18MSB (20-bit)/22MSB (24-bit)/26MSB (32-bit) 10: 15MSB (16-bit)/19MSB (20-bit)/23MSB (24-bit)/27MSB (32-bit) 11: 16MSB (16-bit)/20MSB (20-bit)/24MSB (24-bit)/28MSB (32-bit) (default) Equivalent to audio signal level in 32bits audio bits 00: -73dB (16-bit) / -97Db (20-bit) / -121dB (24-bit) / -145dB (32-bit) 01: -79dB (16-bit) / -103dB (20-bit) / -127dB (24-bit) / -151dB (32-bit) 10: -85dB (16-bit) / -109dB (20-bit) / -133dB (24-bit) / -157dB(32-bit) 11: -91dB (16-bit) / -115dB (20-bit) / -139dB (24-bit) / -163dB (32-bit) (default)
		11:9	SIL_HOLD_TIME	010'b	RW	Silence mode hold time selection 000: 1ms 001: 20ms 010: 40ms (default) 011: 80ms 100: 160ms 101: 320ms 110: 640ms 111: 1.28s
		8	SKIP_RAMP	0'b	RW	0: Skip volume ramp 1: Volume ramp (default)
		7:6	VOL_RAMP_ MODE	00'b	RW	Volume slew step control 00: 4.33ms from mute to 0dB (0.5dB/20.83μs) (default) 01: 8.66ms from mute to 0dB (0.25dB/20.83μs) 10: 17.33ms from mute to 0dB (0.125dB/20.83μs) 11: 34.65ms from mute to 0dB (0.0625dB/20.83μs)
		5	HPF_EN	1'b	RW	High-Pass filter enable 0: Disable 1: Enable (default)
		4	DRE_EN	1'b	RW	DRE function 0: Disable 1: Enable (default)

| Address	Byte	Bits	Bits Name	Default	Type	Description
		3	HARD_CLIP_EN	0'b	RW	Hard clip enable 0: Disable (default) 1: Enable
		2	D_FSS_EN	0'b	RW	Spread spectrum enable 0: Disable (default) 1: Enable
		1	CLIP_DET_EN	1'b	RW	Clip detection enable 0: Disable 1: Enable (default)
		0	CLIP_AGC_EN	0'b	RW	Enable auto gain control for CLIP detection 0: Disable (default) 1: Enable
0x05	2	15	Reserved	0'b	RO	Reserved
		14	PWM_ MODEWHITE	0'b	RW	Noise selection 0: Pink noise (default) 1: White noise
		13	PWM_SELCOEF	0'b	RW	Pink noise coefficient This will affect the noise amplitude for spread spectrum signal, not recommended to modify it. 0: 1/2 (default) 1: 1/4
		12	PWM_NOISE_EN	0'b	RW	Add noise to TRI_GEN 0: Disable (default) 1: Enable
		11:10	D_NOISE_AMP	00'b	RW	Nosie amplitude for SSC 00: 6.3% (default) 01: 11.7% 10: 17.1% 11: 35.1%
		9:8	D_FSS_AMP	01'b	RW	Spread spectrum frequency variation amplitude 00: 14.73% 01: 22.5% (default) 10: 22.5% 11: 30.35%
		7:2	Reserved	6'h0	RO	Reserved
		1	I2C_TIME_OUT_ SEL	0'b	RW	I^{2}C timeout reset selection 0: Reset I^{2}C IP only (default) 1: Reset whole chip
		0	I2C_TIME_OUT_ EN	1'b	RW	I^{2}C timeout function: If SDA and SCL keep low for 100ms, an I^{2}C timeout reset will occur. 0x05 bit 0 is the reset option to select the reset block. 0x05 bit 1 for enabling the I^{2}C timeout function. 0: Disable (default) 1: Enable

Address	Byte	Bits	Bits Name	Default	Type	Description
0x12	2	15:11	Reserved	5'h0	RO	Reserved
		10:0	VOL_GAIN	11'h180	RW	Volume gain control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: mute 0.0625dB per step
0x13	2	15:11	Reserved	5'h0	RO	Reserved
		10:0	HC_TH	11'h180	RW	Hard clip threshold when HARD_CLIP_EN = 1 > 0dB is not allowable for hard clip threshold setting. 11'h180: 0dB (default) 0.0625db per step
0x20	2	15	BCK_ERR	0'b	W0C	0: No BLK error (default) 1: BLK error, write 0 to clear flag
		14	LRCK_ERR	0'b	W0C	0: No LRCK clock error (default) 1: LRCK clock error, write 0 to clear flag
		13	UVP50	0'b	W0C	5V UVP 0: Normal (default) 1: Fault (write 0 to clear)
		12	UVP18	0'b	W0C	1.8V UVP 0: Normal (default) 1: Fault (write 0 to clear)
		11	OTP	0'b	W0C	Channel OTP 0: Normal (default) 1: Fault (write 0 to clear)
		10	OCP	0'b	W0C	Channel OCP 0: Normal (default) 1: Fault (write 0 to clear)
		9	CLIP	0'b	W0C	Clip detection 0: Normal (default) 1: Warning (write 0 to clear)
		8	MODE_ERR	0'b	W0C	Mode detection fault 0: Normal (default) 1: Warning (write 0 to clear)
		7	SR_AUTO_DET	1'b	RW	Sampling rate detection enable bit Detect sampling rate and BCK mode 0: Disable, manual set 0x01 SR mode and BCK mode 1: Enable (default)
		6:4	SR_MODE	101'b	RW	Sampling rate (manual setting or report) If auto sampling rate detection, SR_MODE reports detection result. 000: 8kHz 001: 12kHz 010: 16kHz 011: 24kHz 100: 32kHz 101: 44.1/48kHz (default) 110: 88.2/96kHz 111: Sampling rate error report

Address	Byte	Bits	Bits Name	Default	Type	Description
		3:0	BCK_MODE	0010'b	RW	BCK mode report 0000: BCK = 32fs 0001: BCK = 48fs 0010: BCK = 64fs (default) 0100: BCK = 128fs 0110: BCK = 256fs 1001: BCK mode error report Others: Reserved
0x21	2	15	FAULT_RAMP_ MUTE	0'b	RW	Signal ramp down option when fault occurred 0: Directly mute (default) 1: Ramp mute 1ms
		14	UVP50_EN	1'b	RW	5V UVP enable 0: Disable 1: Enable (default)
		13	UVP18_EN	1'b	RW	1.8V UVP enable 0: Disable 1: Enable (default)
		12	DC_UVP_CAL_EN	0'b	RW	PVDD UVP re-calibration DC offset enable 0: Disable (default) 1: Enable
		11:10	UVP_DEG_SEL	01'b	RW	UVP flag deglitch time 00: Without deglitch 01: 20μs (default) 10: 30μs 11: 40μs
		9:8	CLIP_DET_SEL	01'b	RW	Clip detect threshold, release threshold (unit: PWM cycle) 00: 4, 2 01: 8, 4 (default) 10: 16, 6 11: 32, 12
		7:6	AGC_ATTACK_ RATE	10'b	RW	AGC attack time selection for AGC 00: 0.25dB/20μs 01: 0.25dB/40μs 10: 0.25dB/80μs (default) 11: 0.25dB/160μs
		5:4	AGC_RELEASE_ RATE	10'b	RW	AGC release time selection for AGC 00: 0.25dB/50ms 01: 0.25dB/100ms 10: 0.25dB/200ms (default) 11: 0.25dB/400ms
		2:0	D_SPK_CLP	100'b	RW	SPK duty clamping selection 000: 20.4n 001: 24.6n 010: 26n 011: 30n 100: 31.5n (default) 101: 35.7n 110: 37n 111: 41n

Address	Byte	Bits	Bits Name	Default	Type	Description
0x36	2	15	D_BG_OK	0'b	RO	Bandgap ready signal
		14	D_UVP50_FLAG	0'b	RO	5V undervoltage flag
		13	D_UVP18_FLAG	0'b	RO	1.8V undervoltage flag
		12	D_OT_FLAG	0'b	RO	Over-temperature flag
		11	D_OCP_FLAG	0'b	RO	SPK OCP output flag
		10:0	Reserved	020'h	RW	Reserved

18 Outline Dimension

18.1 WL-CSP-14B 1.81x1.1 (BSC)
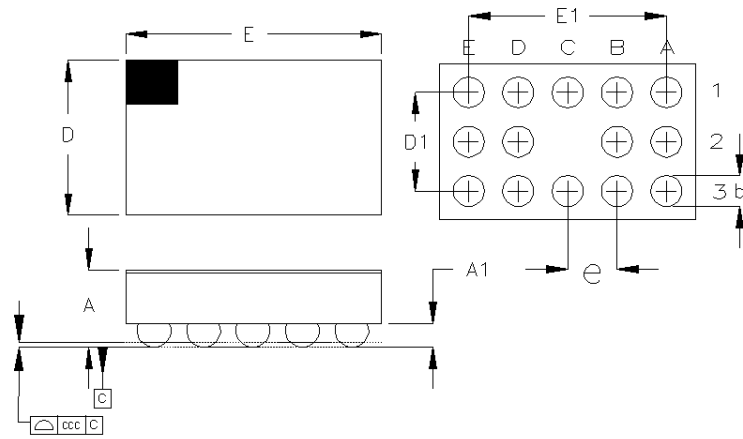
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.120	0.180	0.005	0.007
b	0.190	0.250	0.007	0.010
E	1.770	1.850	0.070	0.073
E1	1.400		0.055	
D	1.060	1.140	0.042	0.045
D1	0.700		0.028	
e	0.350		0.014	
ccc	0.020		0.001	

14B WL-CSP 1.81x1.1 Package (BSC)

18.2   WDFN-12L 3x3
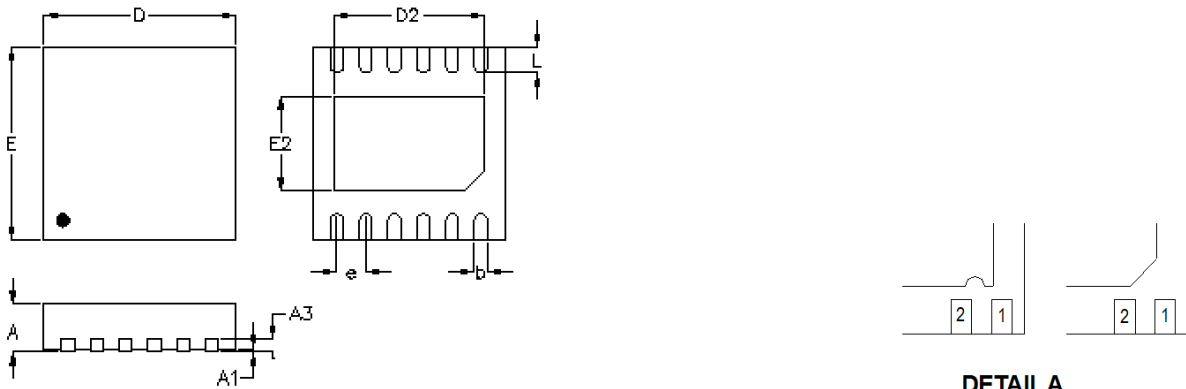
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.250	0.006	0.010
D		2.950	3.050	0.116	0.120
D2	Option1	2.300	2.650	0.091	0.104
	Option2	1.970	2.070	0.078	0.081
E		2.950	3.050	0.116	0.120
E2	Option1	1.400	1.750	0.055	0.069
	Option2	1.160	1.260	0.046	0.050
e		0.450		0.018	
L		0.350	0.450	0.014	0.018

W-Type 12L DFN 3x3 Package

Note 7.   The package of the RT9123 uses Option1.

19 Footprint Information

19.1 WL-CSP-14B 1.81x1.1 (BSC)
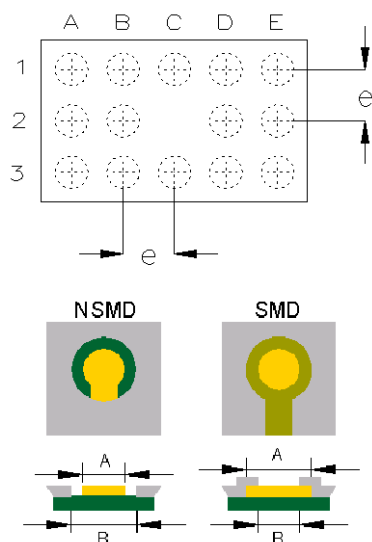
Package	Number of Pins	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.81x1.11-14(BSC)	14	NSMD	0.350	0.220	0.320	±0.025
		SMD		0.250	0.220	

19.2 WDFN-12L 3x3
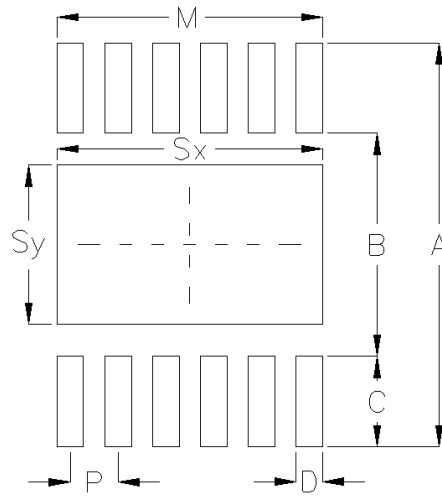
Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN3x3-12	Option1	12	0.45	3.80	2.10	0.85	0.25	2.50	1.50	2.50	±0.05
	Option2							2.12	1.31		

Note 8. The package of the RT9123 uses Option1.

20 Packing Information

20.1 WL-CSP 1.81x1.1 Tape and Reel Data
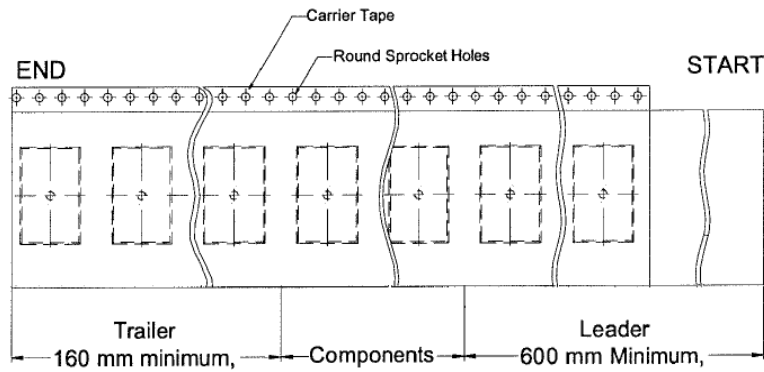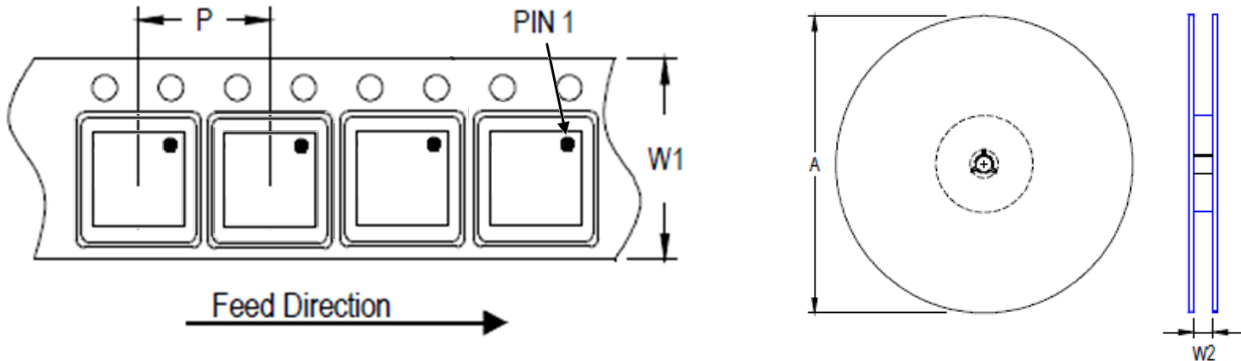
Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 1.81x1.1	8	4	180	7	3,000	160	600	8.4/9.9
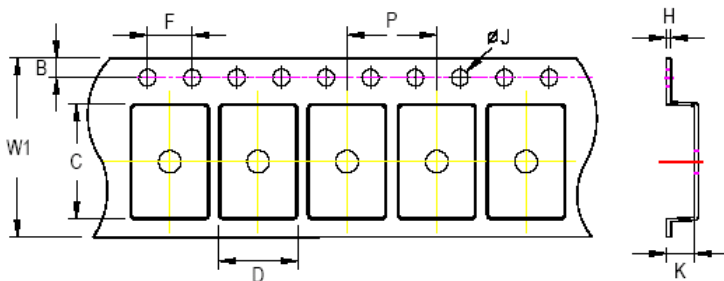
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

20.2 QFN/DFN 3x3 Tape and Reel Data
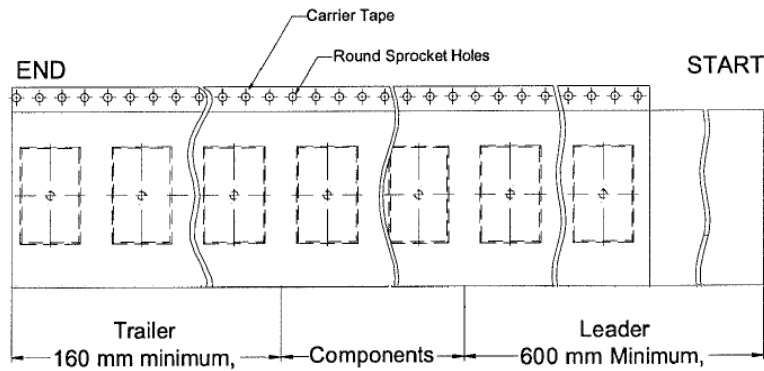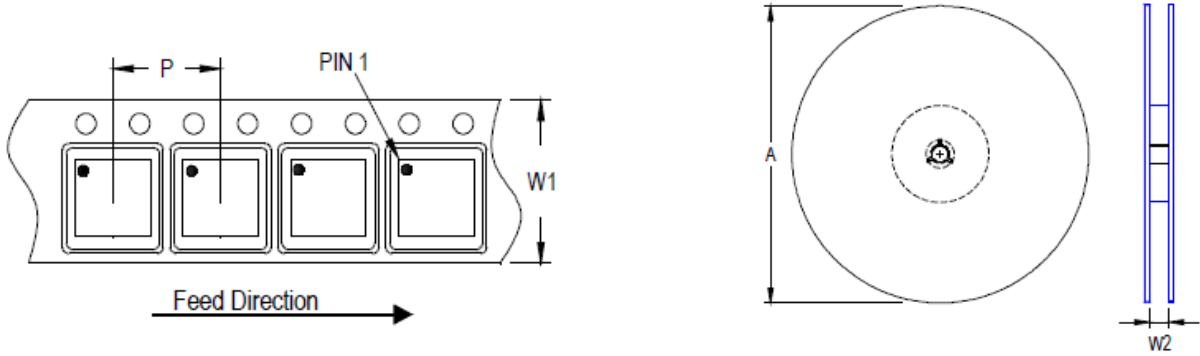
Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	8	4	180	7	3,000	160	600	8.4/9.9
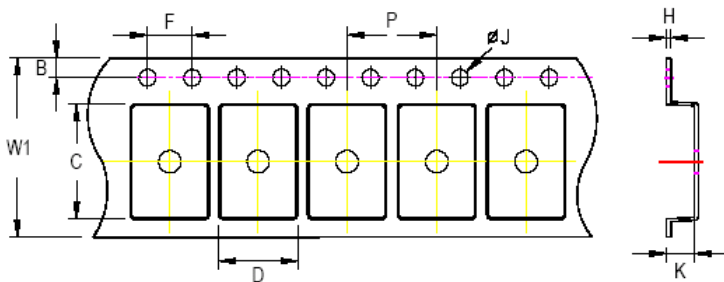
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

20.3   WL-CSP 1.81x1.1 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	Reel 7"	4	12 inner boxes per outer box
2	Packing by Anti-Static Bag	5	Outer box **Carton A**
3	3 reels per inner box **Box A**	6	

Container Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 1.81x1.1	7"	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

20.4 QFN/DFN 3x3 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7"	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Package \ Container	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN/DFN 3x3	7"	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

20.5 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

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21 Datasheet Revision History

Version	Date	Description	Item
00	2024/5/28	Final	Title on P1 Features on P1 Ordering Information on P2 Functional Pin Description on P4 Electrical Characteristics on P8 Application Information on P22, 36 Packing Information on P50, 51