Rail-to-Rail Operational Amplifier

General Description

The RT9137/RT9138/RT9139 consist low power, high slew rates, rail-to-rail input and output operation amplifiers.

The RT9137 contains a single amplifier, RT9138 contains two amplifiers and RT9139 contains four amplifiers in one package.

The RT9137/RT9138/RT9139 have high slew rates (120V/μs), 35mA continuous output current, 300mA peak output current and offset voltage below 16.5mV.

The RT9137 is available in TSOT-23-5 and WDFN-6L 2x2 packages. The RT9138 is available in MSOP-8 and WDFN-6L 2x2 packages. The RT9139 is available in WQFN-16L 4x4, TSSOP-14, TSSOP-14 (Exposed Pad), MSOP-10 and WDFN-10L 3x3 package.

The RT9137/RT9138/RT9139 are specified for operation over the full –40°C to 85°C temperature range.

Features

- **Rail-to-Rail Output Swing**
- **Supply Voltage : 4.5V to 16.5V**
- **Continuous Output Current : 35mA**
- **Peak Output Current : 300mA**
- **High Slew Rate : 120V/μs**
- **RoHS Compliant and Halogen Free**

Applications

- Notebook Computer Displays
- LCD Monitor Panels
- Automotive Displays
- LCD-TVs

Ordering Information

RT9137 □□

- Package Type
  - J5 : TSOT-23-5
  - QW : WDFN-6L 2x2 (W-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

RT9138A □□

- Package Type
  - F : MSOP-8
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

RT9138B □□

- Package Type
  - QW : WDFN-6L 2x2 (W-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

RT9139A □□

- Package Type
  - C : TSSOP-14
  - CP : TSSOP-14 (Exposed Pad)
  - QW : WQFN-16L 4x4 (W-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

RT9139B □□

- Package Type
  - F : MSOP-10
  - QW : WDFN-10L 3x3 (W-Typw)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

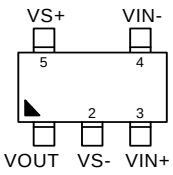
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

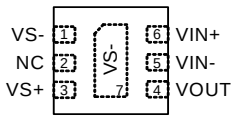
Pin Configurations

(TOP VIEW)



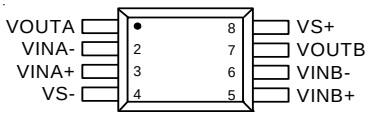
TSOT-23-5

RT9137



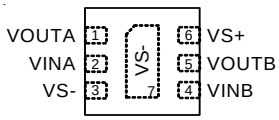
WDFN-6L 2x2

RT9137



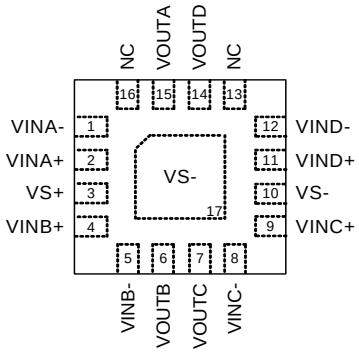
MSOP-8

RT9138A



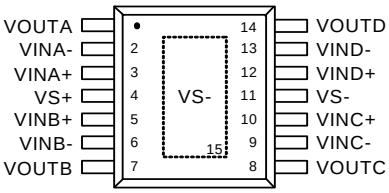
WDFN-6L 2x2

RT9138B



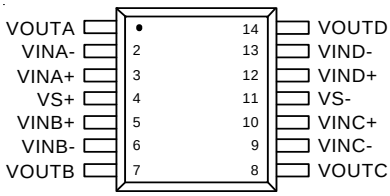
WQFN-16L 4x4

RT9139A



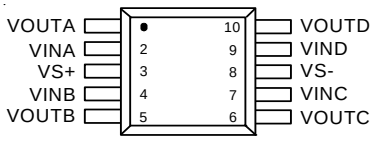
TSSOP-14 (Exposed Pad)

RT9139A



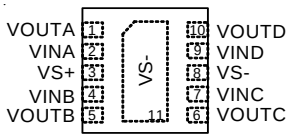
TSSOP-14

RT9139A



MSOP-10

RT9139B

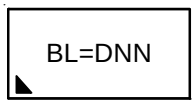


WDFN-10L 3x3

RT9139B

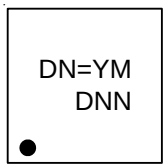
Marking Information

RT9137GJ5



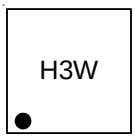
BL= : Product Code
DNN : Date Code

RT9138AGF



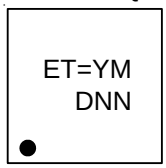
DN= : Product Code
YMDNN : Date Code

RT9138BGQW



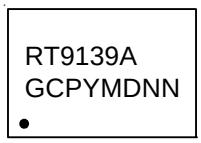
H3 : Product Code
W : Date Code

RT9139AGQW



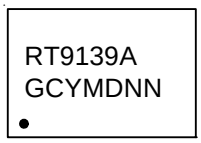
ET= : Product Code
YMDNN : Date Code

RT9139AGCP



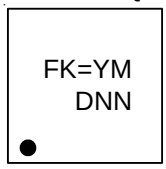
RT9139AGCP : Product Number
YMDNN : Date Code

RT9139AGC



RT9139AGC : Product Number
YMDNN : Date Code

RT9139BGQW



FK= : Product Code
YMDNN : Date Code

Functional Pin Description

RT9137

Pin No.		Pin Name	Pin Function
TSOT-23-5	WDFN-6L 2x2		
1	4	VOUT	Amplifier Output.
--	2	NC	No Internal Connection.
2	1, 7 (Exposed Pad)	VS-	Negative Power Supply.
3	6	VIN+	Amplifier Non-Inverting Input.
4	5	VIN-	Amplifier Inverting Input.
5	3	VS+	Positive Power Supply.

RT9138A

Pin No.	Pin Name	Pin Function
1	VOUTA	Amplifier A Output.
2	VINA-	Amplifier A Inverting Input.
3	VINA+	Amplifier A Non-Inverting Input.
4	VS-	Negative Power Supply.
5	VINB+	Amplifier B Non-Inverting Input.
6	VINB-	Amplifier B Inverting Input.
7	VOUTB	Amplifier B Output.
8	VS+	Positive Power Supply.

RT9138B

Pin No	Pin Name	Pin Function
1	VOUTA	Amplifier A Output.
2	VINA	Amplifier A Input.
3, 7 (Exposed Pad)	VS-	Negative Power Supply.
4	VINB	Amplifier B Input.
5	VOUTB	Amplifier B Output.
6	VS+	Positive Power Supply.

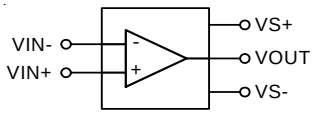
RT9139A

Pin No.			Pin Name	Pin Function
TSSOP-14	TSSOP-14 (Exposed Pad)	WQFN-16L 4x4		
1	1	15	VOUTA	Amplifier A Output.
2	2	1	VINA-	Amplifier A Inverting Input.
3	3	2	VINA+	Amplifier A Non-Inverting Input.
4	4	3	VS+	Positive Power Supply.
5	5	4	VINB+	Amplifier B Non-Inverting Input.
6	6	5	VINB-	Amplifier B Inverting Input.
7	7	6	VOUTB	Amplifier B Output.
8	8	7	VOUTC	Amplifier C Output.
9	9	8	VINC-	Amplifier C Inverting Input.
10	10	9	VINC+	Amplifier C Non-Inverting Input.
11	11, 15 (Exposed Pad)	10, 17 (Exposed Pad)	VS-	Negative Power Supply.
12	12	11	VIND+	Amplifier D Non-Inverting Input.
13	13	12	VIND-	Amplifier D Inverting Input.
14	14	14	VOUTD	Amplifier D Output.
--	--	16	NC	No Internal Connection.

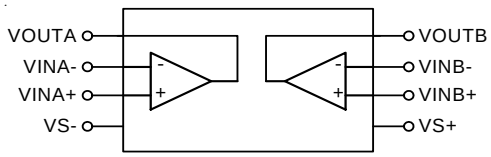
RT9139B

Pin No		Pin Name	Pin Function
MSOP-10	WDFN-10L 3x3		
1	1	VOUTA	Amplifier A Output.
2	2	VINA	Amplifier A Input.
3	3	VS+	Positive Power Supply.
4	4	VINB	Amplifier B Input.
5	5	VOUTB	Amplifier B Output.
6	6	VOUTC	Amplifier C Output.
7	7	VINC	Amplifier C Input.
8	8, 11 (Exposed Pad)	VS-	Negative Power Supply.
9	9	VIND	Amplifier D Input.
10	10	VOUTD	Amplifier D Output.

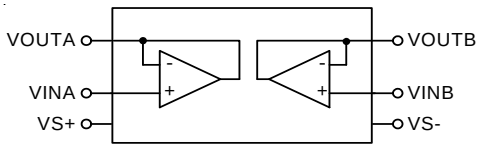
Function Block Diagram



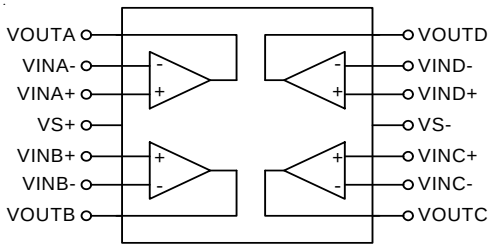
RT9137



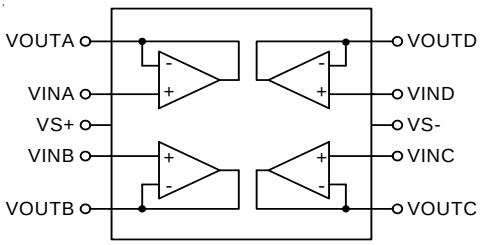
RT9138A



RT9138B



RT9139A



RT9139B

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VS+ to VS- ---------- 18V
- Input Voltage, VINx ---------- VS- – 0.5V to VS+ + 0.5V
- Differential Input Voltage ---------- VS
- Power Dissipation, P_D @ T_A = 25°C
  - TSOT-23-5 ---------- 0.625W
  - WDFN-6L 2x2 ---------- 0.833W
  - MSOP-8 ---------- 0.833W
  - TSSOP-14 (Exposed Pad) ---------- 2W
  - TSSOP-14 ---------- 0.833W
  - WQFN-16L 4x4 ---------- 1.852W
  - MSOP-10 ---------- 0.833W
  - WDFN-10L 3x3 ---------- 1.429W
- Package Thermal Resistance (Note 2)
  - TSOT-23-5, θ_{JA} ---------- 160°C/W
  - WDFN-6L 2x2, θ_{JA} ---------- 120°C/W
  - MSOP-8, θ_{JA} ---------- 120°C/W
  - TSSOP-14 (Exposed Pad), θ_{JA} ---------- 50°C/W
  - TSSOP-14, θ_{JA} ---------- 120°C/W
  - WQFN-16L 4x4, θ_{JA} ---------- 54°C/W
  - MSOP-10, θ_{JA} ---------- 120°C/W
  - WDFN-10L 3x3, θ_{JA} ---------- 70°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage (Single Supply), VS+ ---------- 4.5V to 16.5V
- Supply Voltage (Dual Supply), VS+ and VS- ---------- ± 2.25V to ± 8.25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

To be continued

Electrical Characteristics

(V_S+ = 2.5V, V_S- = –2.5V, R_L = 1kΩ to 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Characteristics						
Input Offset Voltage	V_{OS}	V_{CM} = 0V	--	3	17.5	mV
Average Offset Voltage Drift Note (2)	$\Delta V_{OS}/\Delta T$	–40°C ≤ T_A ≤ 85°C	--	7	--	μV/°C
Input Bias Current	I_B	V_{CM} = 0V	--	2	60	nA
Input Impedance Note (2)	R_{IN}		--	1	--	GΩ
Input Capacitance Note (2)	C_{IN}		--	2	--	pF
Common-Mode Input Range	CMIR		–3	--	3	V
Common-Mode Rejection Ratio	CMRR	For V_{IN} from –3V to 3V	--	70	--	dB
Open-Loop Gain	A_{VOL}	–2V ≤ V_{OUT} ≤ 2V	--	70	--	dB
Output Characteristics						
Output Swing Low	V_{OL}	I_L = –5mA	--	–2.42	–2.35	V
Output Swing High	V_{OH}	I_L = 5mA	2.35	2.42	--	V
Continuous Output Current	I_{OC}		--	±35	--	mA
Peak Output Current	I_{PC}		--	100	--	mA
Power Supply						
Power Supply Rejection Ratio	PSRR	V_S is moved from ±2.25V to ±7.5V	--	70	--	dB
Supply Current/Amplifier	I_{SY}	No Load, Per Channel	--	4.4	--	mA
Dynamic Performance						
Slew Rate Note (1)	SR	–2V ≤ V_{OUT} ≤ 2V, 20% to 80%	--	110	--	V/us
Setting to ±0.1% (A_V = 1) Note (2)	t_S	(A_V = 1), V_{OUT} = 2V step	--	100	--	ns
–3dB Bandwidth	BW	R_L = 10kΩ, C_L =10 pF	--	50	--	MHz
Gain-Bandwidth Product	GBWP	R_L = 10kΩ, C_L =10 pF	--	30	--	MHz
Phase Margin Note (2)	PM	R_L = 10kΩ, C_L =10 pF	--	50	--	°
Channel Separation	CS	f = 5MHz	--	75	--	dB

Note :

(1) Slew rate is measured on rising and falling edges.

(2) Guaranteed by design, not subject to production testing.

(V_S+ = 5V, V_S- = -5V, R_L = 1kΩ to 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Characteristics						
Input Offset Voltage	V_{OS}	V_{CM} = 0	--	3	17.5	mV
Average Offset Voltage Drift Note (2)	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ 85°C	--	7	--	μV/°C
Input Bias Current	I_B	V_{CM} = 0	--	2	60	nA
Input Impedance Note (2)	R_{IN}		--	1	--	GΩ
Input Capacitance Note (2)	C_{IN}		--	2	--	pF
Common-Mode Input Range	CMIR		−5.5	--	5.5	V
Common-Mode Rejection Ratio	CMRR	For V_{IN} from −5.5V to 5.5V	--	70	--	dB
Open-Loop Gain	A_{VOL}	−4.5V ≤ V_{OUT} ≤ 4.5V	--	70	--	dB
Output Characteristics						
Output Swing Low	V_{OL}	I_L = −5mA	--	−4.92	−4.85	V
Output Swing High	V_{OH}	I_L = 5mA	4.85	4.92	--	V
Continuous Output Current	I_{OC}		--	±35	--	mA
Peak Output Current	I_{PC}		--	250	--	mA
Power Supply						
Power Supply Rejection Ratio	PSRR	V_S is moved from ±2.25V to ±7.5V	--	70	--	dB
Supply Current/Amplifier	I_{SY}	No Load, Per Channel	--	4.6	--	mA
Dynamic Performance						
Slew Rate Note (1)	SR	−4.0V ≤ V_{OUT} ≤ 4.0V, 20% to 80%	--	120	--	V/μs
Setting to ±0.1% (A_V = +1) Note (2)	t_S	(A_V = 1), V_{OUT} = 2V step	--	100	--	ns
-3dB Bandwidth	BW	R_L = 10kΩ, C_L =10 pF	--	50	--	MHz
Gain-Bandwidth Product	GBWP	R_L = 10kΩ, C_L =10 pF	--	30	--	MHz
Phase Margin Note (2)	PM	R_L = 10kΩ, C_L =10 pF	--	50	--	°
Channel Separation	CS	f = 5MHz	--	75	--	dB

Note :

(1) Slew rate is measured on rising and falling edges.

(2) Guaranteed by design, not subject to production testing.

(V_S+ = 7.5V, V_S- = –7.5V, R_L = 1kΩ to 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Characteristics						
Input Offset Voltage	V_{OS}	V_{CM} = 0V	--	3	17.5	mV
Average Offset Voltage Drift Note (2)	$\Delta V_{OS}/\Delta T$	–40°C ≤ T_A ≤ 85°C	--	7	--	μV/°C
Input Bias Current	I_B	V_{CM} = 0V	--	2	60	nA
Input Impedance Note (2)	R_{IN}		--	1	--	GΩ
Input Capacitance Note (2)	C_{IN}		--	2	--	pF
Common-Mode Input Range	CMIR		–8	--	8	V
Common-Mode Rejection Ratio	CMRR	For V_{IN} from –8V to 8V	--	70	--	dB
Open-Loop Gain	A_{VOL}	–7V ≤ V_{OUT} ≤ 7V	--	70	--	dB
Output Characteristics						
Output Swing Low	V_{OL}	I_L = –5mA	--	–7.42	–7.35	V
Output Swing High	V_{OH}	I_L = 5mA	7.35	7.42	--	V
Continuous Output Current	I_{OC}		--	±35	--	mA
Peak Output Current	I_{PC}		--	±300	--	mA
Power Supply						
Power Supply Rejection Ratio	PSRR	V_S is moved from ±2.25V to ±7.5V	--	70	--	dB
Supply Current/Amplifier	I_{SY}	No Load, Per Channel	--	5.5	--	mA
Dynamic Performance						
Slew Rate Note (1)	SR	–7V ≤ V_{OUT} ≤ 7V, 20% to 80%	--	140	--	V/μs
Setting to ±0.1% (A_V = 1) Note (2)	t_S	(A_V = 1), V_{OUT} = 2V step	--	100	--	ns
–3dB Bandwidth	BW	R_L = 10kΩ, C_L =10 pF	--	50	--	MHz
Gain-Bandwidth Product	GBWP	R_L = 10kΩ, C_L =10 pF	--	30	--	MHz
Phase Margin Note (2)	PM	R_L = 10kΩ, C_L =10 pF	--	50	--	°
Channel Separation	CS	f = 5MHz	--	75	--	dB

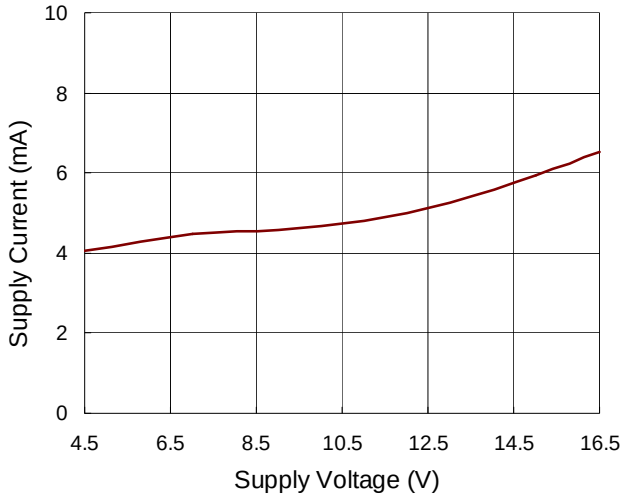
Note :

(1) Slew rate is measured on rising and falling edges.

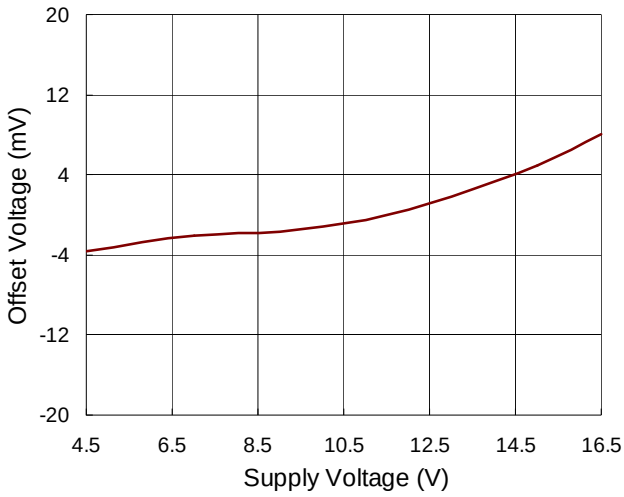
(2) Guaranteed by design, not subject to production testing.

Typical Operating Characteristics

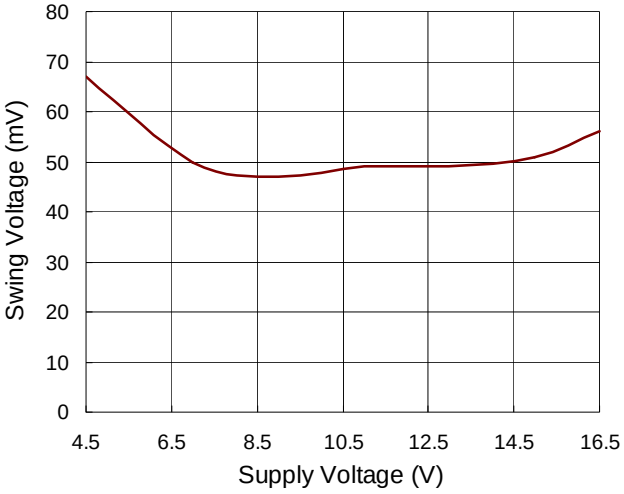
Supply Current vs. Supply Voltage



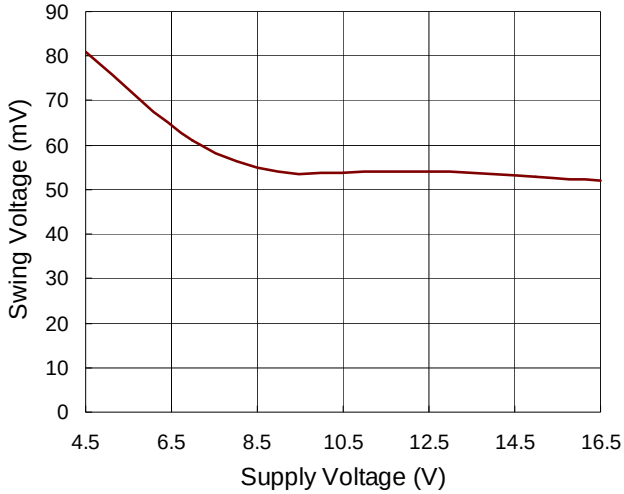
Offset Voltage vs. Supply Voltage



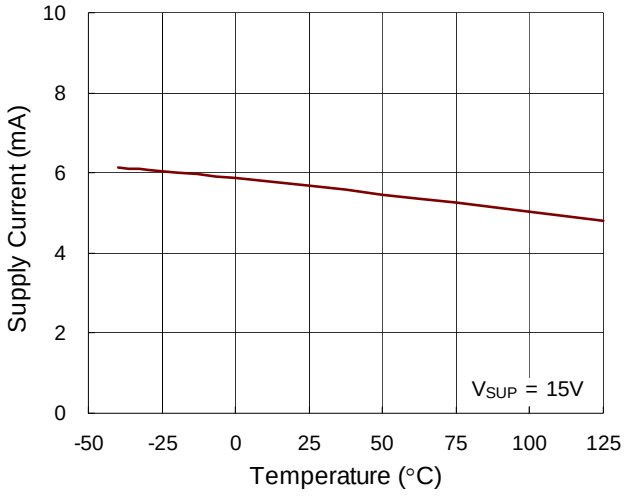
Output Swing Voltage High vs. Supply Voltage



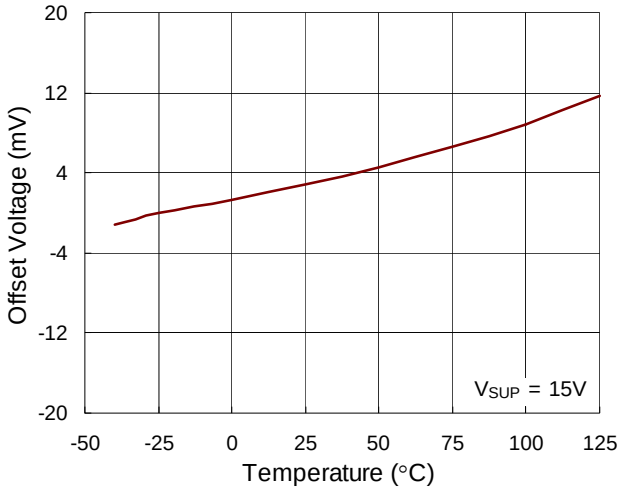
Output Swing Voltage Low vs. Supply Voltage



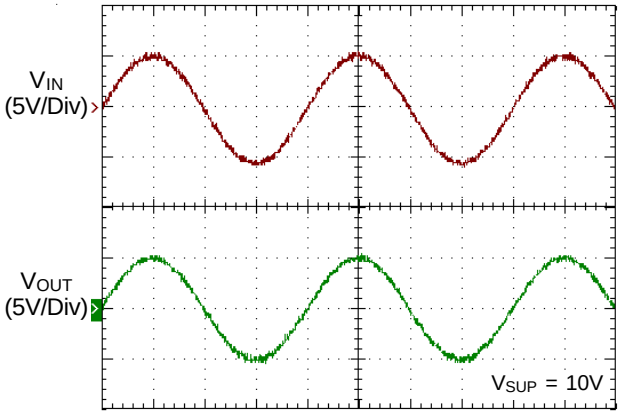
Supply Current vs. Temperature



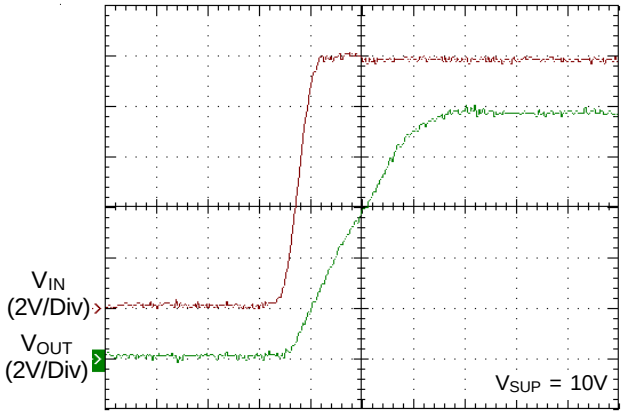
Offset Voltage vs. Temperature



Rail-to-Rail Input and Ouput Voltage



Slew Rate



Application Information

The RT9137/RT9138/RT9139 is a high performance operational amplifier capable of driving large loads for different applications. A high slew rate, rail-to-rail input and output capability, and low power consumption are the features which make the operational amplifier ideal for LCD applications. The RT9137/RT9138/RT9139 also has wide bandwidth and phase margin to drive a panel load.

Operating Voltage

The RT9137/8/9 is specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range of 4.5V to 16.5V. The RT9137/8/9 specifications remain stable over the entire supply range and operating temperature range from –40°C to 85°C. Parameter variations with operating voltage and temperature are shown in the typical performance curves. The output swing of the RT9137/8/9 typically extends to within 80mV of positive/negative supply rails with 5mA load current source/sink.

Short Circuit Condition

An internal short circuit protection circuit is implemented to protect the device from output short circuit. The RT9137/8/9 limits the short circuit current to ±300mA when supply voltage is ±7.5V. For reliability concerns, a continuous output current of not more than ±35mA is recommended.

Unused Amplifier

If the amplifier is unused, it is recommended to connect the positive input to ground while keeping the output pin open.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT9137/8/9, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. The thermal resistance, θ_{JA}, is 160°C/W for TSOT-23-5 package, 120°C/W for WDFN-6L 2x2 package, 120°C/W for MSOP-8 package, 50°C/W for TSSOP-14 (Exposed Pad) package, 120°C/W for TSSOP-14 package, 54°C/W for WQFN-16L 4x4 package, 120°C/W for MSOP-10 package, and 70°C/W for WDFN-10L 3x3 package, on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (160°C/W) = 0.625W for TSOT-23-5 package

$P_{D(MAX)}$ = (125°C – 25°C) / (120°C/W) = 0.833W for WDFN-6L 2x2 package

$P_{D(MAX)}$ = (125°C – 25°C) / (120°C/W) = 0.833W for MSOP-8 package

$P_{D(MAX)}$ = (125°C – 25°C) / (50°C/W) = 2W for TSSOP-14 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C – 25°C) / (120°C/W) = 0.833W for TSSOP-14 package

$P_{D(MAX)}$ = (125°C – 25°C) / (54°C/W) = 1.852W for WQFN-16L 4x4 package

$P_{D(MAX)}$ = (125°C – 25°C) / (120°C/W) = 0.833W for MSOP-10 package

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.429W for WDFN-10L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT9137/8/9 packages, the derating curves in Figure 1 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

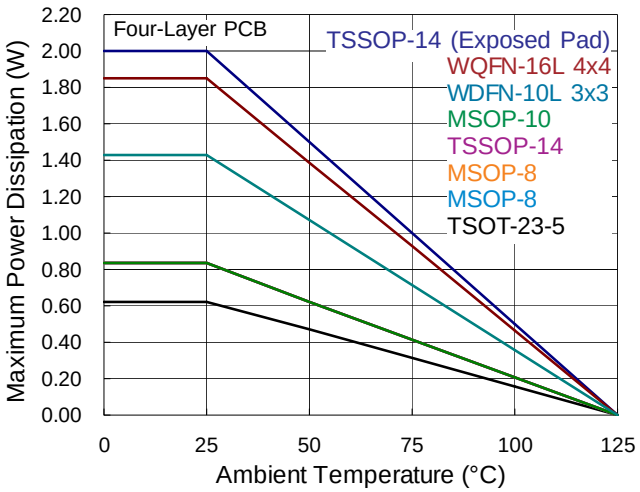


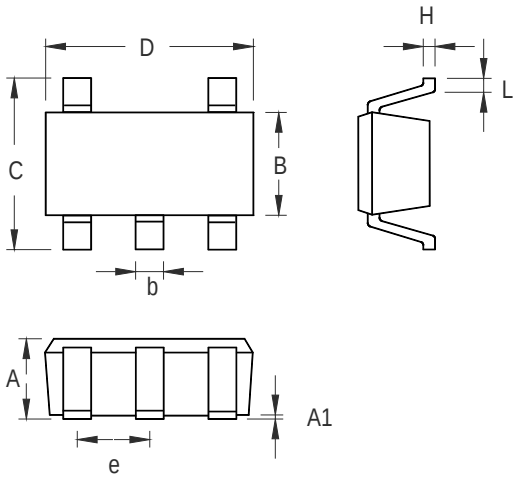
Figure 1. Derating Curves for the RT9137/8/9 Packages

Layout Considerations

PCB layout is very important for designing power circuits. The following layout guidelines should be strictly followed for best performance of the RT9137/8/9.

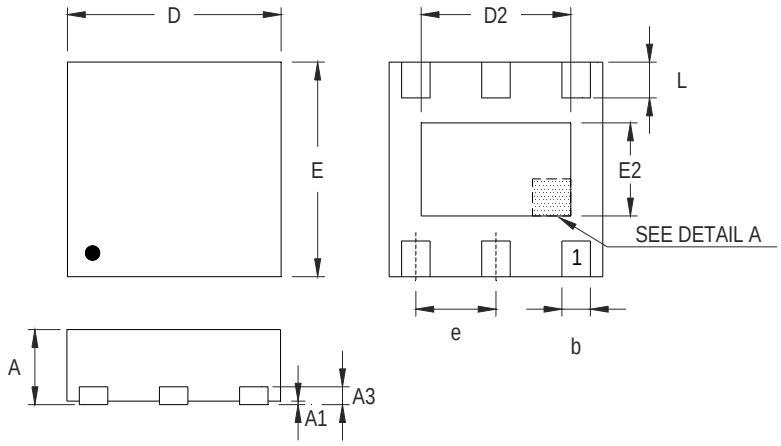
- Place the components as close to the IC as possible. The traces should be wide and short, especially for the high current loop.
- Connect a 0.1µF capacitor from VIN+ to ground and place it as close to the IC as possible for better performance.
- A series resistance may be needed at the output for some applications.
- The exposed pad of the chip should be connected to a strong ground or VS- plane for maximum thermal consideration.

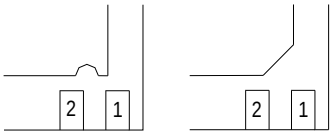
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-5 Surface Mount Package





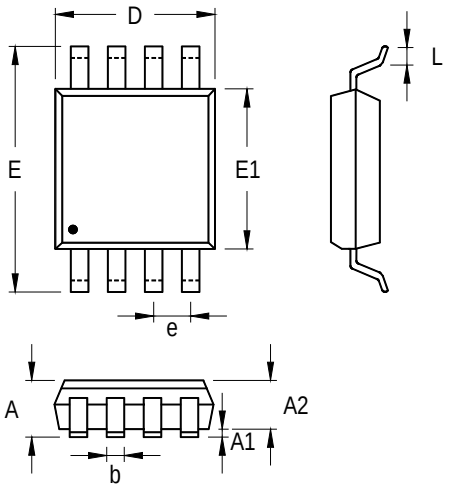
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

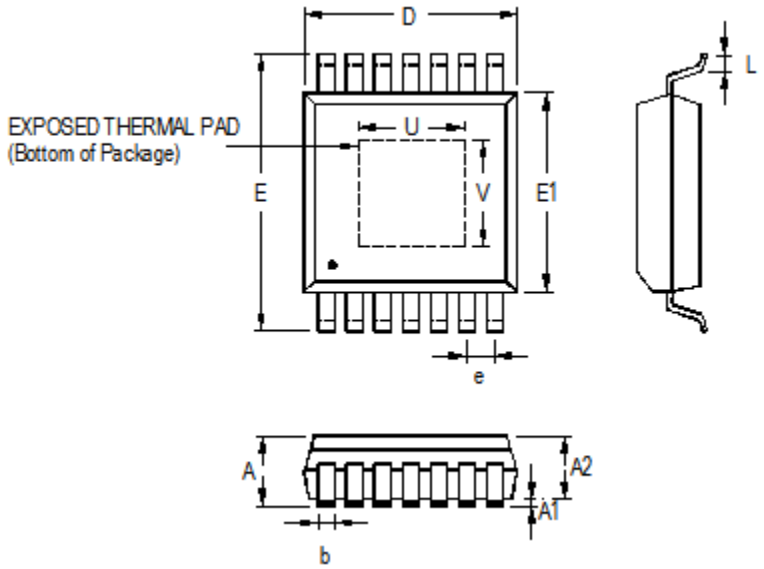
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 6L DFN 2x2 Package



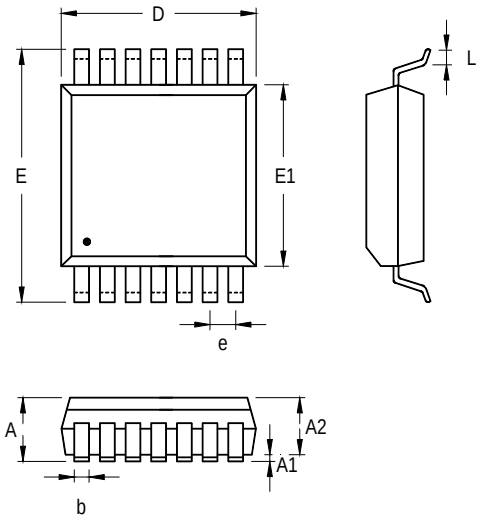
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.810	1.100	0.032	0.043
A1	0.000	0.150	0.000	0.006
A2	0.750	0.950	0.030	0.037
b	0.220	0.380	0.009	0.015
D	2.900	3.100	0.114	0.122
e	0.650		0.026	
E	4.800	5.000	0.189	0.197
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031

8-Lead MSOP Plastic Package



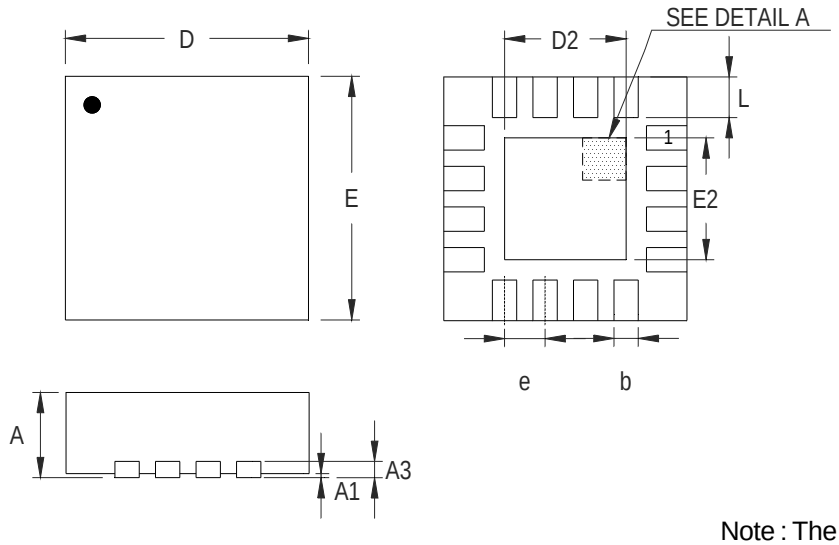
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.200	0.039	0.047
A1	0.000	0.150	0.000	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
D	4.900	5.100	0.193	0.201
e	0.650		0.026	
E	6.300	6.500	0.248	0.256
E1	4.300	4.500	0.169	0.177
L	0.450	0.750	0.018	0.030
U	1.900	2.900	0.075	0.114
V	1.600	2.600	0.063	0.102

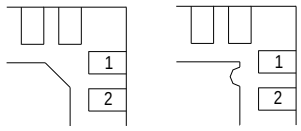
14-Lead TSSOP (Exposed Pad) Plastic Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.200	0.039	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
D	4.900	5.100	0.193	0.201
e	0.650		0.026	
E	6.300	6.500	0.248	0.256
E1	4.300	4.500	0.169	0.177
L	0.450	0.750	0.018	0.030

14-Lead TSSOP Plastic Package





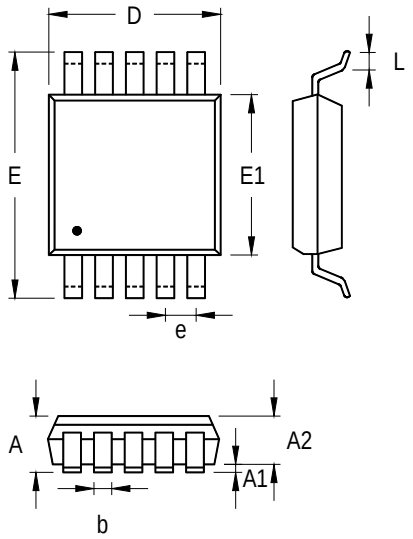
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

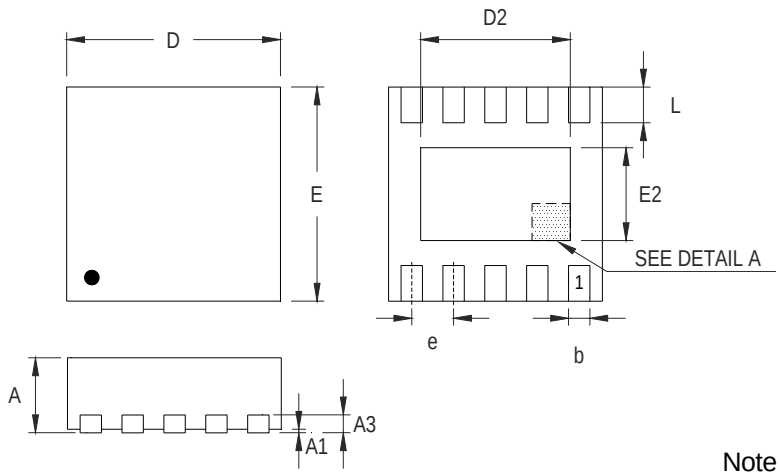
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.250	0.380	0.010	0.015
D	3.950	4.050	0.156	0.159
D2	2.000	2.450	0.079	0.096
E	3.950	4.050	0.156	0.159
E2	2.000	2.450	0.079	0.096
e	0.650		0.026	
L	0.500	0.600	0.020	0.024

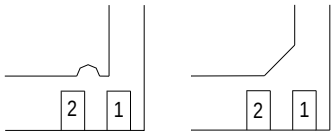
W-Type 16L QFN 4x4 Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.810	1.100	0.032	0.043
A1	0.000	0.150	0.000	0.006
A2	0.750	0.950	0.030	0.037
b	0.170	0.270	0.007	0.011
D	2.900	3.100	0.114	0.122
e	0.500		0.020	
E	4.800	5.000	0.189	0.197
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031

10-Lead MSOP Plastic Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

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