Cost-Effective, 2A Sink/Source Bus Termination Regulator

General Description

The RT9173C is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the JEDEC SSTL_2 and SSTL_18 or other specific interfaces such as HSTL, SCSI-2 and SCSI-3 etc. devices requirements. The regulator is capable of actively sinking or sourcing up to 2A while regulating an output voltage to within 40mV. The output termination voltage can be tightly regulated to track 1/2V_{DDQ} by two external voltage divider resistors or the desired output voltage can be pro-grammed by externally forcing the REFEN pin voltage.

The RT9173C also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shut-down protection.

The RT9173C are available in the SOP-8 (Exposed Pad) surface mount packages.

Ordering Information

RT9173C □□

- Package Type
  SP : SOP-8 (Exposed Pad-Option 1)
- Lead Plating System
  P : Pb Free
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-ST D-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

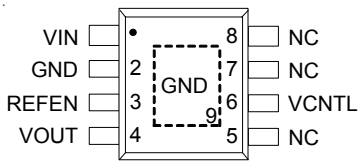
- **Ideal for DDR-I, DDR-II and DDR-III V_{TT} Applications**
- **Sink and Source 2A Continuous Current**
- **Integrated Power MOSFETs**
- **Generates Termination Voltage for SSTL_2, SSTL_18, HSTL, SCSI-2 and SCSI-3 Interfaces**
- **High Accuracy Output Voltage at Full-Load**
- **Output Adjustment by Two External Resistors**
- **Low External Component Count**
- **Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output**
- **Current Limiting Protection**
- **On-Chip Thermal Protection**
- **Available in SOP-8 (Exposed Pad) Packages**
- **V_{IN} and V_{CNTL} No Power Sequence Issue**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses
- DDR-I, DDR-II and DDR-III Memory Systems

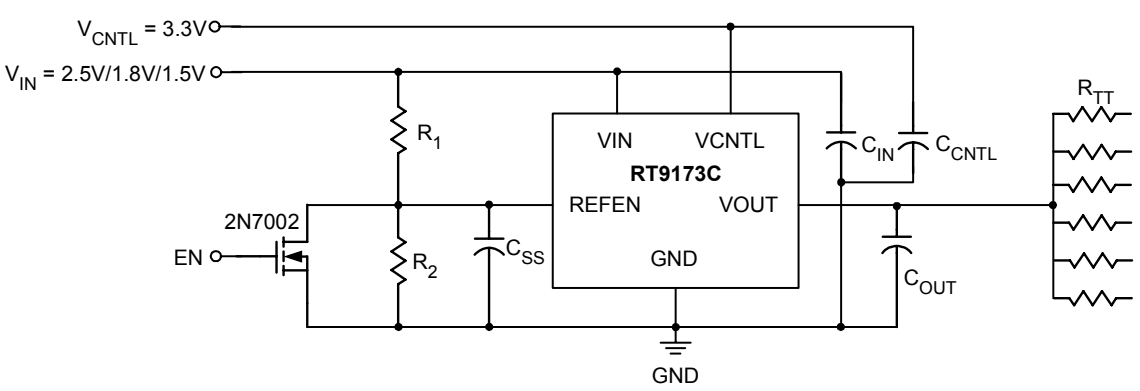
Pin Configurations

(TOP VIEW)



SOP-8 (Exposed Pad)

Typical Application Circuit



$R_1 = R_2 = 100k\Omega$, $R_{TT} = 50\Omega / 33\Omega / 25\Omega$

$C_{OUT(MIN)} = 10\mu F$ (Ceramic) + $1000\mu F$ under the worst case testing condition

$C_{SS} = 1\mu F$, $C_{IN} = 470\mu F$ (Low ESR), $C_{CNTL} = 47\mu F$

Functional Pin Description

VIN (Pin 1)

Input voltage which supplies current to the output pin. Connect this pin to a well-decoupled supply voltage. To prevent the input rail from dropping during large load transient, a large, low ESR capacitor is recommended to use. The capacitor should be placed as close as possible to the VIN pin.

GND [Pin 2, Exposed pad (9)]

Common Ground (Exposed pad is connected to GND). The GND pad area should be as large as possible and using many vias to conduct the heat into the buried GND plate of PCB layer

VCNTL (Pin 6)

VCNTL supplies the internal control circuitry and provides the drive voltage. The driving capability of output current is proportioned to the VCNTL. Connect this pin to 3.3V bias supply to handle large output current with at least 10µF capacitor from this pin to GND.

REFEN (Pin 3)

Reference voltage input and active low shutdown control pin. Two resistors dividing down the VIN voltage on the pin to create the regulated output voltage. Pulling the pin to ground turns off the device by an open-drain, such as 2N7002, signal N-Channel MOSFET.

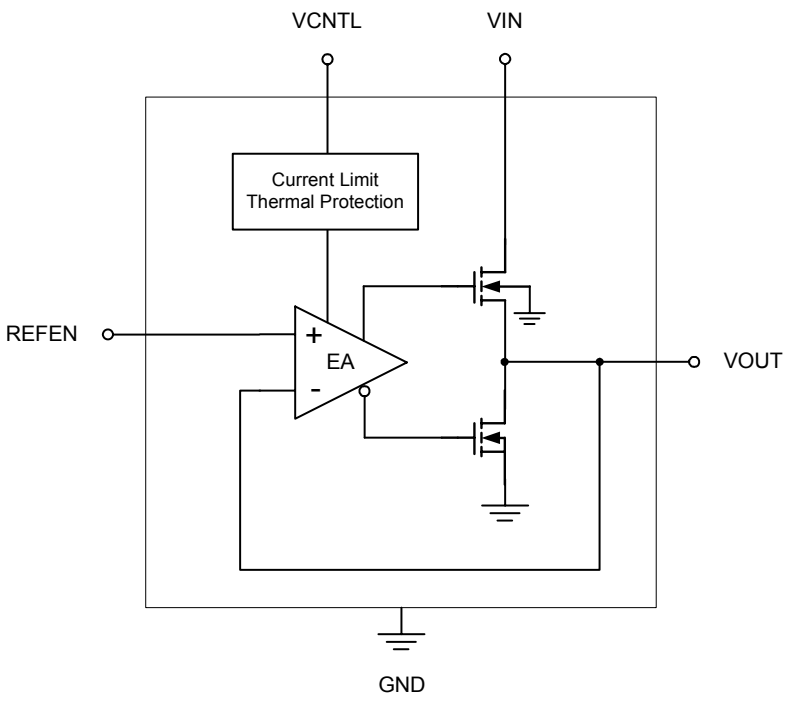
VOUT (Pin 4)

Regulator output. VOUT is regulated to REFEN voltage that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output rail. To maintain adequate large signal transient response, typical value of 1000µF AL electrolytic capacitor with 10µF ceramic capacitors are recommended to reduce the effects of current transients on VOUT.

NC (Pin 5, 7, 8)

No Internal Connect.

Function Block Diagram



Test Circuit

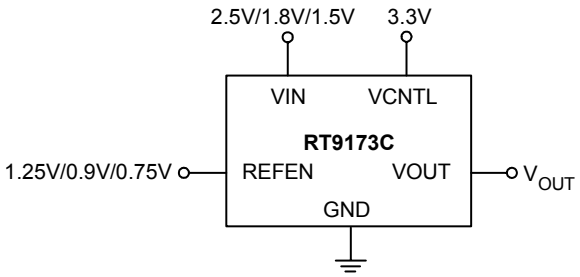


Figure 1. Test Circuit for Typical Operating Characteristics Curves

Absolute Maximum Ratings (Note 1)

- Input Voltage, V_{IN} ---------- 6V
- Control Voltage, V_{CNTL} ---------- 6V
- Power Dissipation, P_D @T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 1.33W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 28°C/W
- Junction Temperature ---------- 125°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode)---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Condition s (Note 4)

- Input Voltage, V_{IN} ---------- 2.5V to 1.5V ± 3%
- Control Voltage, V_{CNTL} ---------- 5V or 3.3V ± 5%
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 2.5V/1.8V/1.5V, V_{CNTL} = 3.3V, V_{REFEN} = 1.25V/0.9V/0.75V, C_{OUT} = 10µF (Ceramic), T_A = 25°C, unless otherwise specified)

Parameter S	ymbol	Test Conditions	Min	Typ	Max	Unit
Input						
V_{CNTL} Operation Current	I_{CNTL}	I_{OUT} = 0A	--	1	2.5	mA
Standby Current (Note 7)	I_{STBY}	V_{REFEN} < 0.2V (Shutdown), R_{LOAD} = 180Ω	-- 50		90	µA
Output (DDR / DDR II / DDR III)						
Output Offset Voltage (Note 5)	V_{OS}	I_{OUT} = 0A	–20	-	+20	mV
Load Regulation (Note 6)	ΔV_{LOAD}	I_{OUT} = 2A	–20	-	+20	mV
		I_{OUT} = –2A				
Protection						
Current limit	I_{LIM}		2.2	--	--	A
Thermal Shutdown Temperature	T_{SD} 3.3V	≤ V_{CNTL} ≤ 5V	125	170	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD} 3.3V	≤ V_{CNTL} ≤ 5V	--	35	--	°C
REFEN Shutdown						
Shutdown Threshold	V_{IH} E	nable	0.6	--	--	V
	V_{IL} S	hutdown	--	--	0.2	

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at the se or a ny other condition s beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may re main possibility to af fect device reli ability.

Note 2. θ_{JA} is me asured in the n atural conve ction at T_A = 25°C on a high ef fective thermal conductivity te st board (4 Layers, 2S2P) of JEDEC 51-7 thermal me asurement standard. The case point of θ_{JC} is on the expose pad for SOP-8 (Exposed Pad) pa ckage.

Note 3. Devices are ESD sen sitive. Ha ndling pre caution re commended.

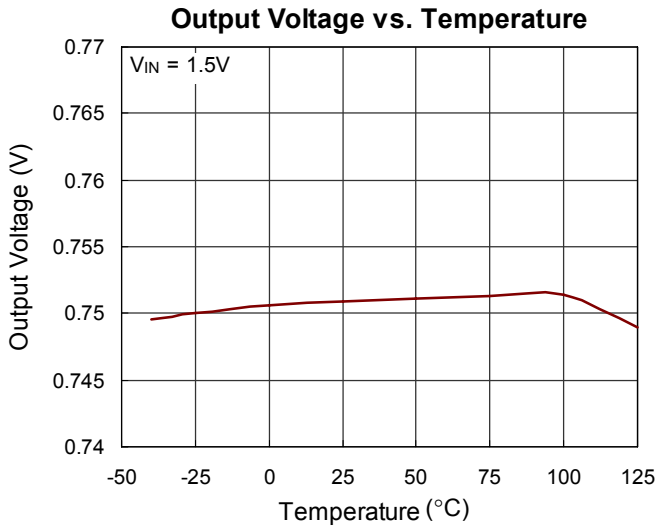
Note 4. The device is not guara nteed to function outside its operating condition s.

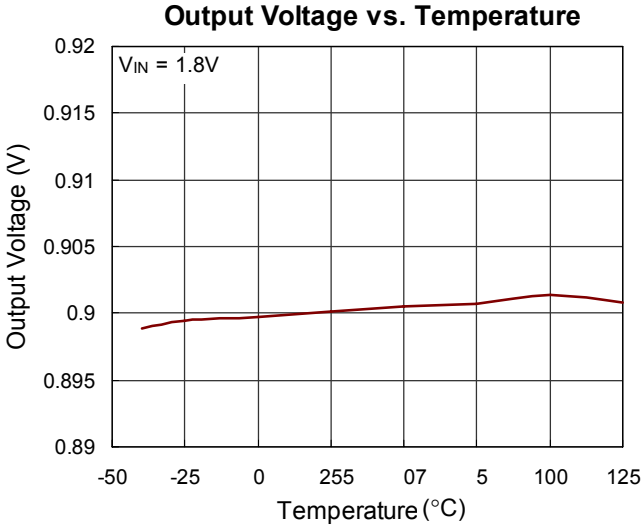
Note 5. V_{OS} offset is the voltage me asurement defined as V_{OUT} subtracted from V_{REFEN}.

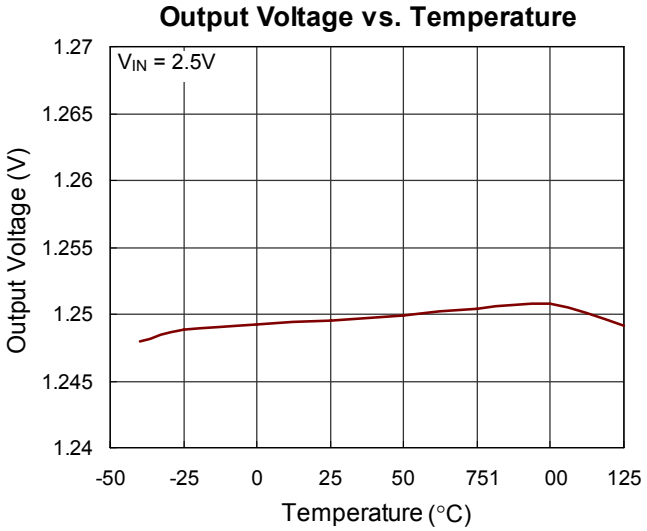
Note 6. Regulation is me asured at con stant junction te mperature by using a 5ms current pulse. Devices are te sted for loa d regulation in the loa d range from 0A to 2A.

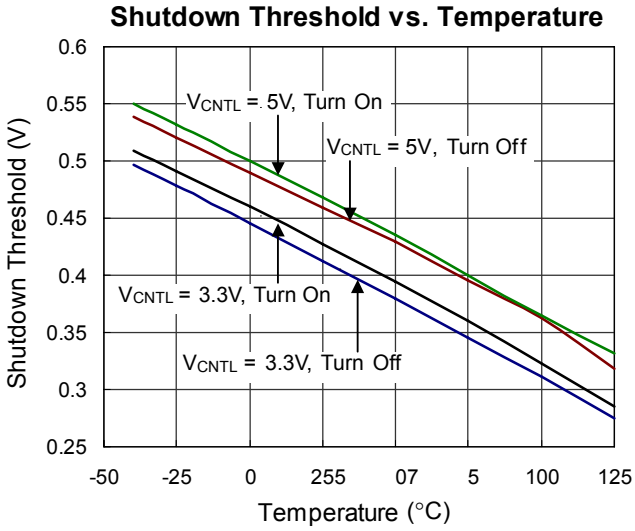
Note 7. Standby current is the in put current drawn by a regulator when the output voltage is disa bled by a shutdown sign al on REFEN pin (V_{IL} < 0.2V). It is measured with V_{IN} = V_{CNTL} = 5V.

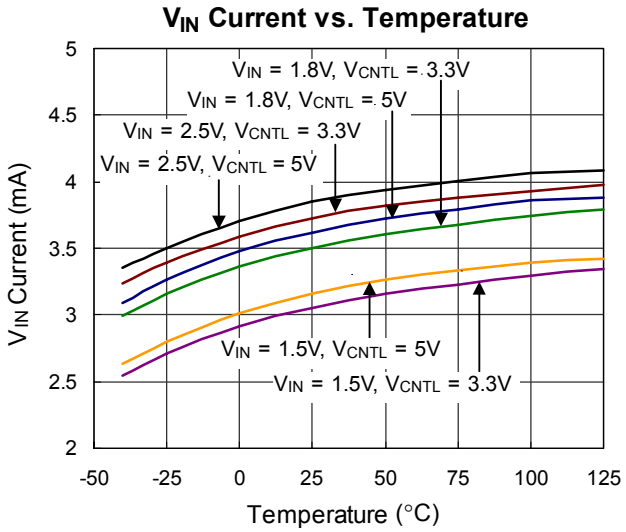
Typical Operating Characteristics

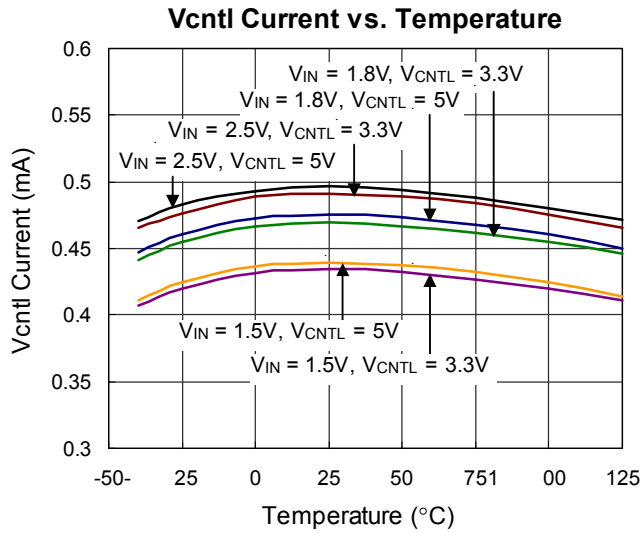




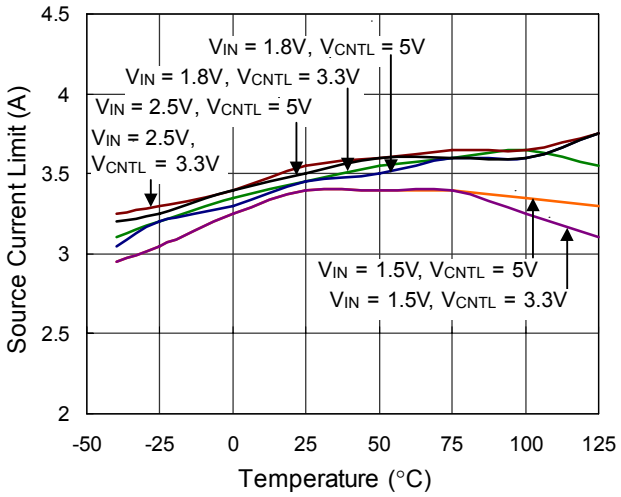




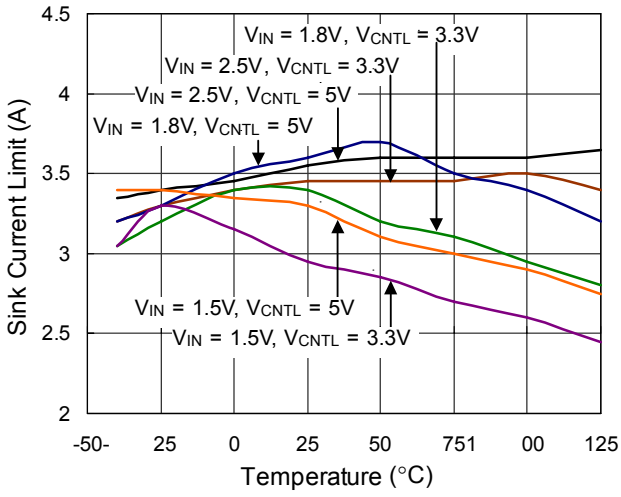




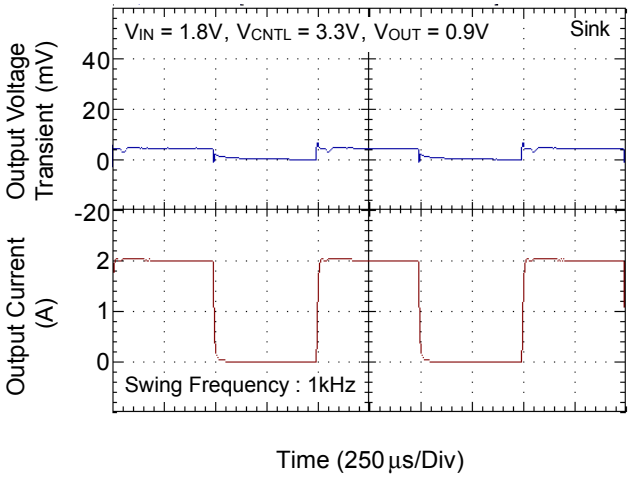
Source Current Limit vs. Temperature



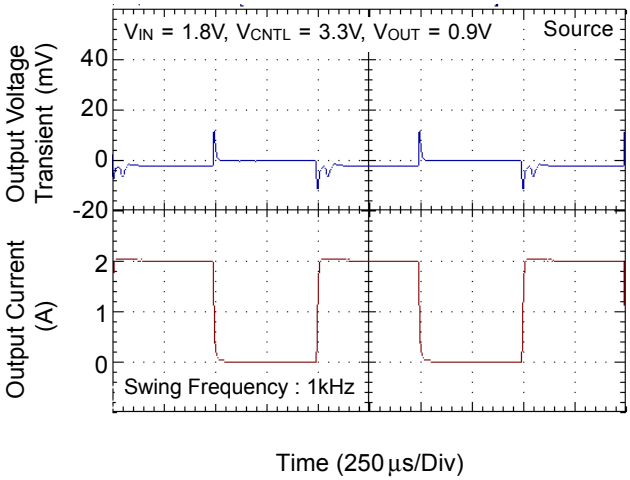
Sink Current Limit vs. Temperature



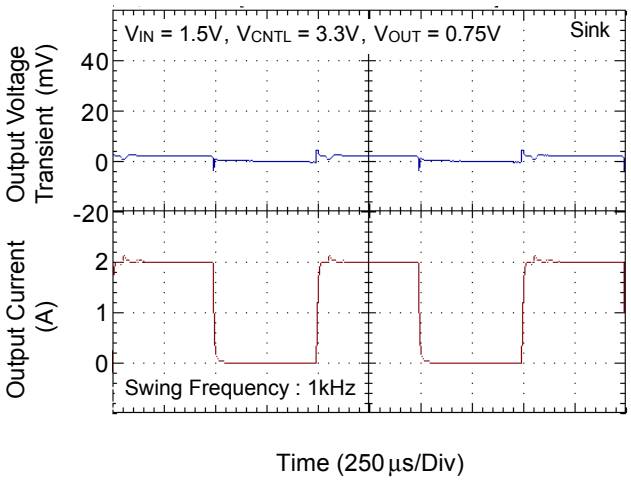
$0.9V_{TT}$ @ 2A Transient Response



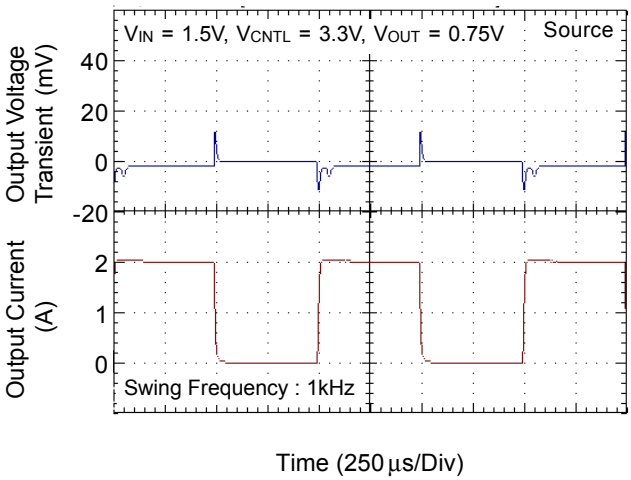
$0.9V_{TT}$ @ 2A Transient Response



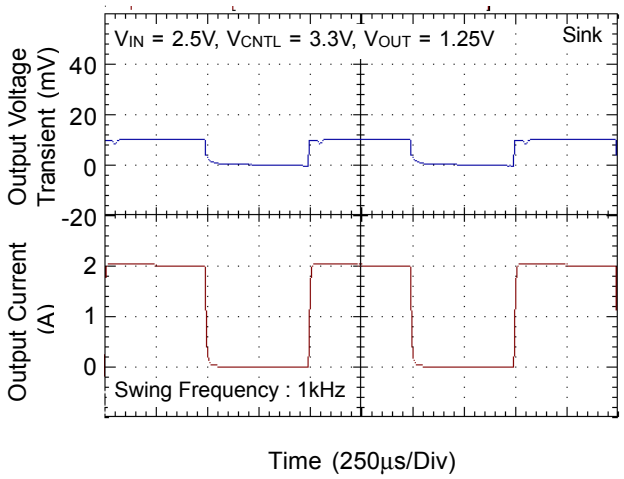
$0.75V_{TT}$ @ 2A Transient Response



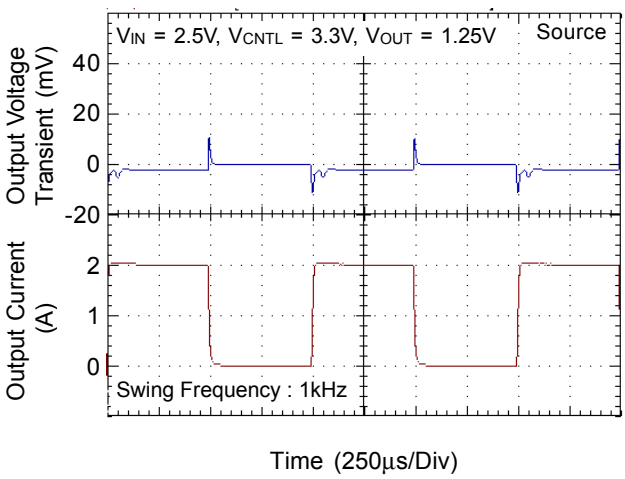
$0.75V_{TT}$ @ 2A Transient Response



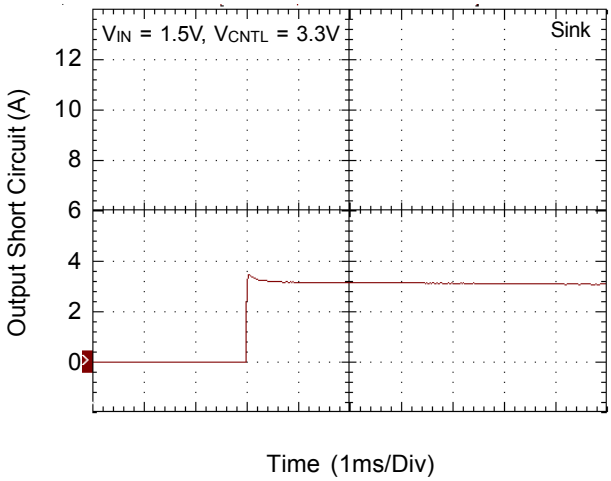
1.25V_{TT} @ 2A Transient Response



1.25V_{TT} @ 2A Transient Response



Output Short-Circuit Protection



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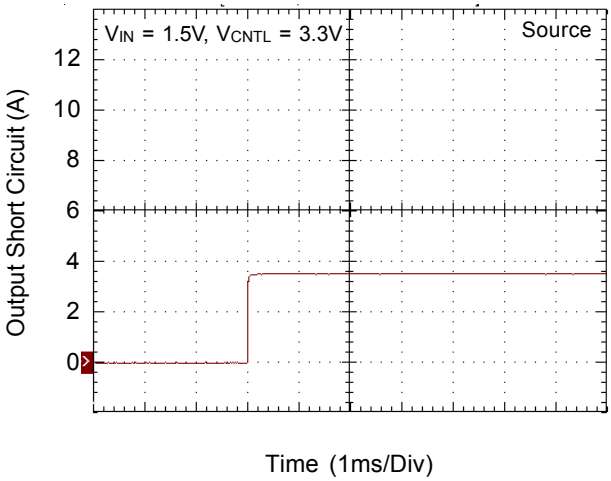
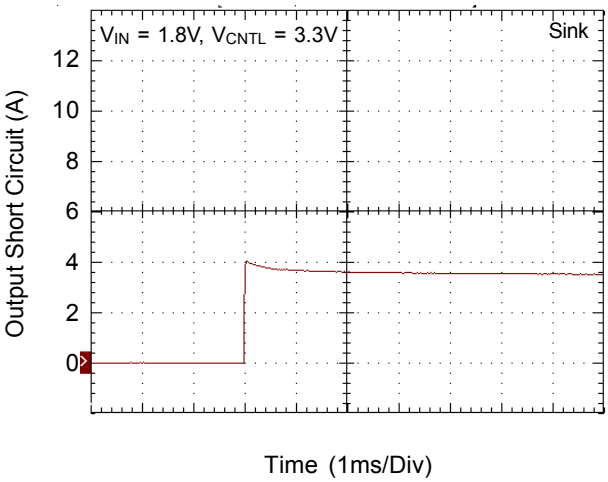


Output Short-Circuit Protection



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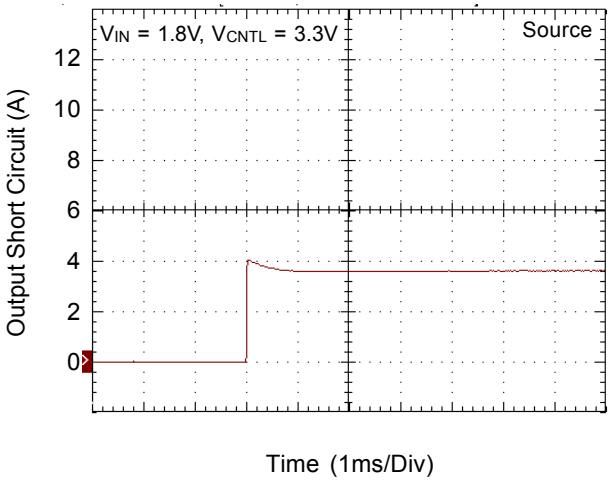
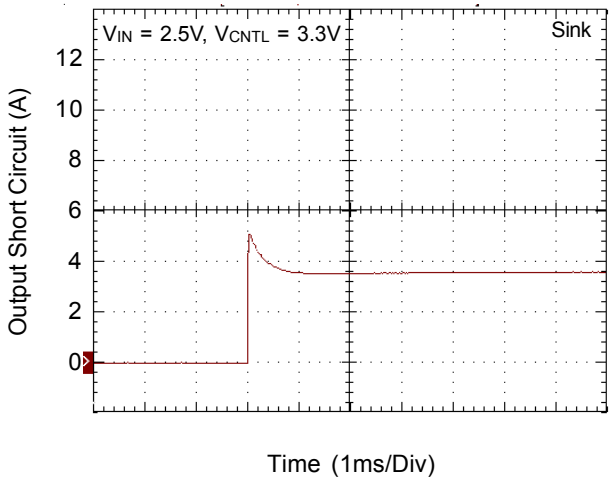
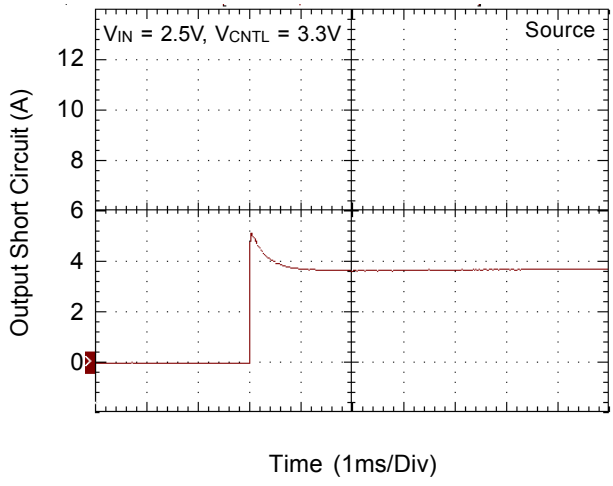


Output Short-Circuit Protection



Output Short-Circuit Protection



Application Information

Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on V_{REFEN} is below 0.2V.

In addition, the capacitor and voltage divider form the low-pass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.

How to reduce power dissipation on Notebook PC or the dual channel DDR SDRAM application?

In notebook application, using RichTek's Patent "Distributed Bus Terminator Topology" with choosing RichTek's product is encouraged.

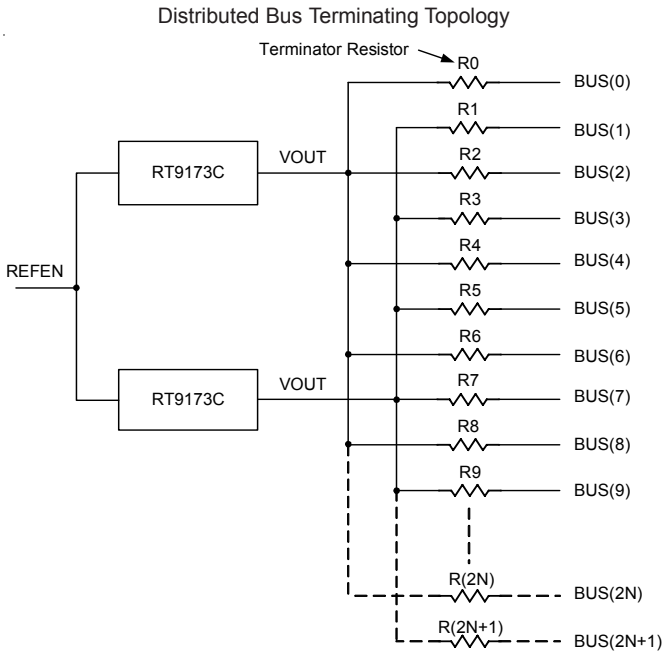


Figure 2

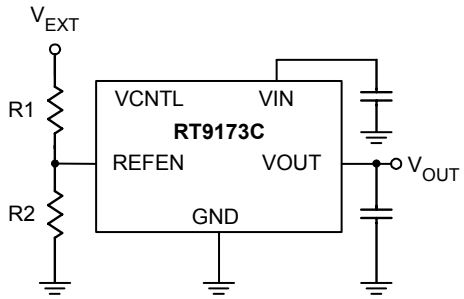


Figure 3

General Regulator

The RT9173C could also serves as a general linear regulator. The RT9173C accepts an external reference voltage at REFEN pin and provides output voltage regulated to this reference voltage as shown in Figure 3, where

$V_{OUT} = V_{EXT} \times R2/(R1+R2)$

For sourcing 2A output applications, the RT9173C could works with low-ESR ceramic capacitors as a general linear regulator. It offers significant cost and space savings for power applications, especially for hand-held wireless devices and notebooks application. The recommended input and output capacitors must be 10μF or greater X7R/X5R ceramic capacitors. The input and output capacitors should be located as close as possible to the IC.

It's not recommended for sinking application while using ceramic capacitors. When the sinking function is used with ceramic capacitors, the system may be unstable. If the current sinking function is necessary for this regulator, please refer to the RT9173C Typical Application Circuit as shown on page 2 for component selection.

As other linear regulator, dropout voltage and thermal issue should be specially considered. Figure 4 and 5 show the $R_{DS(ON)}$ over-temperature of RT9173C in PSOP-8 (Exposed Pad) package. The minimum dropout voltage could be obtained by the product of $R_{DS(ON)}$ and output current. For thermal consideration, please refer to the relative sections.

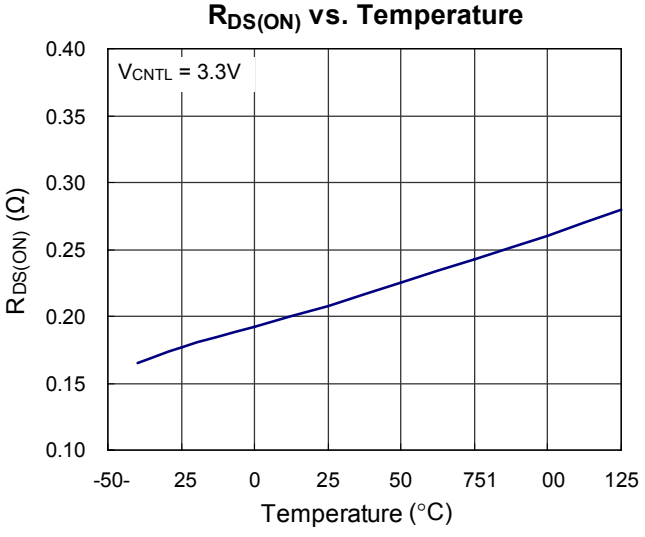


Figure 4

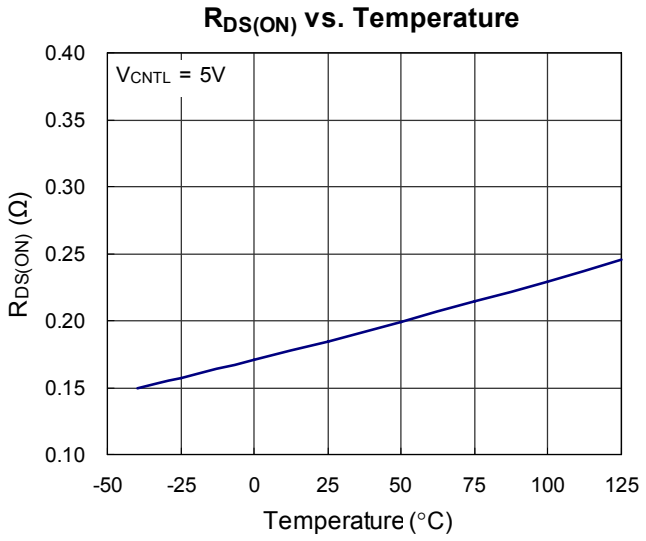


Figure 5

Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the RT9173C. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance. Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between RT9173C and the preceding power converter.

Thermal Consideration

RT9173C regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continued operation, do not exceed maximum operation junction temperature 125 °C. The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for SOP-8 package (Exposed Pad) is 75°C/W on standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula:

$$P_{D(MAX)} = (125°C - 25°C) / 75°C/W = 1.33W$$

Figure 6 show the package sectional drawing of SOP-8 (Exposed Pad). Every package has several thermal dissipation paths. As show in Figure 7, the thermal resistance equivalent circuit of SOP-8 (Exposed Pad). The path 2 is the main path due to these materials thermal conductivity. We define the exposed pad is the case point of the path 2.

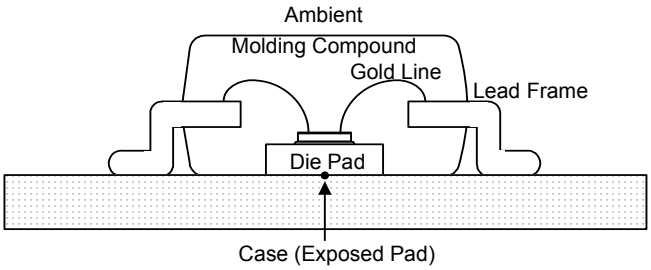


Figure 6. SOP-8 (Exposed Pad) Package Sectional Drawing

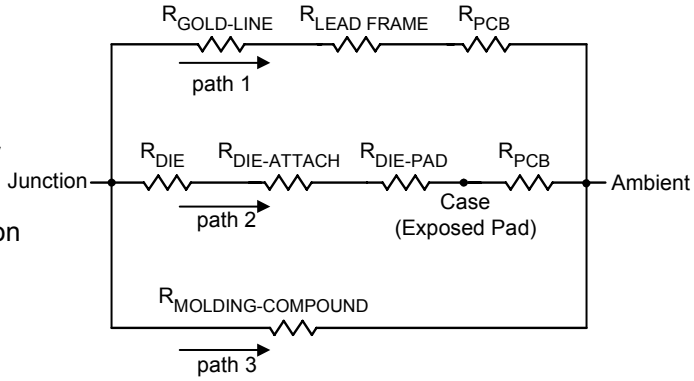


Figure 7. Thermal Resistance Equivalent Circuit

The thermal resistance θ_{JA} of SOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the exposed pad of SOP-8 package.

About PCB layout, the Figure 8 show the relation between thermal resistance θ_{JA} and copper area on standard JEDEC 51-7 (4 layers, 2S2P) thermal test board at T_A = 25°C. We have to consider the copper couldn't stretch

infinitely and avoid the tin overflow. We use the "dog-bone" copper patterns on the top layer as Figure 9.

As shown in Figure 10, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad of 2 oz. copper (Figure 10.a), θ_{JA} is 75°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 10.b) reduces the θ_{JA} to 64°C/W. Even further, increasing the copper area of pad to 70mm^2 (Figure 10.e) reduces the θ_{JA} to 49°C/W.

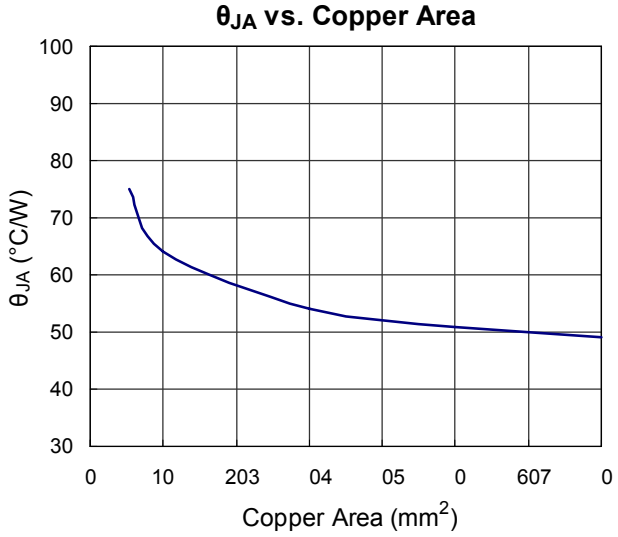


Figure 8

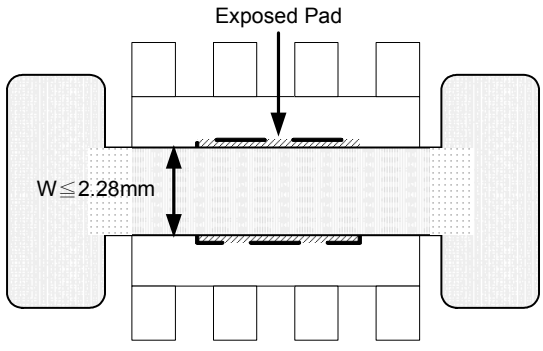


Figure 9.Dog-Bone layout

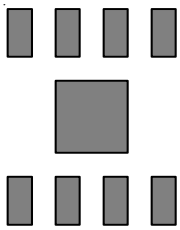


Figure 10 (a). Minimum Footprint, θ_{JA} = 75°C/W

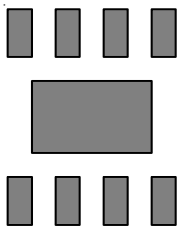


Figure 10 (b). Copper Area = 10mm^2, θ_{JA} = 64°C/W

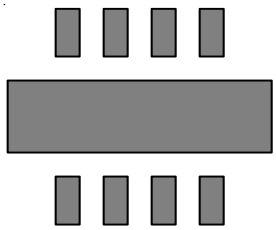


Figure 10 (c). CopperArea = 30mm^2, θ_{JA} = 54°C/W

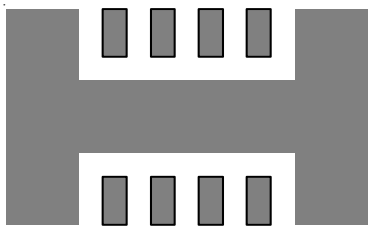


Figure 10 (d). CopperArea = 50mm^2, θ_{JA} = 51°C/W

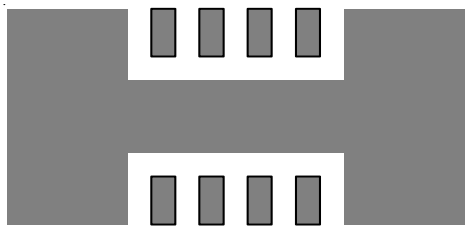
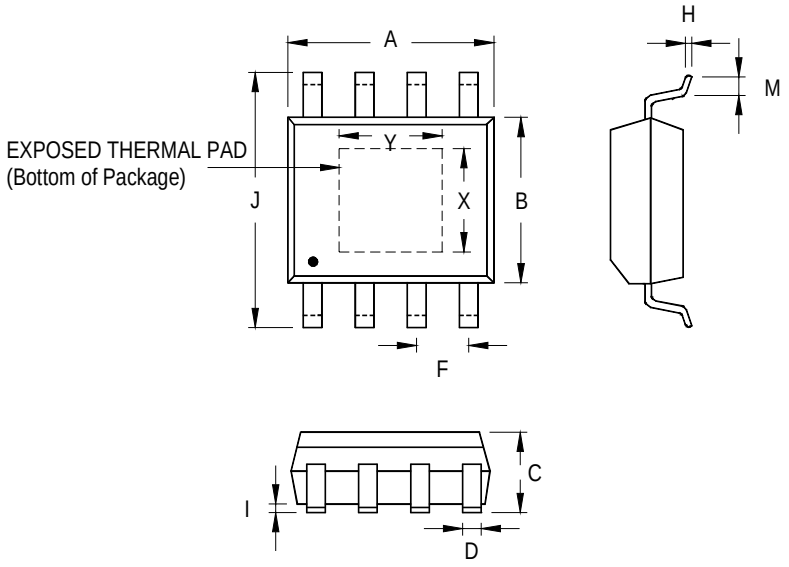


Figure 10 (e). CopperArea = 70mm^2, θ_{JA} = 49°C/W

Figure 10. Thermal Resistance vs. Different Cooper Area Layout Design

Outline Information



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min Ma	x	Min	Max
A 4.		801	5.004	0.189	0.197
B		3.810 4.	000	0.150	0.157
C		1.346 1.	753	0.053	0.069
D		0.330 0.	510	0.013	0.020
F		1.194 1.	346	0.047	0.053
H		0.170 0.	254	0.007	0.010
I		0.000 0.	152	0.000	0.006
J		5.791 6.	200	0.228	0.244
M		0.406 1.	270	0.016	0.050
Option 1	X	2.000 2.	300	0.079	0.091
	Y	2.000 2.	300	0.079	0.091
Option 2	X	2.100 2.	500	0.083	0.098
	Y	3.000	3.500 0.	118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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