

Tiny Package, High Efficiency, Step-Up DC/DC Converter

General Description

The RT9266B is a compact, high efficiency, and low voltage step-up DC/DC converter with an Adaptive Current Mode PWM control loop, includes an error amplifier, ramp generator, comparator, switch pass element and driver in which providing a stable and high efficient operation over a wide range of load currents. It operates in stable waveforms without external compensation.

The low start-up input voltage below 1V makes RT9266B suitable for 1 to 4 battery cells applications with a 500mA internal switch. The 550kHz high switching rate minimized the size of external components. Besides, the 25μA low quiescent current together with high efficiency maintains long battery lifetime.

Ordering Information

RT9266B □ □

- Package Type
E : SOT-23-6
- Lead Plating System
P : Pb Free
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

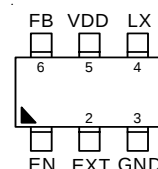
- 1V Low Start-up Input Voltage at 1mA Load
- 25μA Quiescent (Switch-off) Supply Current
- Zero Shutdown Mode Supply Current
- 90% Efficiency
- 550kHz Switching Frequency at 3.3V V_{DD}
- Providing Flexibility for Using Internal and External Power Switches
- Small SOT-23-6 Package
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

- PDA
- DSC
- LCD Panel
- RF-Tags
- MP3
- Portable Instrument
- Wireless Equipment

Pin Configurations

(TOP VIEW)



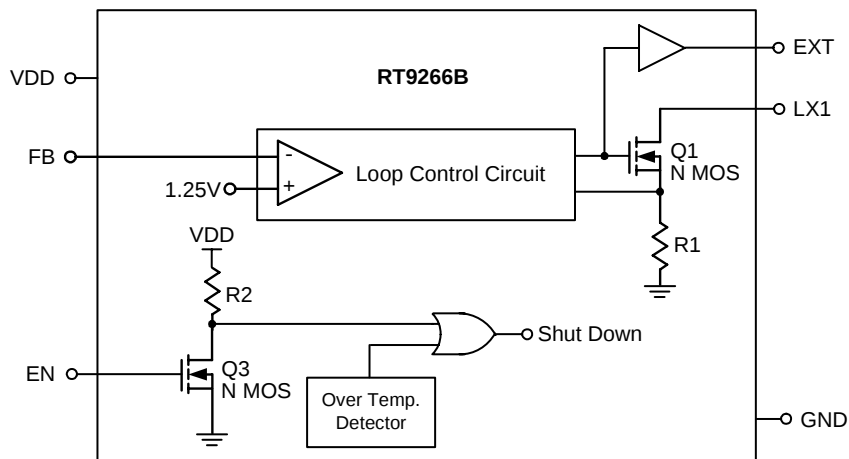
SOT-23-6

The schematic diagram illustrates a 3.3V/5V LDO regulator circuit. The input voltage V_{IN} is connected to the VDD pin of the RT9266B LDO. A 10 μ F capacitor (C3) is connected between the input and ground. The output of the LDO is connected to the output voltage V_{OUT} (3.3V/5V). A 1 μ F capacitor (C2) is connected between the output and ground. The LDO is configured with the EN pin to VDD, the LX pin to the output, and the FB pin to ground. The RT9266B is a 3.3V/5V LDO regulator. The output voltage is regulated by a feedback network consisting of a 1.6M/3M resistor (R1) and a 980k/1M resistor (R2) connected to the FB pin. A 10 μ F capacitor (C1) is connected between the output and ground. The output voltage is also connected to a diode (D1, SS0520) and a 3.3 to 10 μ H inductor (L1) connected to the input.

Functional Pin Description

Pin Name	Pin Function
EN	Chip Enable (Active High)
EXT	Output Pin for Driving External NMOS
GND	Ground
LX	Pin for Switching
VDD	Input Positive Power Pin of RT9266B
FB	Feedback Input Pin Internal Reference Voltage for the Error Amplifier is 1.25V.

Function Block Diagram



Absolute Maximum Ratings

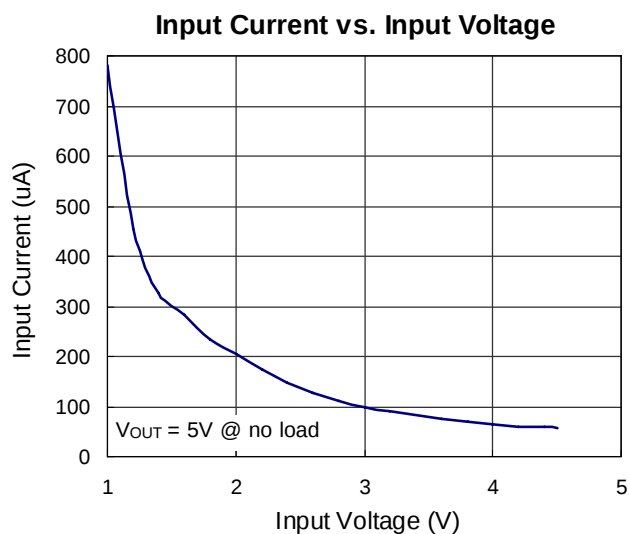
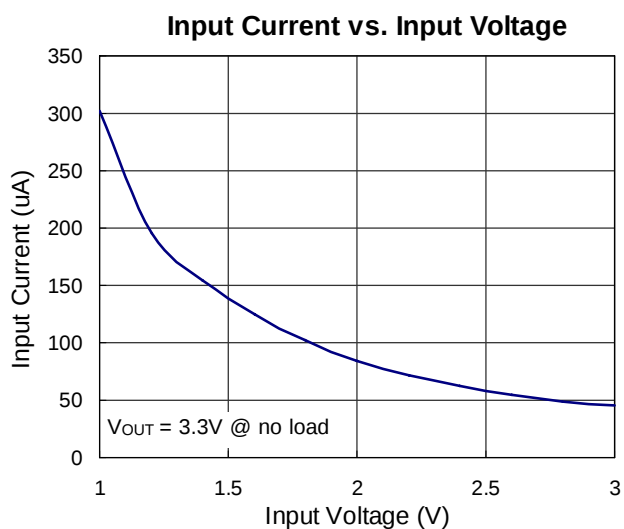
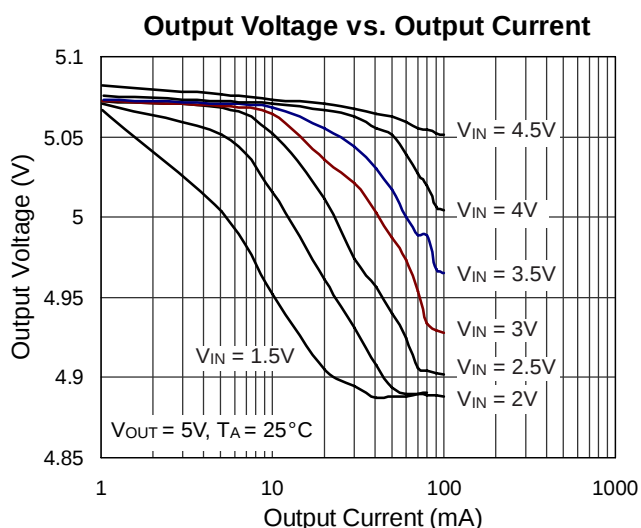
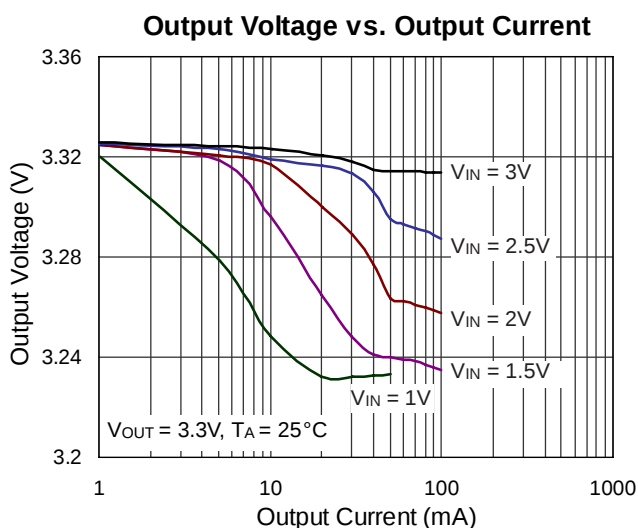
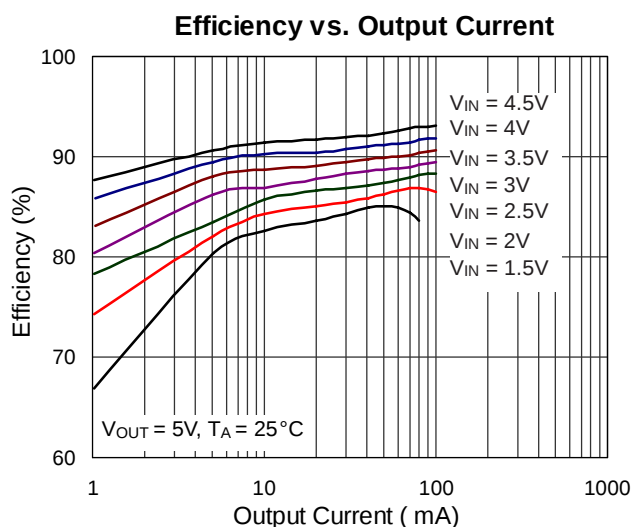
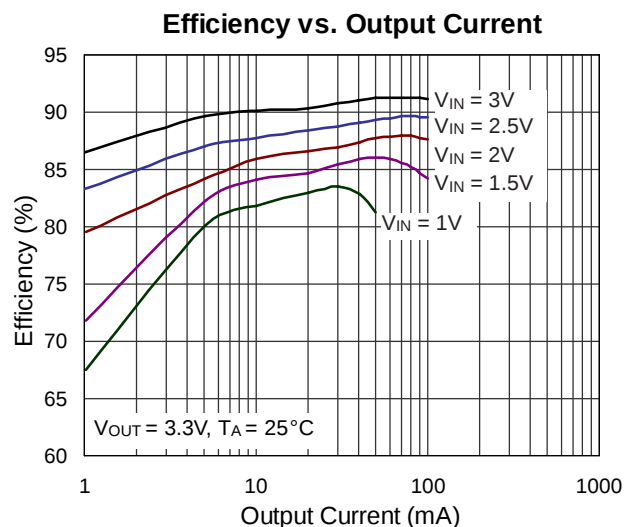
- Supply Voltage ----- -0.3V to 7V
- LX Pin Switch Voltage ----- -0.3V to 6.5V
- Other I/O Pin Voltages ----- -0.3V to ($V_{DD} + 0.3V$)
- LX Pin Switch Current ----- 2.5A
- EXT Pin Driver Current ----- 200mA
- Package Thermal Resistance
SOT-23-6, θ_{JC} ----- 145°C/W
- Operating Junction Temperature ----- 125°C
- Storage Temperature Range ----- -65°C to +150°C

Electrical Characteristics

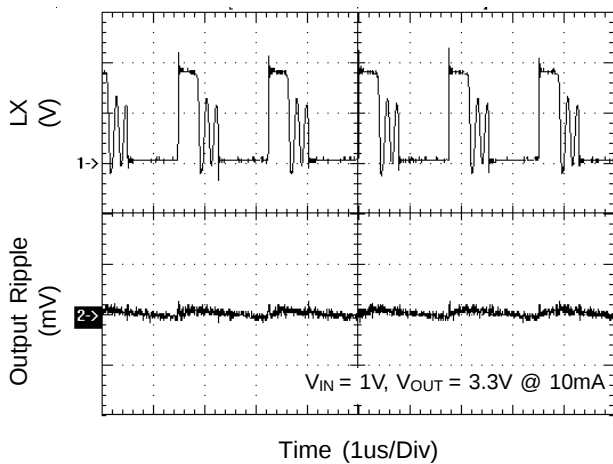
($V_{IN} = 1.5V$, V_{DD} set to 3.3V, Load Current = 0, $T_A = 25^\circ C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Start-UP Voltage	V_{ST}	$I_L = 1mA$	--	0.98	1.05	V
Operating VDD Range	V_{DD}	VDD pin voltage	2	--	6.5	V
No Load Current I (V_{IN})	$I_{NO\ LOAD}$	$V_{IN} = 1.5V$, $V_{OUT} = 3.3V$	--	150	--	μA
Switch-off Current I (V_{DD})	$I_{SWITCH\ OFF}$	$V_{IN} = 6V$	--	25	--	μA
Shutdown Current I (V_{IN})	I_{OFF}	EN Pin = 0V, $V_{IN} = 4.5V$	--	0.01	1	μA
Feedback Reference Voltage	V_{REF}	Close Loop, $V_{DD} = 3.3V$	1.225	1.25	1.275	V
Switching Frequency	F_S	$V_{DD} = 3.3V$	--	550	--	kHz
Maximum Duty	D_{MAX}	$V_{DD} = 3.3V$	--	95	--	%
LX ON Resistance		$V_{DD} = 3.3V$	--	0.35	--	Ω
Current Limit Setting	I_{LIMIT}	$V_{DD} = 3.3V$	--	0.5	--	A
Current Limit Delay Time		$V_{DD} = 3.3V$	--	300	--	ns
EXT ON Resistance to V_{DD}		$V_{DD} = 3.3V$	--	5	--	Ω
EXT ON Resistance to GND		$V_{DD} = 3.3V$	--	5	--	Ω
Line Regulation (refer to V_{FB})	ΔV_{LINE}	$V_{IN} = 1.5 \sim 2.5V$, $I_L = 50mA$	--	12	--	mV/V
Load Regulation (refer to V_{FB})	ΔV_{LOAD}	$V_{IN} = 2.5V$, $I_L = 1 \sim 100mA$	--	0.25	--	mV/mA
EN Pin Trip Level		$V_{DD} = 3.3V$	0.4	0.8	1.2	V
Temperature Stability for V_{out}	T_S		--	50	--	ppm/ $^\circ C$
Thermal Shutdown	T_{SD}		--	165	--	$^\circ C$
Thermal Shutdown Hysteresis	ΔT_{SD}		--	10	--	$^\circ C$

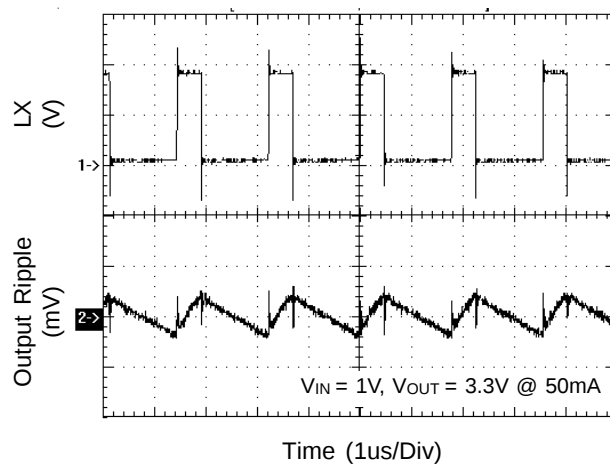
Typical Operating Characteristics



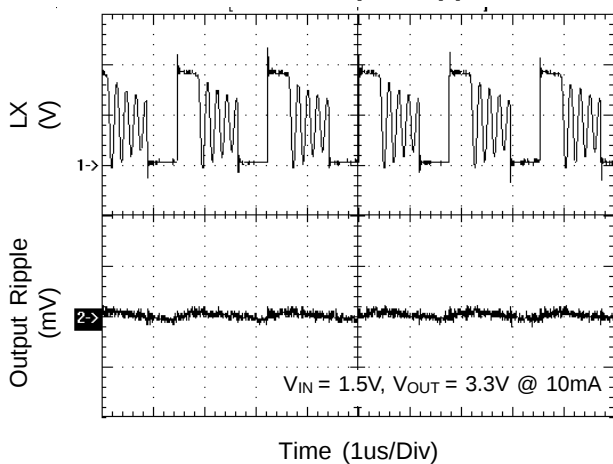
LX & Output Ripple



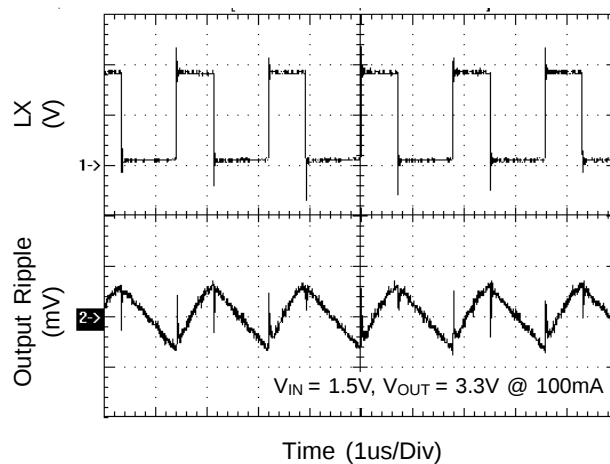
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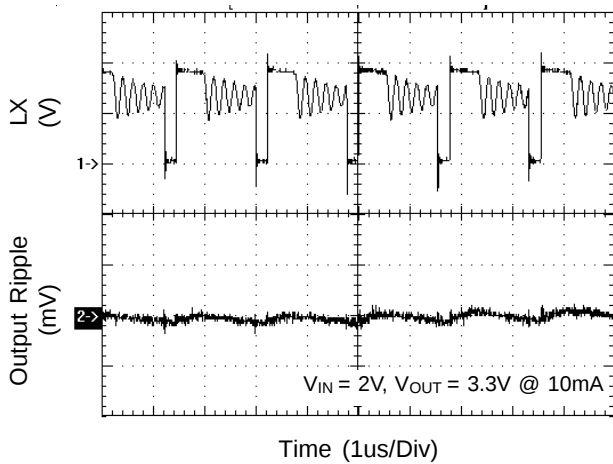
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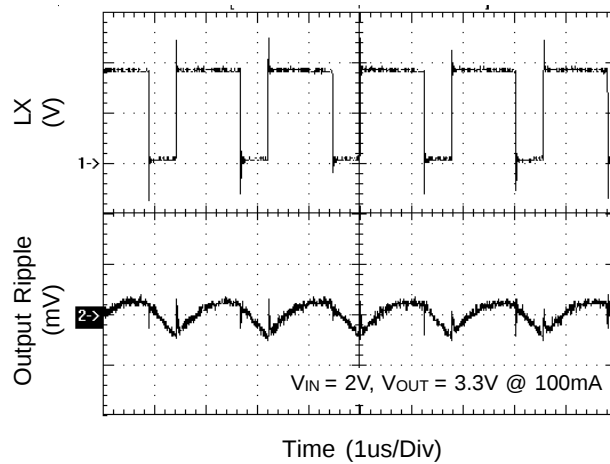
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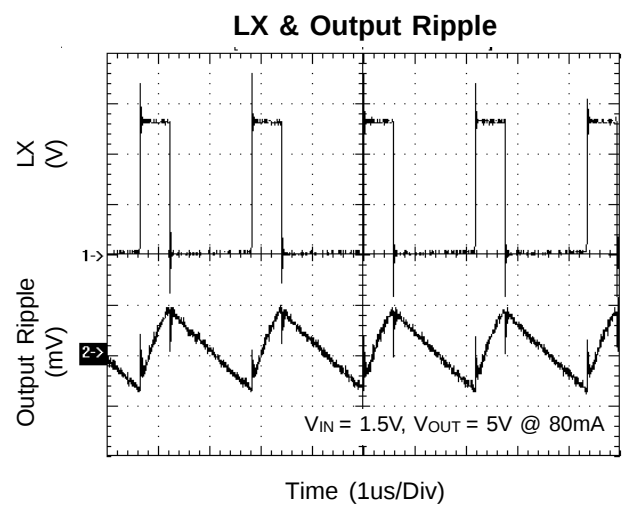
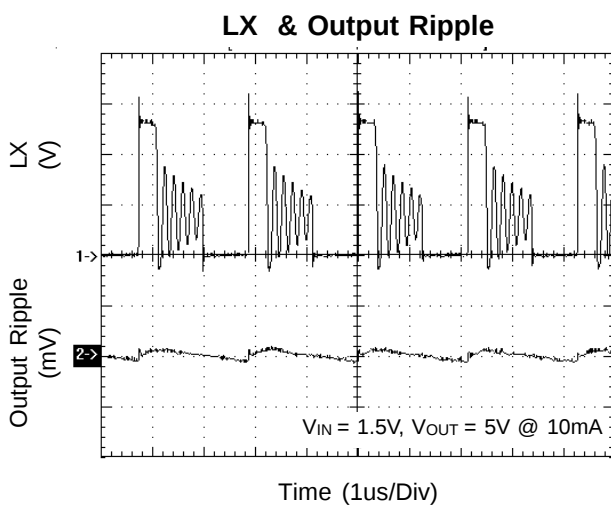
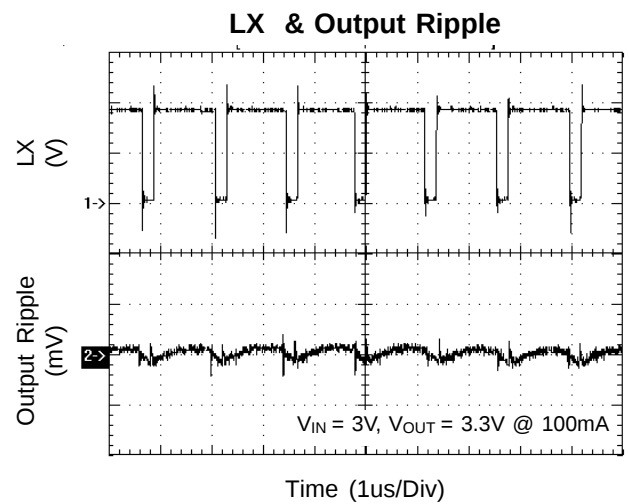
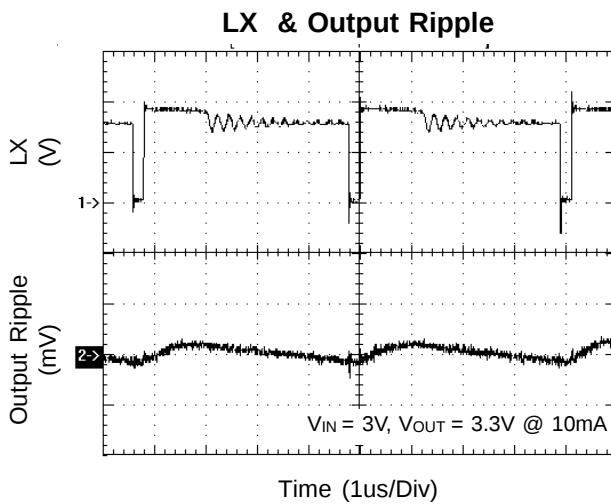
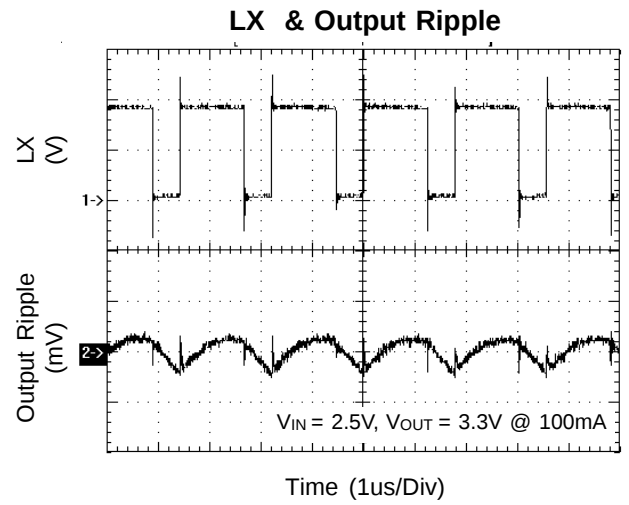
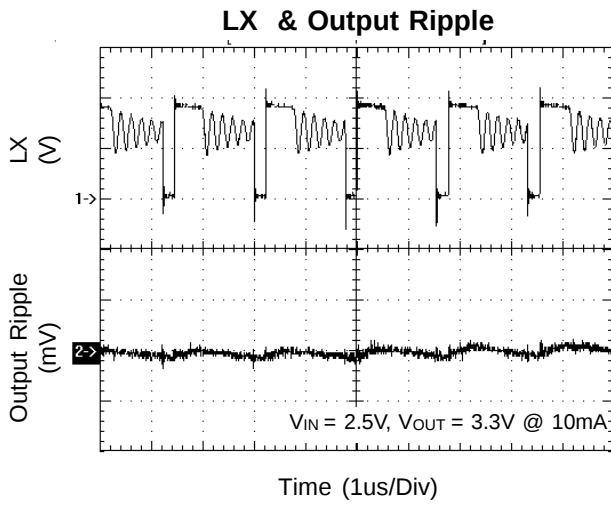


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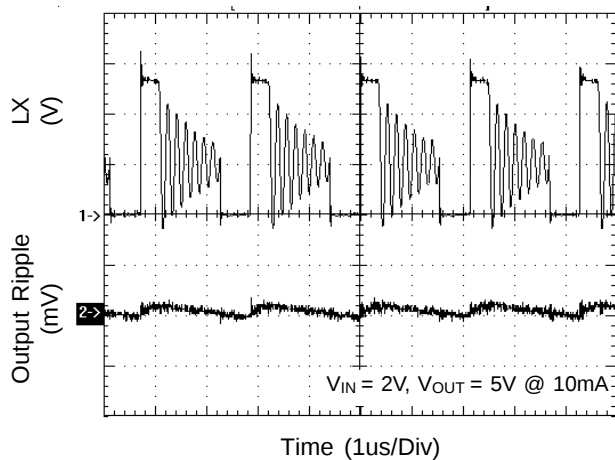


LX & Output Ripple

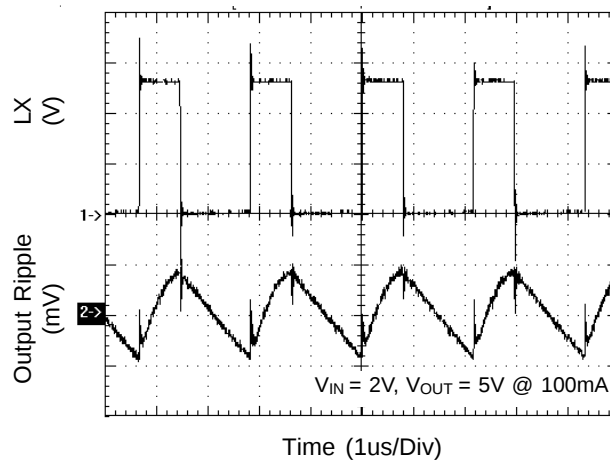




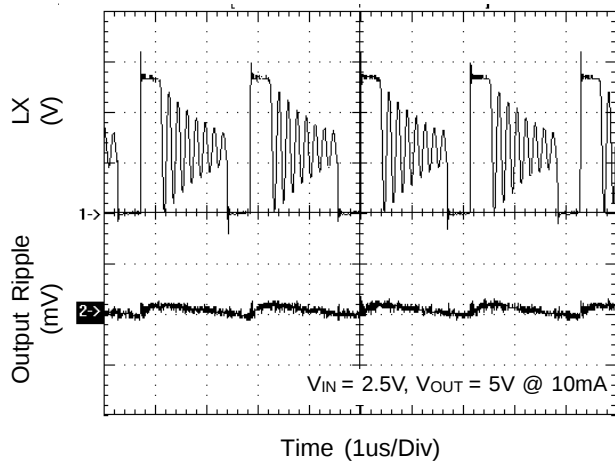
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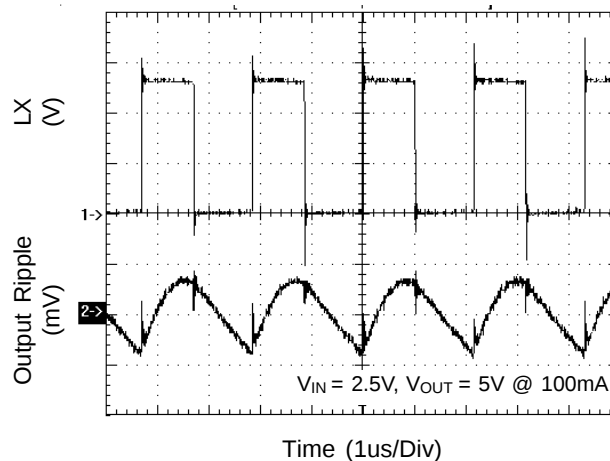
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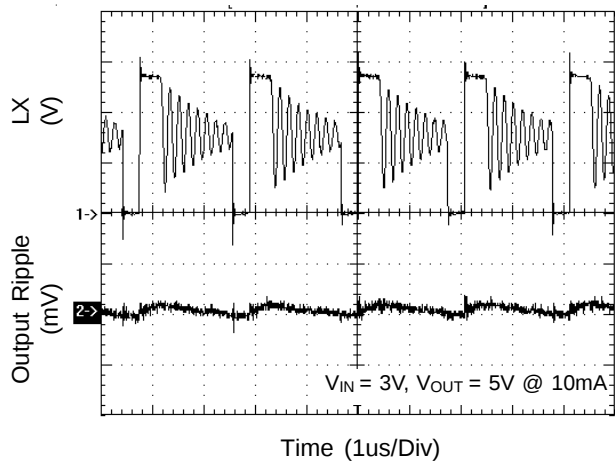
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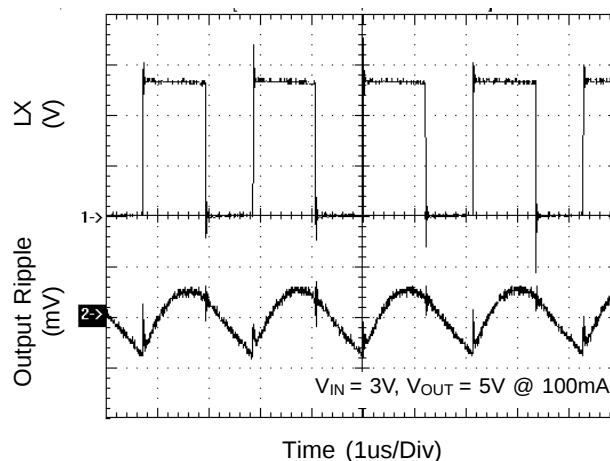
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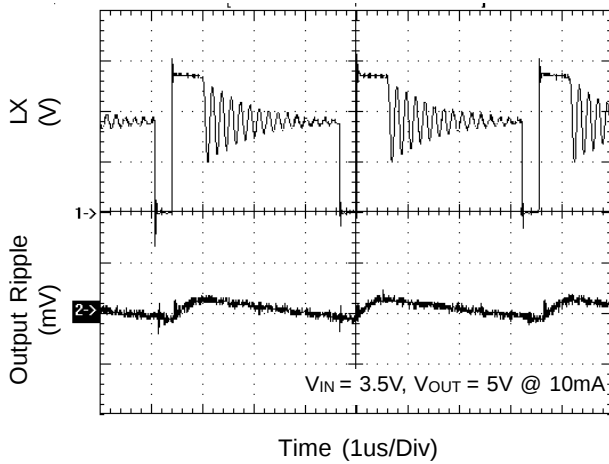
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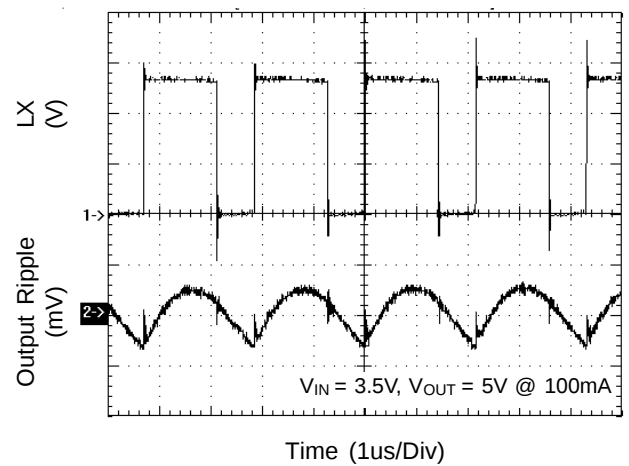
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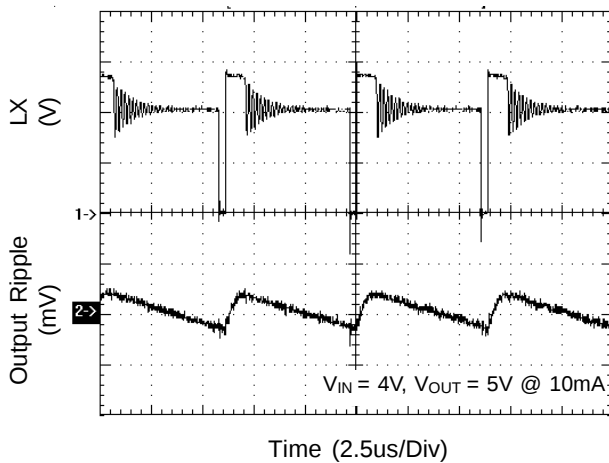
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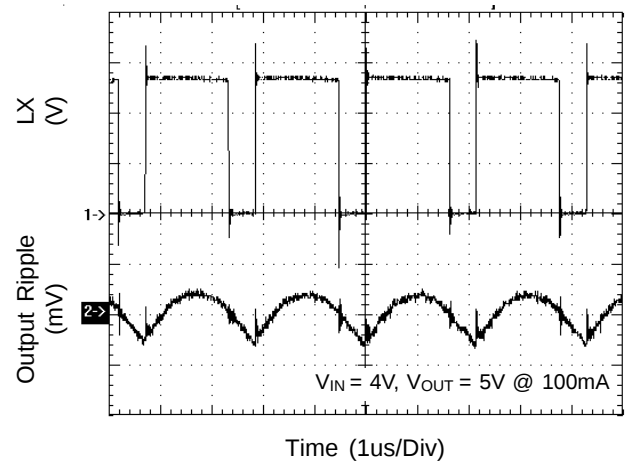
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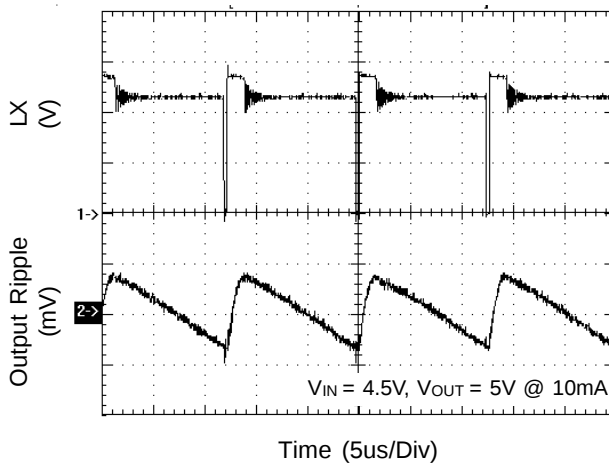
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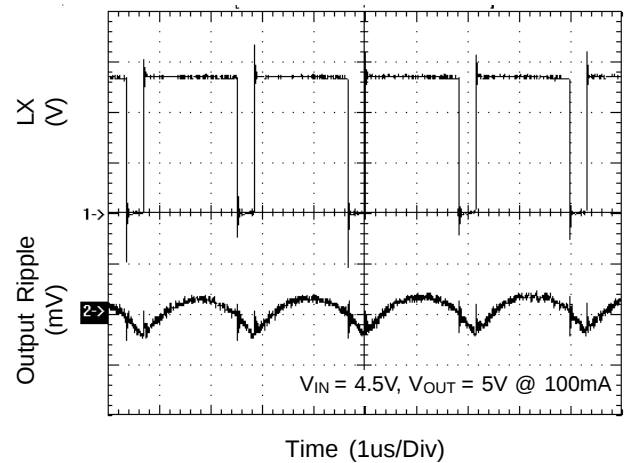
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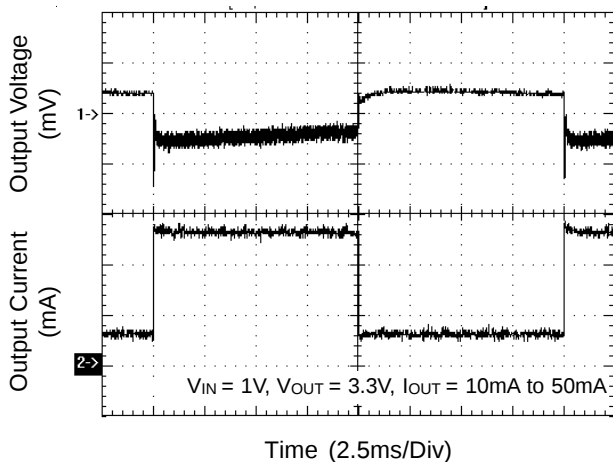
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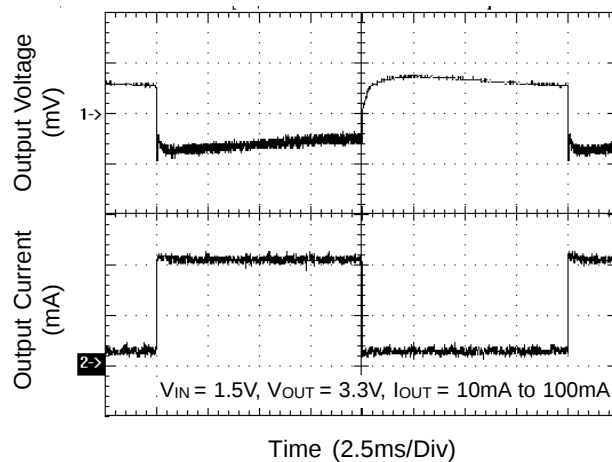
LX & Output Ripple



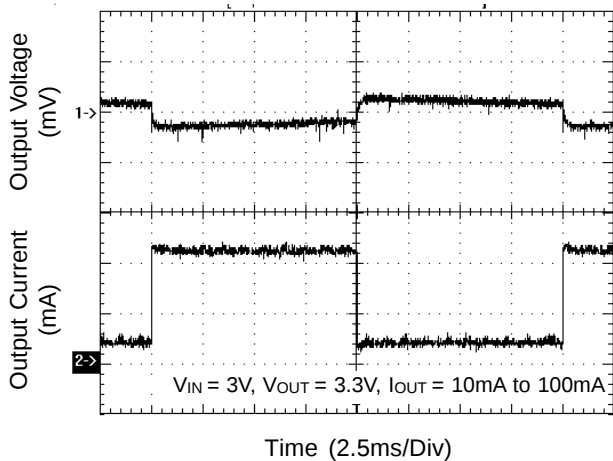
Load Transient Responses



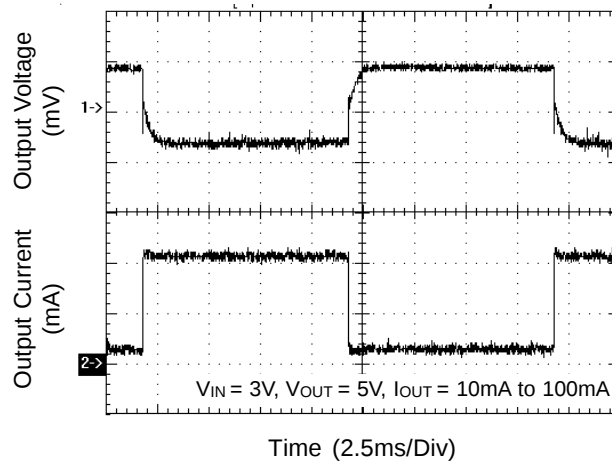
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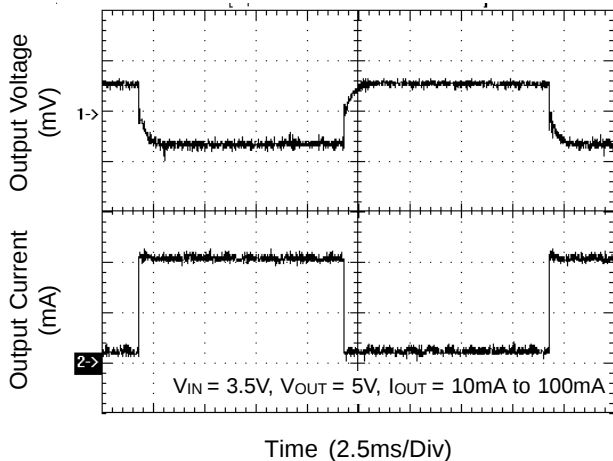
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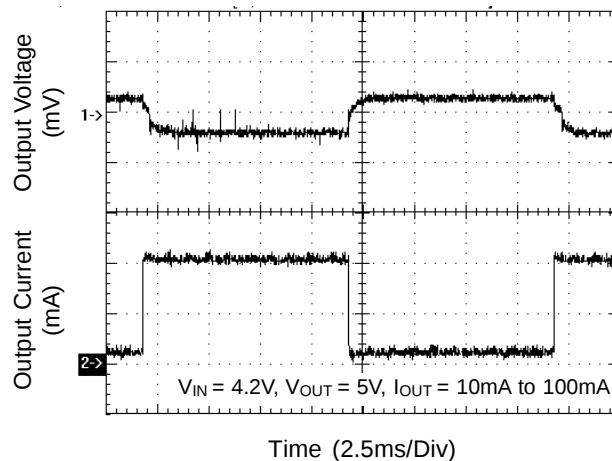
Load Transient Responses

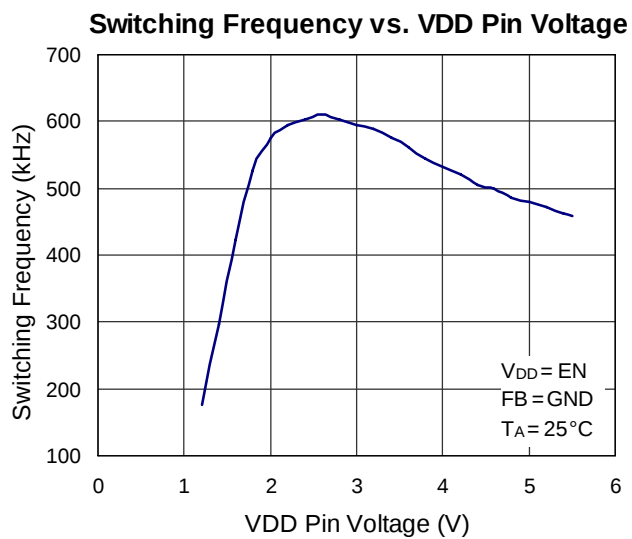


Load Transient Responses



Load Transient Responses





Application Information

Output Voltage Setting

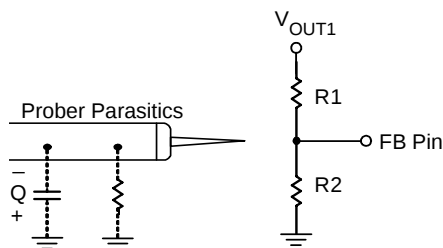
Referring to application circuits, the output voltage of the switching regulator (V_{OUT}) can be set with Equation (1).

$$V_{OUT1} = \left(1 + \frac{R1}{R2}\right) \times 1.25V \quad (1)$$

Feedback Loop Design

Referring to application circuits, The selection of R1 and R2 based on the trade-off between quiescent current consumption and interference immunity is stated below:

- Follow Equation (1).
- Higher R reduces the quiescent current (Path current = $1.25V/R2$), however resistors beyond $5M\Omega$ are not recommended.
- Lower R gives better noise immunity, and is less sensitive to interference, layout parasitics, FB node leakage, and improper probing to FB pins.



- A proper value of feed forward capacitor parallel with R1 can improve the noise immunity of the feedback loops, especially in an improper layout. An empirical suggestion is around 0~33pF for feedback resistors of $M\Omega$, and 10nF~0.1 μF for feedback resistors of tens to hundreds $k\Omega$.

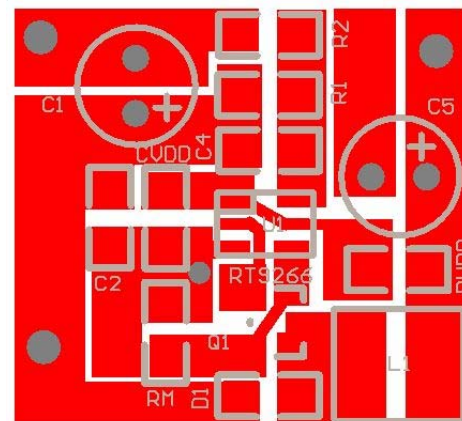
For applications without standby or suspend modes, lower values of R1 and R2 are preferred. For applications concerning the current consumption in standby or suspend modes, the higher values of R1 and R2 are needed. Such “high impedance feedback loops” are sensitive to any interference, which require careful layout and avoid any interference, e.g. probing to FB pin.

Layout Guide

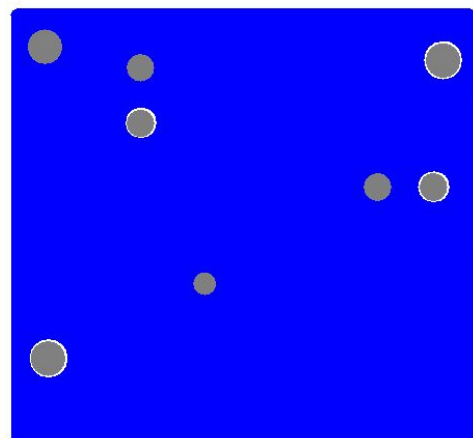
- A full GND plane without gap break.
- V_{DD} to GND noise bypass – Short and wide connection for the 1mF MLCC capacitor between Pin5 and Pin3.
- V_{IN} to GND noise bypass – Add a capacitor close to L1 inductor, when V_{IN} is not an idea voltage source.
- Minimized FB node copper area and keep far away from noise sources.
- Minimized parasitic capacitance connecting to LX and EXT nodes, which may cause additional switching loss.

Board Layout Example (2-Layer Board)

(Refer to Application Circuit Figure 2 for the board)

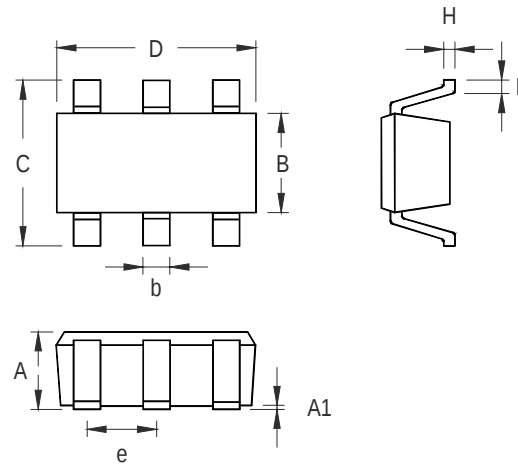


- Top Layer -



- Bottom Layer -

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

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