Boost Converter for WLED Power with Dual LDO

General Description

The RT9287A is an integrated solution for WLED and camera power. It contains a boost converter with internal schottky diode to provide WLED power and Dual LDO for the power of camera image sensor.

In the section of boost converter, RT9287A's optimized operation frequency can meet the requirement of small LC filters value and low operation current with high efficiency. Internal soft start function can reduce the inrush current. The initial current of WLED is set by the external resistor R_{SET}. The feedback voltage is 250mV.

In the section of DLDO, RT9287A is a dual channel, low noise, and low dropout regulator sourcing up to 300mA at each channel. The part offers 2% accuracy, low dropout voltage (240mV@300mA), and low ground current, only 27μA per LDO. The shutdown current is near zero current, which is suitable for battery-power devices. Other features include current limiting, over temperature, output short circuit protection. The part is short circuit thermal folded back protected. RT9287A lowers its OTP trip point from 165°C to 110°C when output short circuit occurs (V_{OUT} < 0.4V) providing maximum safety to end users.

RT9287A is available in a WDFN-12L 3x3 package.

Ordering Information

RT9287A-□□□□

- Package Type
  QW : WDFN-12L 3x3 (W-Type)
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)
- LDO Output Voltage : VOUT1/VOUT2
  MG : 2.8V/1.8V
  FQ : 1.5V/3.1V

Note :

RichTek Pb-free and Green products are :

- ▶RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶Suitable for use in SnPb or Pb-free soldering processes.
- ▶100% matte tin (Sn) plating.

Features

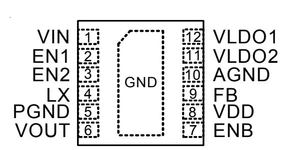
- **Boost Converter**
  - **▶V_{IN} Operating Range : 2.7V to 5.5V**
  - **▶Up to 85% Efficiency**
  - **▶22V Internal Power N-MOSFET**
  - **▶1MHz Switching Frequency**
  - **▶Built-in Diode**
  - **▶Digital Dimming with Zero-Inrush**
  - **▶Input UVLO Protection**
  - **▶Output Over Voltage Protection**
  - **▶Internal Soft Start and Compensation**
- **Dual LDO**
  - **▶Wide Operating Voltage Ranges : 2.7V to 5.5V**
  - **▶Low-Noise for RF Application**
  - **▶No Noise Bypass Capacitor Required**
  - **▶Fast Response in Line/Load Transient**
  - **▶TTL-Logic-Controlled Shutdown Input**
  - **▶Low Temperature Coefficient**
  - **▶Dual LDO Outputs (300mA/300mA)**
  - **▶Ultra-Low Quiescent Current 27μA/LDO**
  - **▶High Output Accuracy 2%**
  - **▶Short Circuit Protection**
  - **▶Thermal Shutdown Protection**
  - **▶Current Limit Protection**
  - **▶Short Circuit Thermal Folded Back Protection**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Cellular Phones
- WLED Driver
- PDAs and Smart Phones
- Probable Instruments

Pin Configurations

(TOP VIEW)

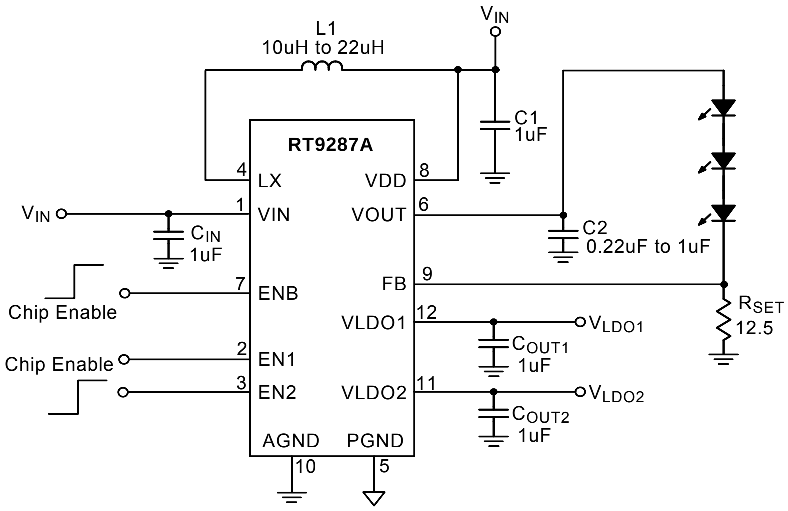


WDFN-12L 3x3

Marking Information

For marking information, contact our sales representative directly or through a RichTek distributor located in your area, otherwise visit our website for detail.

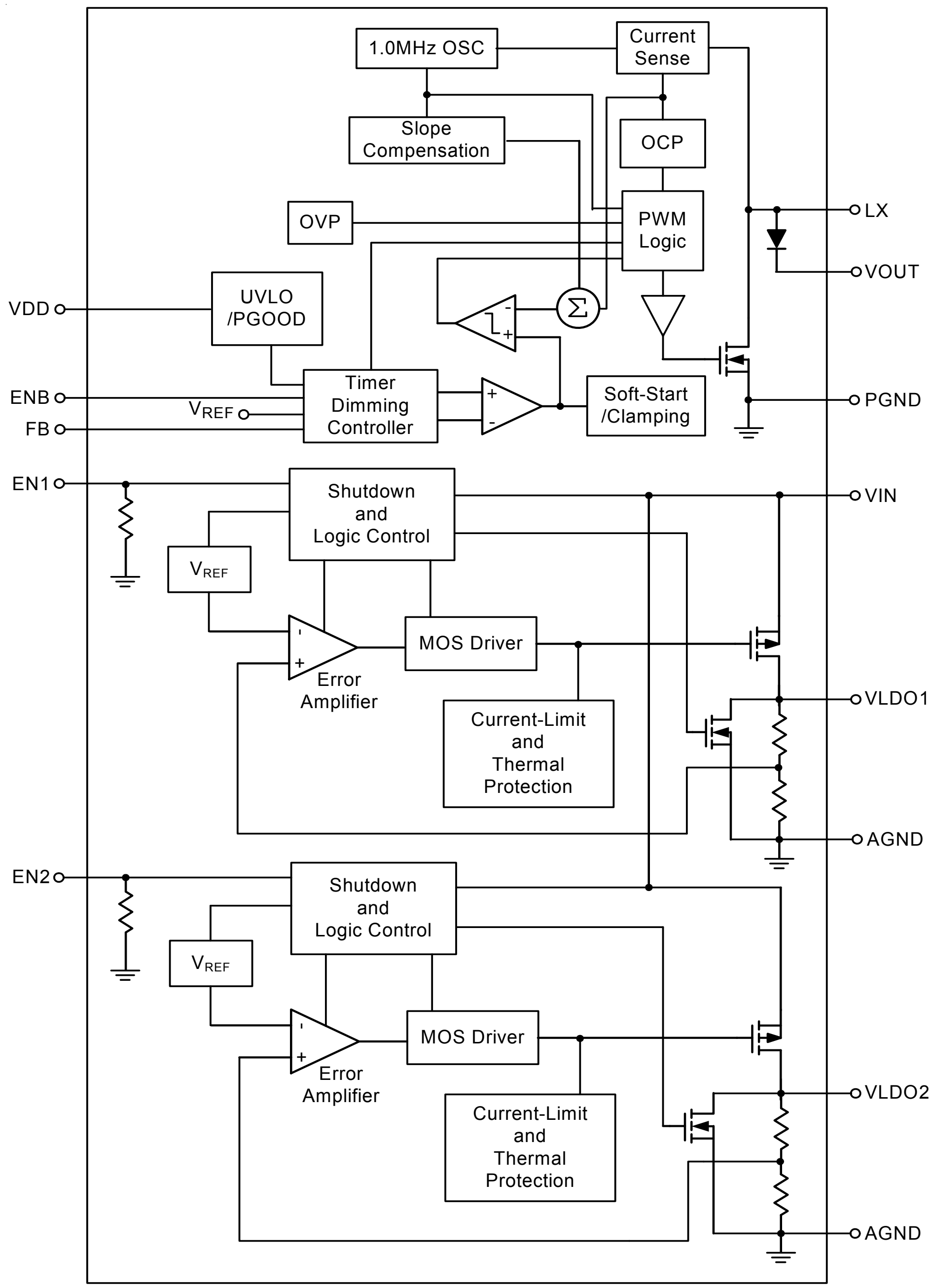
Typical Application Circuit



Functional Pin Description

Pin Number	Pin Name	Pin Function
1	VIN	LDO Power Input Voltage.
2	EN1	Enable pin for LDO channel 1.
3	EN2	Enable pin for LDO channel 2.
4	LX	Boost LX Pin. Connect this Pin to an inductor. Minimize the track area to reduce EMI.
5	PGND	Power Ground.
6	VOUT	Boost Output Voltage pin. The pin internally connects to OVP diode to limit output voltage while LEDs are disconnected.
7	ENB	Boost Chip Enable (Active High). Note that this pin has an internal pull-down resistance around 300kΩ.
8	VDD	Boost Supply Input Voltage Pin. Bypass 1μF capacitor to GND to reduce the input Ripple.
9	FB	Boost Feedback Pin. Series connecting a resistor between WLED and ground as a current sense. Sense the current feedback voltage to set the current rating.
10	AGND	Analog Ground.
11	VLDO2	LDO Channel 2 Output Voltage.
12	VLDO1	LDO Channel 1 Output Voltage.
Exposed Pad	GND	Exposed pad should be soldered to PCB board and connected to GND.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN}, V_{DD} ---------- –0.3V to 6V
- LX Input Voltage ---------- –0.3V to 22V
- Output Voltage, V_{OUT} ---------- –0.3V to 21V
- The Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-12L 3x3 ---------- 0.606W
- Package Thermal Resistance (Note 4)
  WDFN-12L 3x3, θ_{JA} ---------- 165°C/W
  WDFN-12L 3x3, θ_{JC} ---------- 8.2°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 3.7V, FREQ left floating, V_{IN} = V_{OUT} + 1V, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1μA, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Boost						
System Supply Input						
Operation voltage Range	V_{DD}		2.7	--	5.5	V
Under Voltage Lock Out	V_{UVLO}		1.7	2	2.3	V
Quiescent Current	I_Q	V_{FB} = 1.5V, No switch	--	300	450	μA
Supply Current	I_{IN}	V_{FB} = 0V, Switch	--	--	2	mA
Shutdown Current	I_{SHDN}	V_{ENB} < 0.4V	--	2	5	μA
Line Regulation		V_{DD2} = 3V to 4.3V	--	--	3	%
Oscillator						
Operation Frequency	f_{OSC}		--	1	--	MHz
Maximum Duty Cycle			85	90	--	%
Reference Voltage						
Feedback Reference Voltage	V_{REF}		0.237	0.25	0.263	V
Diode						
Forward Voltage	V_{FW}	I_{FW} = 100mA	--	0.9	--	V

To be continued

Parameter		Symbol	Test Condition	Min	Typ	Max	Units
MOSFET							
On Resistance of MOSFET		$R_{DS(ON)}$		0.5	0.9	--	Ω
Protection							
OVP Threshold		V_{OVP}		–	20	--	V
OCP				–	400	--	mA
Control Interface							
ENB Threshold	Logic-Low Voltage	V_{IL}		–	--	0.4	V
	Logic-High Voltage	V_{IH}		1.4	--	--	V
ENB Low Time for Dimming		T_{LO}	Refer to Figure 1	0.5	--	300	μs
Delay Between Steps Time		T_{HI}	Refer to Figure 1	0.5	--	--	μs
Shut Down Delay Time		T_{SHDN}	Refer to Figure 1	1	--	--	ms
Dual LDO							
Input Voltage		V_{IN}	V_{IN} = 2.7V to 5.5V	2.7	--	5.5	V
Dropout Voltage (Note 5)		V_{DROP}	I_{OUT} = 300mA	--	240	330	mV
Output Voltage Range		V_{OUT}		1.2	--	3.6	V
V_{OUT} Accuracy		ΔV	I_{OUT} = 1mA	–2	--	+2	%
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUT} + 0.3V) to 5.5V or V_{IN} > 2.7V, whichever is larger	--	--	0.2	%/V
Load Regulation		ΔV_{LOAD}	1mA < I_{OUT} < 300mA	--	--	0.6	%
Current Limit		I_{LIM}	R_{LOAD} = 1Ω	330	450	700	mA
Quiescent Current		I_Q	$V_{EN1,2}$ > 1.5V	--	58	80	μA
Shutdown Current		I_{SHDN}	$V_{EN1,2}$ < 0.4V	--	--	1	μA
EN1,2 Threshold		V_{IH}	V_{IN} = 2.7V to 5.5V, Power On	1.5	--	–	V
		V_{IL}	V_{IN} = 2.7V to 5.5V, Shutdown	--	--	0.4	V
Output Voltage TC				--	100	–	ppm/°C
Thermal Shutdown		T_{SD}		--	170	–	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	40	–	°C
PSRR I_{LOAD} = 10mA		PSRR	f = 100Hz	--	–65	–	dB
			f = 1kHz	--	–60	–	dB
			f = 10kHz	--	–50	–	dB
PSRR I_{LOAD} = 150mA			f = 100Hz	--	–65	–	dB
			f = 1kHz	--	–50	–	dB
			f = 10kHz	--	–50	–	dB

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

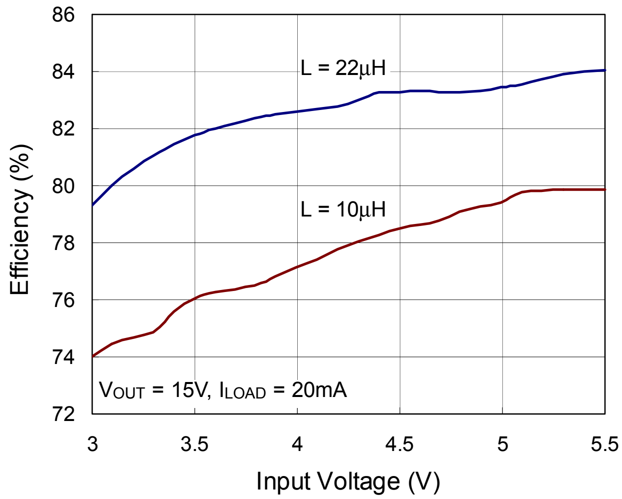
Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the QFN package.

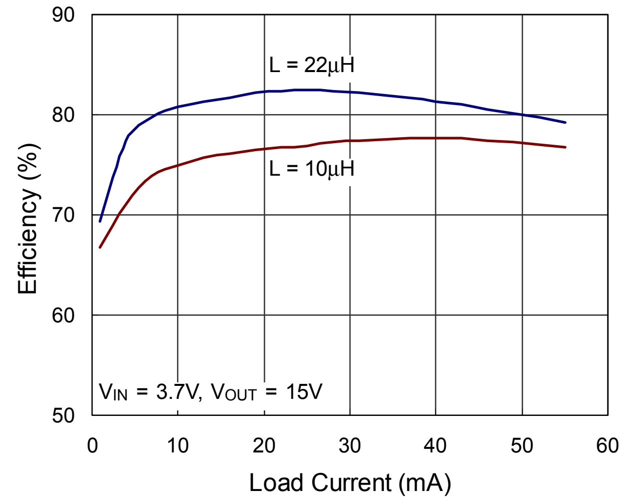
Note 5. The dropout voltage is defined as V_{IN} -V_{OUT}, which is measured when V_{OUT} is $V_{OUT(NORMAL)}$ − 100mV.

Typical Operating Characteristics

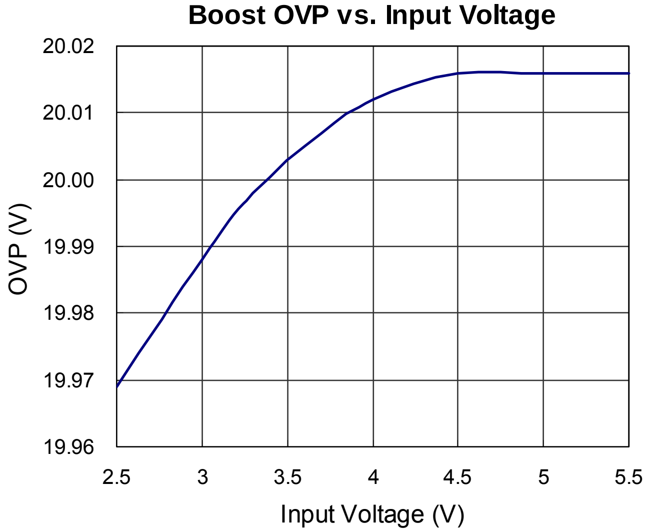
Boost Efficiency vs. Input Voltage



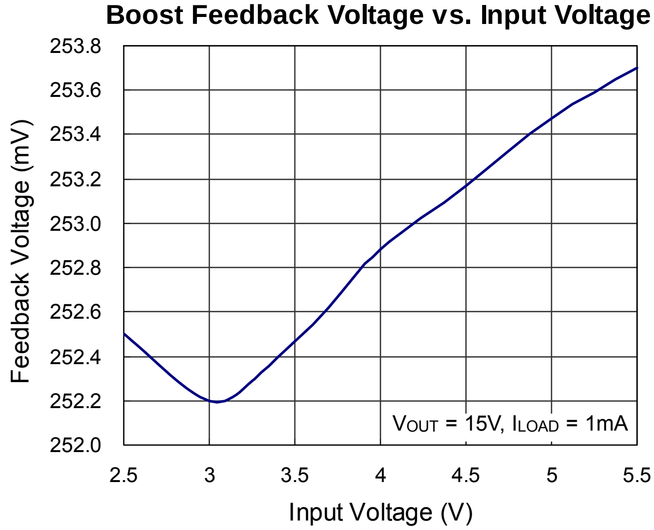
Boost Efficiency vs. Load Current



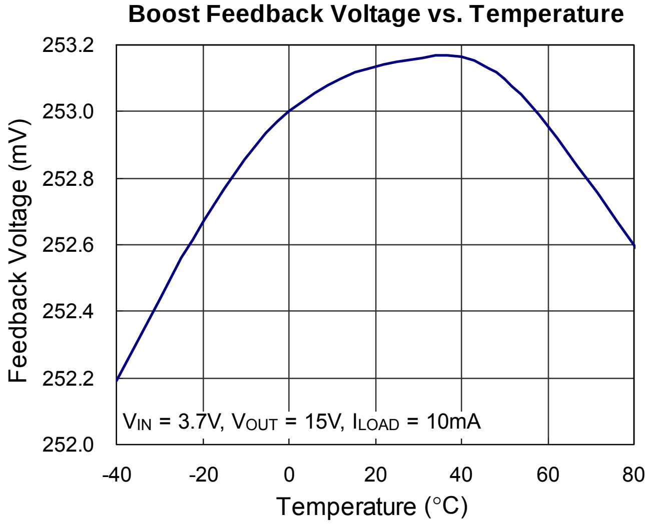
Boost OVP vs. Input Voltage



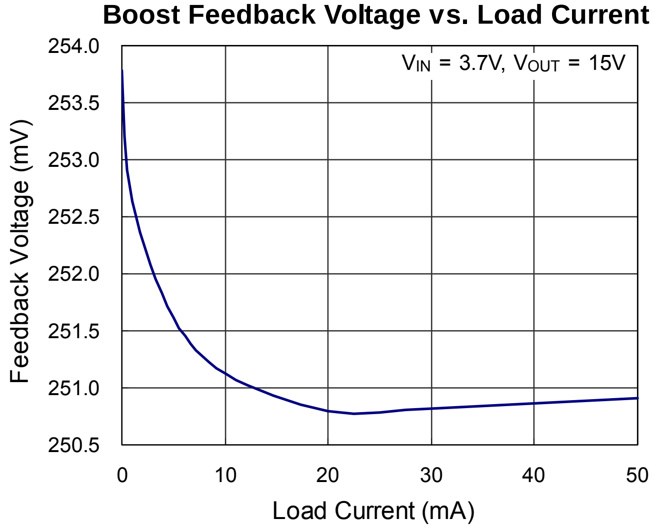
Boost Feedback Voltage vs. Input Voltage



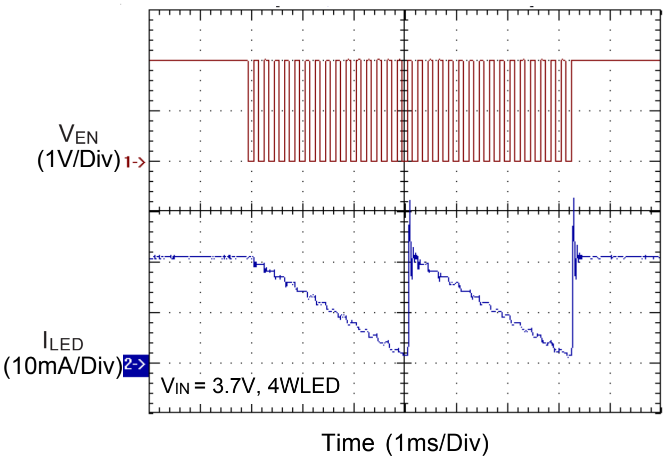
Boost Feedback Voltage vs. Temperature



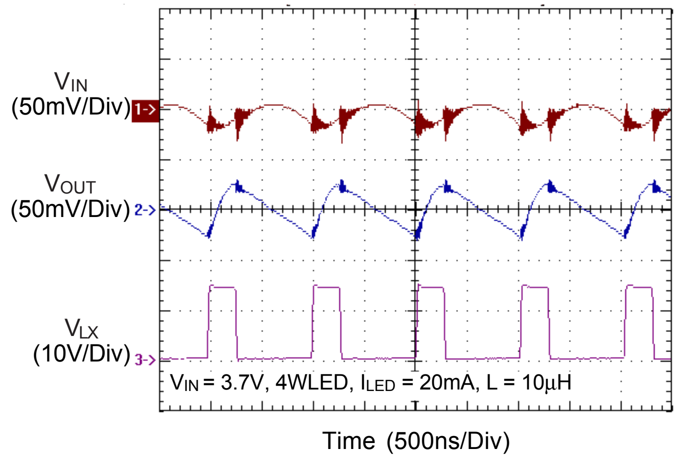
Boost Feedback Voltage vs. Load Current



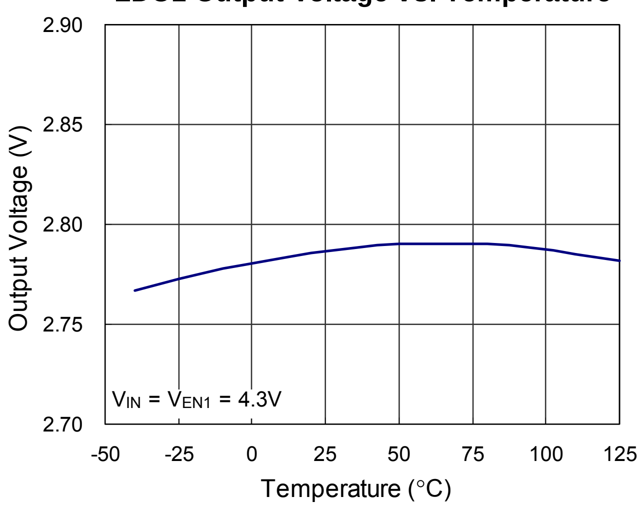
Boost Dimming Operation



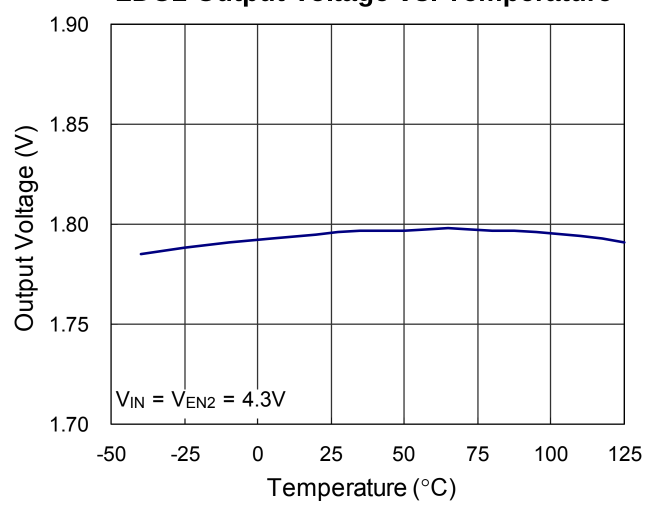
Boost Normal Operation



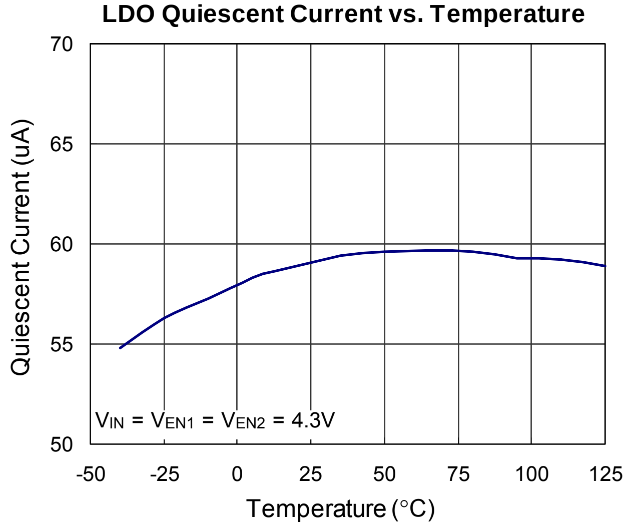
LDO1 Output Voltage vs. Temperature



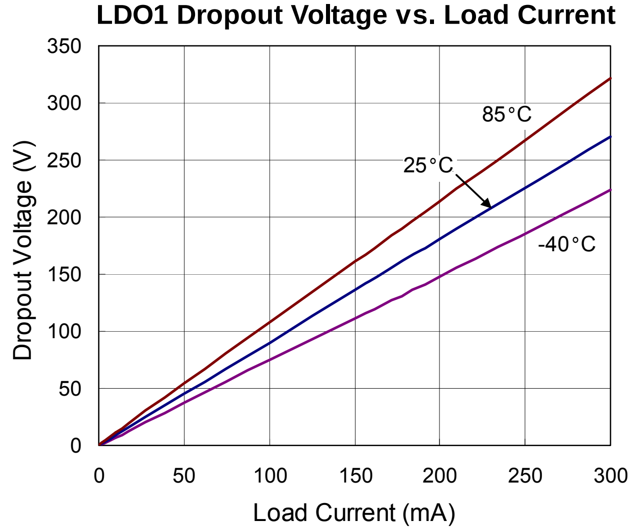
LDO2 Output Voltage vs. Temperature



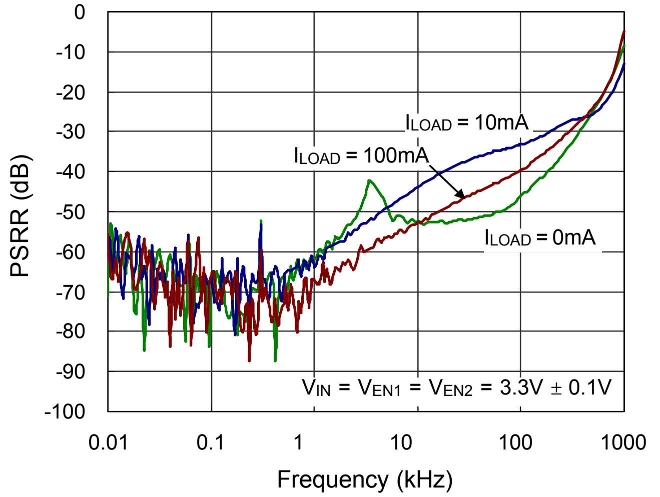
LDO Quiescent Current vs. Temperature



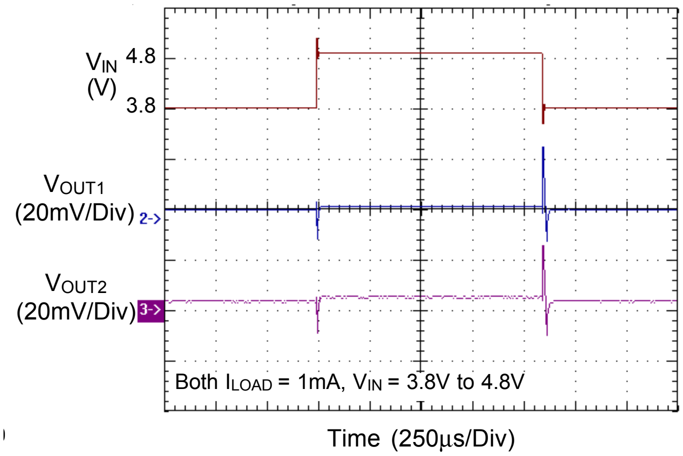
LDO1 Dropout Voltage vs. Load Current



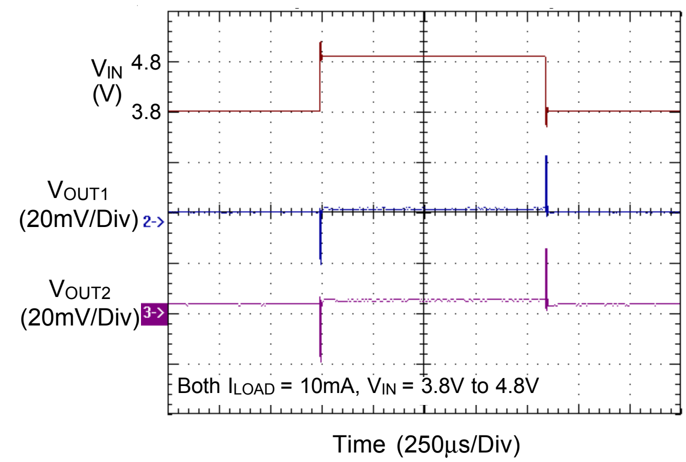
LDO PSRR



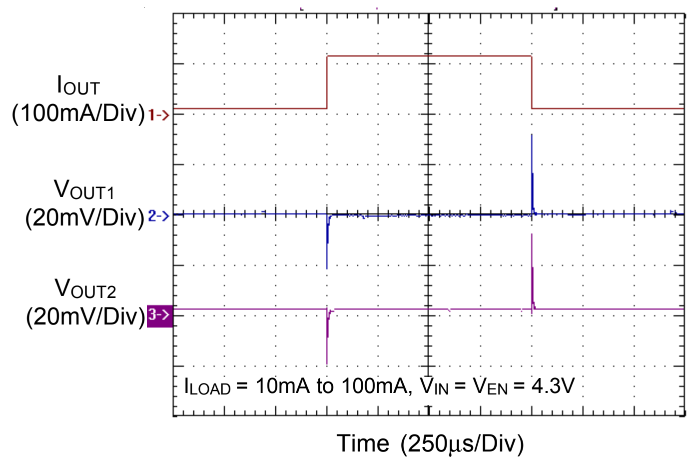
LDO Line Transient Response



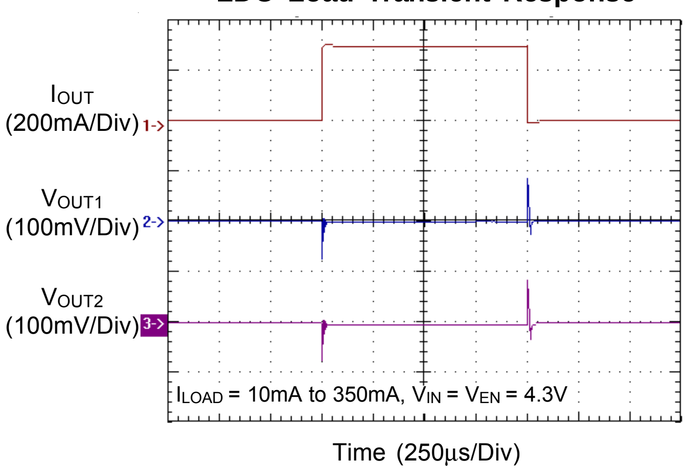
LDO Line Transient Response



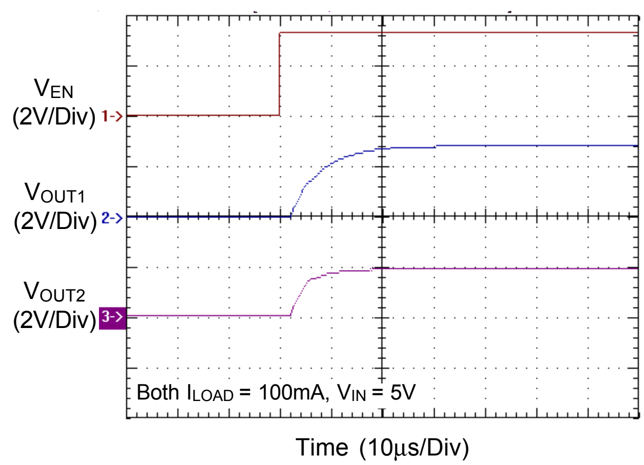
LDO Load Transient Response



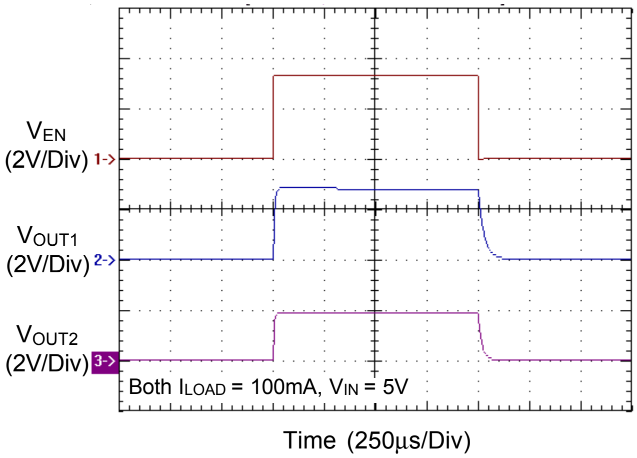
LDO Load Transient Response



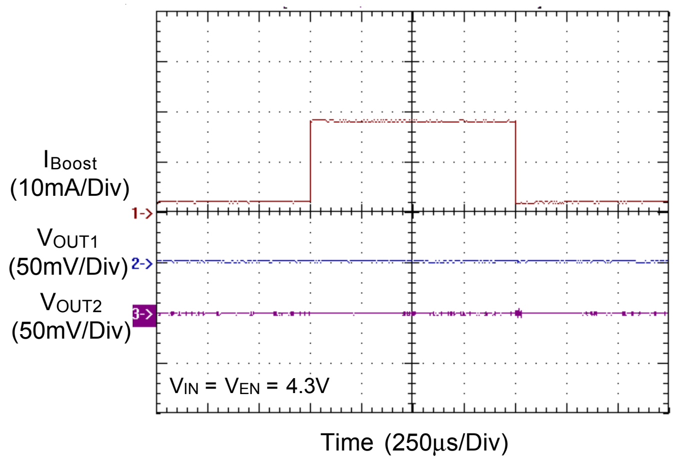
LDO Power On from EN



LDO Power Off from EN



Cross Talk



Application Information

Boost Converter

LED Current Control

As shown in Figure 1, the RT9287A regulates the LED current by setting the current sense resistor (R_{SET}) connected between FB pin and ground. The reference voltage of FB pin is 0.25V in typical. The LED current (I_{LED}) can be calculated by the following Equation.

$$I_{LED} = V_{REF} / R_{SET} \quad (1)$$

In order to have an accurate LED current, a precision resistor is preferred (1% is recommended).

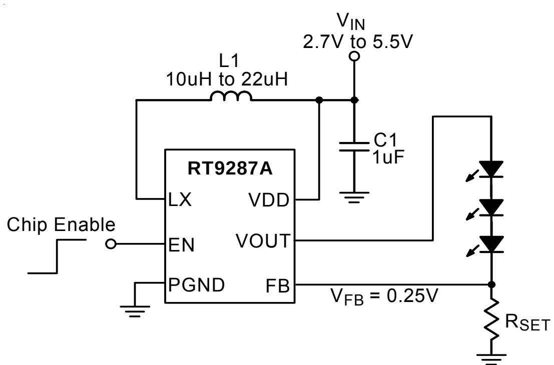


Figure 1. Application for Driving 3 series WLEDs

Inductor Selection

The recommended value of the inductor is from 10μH to 22μH for 4 to 5 WLEDs applications. For 3WLEDs, the recommended value of the inductor is from 4.7μH to 22μH. Small size and better efficiency are the major concerns for portable devices, just as RT9287A's application for mobile phone. The inductor should have low core loss at 1MHz and low DCR for better efficiency.

The inductor saturation current rating should be considered to cover the inductor peak current.

Output Voltage Control

For fixed output voltage application, the output voltage can be adjusted by the divider circuit on FB pin. Figure2 shows a 2-level voltage control circuit for OLED application. The output voltage can be calculated by the following equations. Table 1 is the recommended resistance for different conditions.

$$V_{OUT} = R_A \times \{(F_B/R_B) + (F_B\text{-GPIO})/R_{GPIO}\} + F_B \quad (3)$$

As GPIO = 0V,

$$V_{OUT} = R_A \times \{(0.25/R_B) + (0.25/R_{GPIO})\} + 0.25 \quad (4)$$

As GPIO = 2.8V,

$$V_{OUT} = R_A \times \{(0.25/R_B) + (0.25-2.8)/R_{GPIO}\} + 0.25 \quad (5)$$

As GPIO = 1.8V,

$$V_{OUT} = R_A \times \{(0.25/R_B) + (0.25-1.8)/R_{GPIO}\} + 0.25 \quad (6)$$

For Efficiency Consideration set R_A = 990kΩ.

Table 1. Suggested Resistance for Output Voltage Control

Conditions	R_A (kΩ)	R_B (kΩ)	R_{GPIO} (kΩ)
Case A : Normal Voltage = 16V (GPIO = 0V) Dimming Voltage = 12V (GPIO = 1.8V)	1100	18	495
Case B : Normal Voltage = 16V (GPIO = 0V) Dimming Voltage = 12V (GPIO = 2.8V)	1200	19.5	840

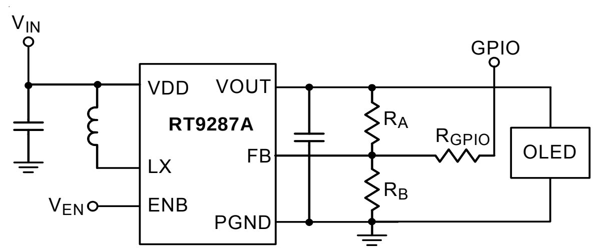


Figure 2. Application Circuit for 2-level Output Voltage Control

Dual LDO

Like any low-dropout regulator, the external capacitors used with the RT9287A must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1μF on the LDO input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any high quality ceramic or tantalum capacitor can be used for this part. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all applications. The LDO is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 20mΩ on the LDO output ensures stability. The LDO still works well with other kinds of output capacitor due to the wide stable ESR range. Figure 3 shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the LDO and returned to a clean analog ground.

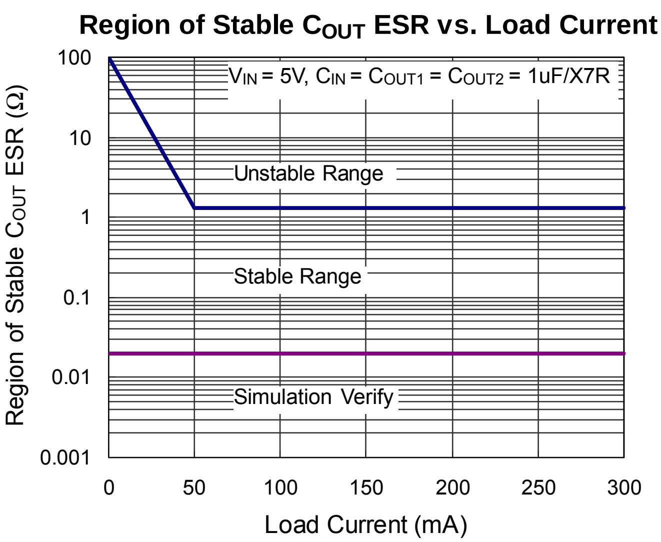


Figure 3. Stable Cout ESR Range

Thermal protection limits power dissipation in LDO. When the operating junction temperature exceeds a certain temperature, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turns on again after the junction temperature is cooled down. The RT9287A lowers its OTP trip level from 170°C to 110°C when output short circuit occurs (V_{OUT} < 0.4V) as shown in Figure 4. It reduces operating junction temperature and provides maximum safety to customer while output short circuit occurring.

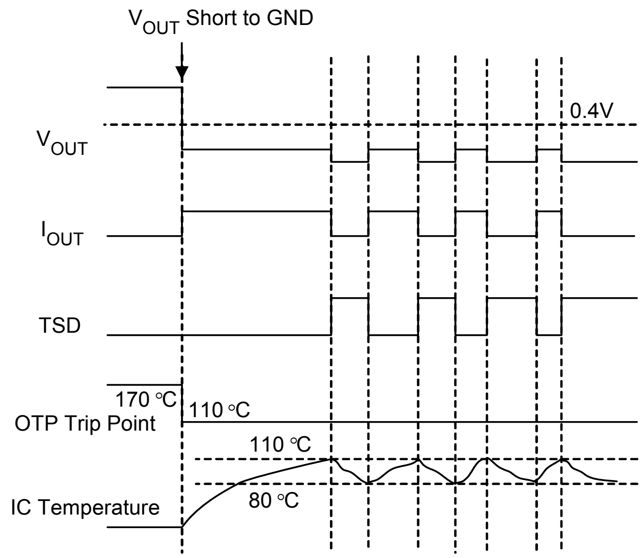


Figure 4. Short Circuit Thermal Folded Back Protection when Output Short Circuit Occurs (Patent)

Thermal Considerations

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junctions to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operating ction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of the T9287A, where $T_{J(MAX)}$ is the maximum junction temperature of the die and T_A is the maximum ambient temperature. The junction to ambient thermal resistance $_{JA}$ is layout dependent. For WDFN-12L 3x3 packages, the thermal resistance $_{JA}$ is 60 °C/W on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula:

$P_{D(MAX)}$ = (120°C − 25°C) / (60°C/W) = 1.667W for WDFN-12L 3x3 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance $_{JA}$. For RT9287A packages, the Figure 5 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

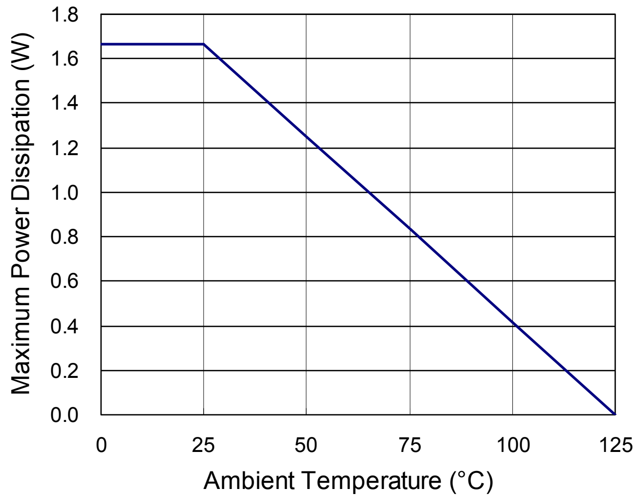


Figure 5. Derating Curves for RT9287A Packages

Layout Guide

- The exposed pad and GND should be connected to a strong ground plane for heat sinking and noise prevention.
- Traces should be kept as short as possible.
- LX node copper area should be minimized for reducing EMI.
- The Dual LDO input capacitor C1 must be located a distance of not more than 0.5 inch from the VDD1 pin and returned to ground plane.
- The Boost input capacitor C2 should be placed as closed as possible to Pin 7.
- The Dual LDO output capacitor C3 and C4 must be located a distance of not more than 0.5 inch from the VLDO1 and VLDO2 pin and returned to ground plane.
- FB node copper area should be minimized and keep far away from noise sources (L_X).
- Feedback resistance R2 should be placed as closed as possible to Pin 5.

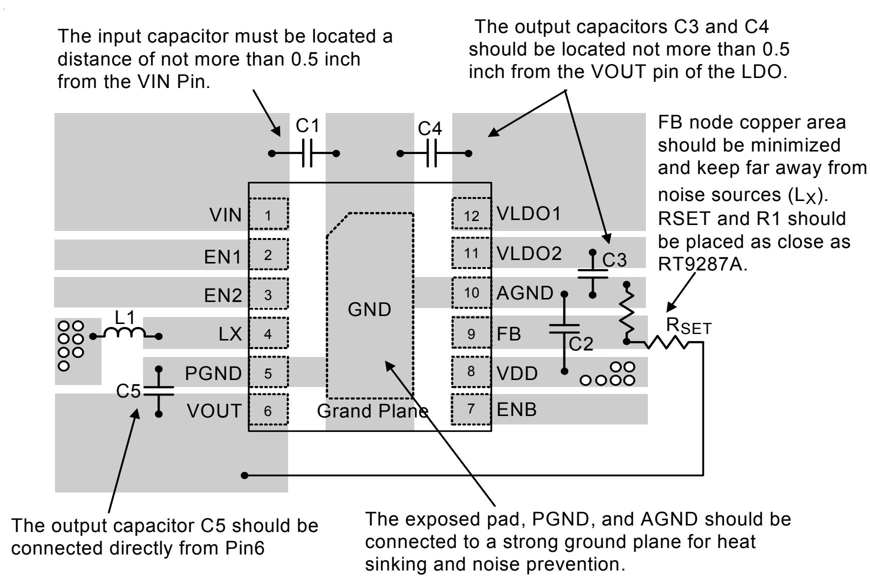
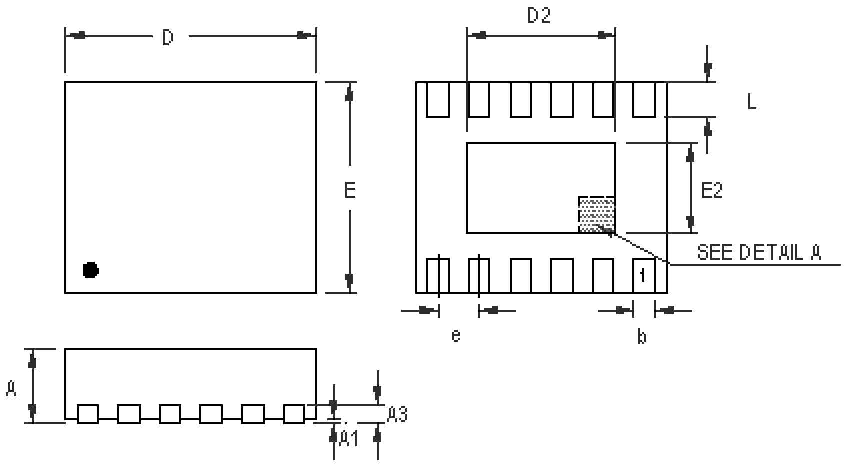
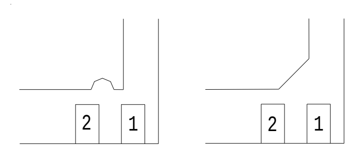


Figure 6

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.400	1.750	0.055	0.069
e	0.450		0.018	
L	0.350	0.450	0.014	0.018

W-Type 12L DFN 3x3 Package

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