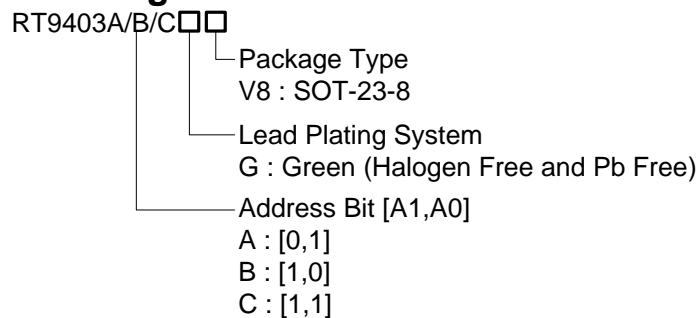


# I<sup>2</sup>C Programmable High Precision Reference Voltage Generator

## General Description

The RT9403A/B/C is a high precision reference voltage generating console consisting of three I<sup>2</sup>C programmable DACs. Each DAC output voltage is controlled by 7 digital bits that are programmed by the I<sup>2</sup>C interface. The RT9403A/B/C features adjustable output slew rate, low switching glitch and adequate driving capability. The RT9403A/B/C is available in SOT-23-8 package.

## Ordering Information



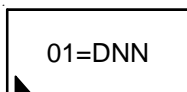
Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

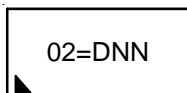
## Marking Information

RT9403AGV8



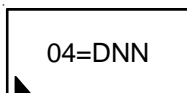
01= : Product Code  
DNN : Date Code

RT9403BGV8



02= : Product Code  
DNN : Date Code

RT9403CGV8



04= : Product Code  
DNN : Date Code

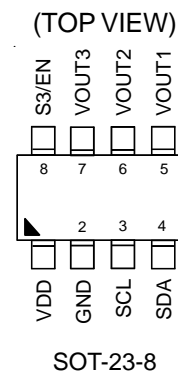
## Features

- 5V Supply Voltage
- Provide 3 Precise Voltage DACs
- I<sup>2</sup>C Programmable 128-Steps Output Voltage
- Output Range and Resolution
  - ▶ DAC1 & DAC2 : 0.6V to 2.1875V, 12.5mV/Step
  - ▶ DAC3 : 1.2V to 3.375V, 12.5mV (or 25mV)/Step for Different Segments
- High Output Accuracy Up to 1% ( $V_{OUT} \geq 1V$ )
- Low External Component Count
- Small Footprint SOT-23-8 Package
- RoHS Compliant and Halogen Free

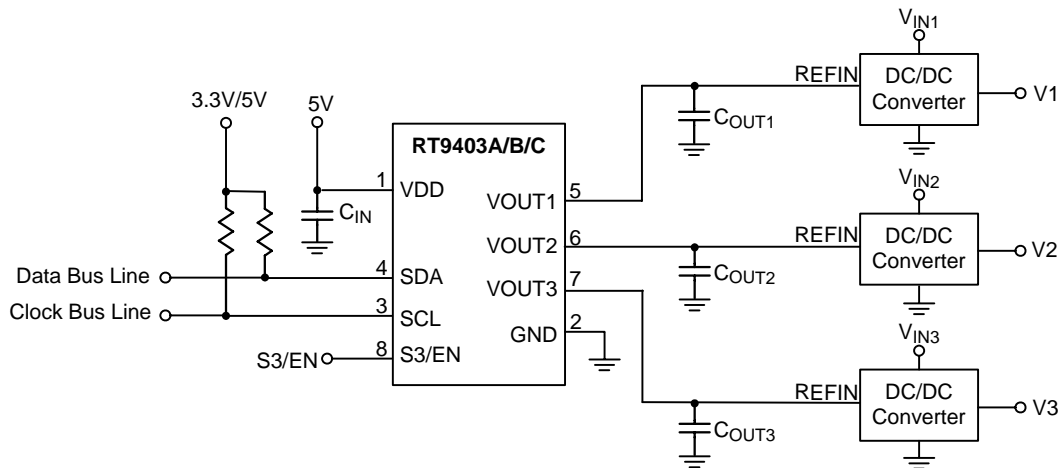
## Applications

- Power Supply Adjustment for Motherboard and Graphic Card
- Low Voltage, High Accuracy Reference Voltage Circuit

## Pin Configurations



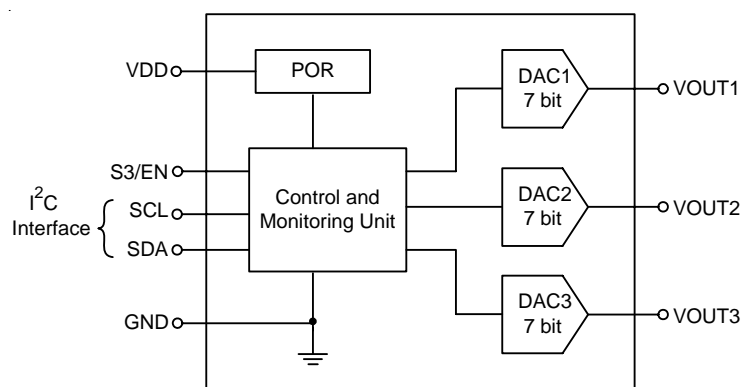
## Typical Application Circuit



## Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VDD	Power Supply Input. Default connected to 5V.
2	GND	Ground.
3	SCL	Serial Clock Input. This pin receives I <sup>2</sup> C serial bus clock signal.
4	SDA	Serial Data Input. This pin is input or output of I <sup>2</sup> C serial bus data signal.
5	VOUT1	I <sup>2</sup> C Programmed VTT Output Voltage. Default = 1.1V
6	VOUT2	I <sup>2</sup> C Programmed PCH_CORE Output Voltage. Default = 1.05V
7	VOUT3	I <sup>2</sup> C Programmed DDR Output Voltage. Default = 1.5V
8	S3/EN	ACPI S3 State/Enable. Active low for entering ACPI S3 State(suspend to RAM), VOUT1/VOUT2 are internally pulled down to zero, only VOUT3 is active.

## Function Block Diagram



**Table 1. DAC1/DAC2 Serial Code Table**

SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0	Output Voltage ( V )
0	0	0	0	0	0	0	2.1875
0	0	0	0	0	0	1	2.1750
0	0	0	0	0	1	0	2.1625
0	0	0	0	0	1	1	2.1500
0	0	0	0	1	0	0	2.1375
0	0	0	0	1	0	1	2.1250
0	0	0	0	1	1	0	2.1125
0	0	0	0	1	1	1	2.1000
0	0	0	1	0	0	0	2.0875
0	0	0	1	0	0	1	2.0750
0	0	0	1	0	1	0	2.0625
0	0	0	1	0	1	1	2.0500
0	0	0	1	1	0	0	2.0375
0	0	0	1	1	0	1	2.0250
0	0	0	1	1	1	0	2.0125
0	0	0	1	1	1	1	2.0000
0	0	1	0	0	0	0	1.9875
0	0	1	0	0	0	1	1.9750
0	0	1	0	0	1	0	1.9625
0	0	1	0	0	1	1	1.9500
0	0	1	0	1	0	0	1.9375
0	0	1	0	1	0	1	1.9250
0	0	1	0	1	1	0	1.9125
0	0	1	0	1	1	1	1.9000
0	0	1	1	0	0	0	1.8875
0	0	1	1	0	0	1	1.8750
0	0	1	1	0	1	0	1.8625
0	0	1	1	0	1	1	1.8500
0	0	1	1	1	0	0	1.8375
0	0	1	1	1	0	1	1.8250
0	0	1	1	1	1	0	1.8125
0	0	1	1	1	1	1	1.8000
0	1	0	0	0	0	0	1.7875
0	1	0	0	0	0	1	1.7750
0	1	0	0	0	1	0	1.7625
0	1	0	0	0	1	1	1.7500
0	1	0	0	1	0	0	1.7375
0	1	0	0	1	0	1	1.7250
0	1	0	0	1	1	0	1.7125
0	1	0	0	1	1	1	1.7000

*To be continued*

Table 1. DAC1/DAC2 Serial Code Table

SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0	Output Voltage ( V )
0	1	0	1	0	0	0	1.6875
0	1	0	1	0	0	1	1.6750
0	1	0	1	0	1	0	1.6625
0	1	0	1	0	1	1	1.6500
0	1	0	1	1	0	0	1.6375
0	1	0	1	1	0	1	1.6250
0	1	0	1	1	1	0	1.6125
0	1	0	1	1	1	1	1.6000
0	1	1	0	0	0	0	1.5875
0	1	1	0	0	0	1	1.5750
0	1	1	0	0	1	0	1.5625
0	1	1	0	0	1	1	1.5500
0	1	1	0	1	0	0	1.5375
0	1	1	0	1	0	1	1.5250
0	1	1	0	1	1	0	1.5125
0	1	1	0	1	1	1	1.5000
0	1	1	1	0	0	0	1.4875
0	1	1	1	0	0	1	1.4750
0	1	1	1	0	1	0	1.4625
0	1	1	1	0	1	1	1.4500
0	1	1	1	1	0	0	1.4375
0	1	1	1	1	0	1	1.4250
0	1	1	1	1	1	0	1.4125
0	1	1	1	1	1	1	1.4000
1	0	0	0	0	0	0	1.3875
1	0	0	0	0	0	1	1.3750
1	0	0	0	0	1	0	1.3625
1	0	0	0	0	1	1	1.3500
1	0	0	0	1	0	0	1.3375
1	0	0	0	1	0	1	1.3250
1	0	0	0	1	1	0	1.3125
1	0	0	0	1	1	1	1.3000
1	0	0	1	0	0	0	1.2875
1	0	0	1	0	0	1	1.2750
1	0	0	1	0	1	0	1.2625
1	0	0	1	0	1	1	1.2500
1	0	0	1	1	0	0	1.2375
1	0	0	1	1	0	1	1.2250
1	0	0	1	1	1	0	1.2125
1	0	0	1	1	1	1	1.2000

To be continued

**Table 1. DAC1/DAC2 Serial Code Table**

SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0	Output Voltage ( V )
1	0	1	0	0	0	0	1.1875
1	0	1	0	0	0	1	1.1750
1	0	1	0	0	1	0	1.1625
1	0	1	0	0	1	1	1.1500
1	0	1	0	1	0	0	1.1375
1	0	1	0	1	0	1	1.1250
1	0	1	0	1	1	0	1.1125
1	0	1	0	1	1	1	1.1000
1	0	1	1	0	0	0	1.0875
1	0	1	1	0	0	1	1.0750
1	0	1	1	0	1	0	1.0625
1	0	1	1	0	1	1	1.0500
1	0	1	1	1	0	0	1.0375
1	0	1	1	1	0	1	1.0250
1	0	1	1	1	1	0	1.0125
1	0	1	1	1	1	1	1.0000
1	1	0	0	0	0	0	0.9875
1	1	0	0	0	0	1	0.9750
1	1	0	0	0	1	0	0.9625
1	1	0	0	0	1	1	0.9500
1	1	0	0	1	0	0	0.9375
1	1	0	0	1	0	1	0.9250
1	1	0	0	1	1	0	0.9125
1	1	0	0	1	1	1	0.9000
1	1	0	1	0	0	0	0.8875
1	1	0	1	0	0	1	0.8750
1	1	0	1	0	1	0	0.8625
1	1	0	1	0	1	1	0.8500
1	1	0	1	1	0	0	0.8375
1	1	0	1	1	0	1	0.8250
1	1	0	1	1	1	0	0.8125
1	1	0	1	1	1	1	0.8000
1	1	1	0	0	0	0	0.7875
1	1	1	0	0	0	1	0.7750
1	1	1	0	0	1	0	0.7625
1	1	1	0	0	1	1	0.7500
1	1	1	0	1	0	0	0.7375
1	1	1	0	1	0	1	0.7250
1	1	1	0	1	1	0	0.7125
1	1	1	0	1	1	1	0.7000

*To be continued*

Table 1. DAC1/DAC2 Serial Code Table

SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0	Output Voltage ( V )
1	1	1	1	0	0	0	0.6875
1	1	1	1	0	0	1	0.6750
1	1	1	1	0	1	0	0.6625
1	1	1	1	0	1	1	0.6500
1	1	1	1	1	0	0	0.6375
1	1	1	1	1	0	1	0.6250
1	1	1	1	1	1	0	0.6125
1	1	1	1	1	1	1	0.6000

Note: (1) 0 : Pull Low to GND

(2) 1 : Open

**Table 2. DAC3 Serial Code Table**

SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0	Output Voltage ( V )
0	0	0	0	0	0	0	3.3750
0	0	0	0	0	0	1	3.3500
0	0	0	0	0	1	0	3.3250
0	0	0	0	0	1	1	3.3000
0	0	0	0	1	0	0	3.2750
0	0	0	0	1	0	1	3.2500
0	0	0	0	1	1	0	3.2250
0	0	0	0	1	1	1	3.2000
0	0	0	1	0	0	0	3.1750
0	0	0	1	0	0	1	3.1500
0	0	0	1	0	1	0	3.1250
0	0	0	1	0	1	1	3.1000
0	0	0	1	1	0	0	3.0750
0	0	0	1	1	0	1	3.0500
0	0	0	1	1	1	0	3.0250
0	0	0	1	1	1	1	3.0000
0	0	1	0	0	0	0	2.9750
0	0	1	0	0	0	1	2.9500
0	0	1	0	0	1	0	2.9250
0	0	1	0	0	1	1	2.9000
0	0	1	0	1	0	0	2.8750
0	0	1	0	1	0	1	2.8500
0	0	1	0	1	1	0	2.8250
0	0	1	0	1	1	1	2.8000
0	0	1	1	0	0	0	2.7750
0	0	1	1	0	0	1	2.7500
0	0	1	1	0	1	0	2.7250
0	0	1	1	0	1	1	2.7000
0	0	1	1	1	0	0	2.6750
0	0	1	1	1	0	1	2.6500
0	0	1	1	1	1	0	2.6250
0	0	1	1	1	1	1	2.6000
0	1	0	0	0	0	0	2.5750
0	1	0	0	0	0	1	2.5500
0	1	0	0	0	1	0	2.5250
0	1	0	0	0	1	1	2.5000
0	1	0	0	1	0	0	2.4750
0	1	0	0	1	0	1	2.4500
0	1	0	0	1	1	0	2.4250
0	1	0	0	1	1	1	2.4000

*To be continued*

Table 2. DAC3 Serial Code Table

SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0	Output Voltage ( V )
0	1	0	1	0	0	0	2.3750
0	1	0	1	0	0	1	2.3625
0	1	0	1	0	1	0	2.3500
0	1	0	1	0	1	1	2.3375
0	1	0	1	1	0	0	2.3250
0	1	0	1	1	0	1	2.3125
0	1	0	1	1	1	0	2.3000
0	1	0	1	1	1	1	2.2875
0	1	1	0	0	0	0	2.2750
0	1	1	0	0	0	1	2.2625
0	1	1	0	0	1	0	2.2500
0	1	1	0	0	1	1	2.2375
0	1	1	0	1	0	0	2.2250
0	1	1	0	1	0	1	2.2125
0	1	1	0	1	1	0	2.2000
0	1	1	0	1	1	1	2.1875
0	1	1	1	0	0	0	2.1750
0	1	1	1	0	0	1	2.1625
0	1	1	1	0	1	0	2.1500
0	1	1	1	0	1	1	2.1375
0	1	1	1	1	0	0	2.1250
0	1	1	1	1	0	1	2.1125
0	1	1	1	1	1	0	2.1000
0	1	1	1	1	1	1	2.0875
1	0	0	0	0	0	0	2.0750
1	0	0	0	0	0	1	2.0625
1	0	0	0	0	1	0	2.0500
1	0	0	0	0	1	1	2.0375
1	0	0	0	1	0	0	2.0250
1	0	0	0	1	0	1	2.0125
1	0	0	0	1	1	0	2.0000
1	0	0	0	1	1	1	1.9875
1	0	0	1	0	0	0	1.9750
1	0	0	1	0	0	1	1.9625
1	0	0	1	0	1	0	1.9500
1	0	0	1	0	1	1	1.9375
1	0	0	1	1	0	0	1.9250
1	0	0	1	1	0	1	1.9125
1	0	0	1	1	1	0	1.9000
1	0	0	1	1	1	1	1.8875

To be continued



**Table 2. DAC3 Serial Code Table**

SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0	Output Voltage ( V )
1	0	1	0	0	0	0	1.8750
1	0	1	0	0	0	1	1.8625
1	0	1	0	0	1	0	1.8500
1	0	1	0	0	1	1	1.8375
1	0	1	0	1	0	0	1.8250
1	0	1	0	1	0	1	1.8125
1	0	1	0	1	1	0	1.8000
1	0	1	0	1	1	1	1.7875
1	0	1	1	0	0	0	1.7750
1	0	1	1	0	0	1	1.7625
1	0	1	1	0	1	0	1.7500
1	0	1	1	0	1	1	1.7375
1	0	1	1	1	0	0	1.7250
1	0	1	1	1	0	1	1.7125
1	0	1	1	1	1	0	1.7000
1	0	1	1	1	1	1	1.6875
1	1	0	0	0	0	0	1.6750
1	1	0	0	0	0	1	1.6625
1	1	0	0	0	1	0	1.6500
1	1	0	0	0	1	1	1.6375
1	1	0	0	1	0	0	1.6250
1	1	0	0	1	0	1	1.6125
1	1	0	0	1	1	0	1.6000
1	1	0	0	1	1	1	1.5875
1	1	0	1	0	0	0	1.5750
1	1	0	1	0	0	1	1.5625
1	1	0	1	0	1	0	1.5500
1	1	0	1	0	1	1	1.5375
1	1	0	1	1	0	0	1.5250
1	1	0	1	1	0	1	1.5125
1	1	0	1	1	1	0	1.5000
1	1	0	1	1	1	1	1.4875
1	1	1	0	0	0	0	1.4750
1	1	1	0	0	0	1	1.4625
1	1	1	0	0	1	0	1.4500
1	1	1	0	0	1	1	1.4375
1	1	1	0	1	0	0	1.4250
1	1	1	0	1	0	1	1.4125
1	1	1	0	1	1	0	1.4000
1	1	1	0	1	1	1	1.3875

*To be continued*

Table 2. DAC3 Serial Code Table

SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0	Output Voltage ( V )
1	1	1	1	0	0	0	1.3750
1	1	1	1	0	0	1	1.3500
1	1	1	1	0	1	0	1.3250
1	1	1	1	0	1	1	1.3000
1	1	1	1	1	0	0	1.2750
1	1	1	1	1	0	1	1.2500
1	1	1	1	1	1	0	1.2250
1	1	1	1	1	1	1	1.2000

Note :

(1)  $V_{OUT} = 1.2V$  to  $1.375V$  and  $V_{OUT} = 2.375V$  to  $3.375V$ , Step =  $25mV$ .

(2)  $V_{OUT} = 1.375V$  to  $2.375V$ , Step =  $12.5mV$ .

**Absolute Maximum Ratings** (Note 1)

- Supply Voltage,  $V_{DD}$  ----- 6.5V
- Input Voltage, SCL, SDA, S3/EN ----- 6.5V
- Output Voltage,  $V_{OUT1}$ ,  $V_{OUT2}$ ,  $V_{OUT3}$  ----- 4V
- Power Dissipation,  $P_D$  @  $T_A = 25^\circ\text{C}$
- SOT-23-8 ----- 0.4W
- Package Thermal Resistance (Note 4)
- SOT-23-8,  $\theta_{JA}$  ----- 250°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 2)
- HBM (Human Body Mode) ----- 2kV
- MM (Machine Mode) ----- 200V

**Recommended Operating Conditions** (Note 3)

- Supply Voltage,  $V_{DD}$  ----- 5V  $\pm$  5%
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

**Electrical Characteristics**

( $V_{DD} = 5V$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specification)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input Voltage	$V_{DD}$		4.75	5	5.25	V
POR Threshold	$V_{POR\_TH}$		4	4.25	4.4	V
POR Hysteresis	$V_{POR\_HYS}$		--	250	--	mV
Supply Input Current	$I_{VDD}$		--	0.65	--	mA
<b><math>V_{REF}</math> &amp; DAC</b>						
DAC Output Accuracy		$V_{OUT} \geq 1V$ , $I_{OUT} = 0A$	-1	--	1	%
Under Voltage Lockout Hysteresis		$V_{OUT} < 1V$ , $I_{OUT} = 0A$	-10	--	10	mV
<b>Output Buffer</b>						
DC Gain		Capacitive Load Only	--	70	--	dB
Bandwidth	GBW	$C_L = 1nF$	--	1.64	--	MHz
Slew Rate	SR	$C_L = 0.1\mu F$	--	11	--	mV/ $\mu s$
Impedance	$R_{OUT}$		--	90	--	$\Omega$
Output Driving Capability	$I_{OUT}$		--	1.1	--	mA
Loading Effect Regulation			-0.002	--	0.002	%/ $\mu A$
<b><math>I^2C</math> Signal</b>						
Input High Threshold	$V_{IH}$		2.4	--	--	V
Input Low Threshold	$V_{IL}$		--	--	0.8	V
SCL Clock Speed			--	--	400	k/bit/s
EN Threshold Voltage	Logic-High	$V_{EN\_H}$	$V_{DD} - 0.3$	--	--	V
	Logic-Low	$V_{EN\_L}$	--	--	0.3	

**Note 1.** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

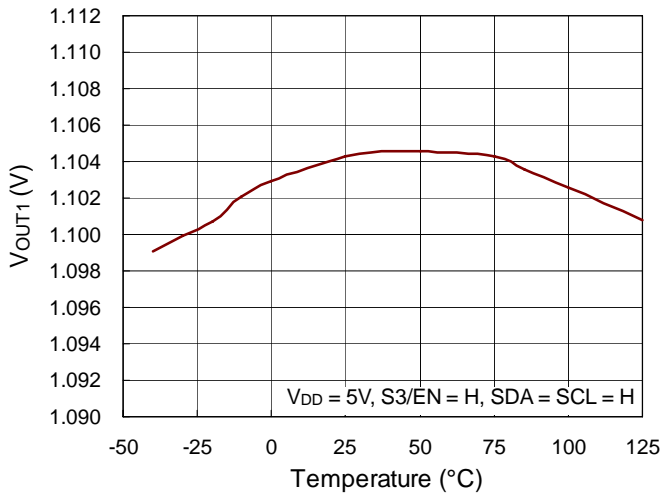
**Note 2.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 3.** The device is not guaranteed to function outside its operating conditions.

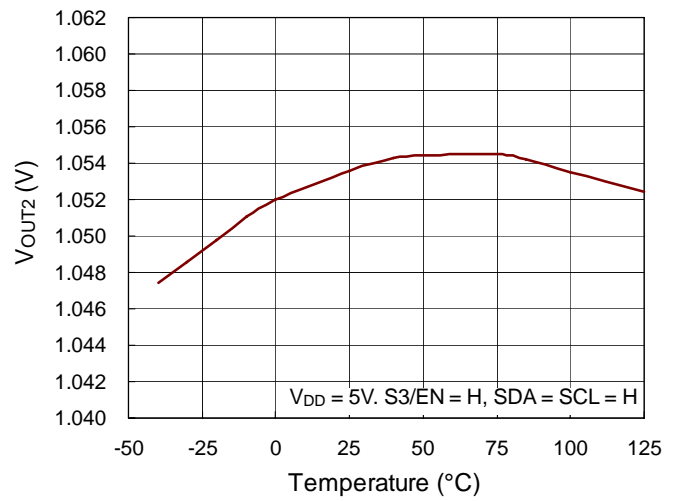
**Note 4.**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ\text{C}$  on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

**Typical Operating Characteristics**

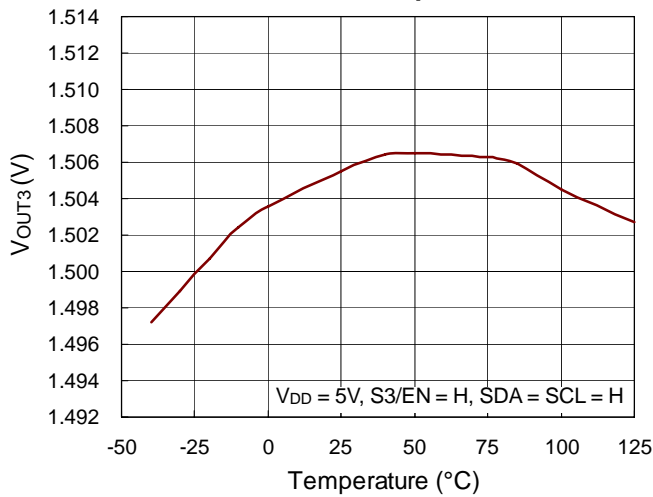
**V<sub>OUT1</sub> vs. Temperature**



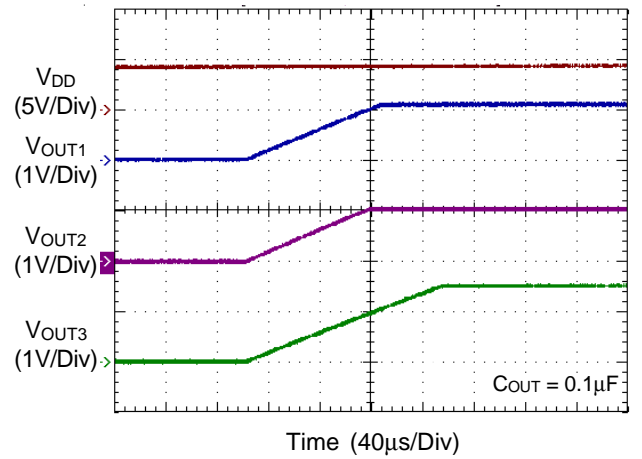
**V<sub>OUT2</sub> vs. Temperature**



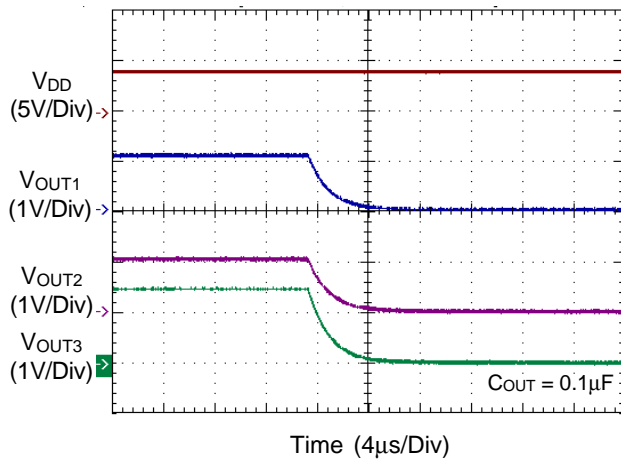
**V<sub>OUT3</sub> vs. Temperature**



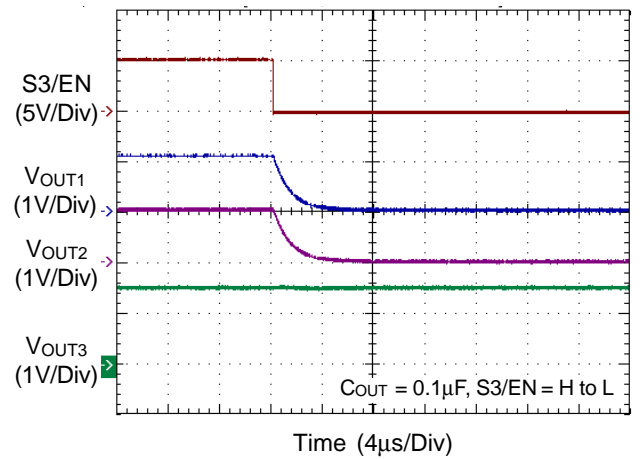
**Star Up from V<sub>DD</sub>**



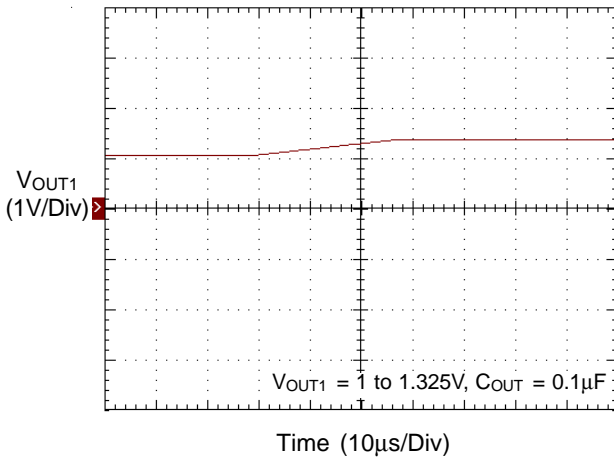
**Power Off from V<sub>DD</sub>**



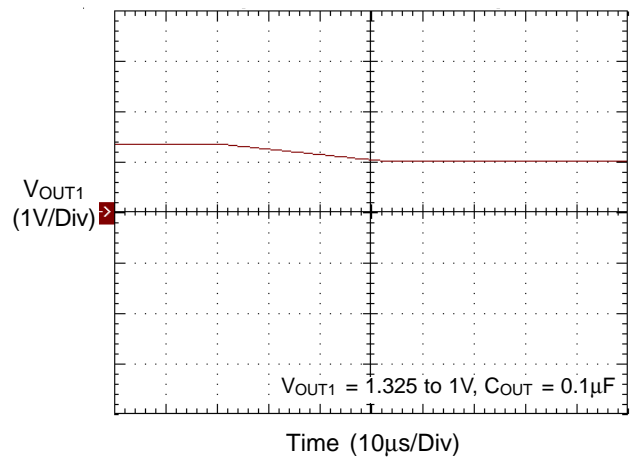
**S3 State**



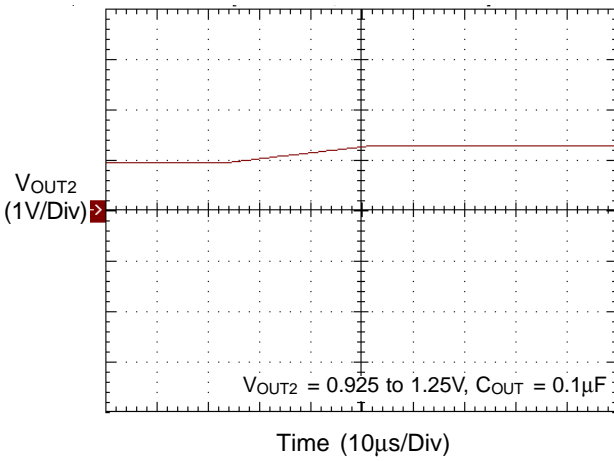
V<sub>OUT1</sub> Ramp-Up by VID



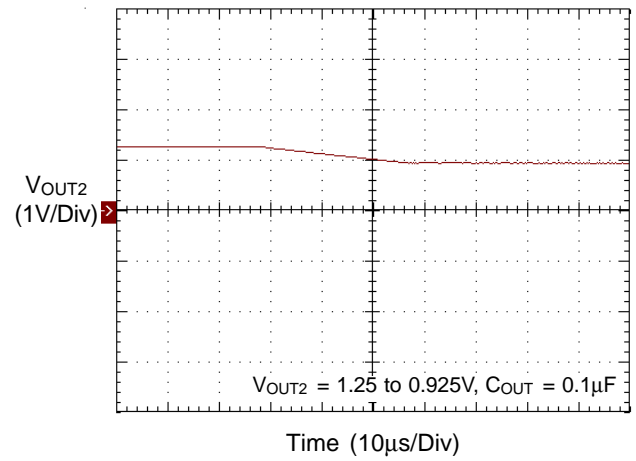
V<sub>OUT1</sub> Ramp-Down by VID



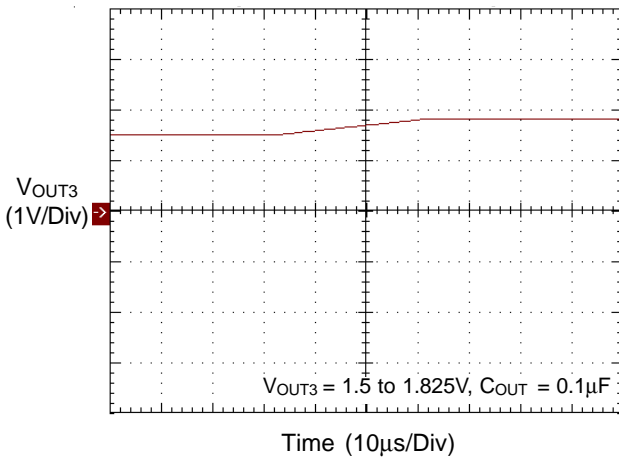
V<sub>OUT2</sub> Ramp-Up by VID



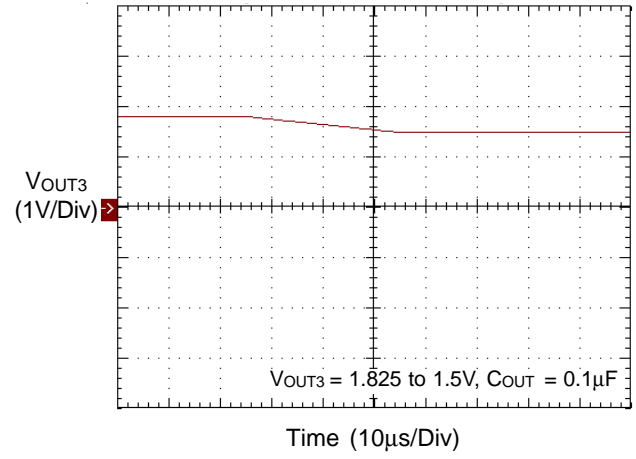
V<sub>OUT2</sub> Ramp-Down by VID



V<sub>OUT3</sub> Ramp-Up by VID



V<sub>OUT3</sub> Ramp-Down by VID



**Applications Information**

**Output Capacitor**

The output capacitance value determines the slew rate of output voltage during voltage transition. For example, if  $C_{OUT} = 0.1\mu F$  and the voltage step is 1.1V, the rising slew rate can be calculated as the following.

$$\text{Slew Rate} = \frac{I_{OUT}}{C_{OUT}} = \frac{1.1 \times 10^{-3}}{0.1 \times 10^{-6}} = 11 \text{mV}/\mu\text{s}$$

For stability consideration, the recommended minimum output capacitance is 10nF. This capacitor should be located as close to the output pin as possible to minimize the PCB trace parasitic inductance and resistance.

**I<sup>2</sup>C Interface**

The RT9403A/B/C receives and decodes the SCL and SDA inputs from the master using the standard I<sup>2</sup>C 2-wire interface to program each output voltage. SCL and SDA must be pulled-up to typically 3.3V or 5V by external pull-up resistors with value is between 10kΩ and 20kΩ. Figure 1 shows the data format of the RT9403A/B/C. After the START bit, the I<sup>2</sup>C master sends an address byte. This address byte includes a 7-bits long address code followed by an eighth bit which is a data direction bit (R/W). The RT9403A/B/C's address is 01100xx and is a write-only (slave) device. Table 4 represent different address mapping to specific part number of RT9403A/B/C. After the address byte, the following 1st Data byte determines which DAC's output voltage will be programmed. Then, the 2nd Data byte is written to set the target output voltage of that selected DAC according to the VID table1 and table 2. After the STOP bit, the output voltage of the selected DAC ramps up/down to the programmed target level.

**S3/EN Function**

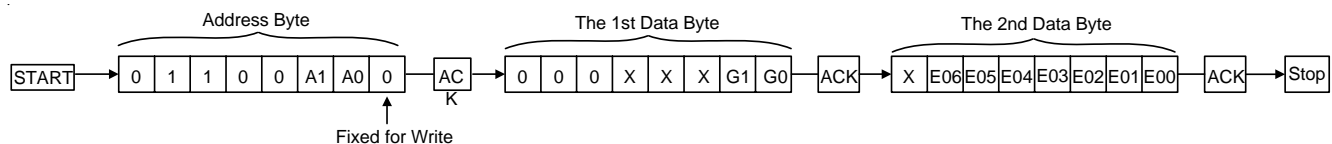
The RT9403A/B/C can be enabled or set to S3 state by the voltage of S3/EN pin. If the applied voltage of S3/EN pin is greater than enable threshold, the RT9403A/B/C will be enabled and all outputs ramp up to its own default preset voltage ( $V_{OUT1} = 1.1V, V_{OUT2} = 1.05V, V_{OUT3} = 1.5V$ ). Then the RT9403A/B/C is available to decode the SCL and SDA inputs to determine the programmed voltage for each output. Pulling down this pin below the enable threshold will set the RT9403A/B/C in S3 state. In the S3 state, both  $V_{OUT1}$  and  $V_{OUT2}$  will be turned off, only  $V_{OUT3}$  is active. If S3/EN goes high again,  $V_{OUT1}$  and  $V_{OUT2}$  will return to its previous active level. Table 3 shows the S3/EN state and output status.

**Table 3. S3/EN State and Output Status**

S3/EN	VOUT1	VOUT2	VOUT3
H (Enable)	Active	Active	Active
L (S3 State)	OFF	OFF	Active

**Table 4. Address Mapping to Specific Part Number of RT9403A/B/C**

Part	A1	A0
RT9403A	0	1
RT9403B	1	0
RT9403C	1	1



G1	G0	Rail to be Programmed
0	0	VOUT1
0	1	VOUT2
1	0	VOUT3
1	1	None

- Note :
1. X = Don't Care
  2. E [6:0] : Follow Serial Code Table

Figure 1. RT9403A/B/C Data Transfer Format

## Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where  $T_{J(MAX)}$  is the maximum operation junction temperature,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance. For recommended operating conditions specification of RT9403A/B/C, the maximum junction temperature is 125°C and  $T_A$  is the maximum ambient temperature. The junction to ambient thermal resistance  $\theta_{JA}$  is layout dependent. For SOT-23-8 package, the thermal resistance  $\theta_{JA}$  is 250°C/W on the standard JEDEC 51-3 single layer thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (250^\circ\text{C/W}) = 0.4\text{W} \text{ for SOT-23-8 package}$$

The maximum power dissipation depends on operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance  $\theta_{JA}$ . For RT9403A/B/C package, the Figure 2 of derating curve allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

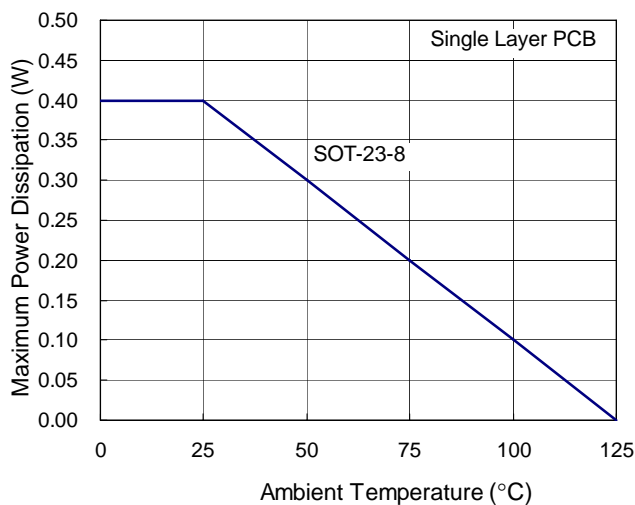


Figure 2. Derating Curve for RT9403A/B/C Package

## Layout Considerations

For best performance of the RT9403A/B/C, the following layout guideline should be strictly followed

- ▶ The input capacitor should be placed as close to VDD pin as possible.
- ▶ The output capacitor should be placed as close to VOUT pin as possible.

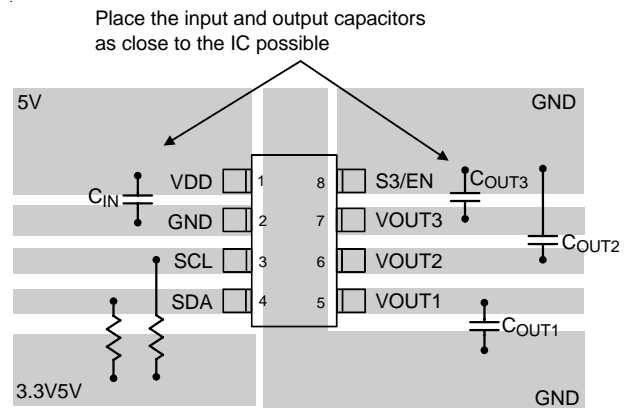
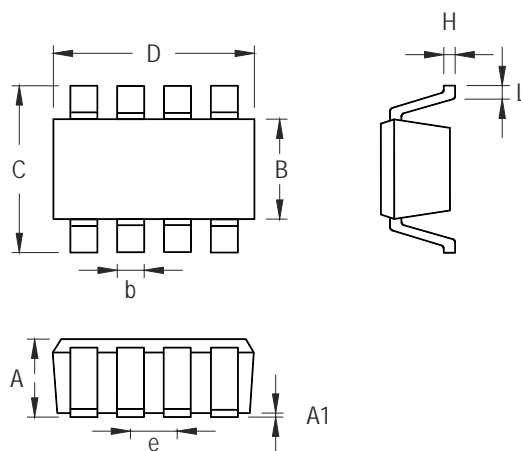


Figure 3. PCB Layout Guide



**Outline Dimension**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.450	0.039	0.057
A1	0.000	0.150	0.000	0.006
B	1.500	1.700	0.059	0.067
b	0.220	0.500	0.009	0.020
C	2.600	3.000	0.102	0.118
D	2.800	3.000	0.110	0.118
e	0.585	0.715	0.023	0.028
H	0.100	0.220	0.004	0.009
L	0.300	0.600	0.012	0.024

**SOT-23-8 Surface Mount Package**

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