5μA System Side Single Cell Fuel Gauge

General Description

The RT9427 Li-Ion/Li-Polymer battery fuel gauge is a microcontroller peripheral that provides fuel gauging for single-cell battery packs. The RT9427 resides within the system's main board and manages a non-removable battery or removable battery pack.

The RT9427 reports *StateOfCharge*, *StateOfHealth*, *FullChargeCapacity*, *TimeToEmpty* and *CycleCount* based on the Voltaic Gauge with Current Sensing (VGCS) algorithm by using the voltage difference between battery voltage and OCV to calculate the increasing or decreasing SOC, with current sensing compensation to report battery SOC.

Voltaic Gauge with Current Sensing algorithm can support smoothly SOC and does not accumulate error with time and current. That is an advantage compared to coulomb counter which suffer from SOC drift caused by current sense error and battery self-discharge.

The RT9427 provides complete battery status monitor with interrupt alarm function. It can alert to host processor actively when condition of battery over/undervoltage, over-temperature in charge/discharge and overcurrent in charge/discharge. Especially for high C-rate battery charging application, it can measure battery voltage by kelvin sense connection to eliminate the IR drop effect for optimal charging profile and safety. More useful alarm functions are Under SOC alert, SOC Change and battery presence status change.

Features

- **Support System Side Fuel Gauging**
- **Battery Fuel Gauge for 1-Series (1sXp) Li-Ion/Li-Polymer Applications**
- **State of Charge (SOC) Calculated by VoltaicGauge™ with Current Sensing (VGCS)**
- **No Accumulation Error on Capacity Calculation**
- **Battery SOC, SOH, FCC, TTE and Cycle Count Report**
- **Ultra Low Power Consumption: 5μA**
- **Voltage Measurement: ±5mV**
- **Current Measurement: ±0.5%**
- **Battery Temperature Measurement: ±1°C (T_A = 0°C to 45°C)**
- **Battery Monitor with Alert Indicator for Voltage, Current, Temperature, SOC and Presence**
- **High C-Rate Battery Charging Compliance**
- **Voltage Kelvin-Sense Connection for WDFN Package**
- **Low-Value Sense Resistor (0.5mΩ to 40mΩ, typical 10mΩ)**
- **9 Bump WL-CSP Package with 0.5mm Pitch**
- **10 Pin WDFN Package with 0.4mm Pitch**
- **I^2C Controlled Interface with 1.2V and 1.8V IO Compatible**

Applications

- Smartphones
- Tablet PC
- Wearable Device
- Digital Still Cameras
- Digital Video Cameras
- Handheld and Portable Applications

Ordering Information

RT9427 □□

Package Type
WSC: WL-CSP-9B 1.68x1.81 (BSC)
QWF: WDFN-10L 2x2.5 (FC) (W-Type)

Lead Plating System
G: Green (Halogen Free and Pb Free)
(For WDFN-10L 2x2.5 (FC) Only)

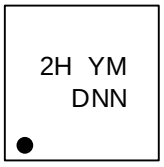
Note:

Richtek products are:

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering.

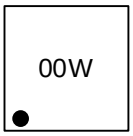
Marking Information

RT9427WSC



2H: Product Code
YMDNN: Date Code

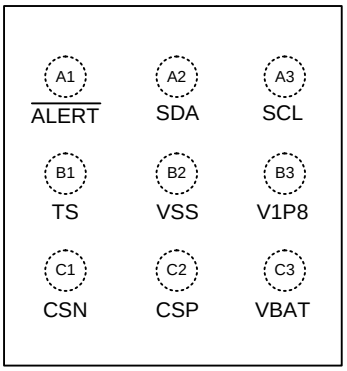
RT9427GQWF



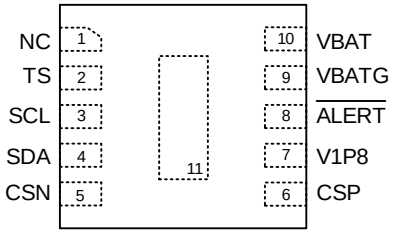
0 : Product Code
W: Date Code

Pin Configuration

(TOP VIEW)



WL-CSP-9B 1.68x1.81 (BSC)



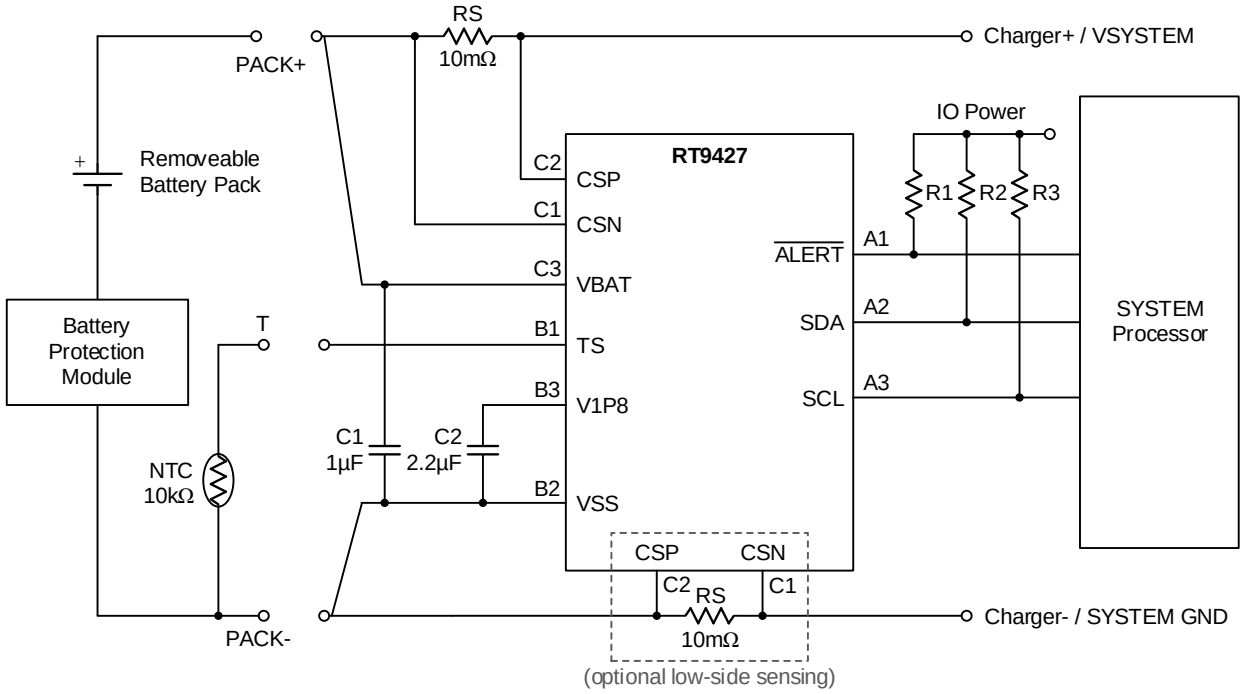
WDFN-10L 2x2.5 (FC)

Functional Pin Description

Pin No.		Pin Name	Pin Function
WL-CSP-9B 1.68x1.81 (BSC)	WDFN-10L 2x2.5 (FC)		
A1	8	$\overline{\text{ALERT}}$	Alert open-drain indicator output.
A2	4	SDA	Serial data input. Slave I^2C serial communications data line for communication with system. Open-drain I/O.
A3	3	SCL	Serial cock input. Slave I^2C serial communications clock line for communication with system. Open-drain I/O.
B1	2	TS	Temperature measurement input.
B2	--	VSS	Device ground.
B3	7	V1P8	1.8V LDO output. Connect 2.2μF ceramic capacitor to VSS. It cannot provide power for other device in the system.
C1	5	CSN	Battery current sensing negative input. Connect a 10mΩ sense resistor with kelvin connection.
C2	6	CSP	Battery current sensing positive input. Connect a 10mΩ sense resistor with kelvin connection.
C3	10	VBAT	Power supply input and battery voltage sensing input.
--	1	NC	No internal connection. Please keep floating.
--	9	VBATG	Battery voltage sensing negative input. Connect to battery connector with kelvin connection.
--	11	EP	Exposed Pad. Connect to CSP.

Typical Application Circuit

For WL-CSP-9B 1.68x1.81 (BSC)



For WDFN-10L 2x2.5 (FC)

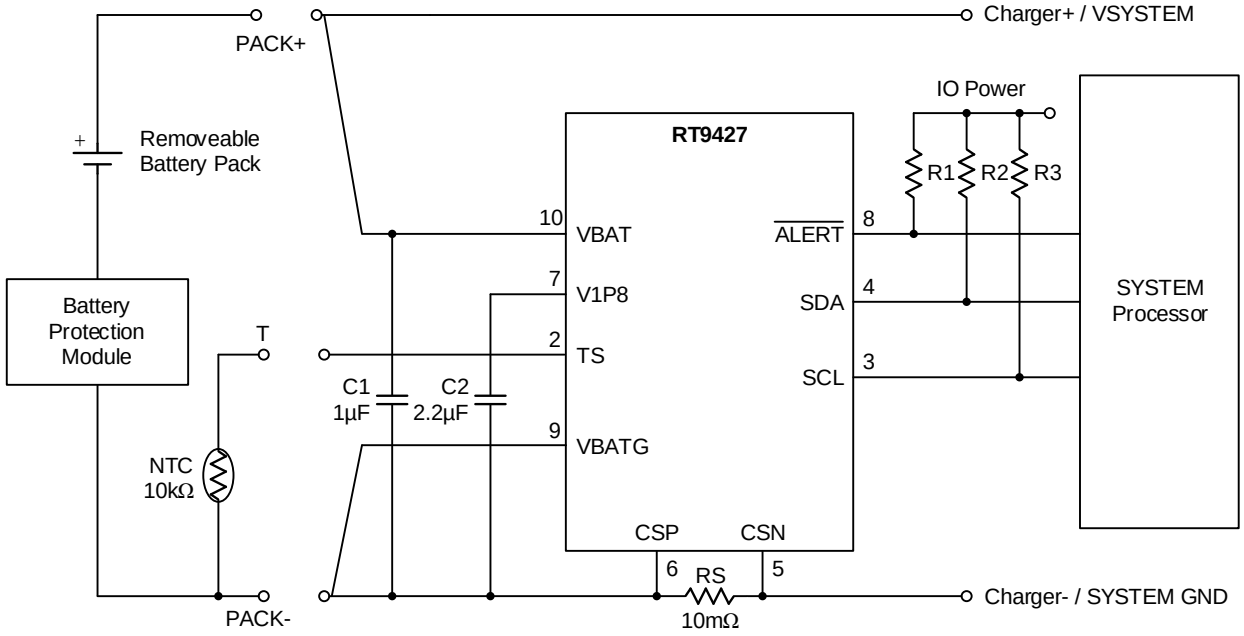
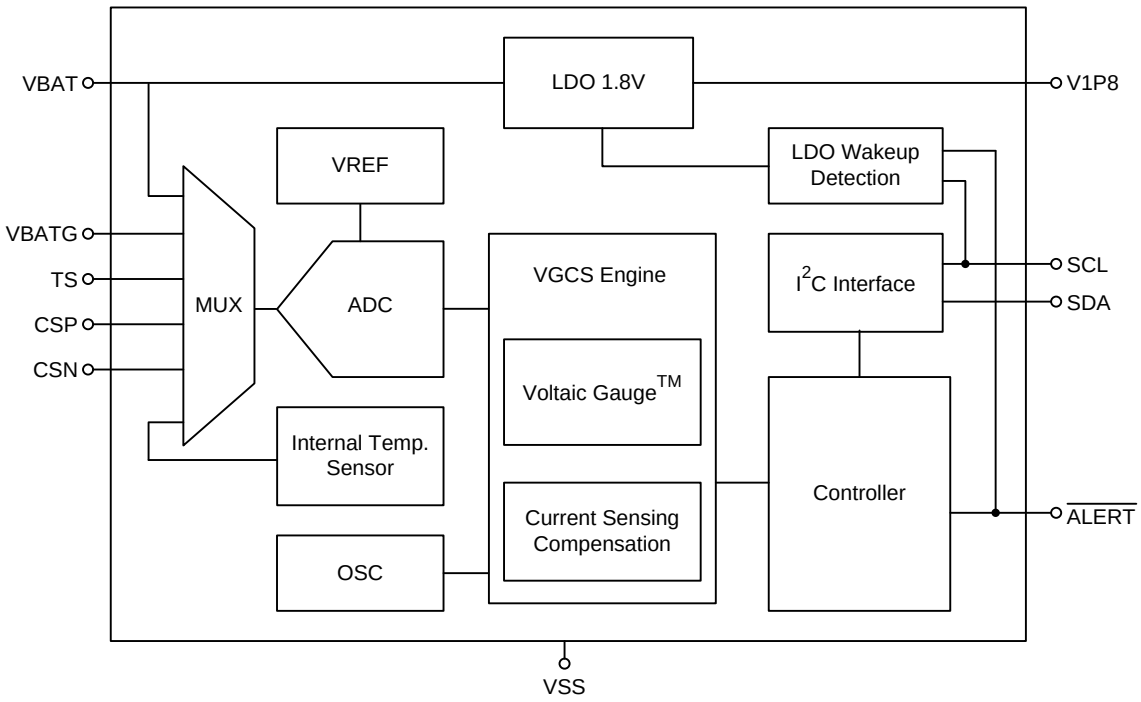


Table 1. BOM List

Name	Part Number	Description	Package	Manufacturer
C1	GRM155R61A105KE01	CAP, CERM, 1μF, 10V, ±10%, X5R	0402	Murata
C2	GRM155R60J225KE01	CAP, CERM, 2.2μF, 6.3V, ±10%, X5R	0402	Murata
R1, R2, R3	WR06X3301FTL	3.3k, 1%, 0.1W	0603	WALSIN
RS	RLM-1220-6F-R010-FNH	10mΩ, 1%, 1W	0805	CYNTEC
NTC	103KT1608-1P	10kΩ, 1%, B = 3435K	0603	SEMITEC

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Voltage on CSN Pin to CSP ---------- –0.3V to 2V
- Voltage on V1P8 pin Relative to VSS ---------- –0.3V to 2V
- Voltage on VBAT Pin Relative to VSS ---------- –0.3V to 6V
- Voltage on All Other Pins Relative to VSS ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WDFN-10L 2x2.5 (FC) ---------- 0.88W

  WL-CSP-9B 1.68x1.81 (BSC) ---------- 1.81W
- Package Thermal Resistance (Note 2)

  WDFN-10L 2x2.5 (FC), θ_{JA} ---------- 112.6°C/W

  WDFN-10L 2x2.5 (FC), θ_{JC} ---------- 0.8°C/W

  WL-CSP-9B 1.68x1.81 (BSC), θ_{JA} ---------- 55°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VBAT ---------- 2.5V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

($2.5V \le V_{BAT} \le 5.5V$, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operation Voltage		VBAT - VSS	2.5	--	5.5	V
Active Current	I_{ACTIVE}	VBAT = 3.8V, battery present & ExTemp disabled	--	12	20	μA
Sleep Current	I_{SLEEP}	VBAT = 3.8V, battery present & ExTemp disabled, period is 4 times of active mode	--	5	12	μA
Shutdown Current	$I_{SHUTDOWN}$	VBAT = 3.8V, LDO off	--	1	1.5	μA
1.8V LDO	V_{1P8}		--	1.85	--	V
Voltage Measurement Range			2.5	--	VBAT	V
Voltage Measurement Error	V_{ERR}	VBAT = 4V	–5	--	5	mV
Current Measurement Range		V_{CSP} - V_{CSN}	–100	--	100	mV
Current Measurement Gain Error	I_{GERR}	$\lvert V_{CSP} - V_{CSN} \rvert$ = 80mV	–0.5	--	0.5	%
Current Measurement Offset Error	I_{OERR}	$\lvert V_{CSP} - V_{CSN} \rvert$ = 0V (Note 5)	–5	±2.5	5	μV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Temperature Measurement Error	ExtTGERR	TA = 0°C to 45°C (Note 6)	–1	--	1	°C
		TA = –40°C to 85°C (Note 6)	–3	--	3	°C
Internal Temperature Measurement Range		(Note 7)	–40	--	85	°C
Internal Temperature Measurement Error	IntTGERR	TA = 25°C	--	±3	--	°C
Battery Presence Detection Threshold			0.93 x VBAT	0.95 x VBAT	0.97 x VBAT	V
Battery Presence Detection Pull High Resistor			--	150	--	kΩ
Battery Insertion Detection Time		Battery detection delay time Programmable	20	--	145	ms
Battery Removal Detection Time			--	--	1.1	sec
Input Logic-High: SCL, SDA, $\overline{ALERT}$	VIH	Reference to VSS	0.78	--	--	V
Input Logic-Low: SCL, SDA, $\overline{ALERT}$	VIL	Reference to VSS	--	--	0.5	V
Output Logic-Low: SDA, $\overline{ALERT}$	VOL	IOL = 3mA, reference to VSS	--	--	0.3	V
Pull Down Current: SCL, SDA, $\overline{ALERT}$	IPDN		0.05	0.2	0.4	μA
SHUTDOWN Low Detection Time: SCL, $\overline{ALERT}$	tSLDT		20	--	--	μs
SHUTDOWN Entry Time	tSHDN	Delay time from SHUTDOWN command to V1P8 turned off, programmable	1	--	256	sec
I^2C ACK Delay Time	tACK	I^2C ACK, register information not ready.	--	--	10	ms
Initialization Ready Time	tRDY	Delay time from rising edge of VBAT to the active state.	--	--	250	ms
I^2C Time Out		Programmable	0.5	--	2.25	sec

Electrical Characteristics: I^2C Interface

(2.5V ≤ VBAT ≤ 5.5V, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Operating Frequency	fSCL	(Note 8)	10	--	400	kHz
Bus Free Time Between a STOP and START Condition	tBUF		1.3	--	--	μs
Hold Time After START Condition	tHD;STA	(Note 8)	0.6	--	--	μs
Low Period of the SCL Clock	tLOW		1.3	--	--	μs
High Period of the SCL Clock	tHIGH		0.6	--	--	μs
Setup Time for a Repeated START Condition	tSU;STA		0.6	--	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Data Hold Time	$t_{HD;DAT}$	(Note 9, 10)	0	--	0.9	μs
Data Setup Time	$t_{SU;DAT}$	(Note 9)	100	--	--	ns
Data Valid Time	$t_{VD;DAT}$	(Note 11, 12)	--	--	0.9	μs
Data Valid Acknowledge Time	$t_{VD;ACK}$	(Note 11, 13)	--	--	0.9	μs
Clock Data Rise Time	t_R		20	--	300	ns
Clock Data Fall Time	t_F		20	--	300	ns
Set-up Time for STOP Condition	$t_{SU;STO}$		0.6	--	--	μs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 14)	0	--	50	ns
Capacitive Load for Each Bus Line	C_B	(Note 15)	--	--	400	pF
SCL, SDA Input Capacitance	C_{BIN}		--	--	5	pF

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the case top of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Typical result is long times average.

Note 6. The thermistor is use 10k NTC and beta 3435k, default is SEMITEC 103KT1608T.

Note 7. Specifications are 100% tested at T_A = 25°C. Limits over the operating range are guaranteed by design and characterization.

Note 8. f_{SCL} must meet the minimum clock low time plus the rise/fall times.

Note 9. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 10. This device internally provides a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN}) of the SCL signal to bridge the undefined region of the falling edge of SCL.

Note 11. The maximum $t_{VD;DAT}$ can be 0.9μs for Fast-mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

Note 12. $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

Note 13. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

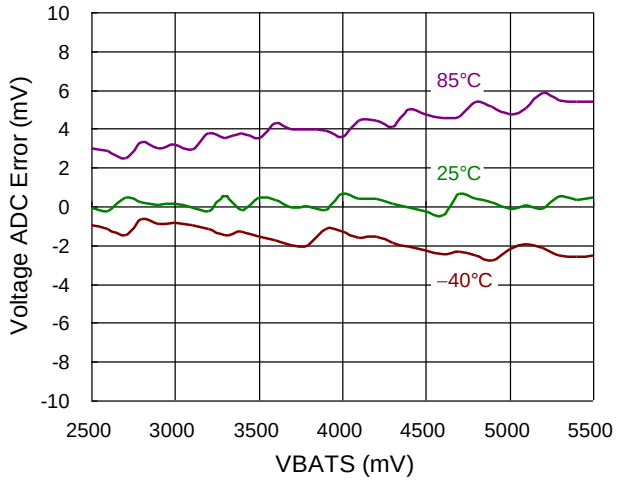
Note 14. Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

Note 15. C_B – total capacitance of one bus line in pF.

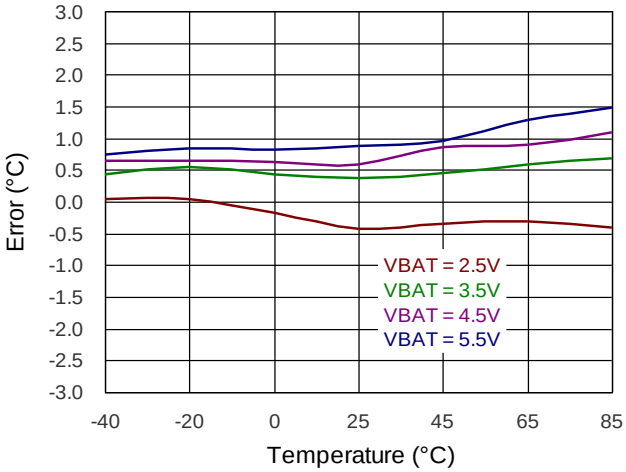
Typical Operating Characteristics

*: SOC accuracy tested by IC with custom parameter.

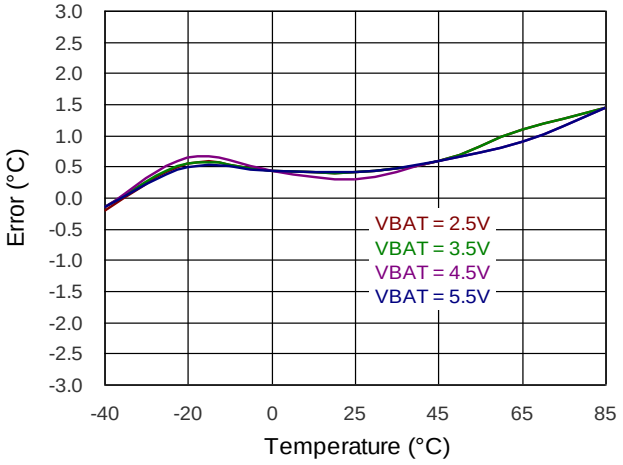
Voltage ADC Error vs. Temperature



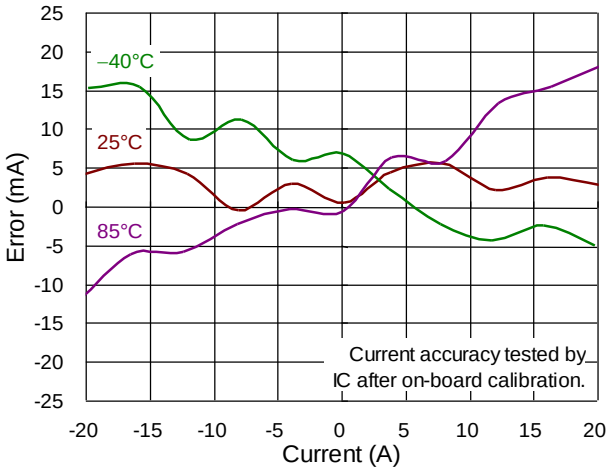
Internal Temperature Measurement Error



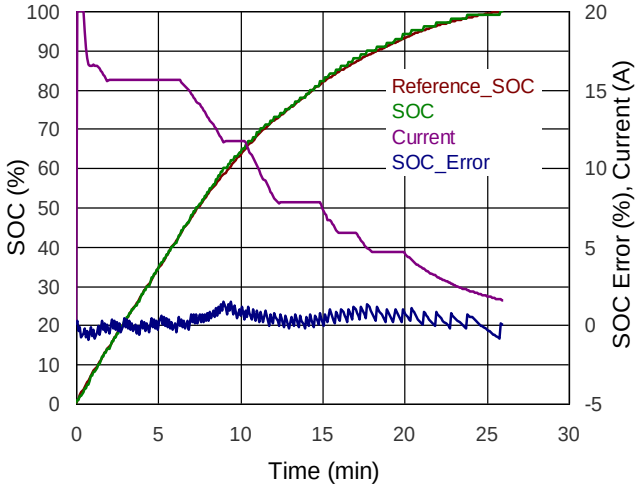
External Temperature Measurement Error



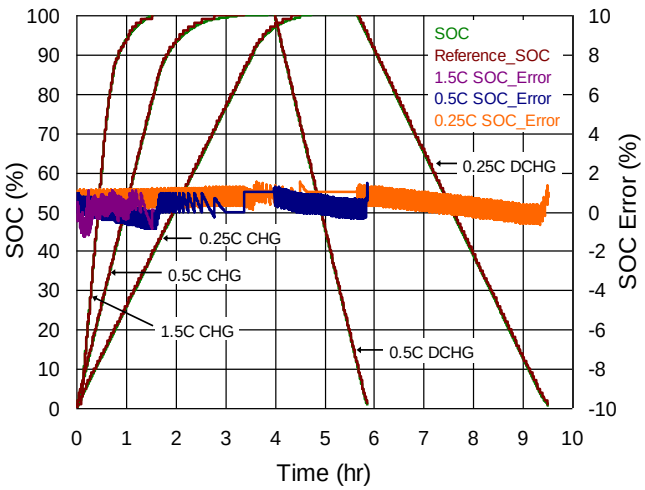
Current ADC Error with 0.5mΩ Rsense vs. Temperature



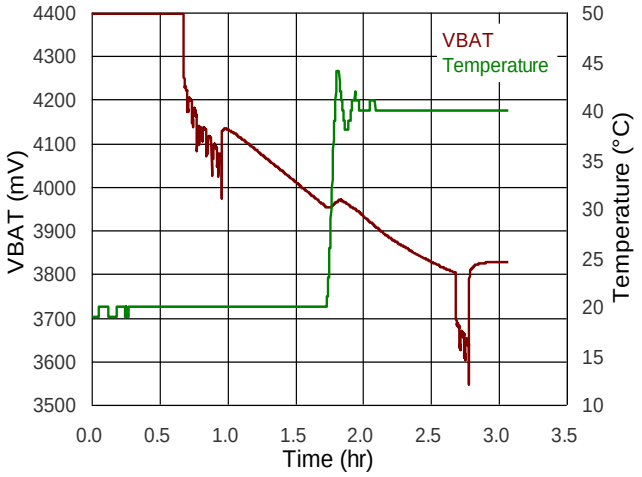
Fast Charging SOC Accuracy*



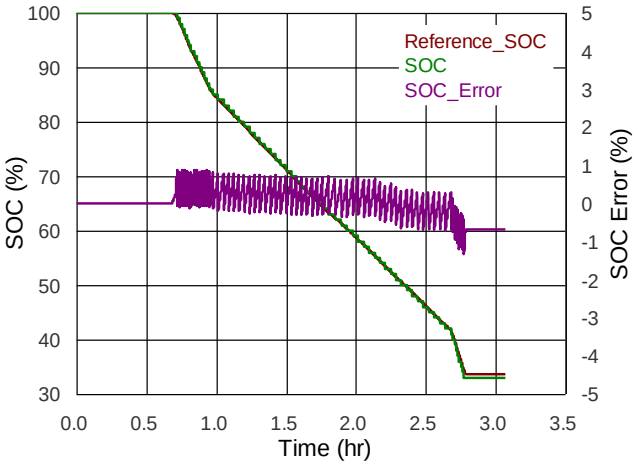
SOC Accuracy*



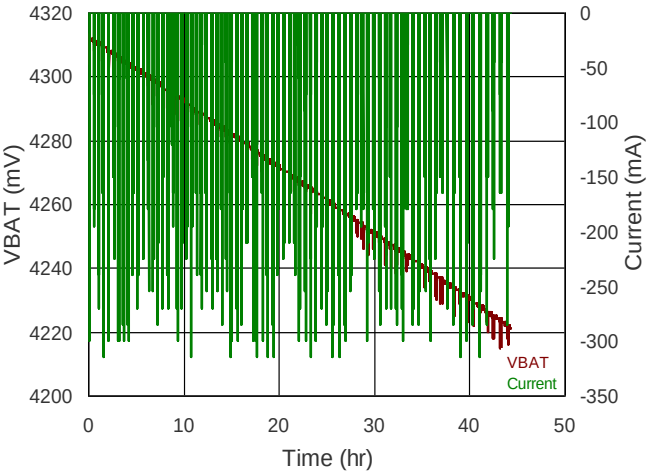
Load / Temperature Transient SOC Accuracy 1/2



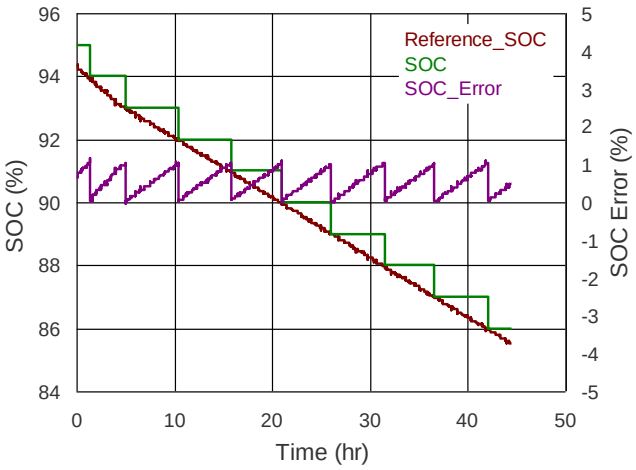
Load / Temperature Transient SOC Accuracy 2/2*



High Pulse Discharge SOC Accuracy 1/2



High Pulse Discharge SOC Accuracy 2/2*



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

ADC for Voltage, Current and Temperature

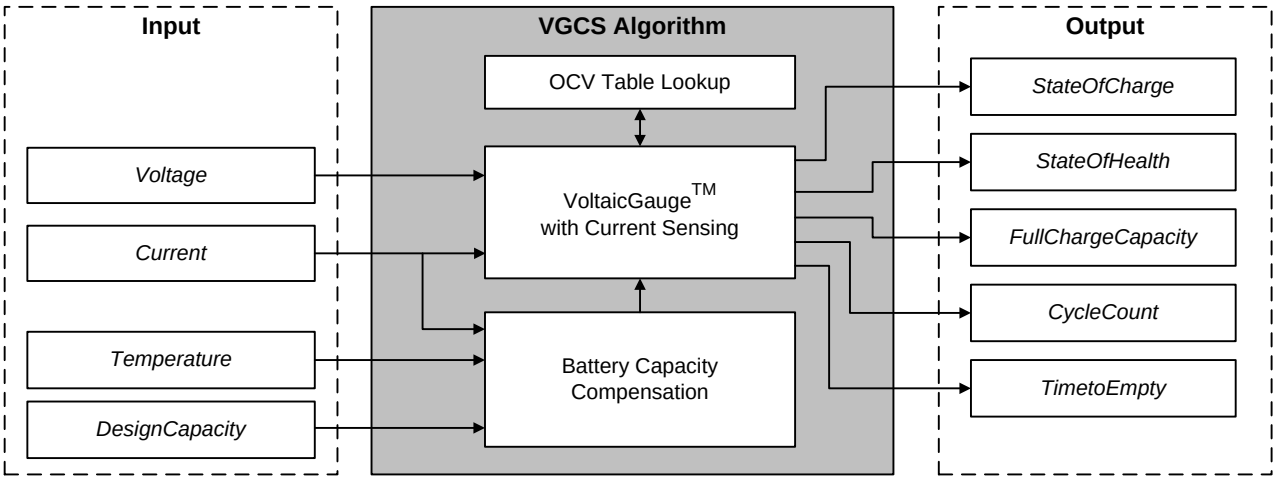
Battery voltage is measured at the VBAT pin input with respect to VBATG over a 2.5 to 5.5V range with resolutions of 1mV. The ADC calculates the first cell voltage for a period of 250ms after IC power on and then for a period of 1s for every cycle afterwards. The Voltage register requires 1s to update after exiting Sleep mode. The result is placed in the *Voltage* register at the end of each conversion period.

The RT9427 Fuel Gauge measures battery current in charging and discharging and reports it to *Current* register. The measurement range is 10A (RS = 10mΩ), and the resolution is 1mA.

The RT9427 reports temperature to *Temperature* register by measuring battery temperature or chip temperature. When measuring battery temperature, an external NTC resistor will be used.

VoltaicGauge™ with Current Sensing (VGCS) Algorithm

The VGCS algorithm is based on the battery voltage and the dynamic difference of battery voltage and battery current measurement, by iterating battery voltage information and compensating with current information to increase or decrease delta SOC, then integrate to SOC. The following figure is for VGCS functional block.



The RT9427 got battery voltage information then using OCV table and iterate calculation with current correction to calculate delta SOC, then using design capacity and battery capacity as a reference to optimize result and output final SOC result.

The coulomb counter based fuel gauge suffers from SOC drift due to current-sense error and cell self-discharge. Even there is a very small current sensing error, the coulomb counter accumulates the error from time to time, VGCS is based on voltage iteration algorithm to reach stable SOC behavior and only using current information to fine tune result for getting good transient state response. VGCS does not accumulate current and suffer SOC drift issue like traditional coulomb counter.

VGCS also support high C-RATE charging technology, battery capacity aging compensation by full charge, full discharge, relax condition and Battery Aging Profile Adjust (BAPA) command.

Design Capacity

The *DesignCapacity* register should be set with proper value after IC power on, Design Capacity is the expected capacity when cell has been made and it is not been changed when VGCS active. Design Capacity is used as a reference input for VGCS algorithm. The resolution of Design Capacity is 1mAh and default value is 0x07D0 (2000mAh).

SOC Report

The *StateOfCharge* register is a read-only register that displays the state of charge of the cell as calculated by the VGCS algorithm. The result is displayed as a percentage of the cell's full capacity. This register automatically adapts to variation in battery size since the Fuel Gauge naturally recognize relative SOC. The units of SOC is %. The reported SOC also includes residual capacity, which might not be available to the actual application because of early termination voltage requirements. When SOC = 0, typical applications have no remaining capacity. The first update occurs in 250ms after IC power on.

Power Mode

There are three power mode for the RT9427. Each power mode can be applied on different application for different power consumption considering. The three power modes are Active mode, Sleep mode and Shutdown mode.

Active Mode

The active mode is recommended and it is the default power mode after power on. In active mode, the *Voltage*, *Current*, *Temperature*, *AverageVoltage*, *AverageCurrent* and *AverageTemperature* will be updated every second.

Sleep Mode

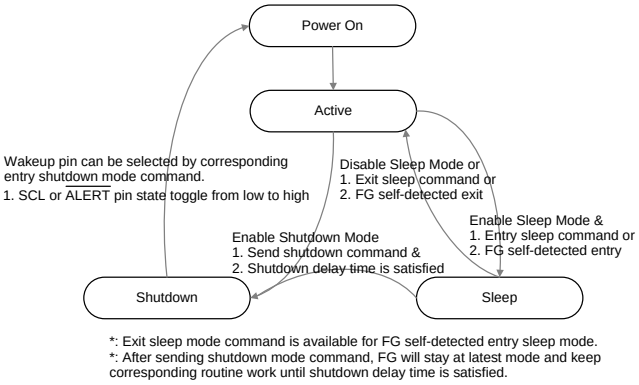
The sleep mode behavior is the same as the active mode but it has the longer measurement period. The period in the sleep mode is programmable. The minimum period is 2 times of active mode and the maximum period is 16 times of active mode. The default period is 4 times of active mode. When sleep mode function is enabled, it can be entered/exited by sending commands or by Fuel Gauge self-detection.

Shutdown Mode

In shutdown mode, the RT9427 will turn off internal LDO to keep the minimum power consumption and all the RAM-based data are lost. To enter shutdown mode, the function should be enabled firstly and shutdown delay time is satisfied after sending entry shutdown mode command.

To exit shutdown mode, it can be wakeup by SCL or $\overline{\text{ALERT}}$ pin transition from low to high and the low period should satisfy t_{WAKE}. Wakeup pin can be selected by corresponding entry shutdown mode command.

Power Mode Switching



Controller

The controller takes care of the control flow of system routine, ADC measurement flow, algorithm calculation and alert determined.

Power Up Sequence

When the RT9427 is power on, the Fuel Gauge (FG) measures the battery voltage and then predicts the first SOC according to the voltage for a period of 250ms. The first SOC will be accurate if the battery has been well relaxed for over 30 minutes. Otherwise, the initial SOC error occurs. However, the initial SOC error will be convergent and the SOC will be adjusted gradually and finally approach to the OCV when battery is relaxed.

Quick Sensing

A Quick Sensing operation allows the RT9427 to restart battery voltage sensing and *StateOfCharge* calculation. The operation is used to reduce the initial *StateOfCharge* error caused by improper power-on sequence. A Quick Sensing operation can be performed by I^2C Quick Sensing command (0x4000) to the *Control* register.

Alert Function

The RT9427 support several kinds of alert to alarm system there is abnormal condition need to be noticed, such as over-temperature or undervoltage. It total includes over-temperature in charge (OTC), over-temperature in discharge (OTD), overvoltage (OV), undervoltage (UV), under-SOC (US) and SOC change (SC), overcurrent in charge (OCC), over- current in discharge (ODC) and temperature change (TC) alerts.

Host can polling the ALERT Flag for a period to monitor system status or accept the interrupt notice from the RT9427 $\overline{\text{ALERT}}$ pin. Alert need to be enabled before it works. There are 2 ways to enable alert function. One is to enable specified bit operation, the other is just to set a proper value to detection threshold. Please refer to below diagram and descriptions for detailed.

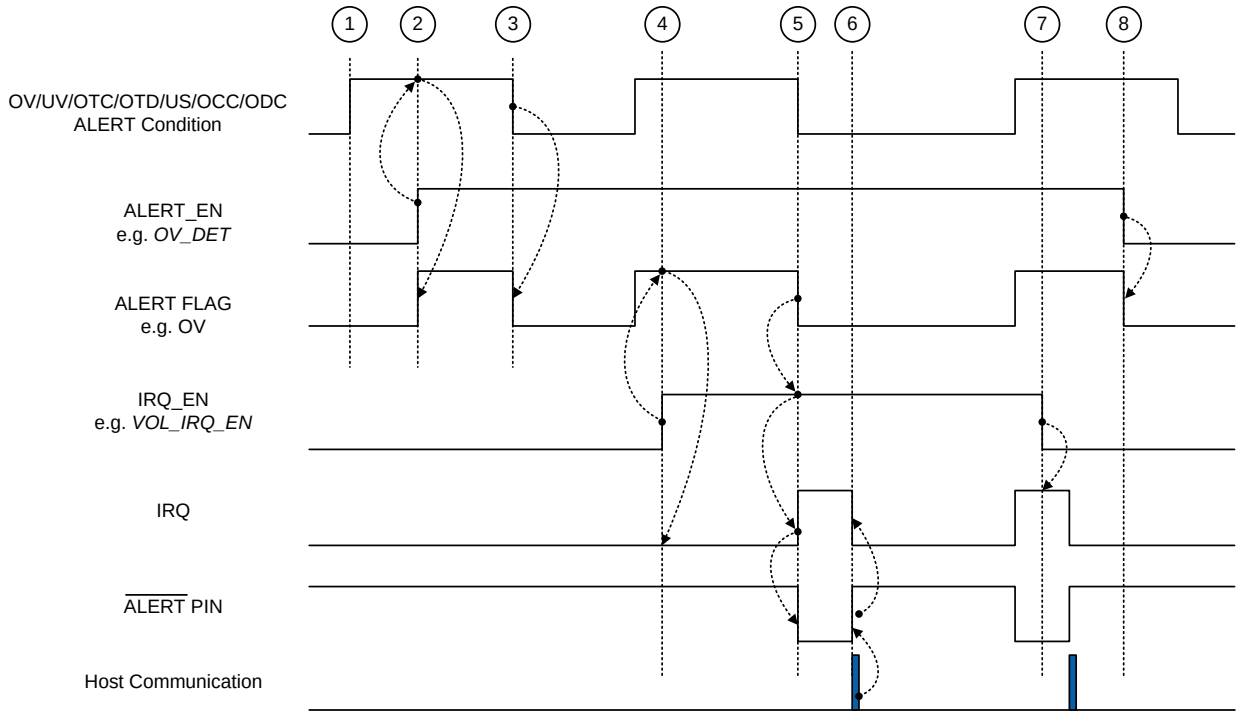


Figure 1. ALERT Function Timing Diagram

1. ALERT occur but ALERT_EN is disabled, ALERT FLAG have no response.
2. ALERT_EN enable, ALERT FLAG is set when ALERT condition occur.
3. ALERT FLAG is cleared when ALERT condition recover.
4. When ALERT FLAG is already set and IRQ_EN is set, IRQ and $\overline{\text{ALERT}}$ PIN output have no response.
5. IRQ is set and $\overline{\text{ALERT}}$ PIN output low only when IRQ_EN is set and ALERT FLAG state change.
6. IRQ and $\overline{\text{ALERT}}$ PIN are read clear only.
7. Clear IRQ_EN have no effect on IRQ and $\overline{\text{ALERT}}$ PIN output.
8. Disable ALERT_EN will also clear ALERT FLAG.

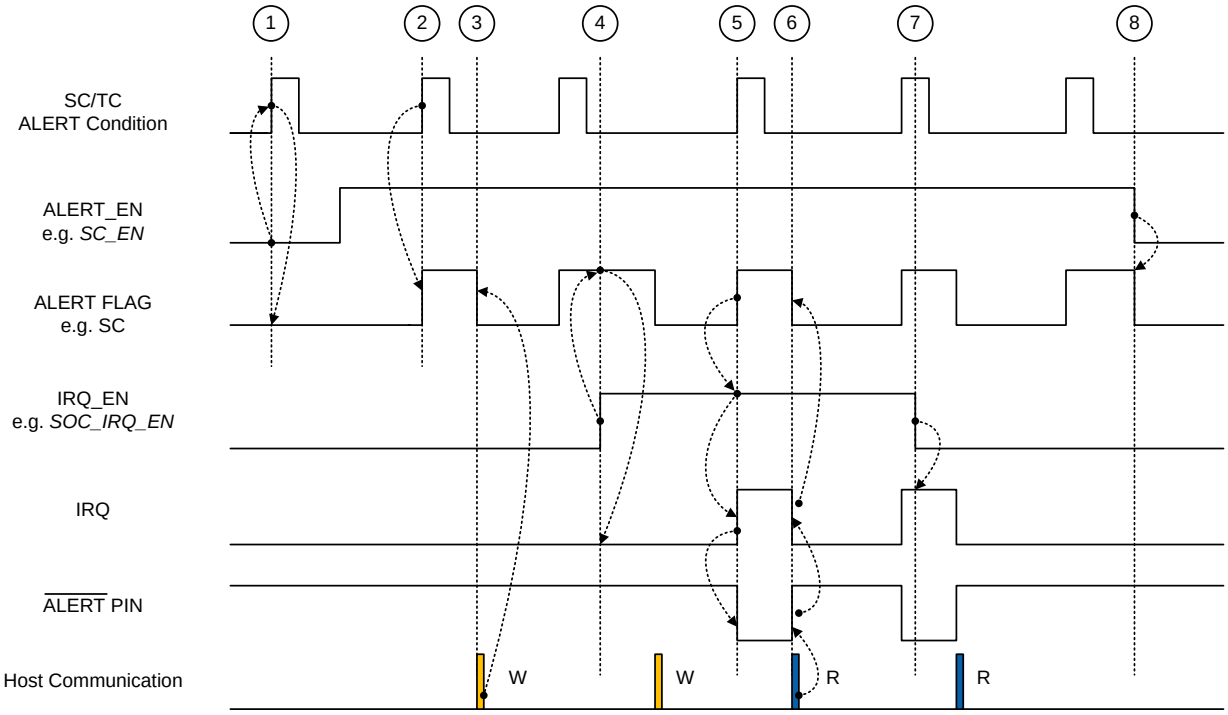


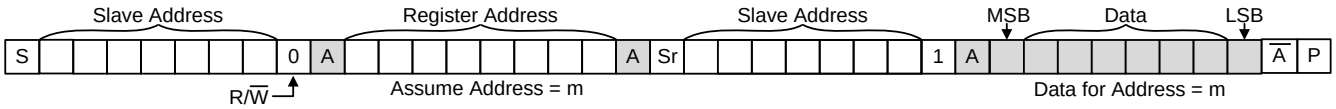
Figure 2. SC/TC ALERT Function Timing Diagram

1. ALERT condition occur but ALERT_EN disable, ALERT FLAG have no response
2. ALERT_EN enable, ALERT FLAG is set when ALERT condition occur.
3. ALERT FLAG is cleared when driver write ALERT FLAG to 0.
4. When ALERT FLAG is already set and IRQ_EN is set, IRQ and $\overline{\text{ALERT}}$ PIN output have no response.
5. IRQ is set and $\overline{\text{ALERT}}$ PIN output low only when IRQ_EN is set and ALERT FLAG state set.
6. IRQ and $\overline{\text{ALERT}}$ PIN are read clear only, driver read clear IRQ will also clear ALERT FLAG
7. Clear IRQ_EN have no effect on IRQ and $\overline{\text{ALERT}}$ PIN output.
8. Disable ALERT_EN will also clear ALERT FLAG.

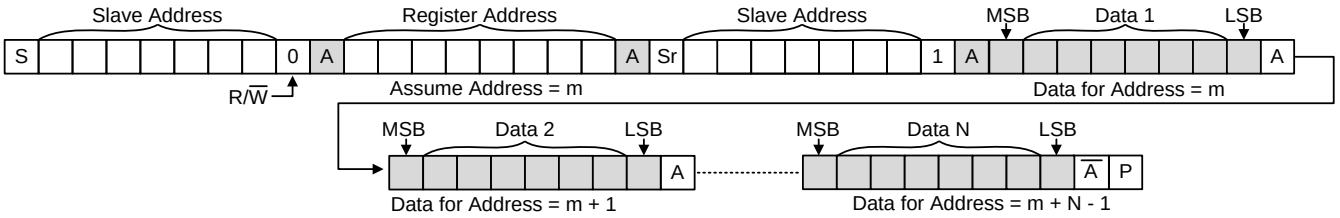
I²C Interface

The RT9427 I²C slave address = 7'b1010101. I²C interface support fast mode (bit rate up to 400kb/s). The write or read bit stream is shown below:

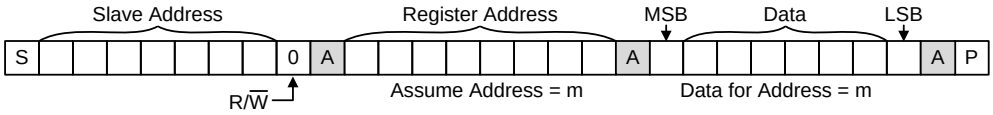
Read single byte of data from Register



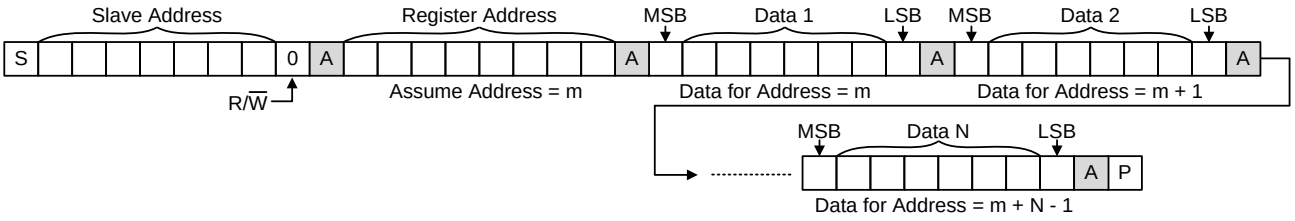
Read N bytes of data from Registers



Write single byte of data to Register

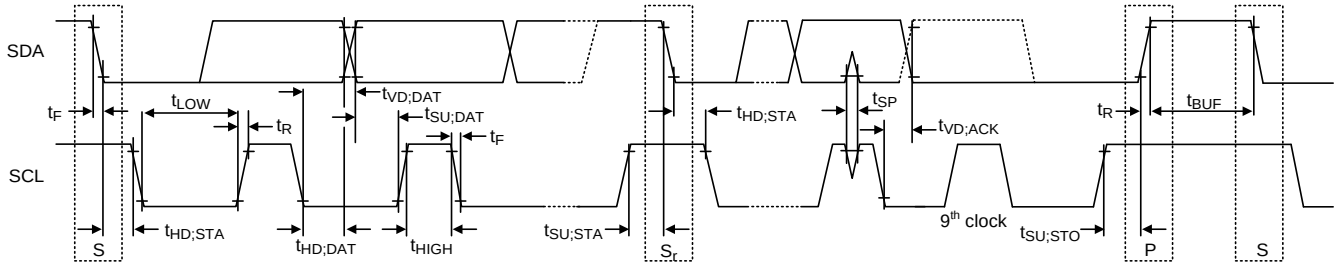


Write N bytes of data to Registers

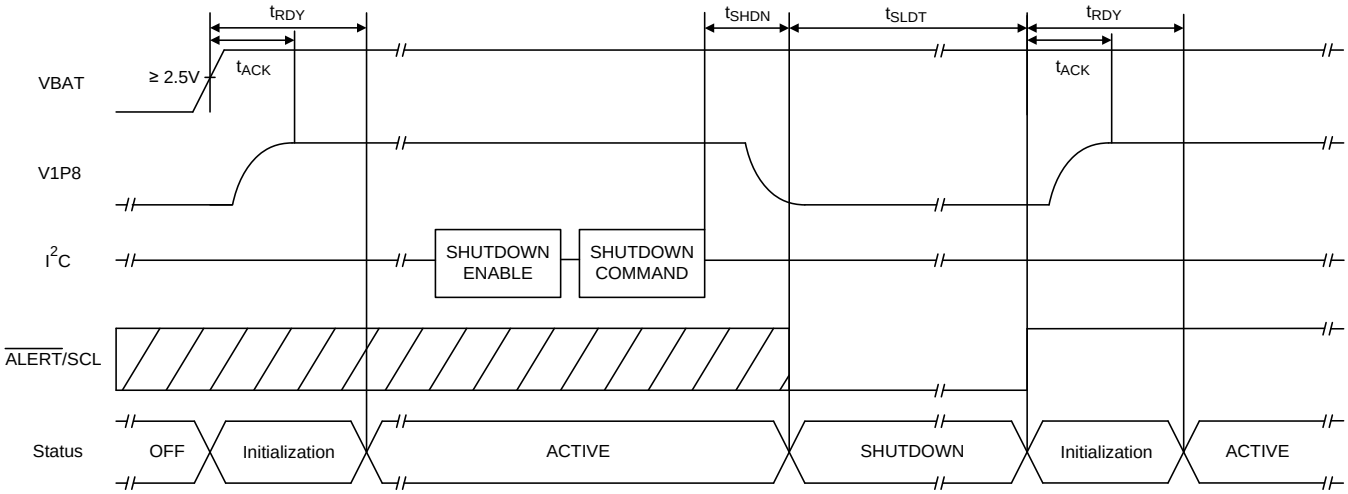


Driven by Master, Driven by Slave, P Stop, S Start, Sr Repeat Start

I²C Waveform Information



Shutdown and Wake-Up Timing



*: Wake-up pin can be selected by corresponding entry shutdown mode command.

Register Summary Table

Name	Symbol	Address	Unit	Mode	Reset
Control	CNTL	0x00 to 0x01	--	R/W	0x0000
Current	CURR	0x04 to 0x05	mA	R	0x0000
Temperature	TEMP	0x06 to 0x07	0.1°K	R/W	0x0BA6
Voltage	VBAT	0x08 to 0x09	mV	R	0x0ED8
Flag1	FLAG1	0x0A to 0x0B	--	R	0x0000
Flag2	FLAG2	0x0C to 0x0D	--	R	0x0000
DeviceID	DVCID	0x0E to 0x0F	--	R	0x2720
RemainingCapacity	RM	0x10 to 0x11	mAh	R	0x03E8
FullChargeCapacity	FCC	0x12 to 0x13	mAh	R	0x07D0
AverageCurrent	AI	0x14 to 0x15	mA	R	0x0000
TimeToEmpty	TTE	0x16 to 0x17	minute	R	0xFFFF
Version	VER	0x20 to 0x21	--	R	0x0001
VGCOMP12	VGCOMP12	0x24 to 0x25	--	R/W	0x3232
VGCOMP34	VGCOMP34	0x26 to 0x27	--	R/W	0x3232
InternalTemerature	INTT	0x28 to 0x29	0.1°K	R	0x0BA6
CycleCount	CYC	0x2A to 0x2B	Counts	R/W	0x0000
StateOfCharge	SOC	0x2C to 0x2D	%	R	0x0032
StateOfHealth	SOH	0x2E to 0x2F	%	R	0x0064
Flag3	FLAG3	0x30 to 0x31	--	R	0x0000
IRQ	IRQ	0x36 to 0x37	--	R	0x0000
DesignCapacity	DC	0x3C to 0x3D	mAh	R	0x07D0
ExtendedControl	EXTDCNTL	0x3E to 0x3F	--	W	0x0000
ExtendReg0 to 15	EXTREG0 to 15	0x40 to 0x4F	--	R/W	0xFFFF
ExtPageChecksum	PAGE_CKS	0x50 to 0x51	--	R	0xFFFF
AverageVoltage	AV	0x64 to 0x65	mV	R	0x0ED8
AverageTemperature	AT	0x66 to 0x67	0.1°K	R	0x0BA6
ExtTotalChecksum	TOTAL_CKS	0x68 to 0x69	--	R	0x0000

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-10L 2x2.5 (FC) package, the thermal resistance, θ_{JA}, is 112.6°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a WL-CSP-9B 1.68x1.81 (BSC) package, the thermal resistance, θ_{JA}, is 55°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (112.6°C/W) = 0.88W for a WDFN-10L 2x2.5 (FC) package.

$P_{D(MAX)}$ = (125°C - 25°C) / (55°C/W) = 1.81W for a WL-CSP-9B 1.68x1.81 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

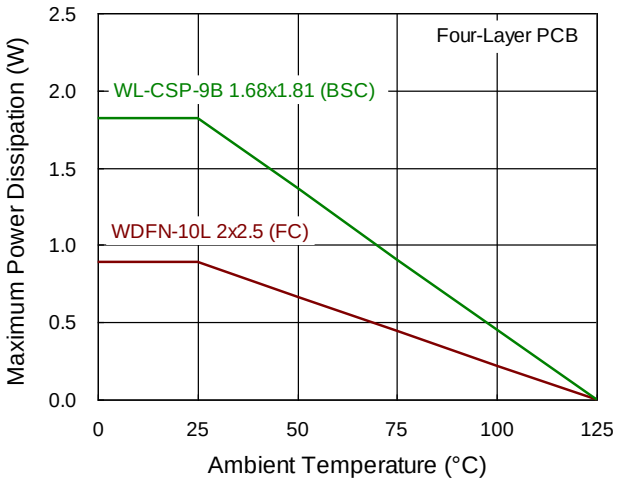


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

To ensure the measurement accuracy of the RT9427, the recommended layout guideline is as below:

- The capacitor of VBAT pin must be put as close as possible to avoid the noise effect.
- The VBAT and VBATG path must be make Kelvin sense connection to the P+ and P- to minimize the IR drop effect on voltage measurement accuracy.
- The CSN and CSP path must be make Kelvin Sense connection to RS to avoid the IR drop effect on current measurement accuracy.
- The NTC should be as close as possible to the Battery and far away from the thermal area.
- The capacitor of V1P8 pin must be put as close as possible to the IC.
- There are no special layout requirements for other pins.

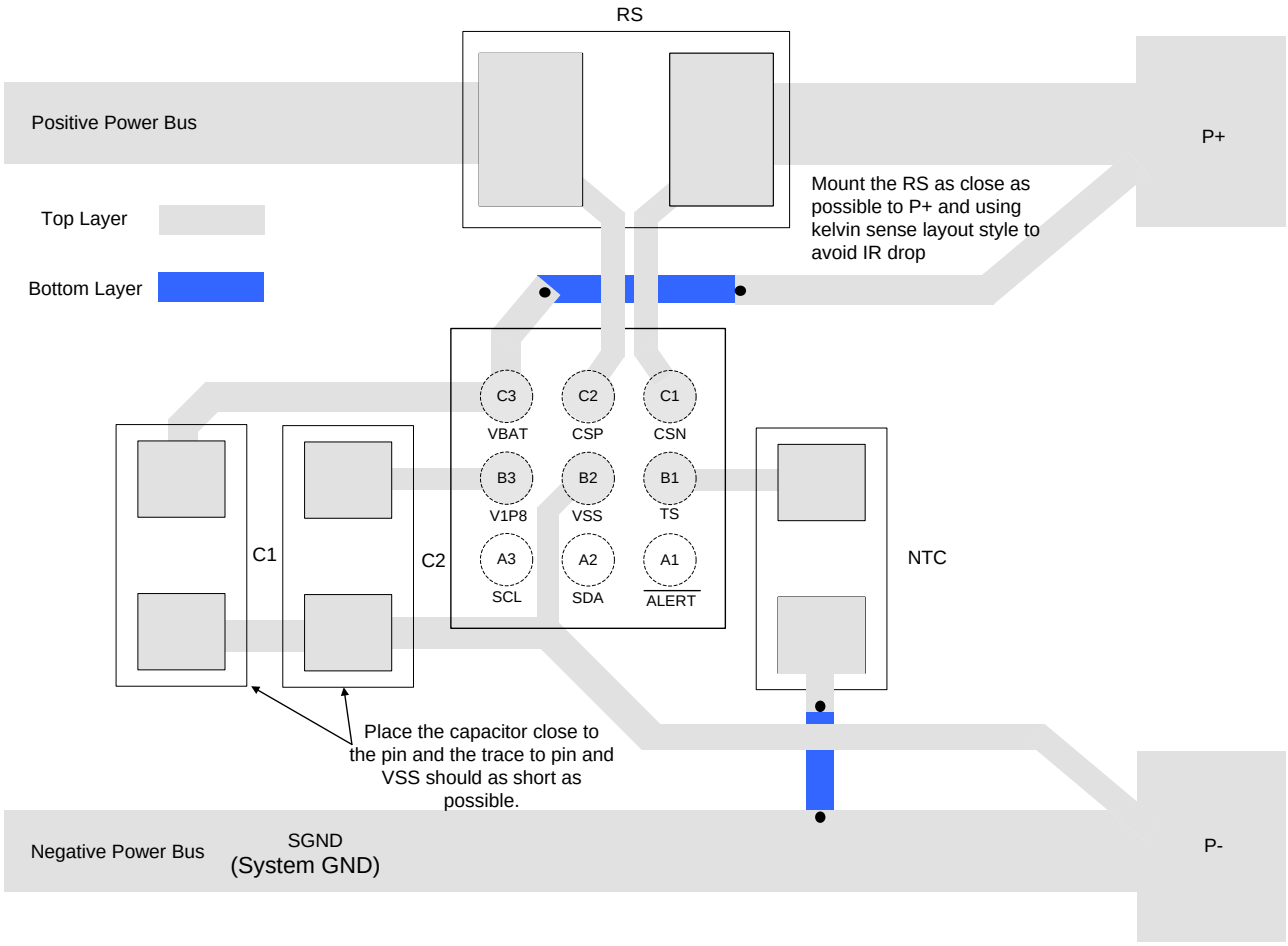


Figure 4. High-Side Sensing PCB Layout Guide for WL-CSP-9B 1.68x1.81 (BSC) Package

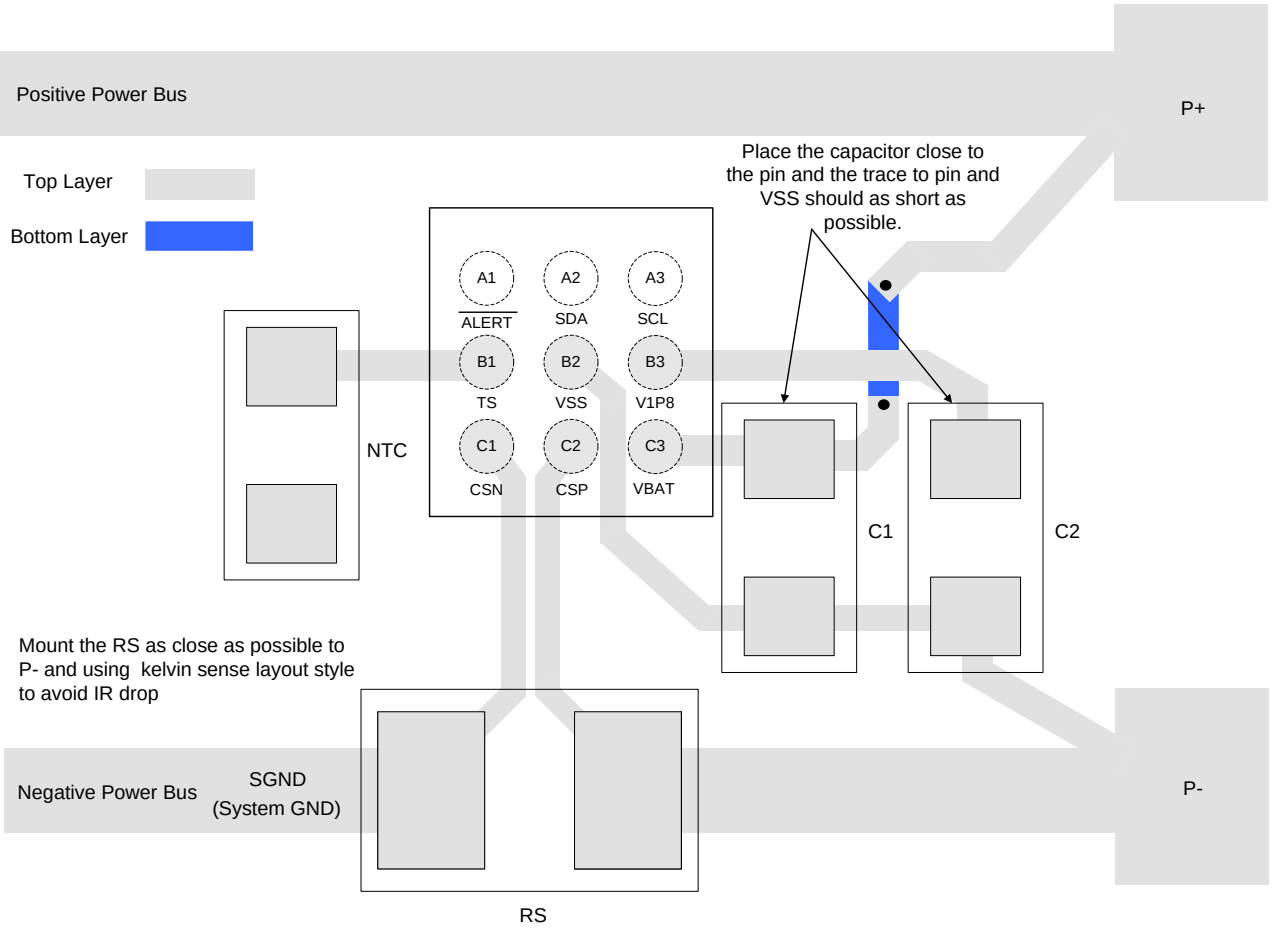


Figure 5. Low-Side Sensing PCB Layout Guide for WL-CSP-9B 1.68x1.81 (BSC) Package

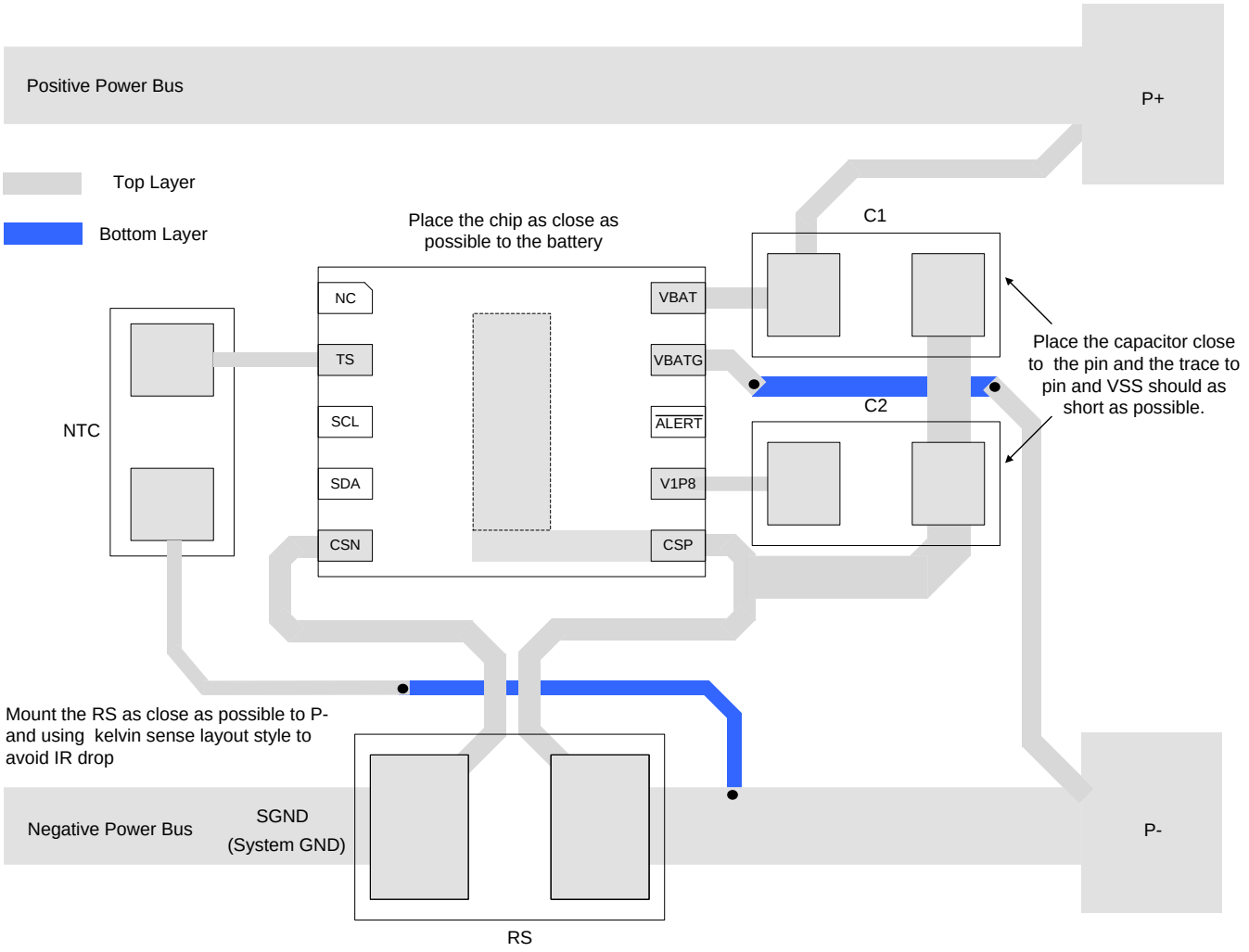
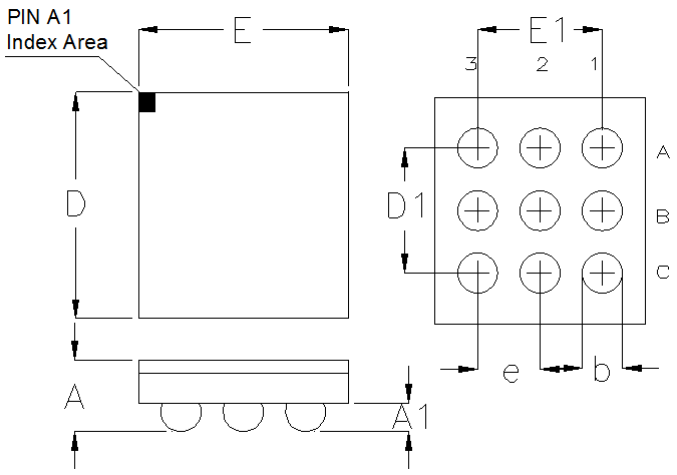


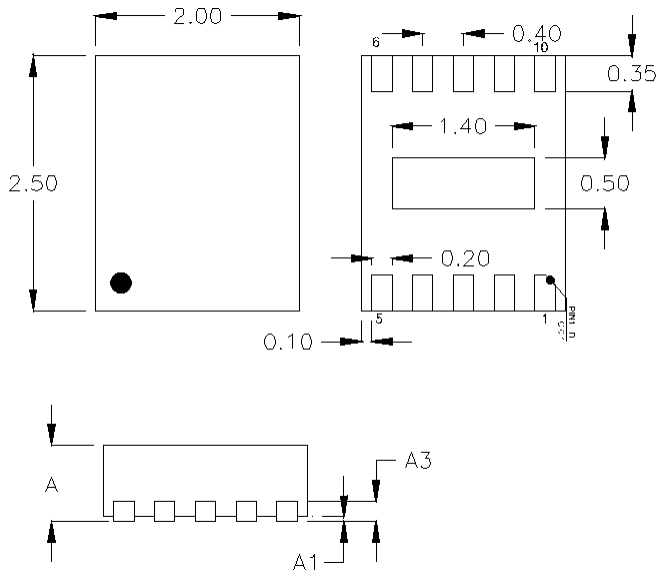
Figure 6. Low-Side Sensing PCB Layout Guide for WDFN-10L 2x2.5 (FC) Package

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.525	0.625	0.021	0.025
A1	0.200	0.260	0.008	0.010
b	0.290	0.350	0.011	0.014
D	1.770	1.850	0.070	0.073
D1	1.000		0.039	
E	1.640	1.720	0.065	0.068
E1	1.000		0.039	
e	0.500		0.020	

9B WL-CSP 1.68x1.81 Package (BSC)

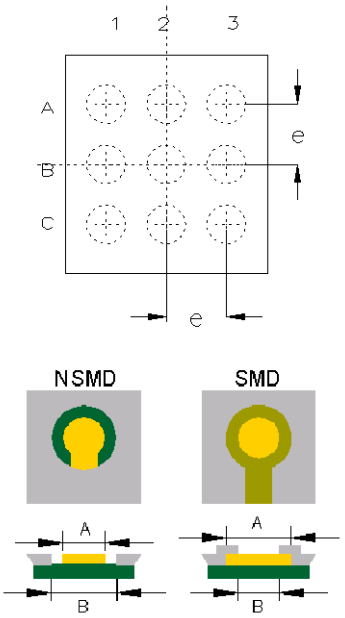


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

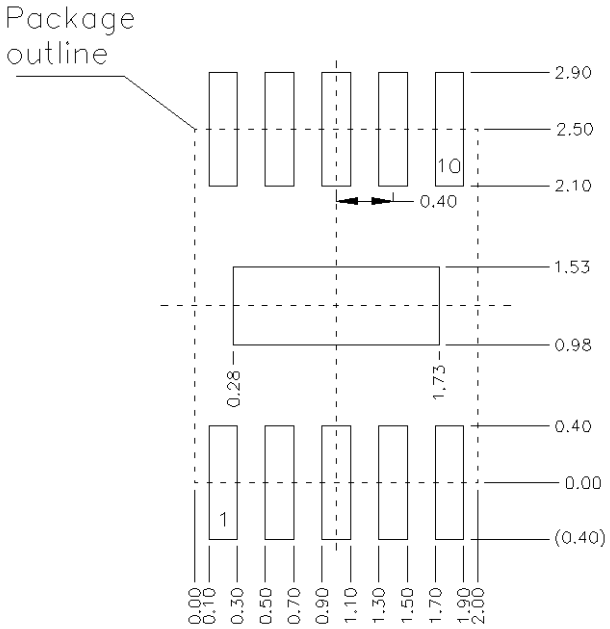
Tolerance
±0.050

W-Type 10L DFN 2x2.5 Package (FC)

Footprint Information



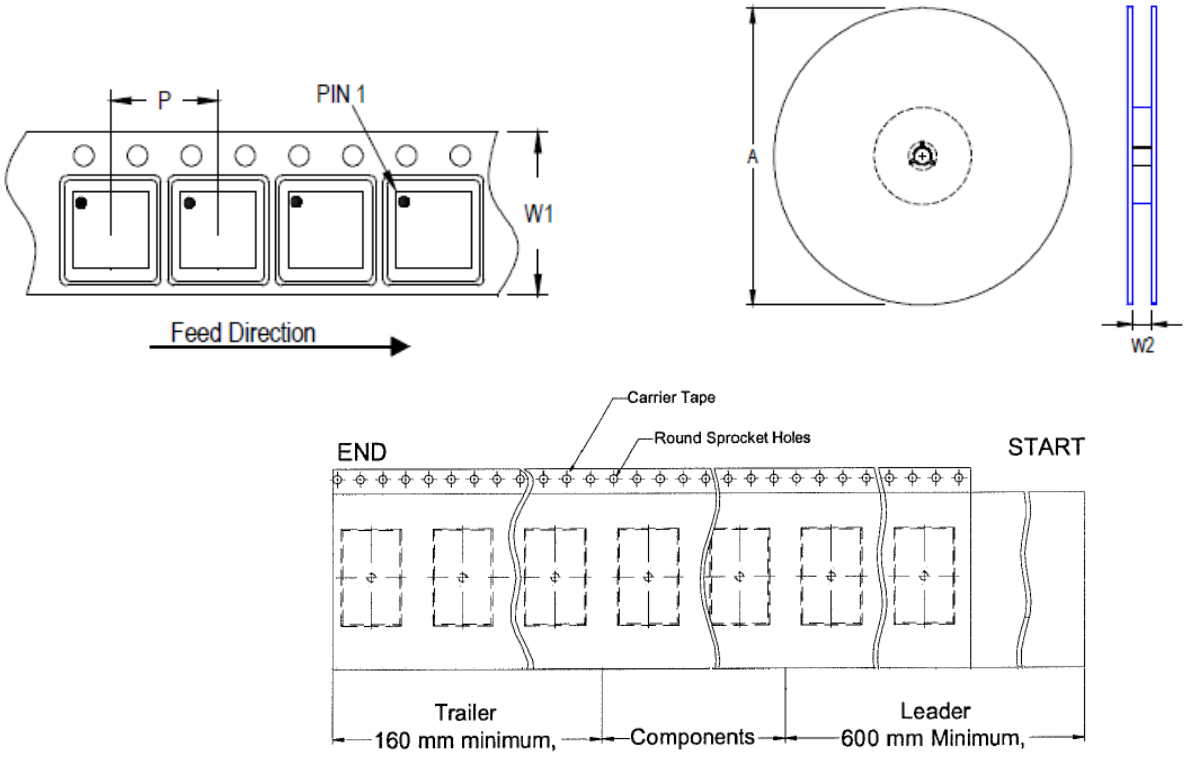
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.68x1.81-9(BSC)	9	NSMD	0.500	0.275	0.375	±0.025
		SMD		0.305	0.275	



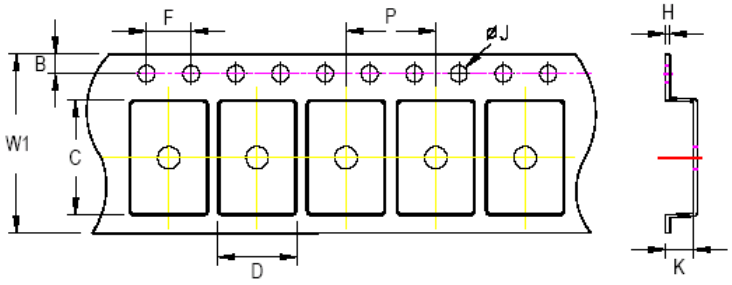
Package	Number of Pin	Tolerance
V/W/U/XDFN2x2.5-10(FC)	10	±0.05

Packing Information

Tape and Reel Data (WL-CSP 1.68x1.81)



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 1.68x1.81	8	4	180	7	3,000	160	600	8.4/9.9

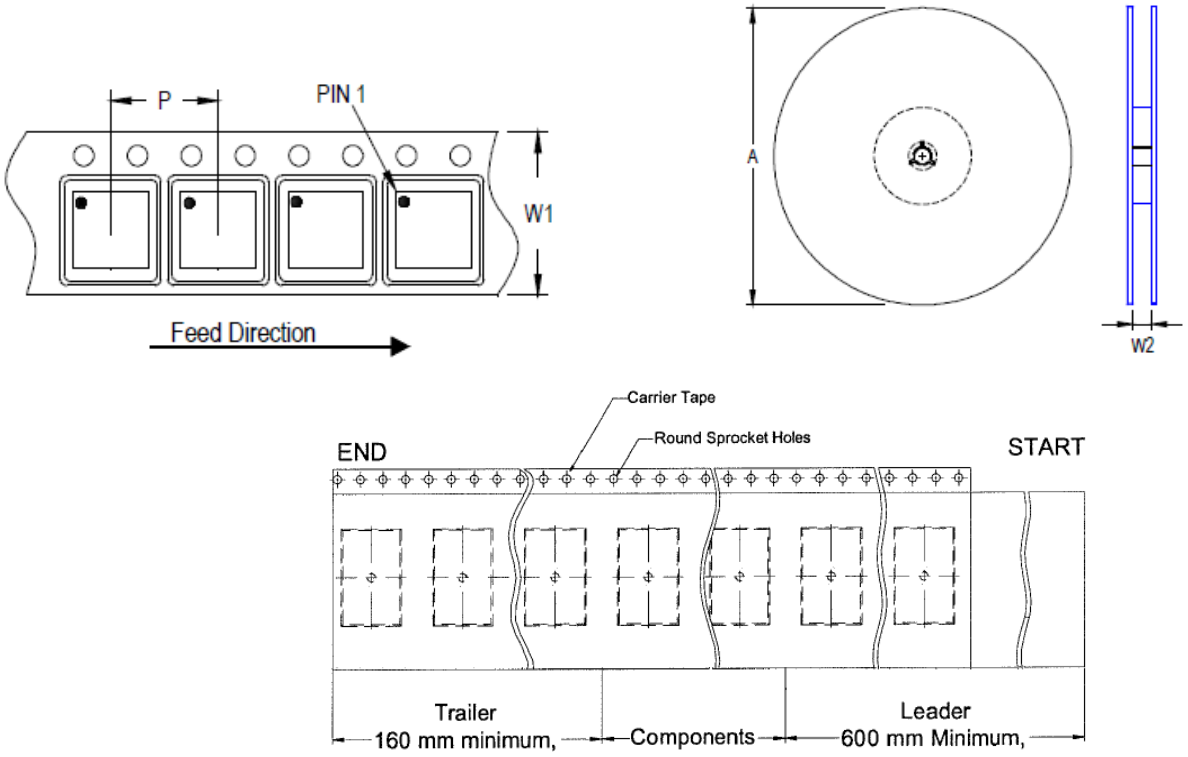


C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

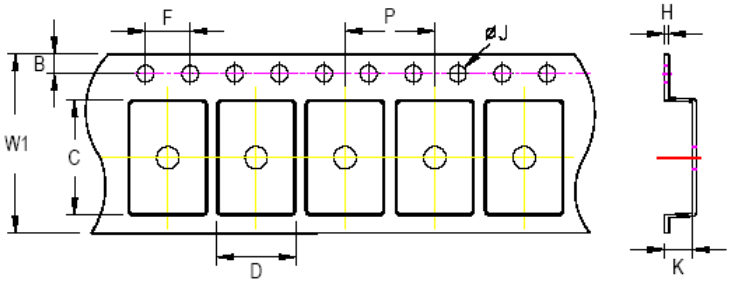
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Data (QFN/DFN 2x2.5)



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 2x2.5	12	8	180	7	1,500	160	600	12.4/14.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing (WL-CSP 1.68x1.81)

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
WL-CSP 1.68x1.81	7”	3,000	Box A	18.3*18.3*8.0	3	9,000	Carton A	38.3*27.2*38.3	12	108,000
			Box E	18.6*18.6*3.5	1	3,000	For Combined or Partial Reel.			

Tape and Reel Packing (QFN/DFN 2x2.5)

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN & DFN 2x2.5	7”	1,500	Box A	18.3*18.3*8.0	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	1	1,500	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
00	2023/1/17	Final	Packing Information on P26 to P30