MOSFET Integrated Smart Photoflash Capacitor Charger with IGBT Driver

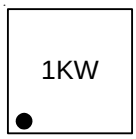
General Description

The RT9598 is a complete photoflash module solution for digital and film cameras. It is targeted for applications that use 2 to 4 AA batteries or 1 to 2 Lithium-Ion batteries. The RT9598 adopts Flyback topology which uses constant primary peak current and zero secondary valley current to charge photoflash capacitor quickly and efficiently. The built-in 55V MOSFET allows flexibility in transformer design and simplifies the PCB layout. The RT9598 also integrates an IGBT driver for igniting photoflash tube. Only a few external components are required, which greatly reduces the PCB space and cost. The RT9598 is available in the WDFN-8L 2x2 package.

Features

- **55V MOSFET Integrated**
- **Charge any Size Photoflash Capacitor**
- **Adjustable Input Current**
- **Adjustable Output Voltage**
- **Charge Complete Indicator**
- **Built-In IGBT Driver for IGBT Application**
- **Constant Peak Current Control**
- **Over-Voltage Protection**
- **Maximum On-Time Protection**
- **8-Lead WDFN Package**
- **RoHS Compliant and Halogen Free**

Marking Information



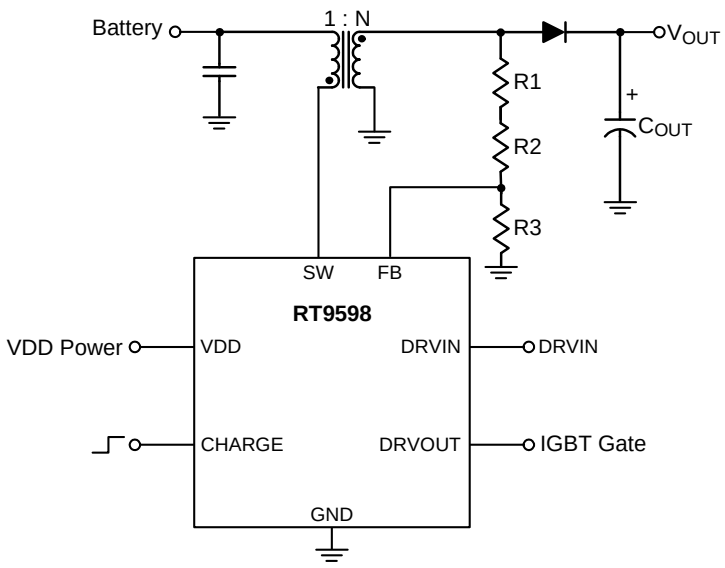
1K : Product Code

W : Date Code

Applications

- Digital Still Camera
- Film Camera Flash Unit
- Camera Phone Flash

Simplified Application Circuit



Ordering Information

RT9598□□

- Package Type
  QW : WDFN-8L 2x2 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

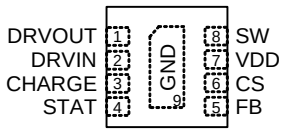
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)

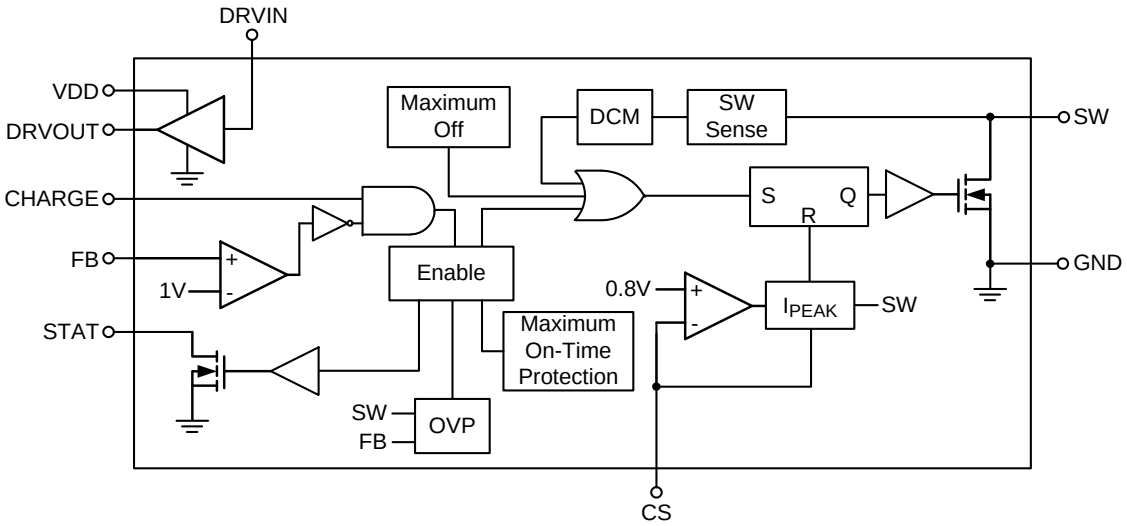


WDFN-8L 2x2

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	DRVOUT	IGBT Driver Output.
2	DRVIN	IGBT Driver Input.
3	CHARGE	Charge Enable Control Input. The charge function is executed when CHARGE pin is set from Low to High. The chip is in Shutdown mode when CHARGE pin is set to Low.
4	STAT	Charge Status Open-Drain Output. When target output voltage is reached, this pin will be pulled low. This pin needs a pull-up resistor.
5	FB	Feedback Voltage Input.
6	CS	Input Current Setting.
7	VDD	Supply Voltage Input.
8	SW	N-MOSFET Switch Node.
9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Operation

Basic Operation

The RT9598 is a photo flash charger comprised of several building blocks. The following paragraphs are described in detail.

Enable

If the output voltage is below its target voltage, the CHARGE pin pulling high enables charging cycle and pulling low stops charging. When the output voltage reaches the target voltage, the MOSFET will be turned off and the STAT pin will be pulled low to indicate that charging is completed.

Peak Current Control

The MOSFET peak current is set by an external resistor on the CS pin.

DCM

The RT9598 uses DCM operation mechanism to decide the timing to turn on MOSFET. This block senses transformer's secondary current through the SW pin. When the current drops to zero, the energy is delivered to output, and the MOSFET will turn on for next cycle.

Maximum Off-Time

During pre-charge, a 9µs maximum off-time is used to reduce the charging time.

Maximum On-Time Protection

If the on-time of the internal MOSFET is over 2ms, the maximum on-time protection will be triggered to shut down the charging system.

OVP Protection

The over-voltage protection supervises the abnormal voltage via the FB and SW pins. If OVP occurs, the internal MOSFET will turn off immediately.

IGBT Driver

The DRVOUT is used to trigger flash tube module when HV capacitor is charged ready. It also equips with false trigger protection when VDD is low or the STAT pin is not at low status.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VDD ---------- –0.3V to 6V
- Built-in N-Channel Enhancement MOSFET
  - Drain-Source Voltage ---------- –0.3V to 55V
  - CS, CHARGE, DRVIN, DRVOUT, STAT, FB ---------- –0.3V to 6V
  - SW Pulse Current (Pulse Width 1μs) ---------- 4A
  - SW Continuous Current ---------- 2A
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-8L 2x2 ---------- 2.19W
- Package Thermal Resistance (Note 2)
  - WDFN-8L 2x2, θ_{JA} ---------- 45.5°C/W
  - WDFN-8L 2x2, θ_{JC} ---------- 11.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV
  - MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, VDD ---------- 2.9V to 5.5V
- Battery Voltage ---------- 1.6V to 9V
- Drain Source Voltage ---------- 50V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switch Off Current	$I_{VDD\_SW\_OFF}$	V_{FB} = 1.1V	--	1	10	μA
Shutdown Current	I_{OFF}	CHARGE pin = 0V	--	0.1	1	μA
FB Voltage	V_{FB}		0.985	1	1.015	V
Line Regulation	$\lvert \Delta V_{FB} \rvert$	2.9V < V_{DD} < 5.5V	--	--	10	mV
STAT Open Drain $R_{DS(ON)}$			--	11	19	Ω
Charge Enable High	V_{CEH}		1.3	--	--	V
Charge Enable Low	V_{CEL}		--	--	0.4	V
Built-In N-Channel Enhancement MOSFET						
Drain-Source On-Resistance	$R_{DS(ON)}$	V_{DD} = 3.3V, I_D = 10mA	--	0.3	0.4	Ω
Maximum Off-Time During Pre-Charge			--	7	--	μs
Minimum Off-Time			--	400	--	ns
Maximum On-time Protection		V_{DD} = 3.3V	1	1.5	2	ms
		V_{DD} = 5V	1	1.5	2	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IGBT Driver						
DRVIN Trip Point		V_{DD} = 3.3V to 5V	0.8	1.05	1.4	V
DRVOUT On-Resistance to V_{DD}		V_{DD} = 3.3V	5	10	15	Ω
DRVOUT On-Resistance to GND		V_{DD} = 3.3V	10	16	22	Ω
Propagation Delay (Rising)	T_{PD_R}	V_{DD} = 5V	--	11	20	ns
		V_{DD} = 3.3V	--	13.5	20	
Propagation Delay (Falling)	T_{PD_F}	V_{DD} = 5V	50	110	200	ns
		V_{DD} = 3.3V	40	70	120	

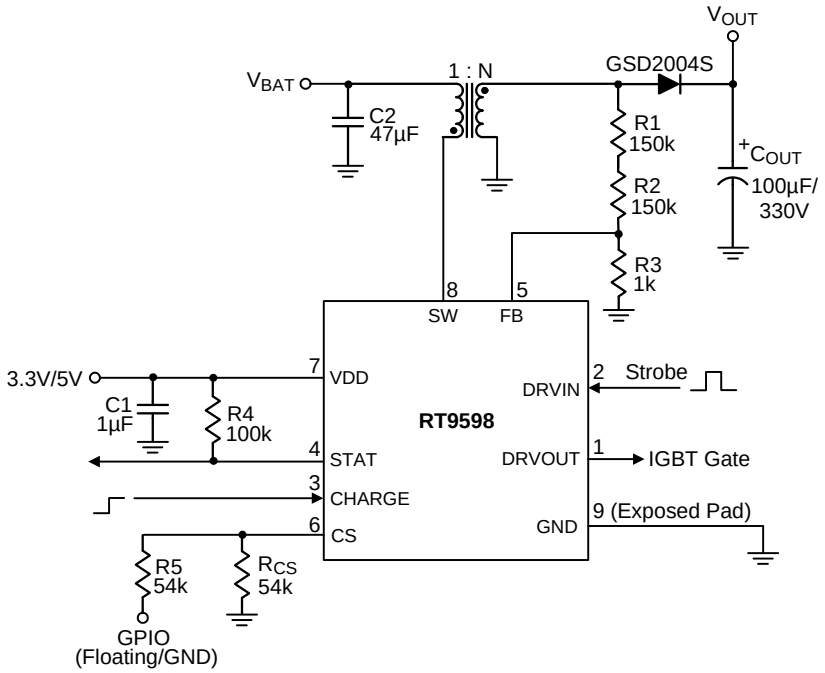
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

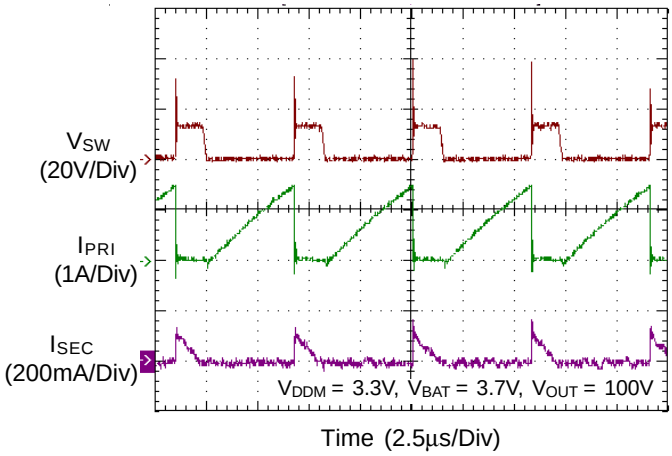
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

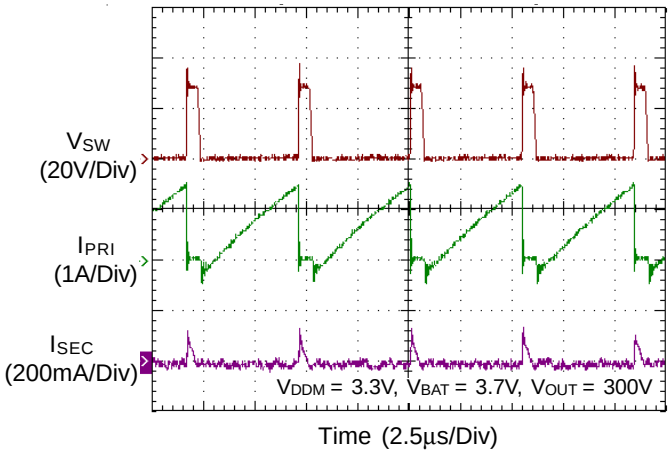


Typical Operating Characteristics

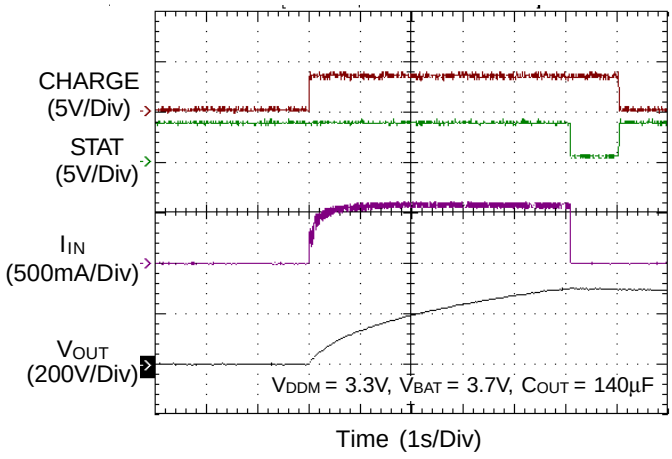
Switching



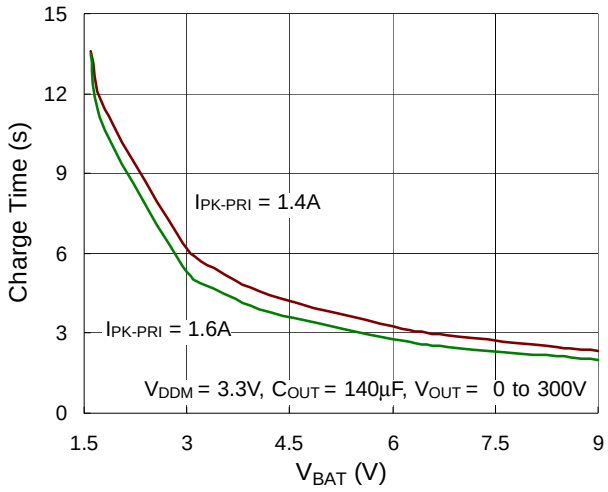
Switching



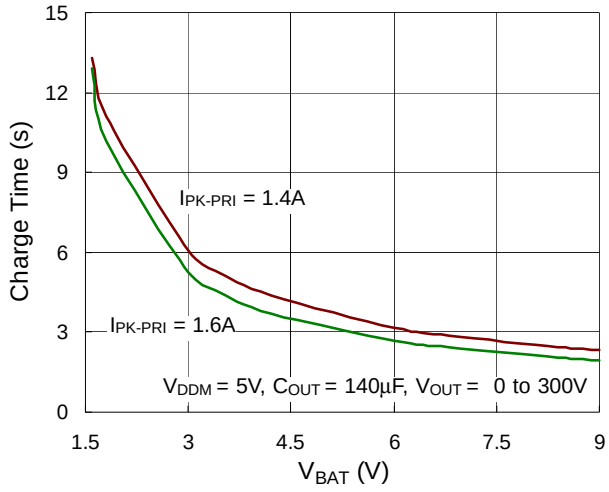
Charging Time



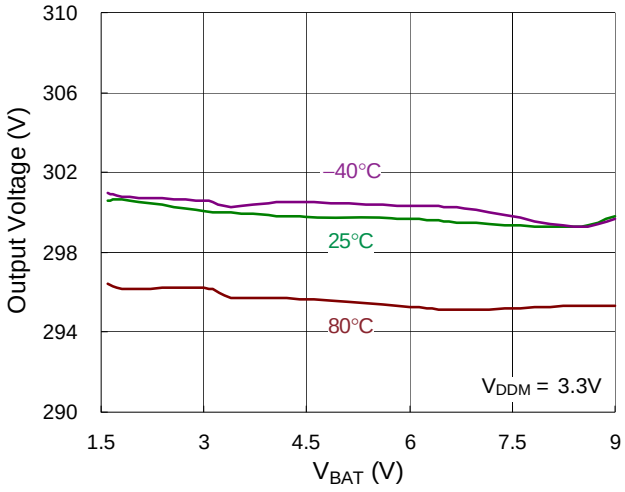
Charge Time vs. V_{BAT}



Charge Time vs. V_{BAT}



Output Voltage vs. V_{BAT}



Application Information

The RT9598 integrates a constant peak current controller for charging photoflash capacitor and an IGBT driver for igniting flash tube. The photoflash capacitor charger uses constant primary peak current and SW falling control to efficiently charge the photoflash capacitor.

Pulling the CHARGE pin high will initiate the charging cycle. However, the CHARGE signal must go from low to high after V_{DD} > 2V for at least 1μs delay time.

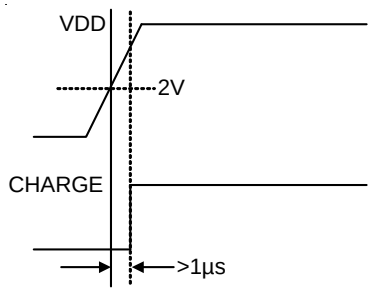


Figure 1. Recommend Charge Timing Chart

During MOSFET on-period, the primary current ramps up linearly according to V_{BAT} and primary inductance. A resistor connecting from the CS pin to GND determines the primary peak current.

During the MOSFET off-period, the energy stored in the Flyback transformer is boosted to the output capacitor. The secondary current decreases linearly at a rate determined by the secondary inductance and the output voltage (neglecting the voltage drop of the diode).

The SW pin monitors the secondary current. When the secondary current drops to 0A, SW voltage falls, and then the MOSFET on-period starts again. The charging cycle repeats itself and charges the output capacitor. The output voltage is sensed by a voltage divider connecting to the anode of the rectifying diode. When the output voltage reaches the desired voltage set by the resistor divider, the charging block will be disabled and charging will be stopped.

Then STAT pin will be pulled low to indicate complete charging.

The voltage sensing path will be cut off when charging is completed to minimize the output voltage decay. Both the CHARGE and STAT pins can be easily interfaced to a microprocessor in a digital system.

Charge Current Setting

The RT9598 simply adjusts peak primary current by a resistor R_{CS} connecting to the CS pin as shown in the Function Block Diagram. R_{CS} determines the peak current of the primary N-MOSFET according to the following equation :

$$I_{PK\_PRI} = \frac{40000}{R_{CS}} \quad (A)$$

where I_{PK-PRI} is the primary peak current. Users could select appropriate R_{CS} according to the battery capability and required charging time. We recommend RCS should be greater than 13kΩ.

Transformer

The Flyback transformer should be appropriately designed to ensure effective and efficient operation.

1. Turns Ratio

The turns ratio of transformer (N) should be high enough so that the absolute maximum voltage rating for the internal N-MOSFET Drain to Source voltage is not exceeded. Choose the minimum turns ratio according to the following formula :

$$N_{MIN} \geq \frac{V_{OUT}}{50 - V_{BAT}}$$

Where :

V_{OUT} : Target Output Voltage

V_{BAT} : Battery Voltage

2. Primary Inductance

Each switching cycle, energy transferred to the output capacitor is proportional to the primary inductance for a constant primary current. The higher the primary inductance, the higher the charging efficiency. Besides, to ensure enough off-time for the output voltage sensing, the primary inductance should be high enough according to the following formula :

$$L_{PRI} \geq \frac{400 \times 10^{-9} \times V_{OUT}}{N \times I_{PK\text{-}PRI}}$$

V_{OUT} : Target Output Voltage

N : Transformer turns ratio

I_{PK-PRI} : Primary peak current

3. Leakage Inductance

The leakage inductance of the transformer results in the first spike voltage when N-MOSFET turns off. The spike voltage is proportional to the leakage inductance and inductor peak current. The spike voltage must not exceed the dynamic rating of the N-MOSFET Drain to Source voltage (50V).

4. Transformer Secondary Capacitance

Any capacitance on the secondary can severely affect the efficiency. A small secondary capacitance is multiplied by N^2 when reflected to the primary side, so the equiralent capacitance will become large.

This capacitance forms a resonant circuit with the primary leakage inductance of the transformer. Therefore, both the primary leakage inductance and secondary side capacitance should be minimized.

Rectifying Diode

The rectifying diode should be with short reverse recovery time (small parasitic capacitance). Large parasitic capacitance increases switching loss and lowers charging efficiency.

In addition, the peak reverse voltage and peak current of the diode should be sufficient.

The peak reverse voltage of the diode can be calculated as the following equation :

$$V_{PK-R} \approx V_{OUT} + (N \times V_{BAT})$$

The peak current of the diode is equal to the primary peak current divided by the transformer turn ratio as the following equation :

$$I_{PK-SEC} = \frac{I_{PK-PRI}}{N}$$

Where : N is the transformer turns ratio.

Output Voltage Setting

The RT9598 senses the output voltage by a voltage divider connecting to the anode of the rectifying diode during off-time as shown in Figure 2. This eliminates power loss at voltage sensing circuit when charging is completed. R1 to R2 ratio determines the output voltage as shown in the typical application circuit. The feedback reference voltage is 1V.

If V_{OUT} = 300V, according the following equation :

$$V_{OUT} = V_{FB} \times (1 + \frac{R1+R2}{R3}) \text{ and } \frac{R1+R2}{R3} = 299$$

It is recommended to set R3 = 1kΩ and R1 = R2 = 150kΩ for reducing parasitic capacitance coupling effect of the FB pin. R1 and R2 ***MUST*** be larger than 0805 package size for enduring secondary HV. Another sensing method is to sense the output voltage directly as shown in Figure 3.

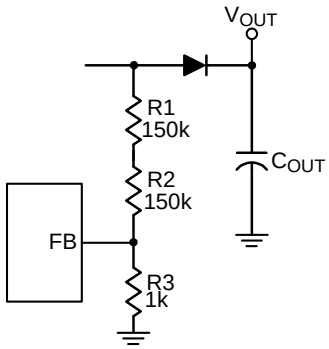


Figure 2. Sensing Anode of Diode

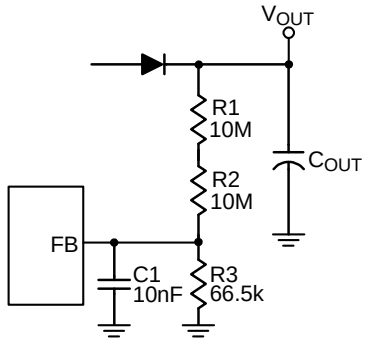


Figure 3. Sensing Output Voltage

Over-Voltage Protection (OVP)

The RT9598 provides an Over-Voltage Protection (OVP) function. In the typical application circuit, if the FB resistor R1, R2 or R3 is open, the FB voltage will be pulled low or floating. In this condition, when the CHARGE pin goes high, the RT9598 begins switching. When the SW voltage reaches 14V, the OVP function will be triggered.

False Triggering Prevention

The RT9598 includes a mechanism to prevent false triggering of the DRVOUT pin while the device is still in charging mode.

With this mechanism, the DRVIN pin is only allowed to trigger DRVOUT when the CHARGE pin is low.

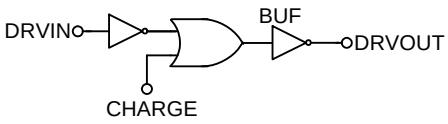


Figure 4. Trigger Logic

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WDFN-8L 2x2 package, the thermal resistance θ_{JA} is 45.5°C/W on the standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (45.5°C/W) = 2.19W for WDFN-8L 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

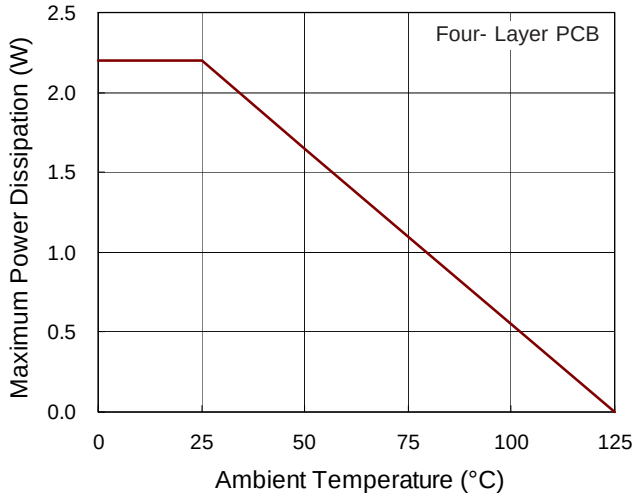


Figure 5. Derating Curve of Maximum Power Dissipation

Layout Considerations

For the best performance of the RT9598, the following PCB layout guidelines must be strictly followed.

- Both of primary and secondary power paths should be as short as possible.
- Place the current setting resistor R_{CS} to the CS pin as close as possible. The GND side of R_{CS} should be directly connected to ground plane to avoid noise coupling.
- Keep the switching node area as small as possible to reduce parasitic capacitance coupling effect.
- Place the feedback resistors as close as possible to the FB pin.
- The GND should be connected to a strong ground plane to reduce switching noise.

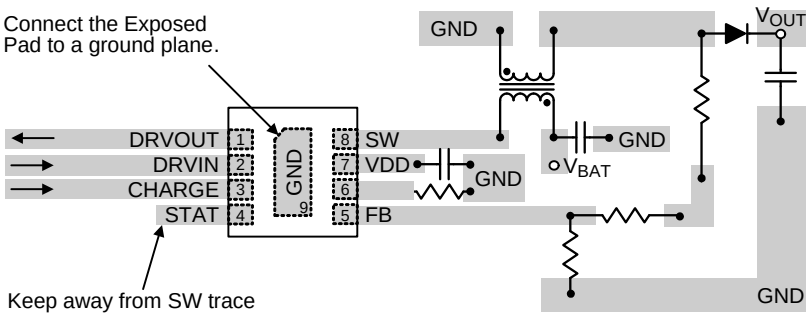
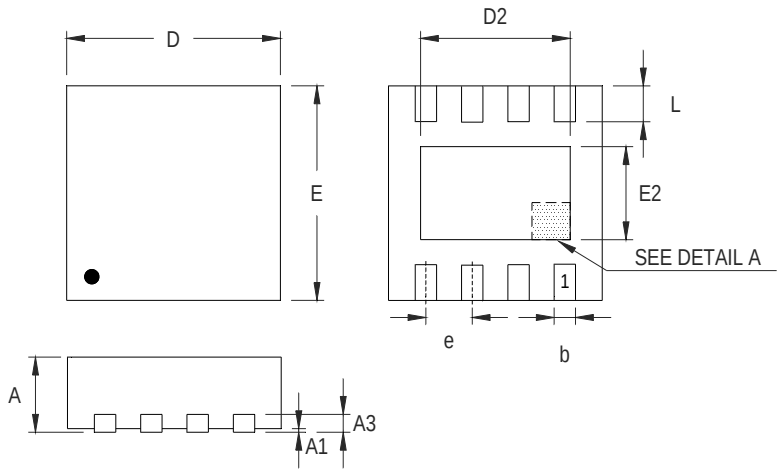
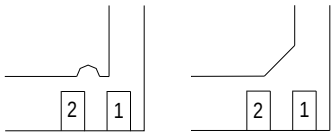


Figure 6. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 8L DFN 2x2 Package

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