Single Phase Synchronous Rectified Buck MOSFET Driver

General Description

The RT9614C is a high performance, synchronous rectified, single phase MOSFET driver designed for general MOSFET driving applications and high performance CPU VR driving capabilities.

The RT9614C can be supplied from 4.5V to 13.2V. The applicable power stage VIN range is from 5V to 24V. The RT9614C also builds in an internal power switch to replace external bootstrap diode.

The RT9614C can support switching frequency efficiently up to 500kHz. The RT9614C has both the UGATE and LGATE driving circuits for synchronous rectified DC-DC converter applications. The pre-OVP protection is designed to protect system when output has high voltage and shoot through protection mechanism is designed to prevent shoot through between high side and low side power MOSFETs. The RT9614C has tri-state PWM input with shutdown and EN input shutdown functions, which can force driver to output low UGATE and LGATE signals.

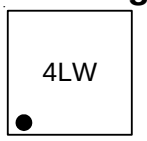
Features

- **Shoot-Through Protection**
- **Embedded Bootstrap Switch**
- **Up to 500kHz Operating Frequency**
- **Fast Rising and Falling Time**
- **Tri-State PWM Input**
- **Enable Control**
- **Pre-OVP Protection**
- **Small 8-Lead WDFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Desktop, Systems
- VGA Card

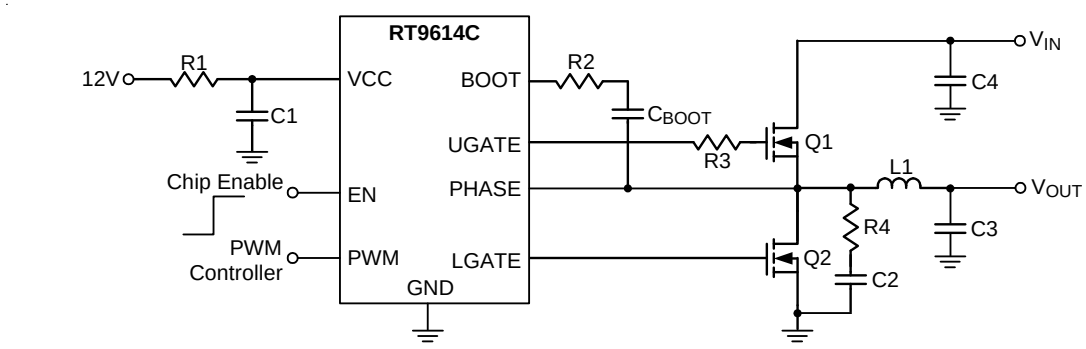
Marking Information



4L : Product Code

W : Date Code

Simplified Application Circuit



Ordering Information

RT9614C□□

Package Type
QW : WDFN-8SL 2x2 (W-Type)
(Exposed Pad-Option 1)

Lead Plating System
G : Green (Halogen Free and Pb Free)

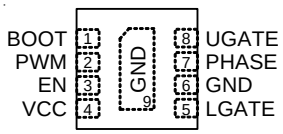
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)

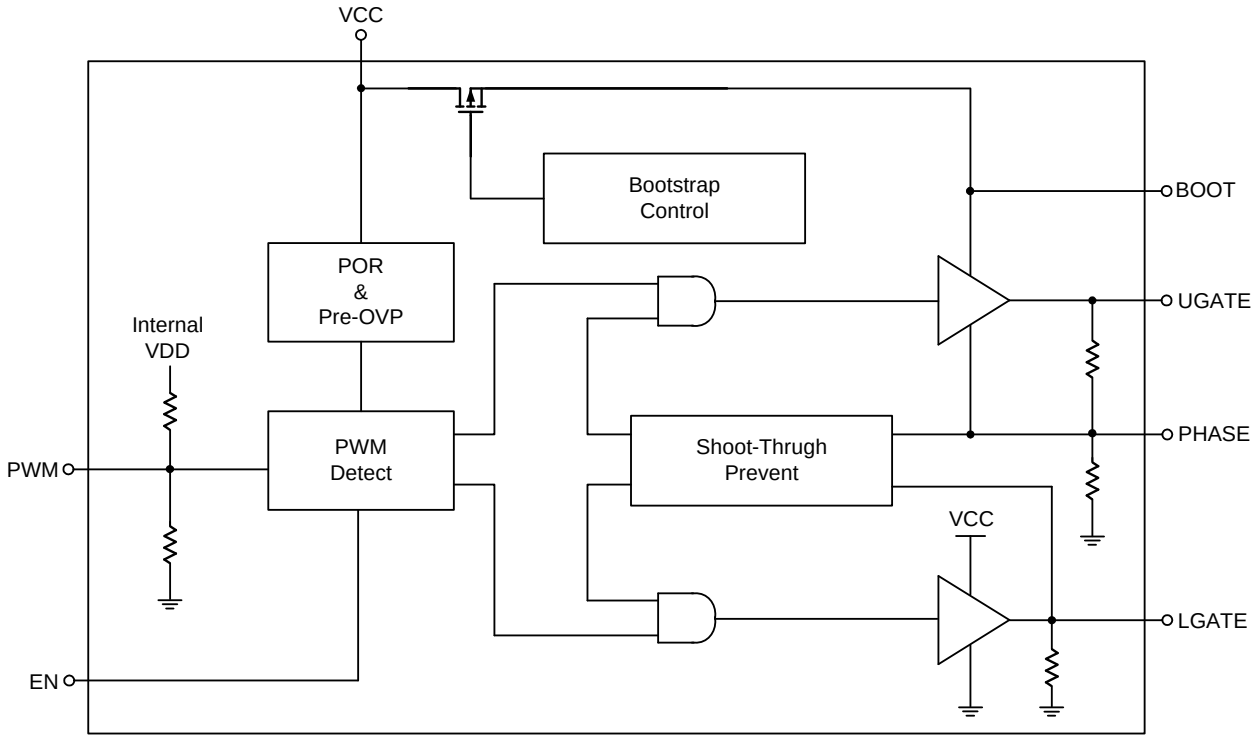


WDFN-8SL 2x2

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap supply for high side gate driver.
2	PWM	PWM signal input. Connect this pin to the PWM output of the controller.
3	EN	Chip enable (Active High). When this pin is low, both UGATE and LGATE are driven to low.
4	VCC	Supply voltage input.
5	LGATE	Low side gate driver output. Connect this pin to the Gate of low side power N-MOSFET.
6, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
7	PHASE	Connect this pin to the source of the high side N-MOSFET and the drain of the low side N-MOSFET.
8	UGATE	High side gate driver output. Connect this pin to the Gate of high side power N-MOSFET.

Functional Block Diagram



Operation

POR & Pre-OVP

POR block detects the voltage at the VCC pin. When the VCC pin voltage is higher than POR rising threshold, POR block output is high. POR output is low when VCC is not higher than POR rising threshold. When the POR block output is high, UGATE and LGATE can be controlled by PWM input voltage. If the POR block output is low, both UGATE and LGATE will be pulled to low.

The Pre-Overvoltage Protection (Pre-OVP) feature is used to protect the load if there is a short across the high-side FET.

PWM Detect

PWM Detect block detects the level of PWM pin and decides to turn on/off UGATE and LGATE. Once the POR and EN are ready then PWM detect block is ready to work. If PWM is higher than rising threshold then UGATE is pulled to BOOT and LGATE is pulled to ground. If PWM is lower than falling threshold then UGATE is pulled to PHASE and LGATE is pulled to VCC.

Bootstrap Control

Bootstrap control block controls the integrated bootstrap switch. When LGATE is high (low side MOSFET is turned on), the bootstrap switch is turned on to charge the bootstrap capacitor connected to BOOT pin. When LGATE is low (low side MOSFET is turned off), the bootstrap switch is turned off to disconnect VCC pin and BOOT pin.

Shoot-Through Protection

Shoot-through protection block implements the dead time when both high side and low side MOSFETs are turned off. With shoot-through protection block, high side and low side MOSFET are never turned on simultaneously. Thus, shoot-through between high side and low side MOSFETs is prevented.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VCC ---------- –0.3V to 15V
- BOOT to PHASE
  - DC ---------- –0.3V to 15V
  - < 20ns ---------- –3V to 25V
- BOOT to GND
  - DC ---------- –0.3V to 45V
  - < 20ns ---------- –20V to 46V
- PHASE to GND
  - DC ---------- –0.3V to 30V
  - < 20ns ---------- –20V to 31V
- UGATE to PHASE
  - DC ---------- –0.3V to 15V
  - < 20ns ---------- –3V to 25V
- UGATE to GND
  - DC ---------- –0.3V to 30V
  - < 20ns ---------- –20V to 31V
- LGATE to GND
  - DC ---------- –0.3V to 15V
  - < 20ns ---------- –3V to 16V
- EN, PWM to GND ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-8SL 2x2 ---------- 2.17W
- Package Thermal Resistance (Note 2)
  - WDFN-8SL 2x2, θ_{JA} ---------- 46°C/W
  - WDFN-8SL 2x2, θ_{JC} ---------- 11.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 1.5kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC ---------- 4.5V to 13.2V
- Input Voltage, (V_{IN} + VCC) ---------- < 35V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Power Supply Voltage	V_{CC}		4.5	--	13.2	V
Power Supply Current	I_{VCC}	V_{BOOT} = 12V, PWM input floating	--	120	--	μA
Power On Reset (POR)						
POR Rising Threshold	V_{POR_R}	V_{CC} rising	--	4	4.4	V
POR Falling Threshold	V_{POR_F}	V_{CC} falling	3	3.5	--	V
EN Input						
EN Rising Threshold	V_{ENH}		--	1.3	1.6	V
EN Falling Threshold	V_{ENL}		0.7	1	--	V
PWM Input						
Maximum Input Current	I_{PWM}	PWM = 0V or 5V	--	160	--	μA
PWM Floating Voltage	V_{PWM_FL}	PWM = open	--	1.8	--	V
PWM Rising Threshold	V_{PWM_RTH}		2.3	2.8	3.2	V
PWM Falling Threshold	V_{PWM_FTH}		0.7	1.1	1.4	V
Timing						
UGATE Rising Time	t_{UGATER}	3nF load	--	25	--	ns
UGATE Falling Time	t_{UGATEF}	3nF load	--	12	--	ns
LGATE Rising Time	t_{LGATER}	3nF load	--	24	--	ns
LGATE Falling Time	t_{LGATEF}	3nF load	--	10	--	ns
UGATE Propagation Delay	$t_{UGATEPDH}$	$V_{BOOT} - V_{PHASE}$ = 12V see timing diagram	--	35	--	ns
	$t_{UGATEPDL}$		--	22	--	
LGATE Propagation Delay	$t_{LGATEPDH}$	See timing diagram	--	30	--	ns
	$t_{LGATEPDL}$	See timing diagram	--	8	--	
EN to PWM Delay	$t_{ENTOPWMDL}$		--	3	--	ns
Tri-State to High Delay	t_{UGPTST}		--	30	--	ns
High to Tri-State Delay	t_{UGSSHD}		--	20	--	ns
Tri-State to Low Delay	t_{LGPTST}		--	42	--	ns
Low to Tri-State Delay	t_{LGSSHD}		--	15	--	ns
Output						
UGATE Drive Source	R_{UGATE_SR}	$V_{BOOT} - V_{PHASE}$ = 12V, I_{Source} = 100mA	--	1.7	--	Ω
UGATE Drive Sink	R_{UGATE_SK}	$V_{BOOT} - V_{PHASE}$ = 12V, I_{Sink} = 100mA	--	1.4	--	Ω
LGATE Drive Source	R_{LGATE_SR}	I_{Source} = 100mA	--	1.6	--	Ω
LGATE Drive Sink	R_{LGATE_SK}	I_{Sink} = 100mA	--	1.1	--	Ω

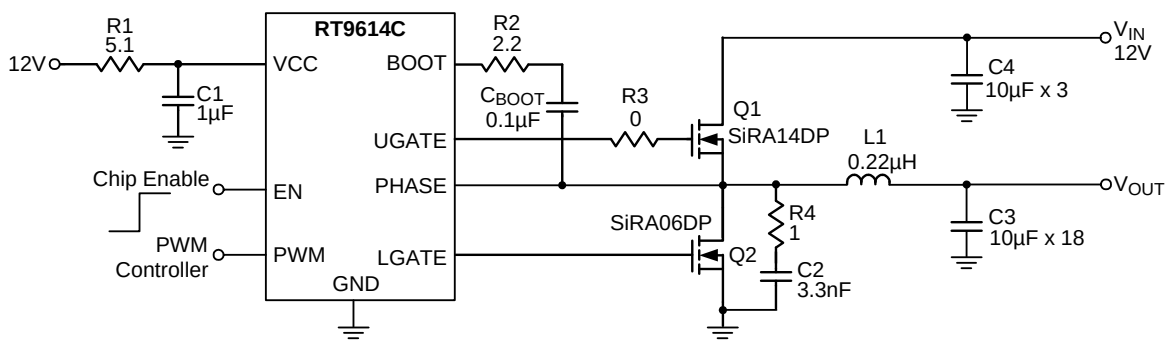
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

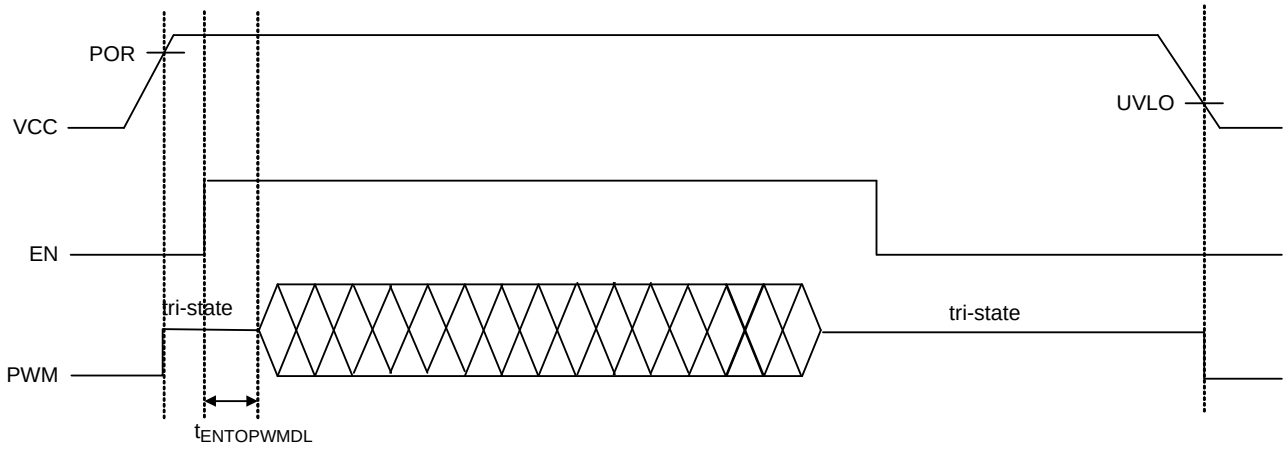
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

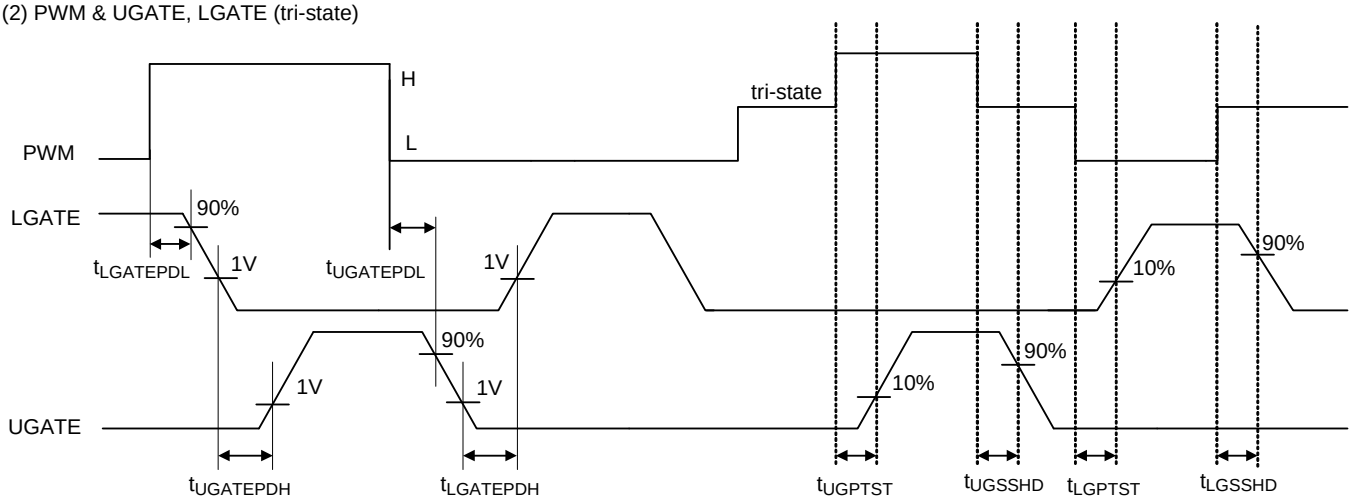


Timing Diagram

(1) VCC & EN & PWM

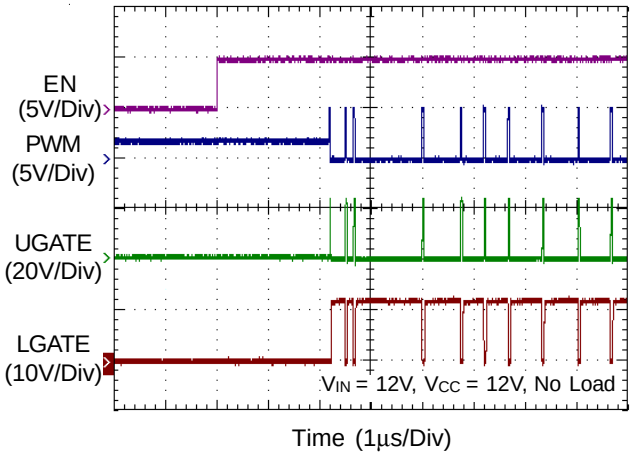


(2) PWM & UGATE, LGATE (tri-state)

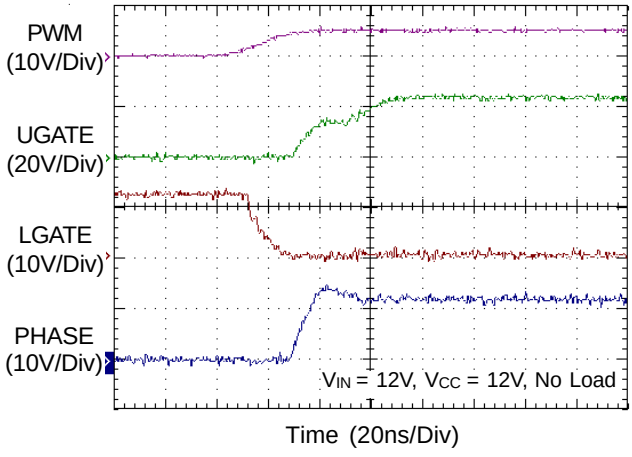


Typical Operating Characteristics

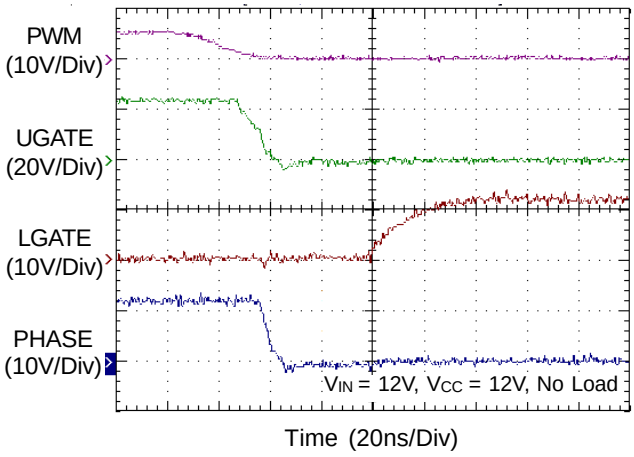
Drive Enable



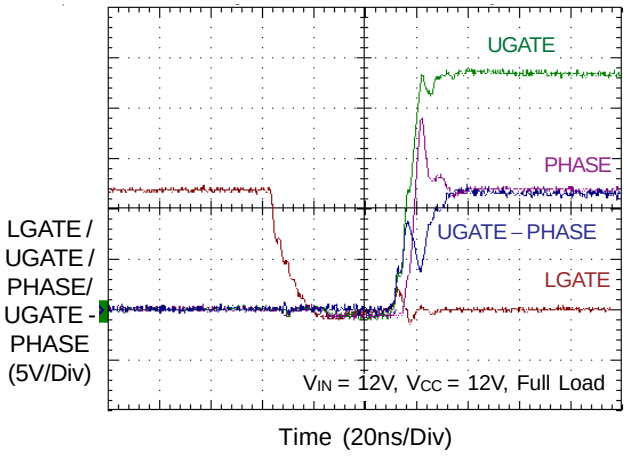
PWM Rising Edge



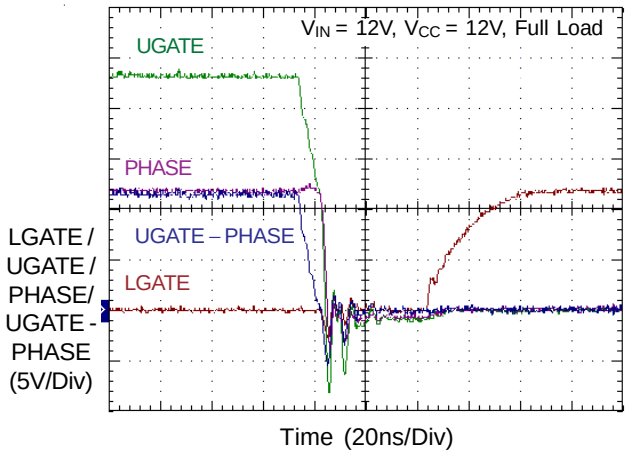
PWM Falling Edge



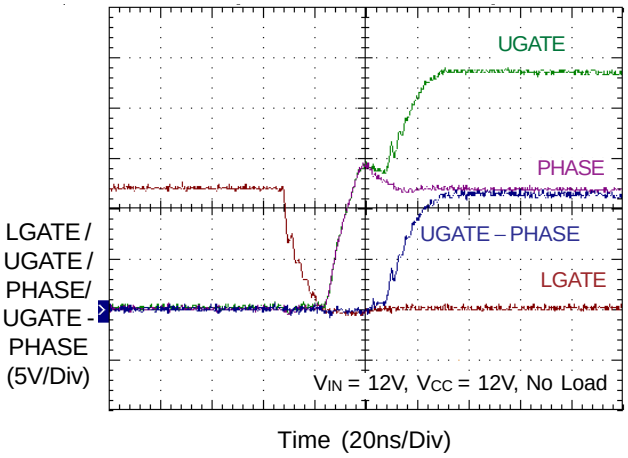
Dead Time



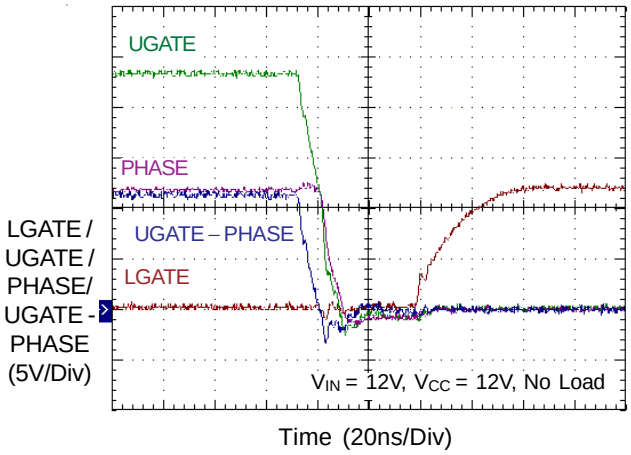
Dead Time



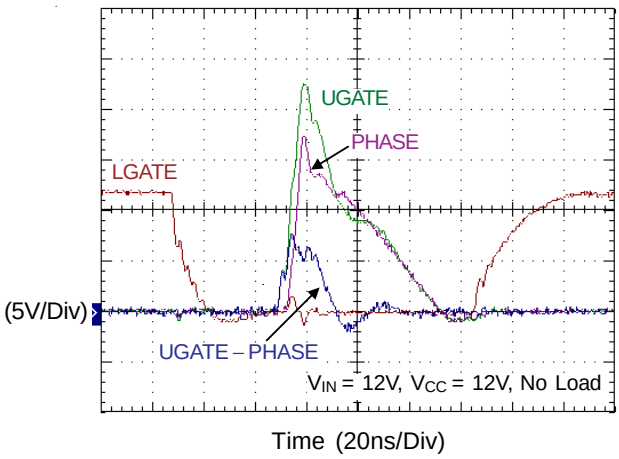
Dead Time



Dead Time



Short Pulse



Application Information

The RT9614C is a high frequency, synchronous rectified, single phase dual MOSFET driver containing Richtek's advanced MOSFET driver technologies. The RT9614C is designed to be able to adapt from normal MOSFET driving applications to high performance CPU VR driving capabilities.

Supply Voltage and Power On Reset

The RT9614C can be utilized under both V_{CC} = 5V or V_{CC} = 12V applications which may happen in different fields of electronics application circuits. In terms of efficiency, higher V_{CC} equals higher driving voltage of UGATE/LGATE which may result in higher switching loss and lower conduction loss of power MOSFETs. The choice of V_{CC} = 12V or V_{CC} = 5V can be a tradeoff to optimize system efficiency.

The RT9614C is designed to drive both high side and low side N-MOSFET through external input PWM control signal. It has power on protection function which held UGATE and LGATE low before the VCC voltage rises to higher than rising threshold voltage.

Pre-Over Voltage Protection

If the RT9614C is powered on but not enabled and PVCC pin is higher than 3V, the PHASE pin will be monitored for Pre-OVP condition. If the PHASE pin is higher than PREOVP threshold, the device will force LGATE pin high to discharge the PHASE voltage.

If the RT9614C operates normally and EN pin is pulled low then UGATE pulled to PHASE and LGATE pulled to GND, the PHASE pin will be monitored for Pre-OVP condition. If the PHASE pin is higher than PREOVP threshold, the device will force LGATE pin high to discharge the PHASE voltage.

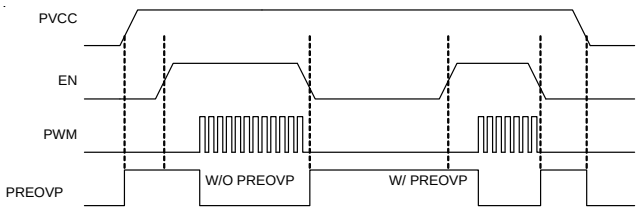


Figure 1. Power-On Sequence

- PREOVP threshold

  2.7V < PREOVP threshold <3V

- Must follow the power-on sequence

  PVCC > PVCC threshold max & must be earlier than EN > EN threshold max

- Driver should connect to Controller

  Driver EN connect to controller DRVEN. In this way, PREOVP can normally work in start-up and PS4

Enable and Disable

The RT9614C includes an EN pin for sequence control. When the EN pin rises above the V_{ENH} trip point, the RT9614C begins a new initialization and follows the PWM command to control the UGATE and LGATE. When the EN pin falls below the V_{ENL} trip point, the RT9614C shuts down and keeps UGATE and LGATE low.

Tri-state PWM Input

After the initialization, the PWM signal takes the control. The rising PWM signal first forces the LGATE signal to turn low then UGATE signal is allowed to go high just after a non-overlapping time to avoid shoot through current. The falling of PWM signal first forces UGATE to go low. When UGATE and PHASE signal reach a predetermined low level, LGATE signal is allowed to turn high.

The PWM signal is acted as "High" if the signal is above the rising threshold and acted as "Low" if the signal is below the falling threshold. When PWM signal level enters and remains within the shutdown window, the output drivers are disabled and both MOSFET gates are pulled and held low. If the PWM signal is left floating, the pin will be kept around 1.8V by the internal divider and provide the PWM controller with a recognizable level.

Internal Bootstrap Power Switch

The RT9614C builds in an internal bootstrap power switch to replace external bootstrap diode, and this can facilitate PCB design and reduce total BOM cost of the system. Hence, no external bootstrap diode is required in real applications.

Non-overlap Control

To prevent the overlap of the gate drivers during the UGATE pull low and the LGATE pull high, the non-overlap circuit monitors the voltages at the PHASE node and high side gate drive (UGATE-PHASE). When the PWM input signal goes low, UGATE begins to pull low (after propagation delay). Before LGATE is pulled high, the non-overlap protection circuit ensures that the monitored voltages have gone below 1.1V. Once the monitored voltages fall below 1.1V, LGATE begins to turn high. By waiting for the voltages of the PHASE pin and high side gate driver to fall below 1.1V, the non-overlap protection circuit ensures that UGATE is low before LGATE pulls high.

Also to prevent the overlap of the gate drivers during LGATE pull low and UGATE pull high, the non-overlap circuit monitors the LGATE voltage. When LGATE goes below 1.1V, UGATE goes high after propagation delay.

Driving Power MOSFETs

The DC input impedance of the power MOSFET is extremely high. When V_{gs1} or V_{gs2} is at 12V or 5V, the gate draws the current only for few nano-amperes. Thus once the gate has been driven up to "ON" level, the current could be negligible.

However, the capacitance at the gate to source terminal should be considered. It requires relatively large currents to drive the gate up and down 12V (or 5V) rapidly. It is also required to switch drain current on and off with the required speed. The required gate drive currents are calculated as follows.

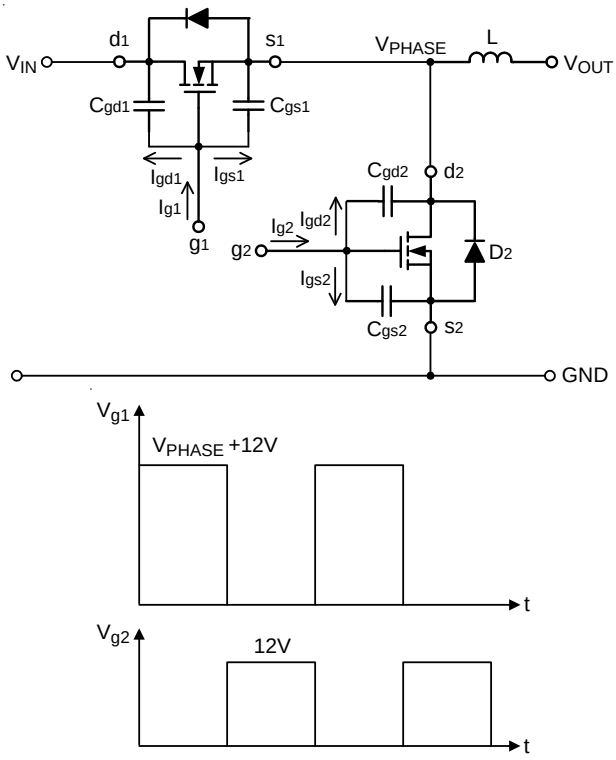


Figure 2. Equivalent Circuit and Waveforms (V_{CC} = 12V)

In Figure 2, the current I_{g1} and I_{g2} are required to move the gate up to 12V. The operation consists of charging C_{gd1}, C_{gd2} , C_{gs1} and C_{gs2}. C_{gs1} and C_{gs2} are the capacitors from gate to source of the high side and the low side power MOSFETs, respectively. In general data sheets, the C_{gs1} and C_{gs2} are referred as "C_{iss}" which are the input capacitors. C_{gd1} and C_{gd2} are the capacitors from gate to drain of the high side and the low side power MOSFETs, respectively and referred to the data sheets as "C_{rss}" the reverse transfer capacitance. For example, t_{r1} and t_{r2} are the rising time of the high side and the low side power MOSFETs respectively, the required current I_{gs1} and I_{gs2}, are shown as below :

$$I_{gs1} = C_{gs1} \frac{dV_{g1}}{dt} = \frac{C_{gs1} \times 12}{t_{r1}} \quad (1)$$

$$I_{gs2} = C_{gs2} \frac{dV_{g2}}{dt} = \frac{C_{gs2} \times 12}{t_{r2}} \quad (2)$$

Before driving the gate of the high side MOSFET up to 12V, the low side MOSFET has to be off; and the high side MOSFET will be turned off before the low side is turned on. From Figure 2, the body diode "D_2" will be turned on before high side MOSFETs turn on.

$$I_{gd1} = C_{gd1}\frac{dV}{dt} = C_{gd1}\frac{12}{t_{r1}} \quad (3)$$

Before the low side MOSFET is turned on, the C_{gd2} have been charged to V_{IN}. Thus, as C_{gd2} reverses its polarity and g_2 is charged up to 12V, the required current is

$$I_{gd2} = C_{gd2}\frac{dV}{dt} = C_{gd2}\frac{V_{IN}+12}{t_{r2}} \quad (4)$$

It is helpful to calculate these currents in a typical case. Assume a synchronous rectified Buck converter, input voltage V_{IN} = 12V, V_{gs1} = 12V, V_{gs2} = 12V. The high side MOSFET is PHB83N03LT whose C_{iss} = 1660pF, C_{rss} = 380pF, and t_r = 14ns. The low side MOSFET is PHB95N03LT whose C_{iss} = 2200pF, C_{rss} = 500pF and t_r = 30ns, from the equation (1) and (2) we can obtain

$$I_{gs1} = \frac{1660 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 1.428 \quad (A) \quad (5)$$

$$I_{gs2} = \frac{2200 \times 10^{-12} \times 12}{30 \times 10^{-9}} = 0.88 \quad (A) \quad (6)$$

from equation. (3) and (4)

$$I_{gd1} = \frac{380 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 0.326 \quad (A) \quad (7)$$

$$I_{gd2} = \frac{500 \times 10^{-12} \times (12+12)}{30 \times 10^{-9}} = 0.4 \quad (A) \quad (8)$$

the total current required from the gate driving source can be calculated as the following equations.

$$I_{g1} = I_{gs1} + I_{gd1} = (1.428 + 0.326) = 1.754 \quad (A) \quad (9)$$

$$I_{g2} = I_{gs2} + I_{gd2} = (0.88 + 0.4) = 1.28 \quad (A) \quad (10)$$

By a similar calculation, we can also get the sink current required from the turned off MOSFET.

Select the Bootstrap Capacitor

Figure 3 shows part of the bootstrap circuit of the RT9614C. The V_{CB} (the voltage difference between BOOT and PHASE on the RT9614C) provides a voltage to the gate of the high side power MOSFET. This supply needs to be ensured that the MOSFET can be driven. For this, the capacitance C_{BOOT} has to be selected properly. It is determined by the following constraints.

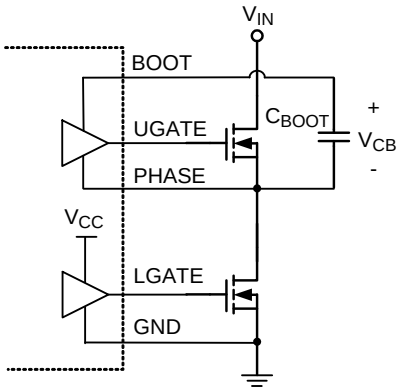


Figure 3. Part of Bootstrap Circuit of RT9614C

In practice, a low value capacitor C_{BOOT} will lead to the over charging that could damage the IC. Therefore, to minimize the risk of overcharging and to reduce the ripple on V_{CB}, the bootstrap capacitor should not be smaller than 0.1µF, and the larger the better. In general design, using 1µF can provide better performance. At least one low-ESR capacitor should be used to provide good local de-coupling. It is recommended to adopt a ceramic or tantalum capacitor.

Power Dissipation

To prevent driving the IC beyond the maximum recommended operating junction temperature of 125°C, it is necessary to calculate the power dissipation appropriately. This dissipation is a function of switching frequency and total gate charge of the selected MOSFET.

Figure 4 shows the power dissipation test circuit. C_L and C_U are the UGATE and LGATE load capacitors, respectively. The bootstrap capacitor value is 1µF.

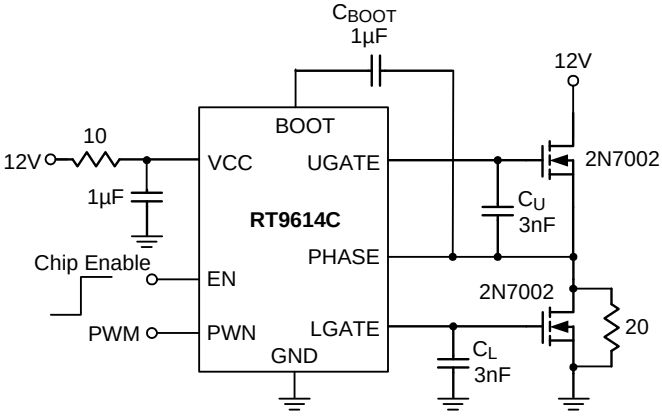


Figure 4. Power Dissipation Test Circuit

Figure 5 shows the power dissipation of the RT9614C as a function of frequency and load capacitance when V_{CC} = 12V. The value of C_U and C_L are the same and the frequency is varied from 100kHz to 1MHz.

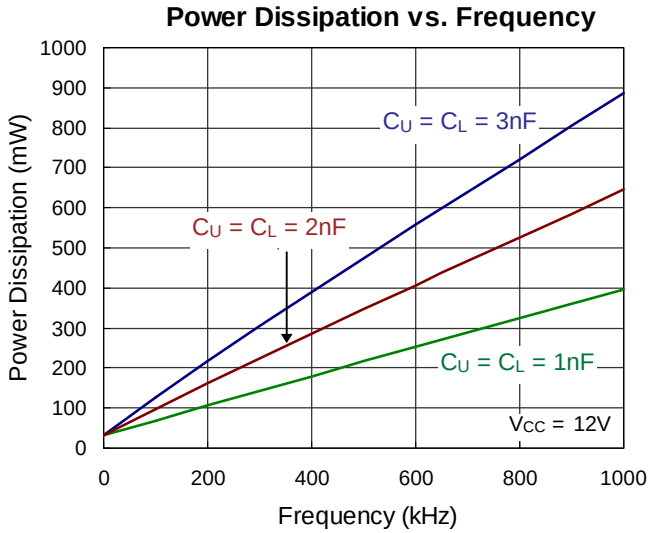


Figure 5. Power Dissipation vs. Frequency

The operating junction temperature can be calculated from the power dissipation curves (Figure 5). Assume V_{CC} = 12V, operating frequency is 200kHz and C_U = C_L = 1nF which emulate the input capacitances of the high side and low side power MOSFETs. From Figure 5, the power dissipation is 100mW. Thus, for example, with the WDFN-8SL 2x2 package, the package thermal resistance θ_{JA} is 46°C/W. The operating junction temperature is then calculated as :

$$T_J = (46°C/W \times 100mW) + 25°C = 29.6°C \quad (11)$$

where the ambient temperature is 25°C.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-8SL 2x2 , the thermal resistance, θ_{JA}, is 46°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (46°C/W) = 2.17W for a WDFN-8SL 2x2 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

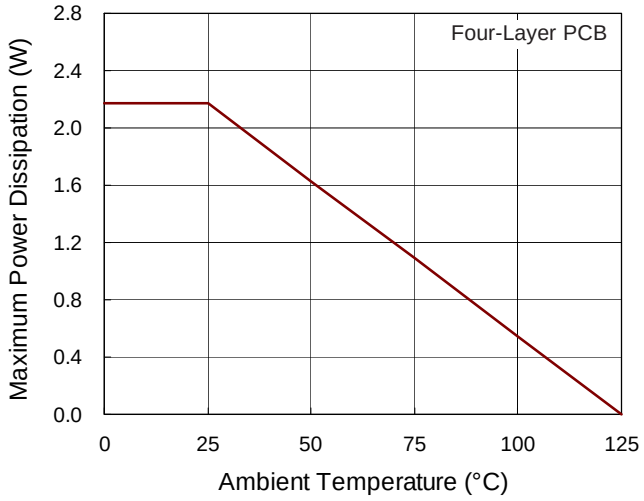


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Consideration

Figure 7 shows the schematic circuit of a synchronous buck converter to implement the RT9614C. The converter operates from 5V to 12V of input Voltage.

For the PCB layout, it should be very careful. The power circuit section is the most critical one. If not configured properly, it will generate a large amount of EMI. The location of Q1, Q2, L1 should be very close.

Next, the trace from UGATE, and LGATE should also be short to decrease the noise of the driver output signals. PHASE signals from the junction of the power MOSFET, carrying the large gate drive current pulses, should be as heavy as the gate drive trace. The bypass capacitor C1 should be connected to GND directly. Furthermore, the bootstrap capacitors (C_{BOOT}) should always be placed as close to the pins of the IC as possible.

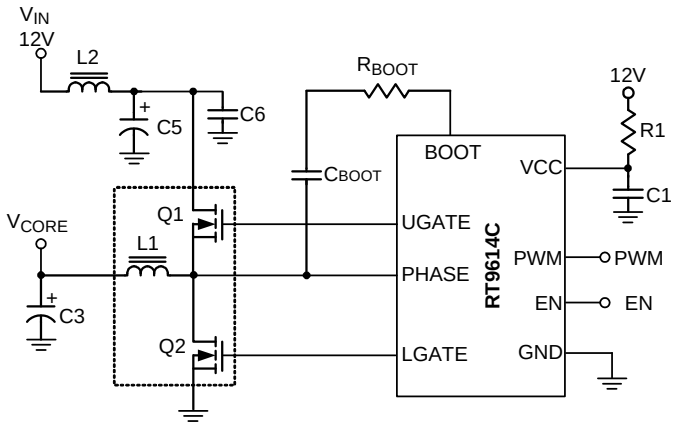
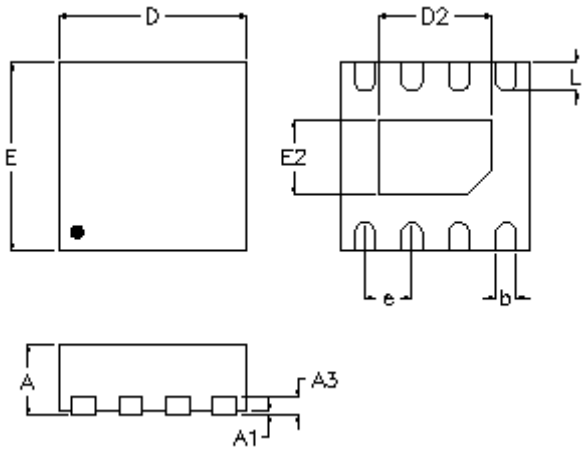
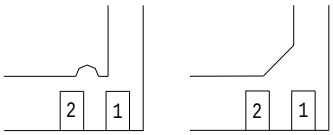


Figure 7. Synchronous Buck Converter Circuit

Outline Dimension





DETAIL A

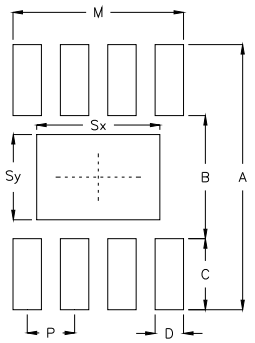
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.200	0.300	0.008	0.012
D		1.900	2.100	0.075	0.083
D2	Option1	1.150	1.250	0.045	0.049
	Option2	1.550	1.650	0.061	0.065
E		1.900	2.100	0.075	0.083
E2	Option1	0.750	0.850	0.030	0.033
	Option2	0.850	0.950	0.033	0.037
e		0.500		0.020	
L		0.250	0.350	0.010	0.014

W-Type 8SL DFN 2x2 Package

Footprint Information



Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-8S	Option1	8	0.50	2.80	1.30	0.75	0.30	1.30	0.90	1.80	±0.05
	Option2							1.60	0.90		

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