ACPI Regulator/Controller for Dual Channel DDR Memory Systems

General Description

The RT9644/A is a complete ACPI compliant power solution for DDR and DDR2 memory system with up to 4 DIMMs dual channel systems. This RT9644 includes one synchronous buck controller for DDR/DDR2 V_{DDQ}, one DDR/DDR2 bus terminator V_{TT} (equal to $V_{DDQ}/2$) regulator with source and sinking ability, three LDO controllers for V_{GMCH} (cascode), and GMCH/CPU termination $V_{TT\_GMCH/CPU}$. The RT9644A includes one synchronous buck controller for DDR/DDR2 V_{DDQ}, one PWM controller for V_{GMCH} (with external MOSFET driver), one DDR/DDR2 bus terminator V_{TT} (equal to $V_{DDQ}/2$) regulator with source and sinking ability, and two LDO controllers for $V_{TT\_GMCH/CPU}$ and V_{DAC}.

These parts also provide a reference buffer for DDR/DDR2 input reference voltage generator. When during S0 state, the VIDPGD indicates the GMCH_CPU V_{TT} within spec and operational. The synchronous buck DC-DC PWM is implemented by two N-MOSFETs as upper and lower MOSFETs with voltage mode control. The linear controllers are implemented with one N-MOSFET with suitable capacitance. Each output is monitored by under voltage protection (RT9644 except V_{GMCHH} and RT9644A except V_{DAC}). V_{DDQ} PWM controller and DDR/DDR2 bus terminator regulator have over voltage protection. Moreover, the V_{DDQ} PWM controller has the over current protection by external resister adjustment. Thermal shut down is integrated. All the internal voltage reference is fixed at 0.8V, and users can adjust the resistance divider for desired voltage output.

Applications

- Motherboard, Desktop Servers : Single/Dual channel DDR/DDR2 ACPI compliant
- Graphic Card : GPU and memory supply
- IA Equipments
- Telecomm Equipments
- DSP, ASIC or embedded processor and IO supplies
- High Power DC-DC Regulators

Features

- **RT9644 Includes Three LDO Controllers, One LDO Regulator and One PWM Controller**
  - **One DDR/DDR2 V_{DDQ} with Synchronous Buck PWM**
  - **One DDR/DDR2 Bus Terminator V_{TT} Regulator Source/Sink 3A**
  - **Two Cascode LDO Controllers for GMCH Core**
  - **One LDO Controller for GMCH/CPU Bus Terminator $V_{TT\_GMCH/CPU}$**
- **RT9644A Includes Two LDO Controllers, One LDO Regulator and Two PWM Controllers**
  - **One DDR/DDR2 V_{DDQ} with Synchronous Buck PWM**
  - **One V_{GMCH} with External Richtek MOSFET Driver**
  - **One DDR/DDR2 Bus Terminator V_{TT} Regulator Source/Sink 3A**
  - **One LDO Controller for V_{DAC}**
  - **One LDO Controller for GMCH/CPU Bus Terminator $V_{TT\_GMCH/CPU}$**
- **Operating with 5V and 12V Supply Voltage**
- **ACPI Compliant Sleep Mode Control**
- **Drive All Low Cost N-MOSFETs**
- **Voltage Mode PWM Control**
  - **250kHz Fixed Frequency Oscillator (RT9644A : Two PWM controllers with phase shift 90°)**
  - **Simple Voltage Mode Loop Control**
  - **Fast Transient Response**
  - **Over Current Protection**
- **Fully Adjustable Output Voltage Down to Compatible with DDR2**
- **Integrated DDR/DDR2 Reference Buffer**
- **Integrated VIDPGD to Indicated $V_{TT\_GMCH/CPU}$ Operational**
- **All Regulator Outputs Monitored by Under Voltage Protection**
- **DDR/DDR2 V_{DDQ} and Bus Terminator V_{TT} Also Integrated Over Voltage Protection**
- **Integrated Thermal Shut Down**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Ordering Information

RT9644/A □ □

- Package Type
  QV : VQFN-28L 6x6 (V-Type)
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)
- Two PWM Controller
- One PWM Controller

Note :

RichTek Pb-free and Green products are :

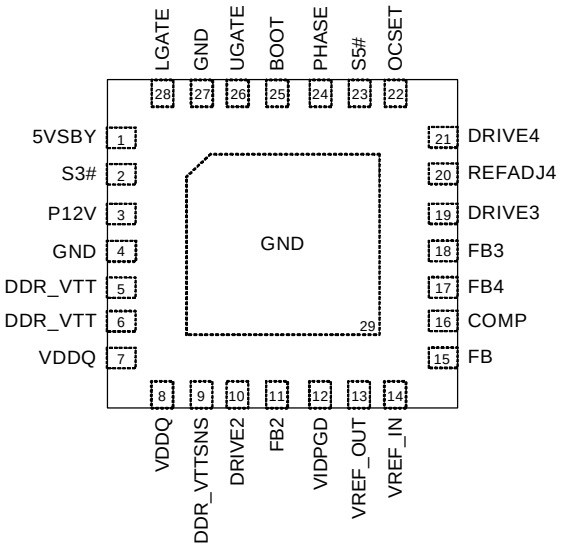
}RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

}Suitable for use in SnPb or Pb-free soldering processes.

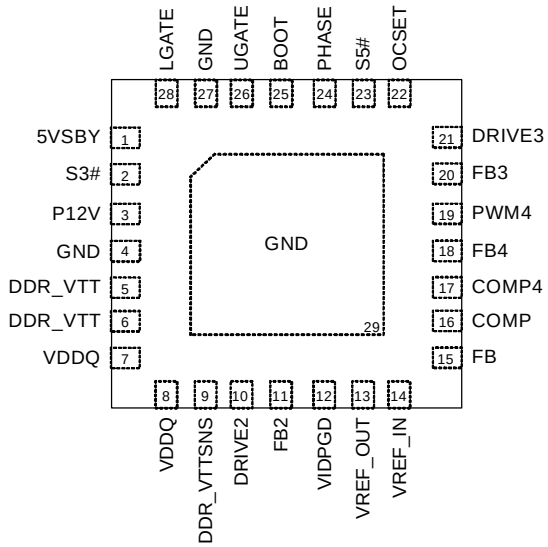
}100% matte tin (Sn) plating.

Pin Configurations

(TOP VIEW)



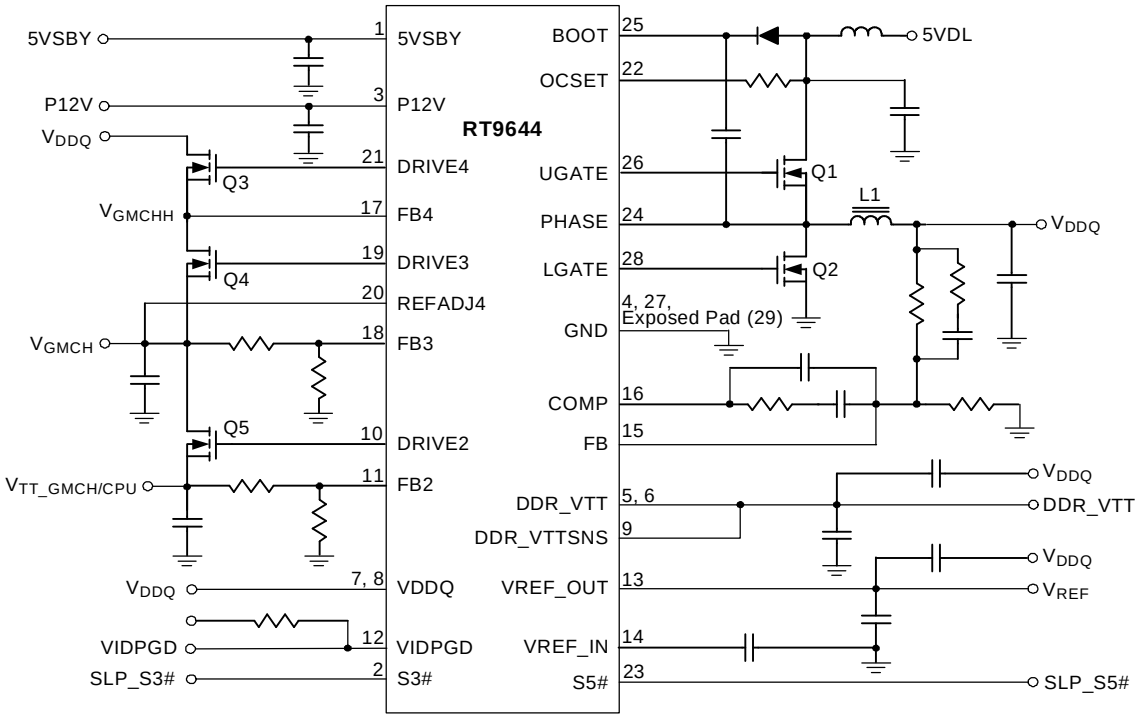
RT9644

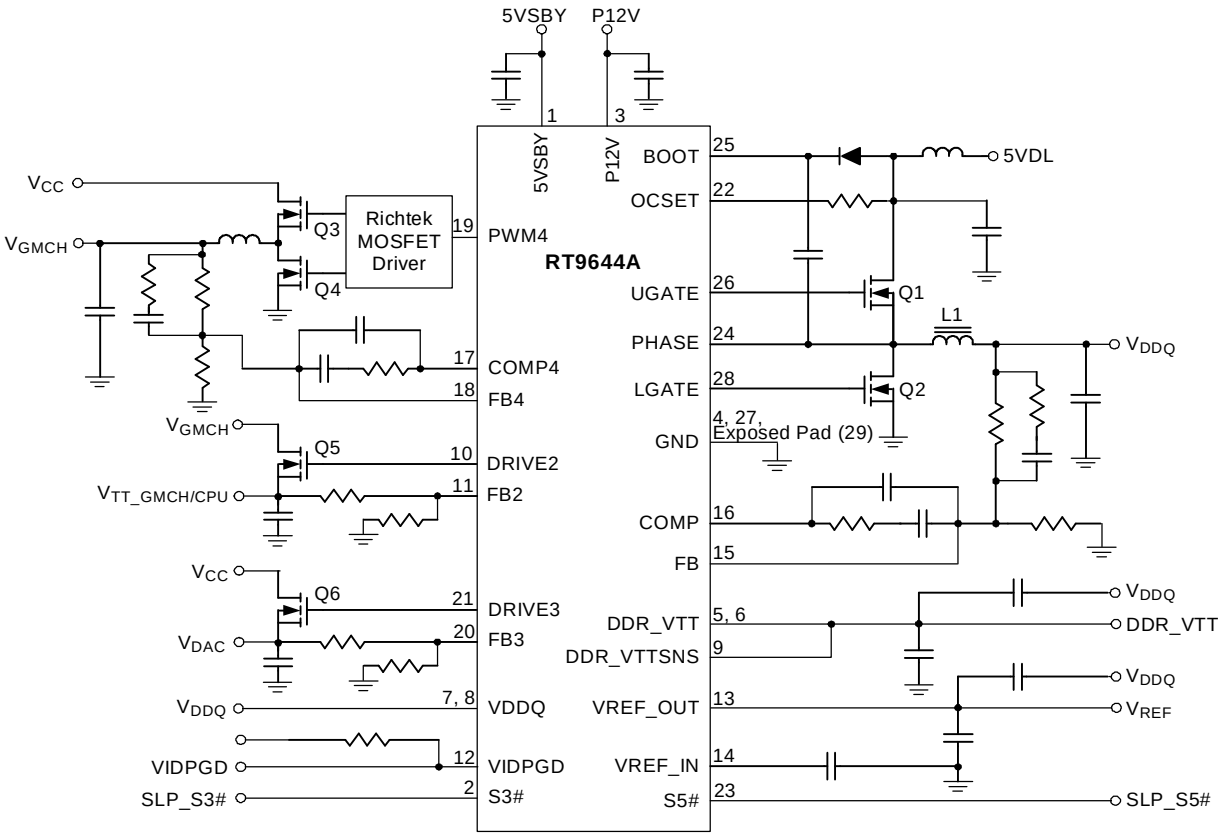


RT9644A

VQFN-28L 6x6

Typical Application Circuit





Functional Pin Description

Pin No.		Pin Name	Pin Function
RT9644	RT9644A		
1	1	5VSBY	5VSBY is the main internal power supply. The part works at normal operation mode (Icc_S0) and stand_by mode Icc_S5 (<1mA). The 5VSBY should be locally bypassed using a 0.1µF capacitor.
2	2	S3#	This pin accepts the SLP_S3# sleep state signal.
3	3	P12V	The internal LDO controller and DDR/DDR2 bus terminator V_{TT_DDR} regulator are powered by the P12V. P12V is typically connected to the +12V rail of an ATX power supply. The P12V is not necessary in S3, S4, and S5 states.
4, 27, Exposed Pad (29)	4, 27, Exposed Pad (29)	GND	The GND terminals provide the return path for the chip. Large ground currents flow through the Exposed pad of the QFN package. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5, 6	5, 6	DDR_VTT	These two DDR_VTT pins (Pin 5 and 6) should be connected externally together. The pins are the output of DDR/DDR2 bus terminator that active in S0 and S1 states.
7, 8	7, 8	VDDQ	These two VDDQ pins (Pin 7 and 8) should be connected externally together to the regulated VDDQ output. The pins are the power rail of DDT_VTT regulator. Large ground currents flow through these VDDQ pins.
9	9	DDR_VTTSNS	DDR_VTTSNS is used as the feedback for control of the DDR/DDR2 bus terminator VTT_DDR regulator. Connect this pin to the DDR_VTT outputs (Pin 5 and 6) physical desired portion.
10	10	DRIVE2	This pin provides the gate voltage for the $V_{TT\_GMCH/CPU}$ linear regulator. Connect this pin to the gate of an external N-MOSFET transistor.
11	11	FB2	Connect the output of the $V_{TT\_GMCH/CPU}$ linear regulator to this pin through a properly sized resistor divider. The voltage at this pin is regulated to 0.8V. This pin is also monitored for under-voltage events.
12	12	VIDPGD	The VIDPGD pin is an open-drain logic output that changes to logic low if the $V_{TT\_GMCH/CPU}$ linear regulator is out of regulation in S0/S1/S2 state. It should be externally pulled high when $V_{TT\_GMCH/CPU}$ is under regulated in S0, S1 and S2 states.
13	13	VREF_OUT	VREF_OUT is a buffered version of DDR_VTT and also acts as the reference voltage for the DDR_VTT linear regulator. It is recommended that a typical capacitance of 0.1µF is connected between V_{DDQ} and VREF_OUT and also between VREF_OUT and ground for proper operation. Larger then 0.3µF capacitance is not recommended.

To be continued

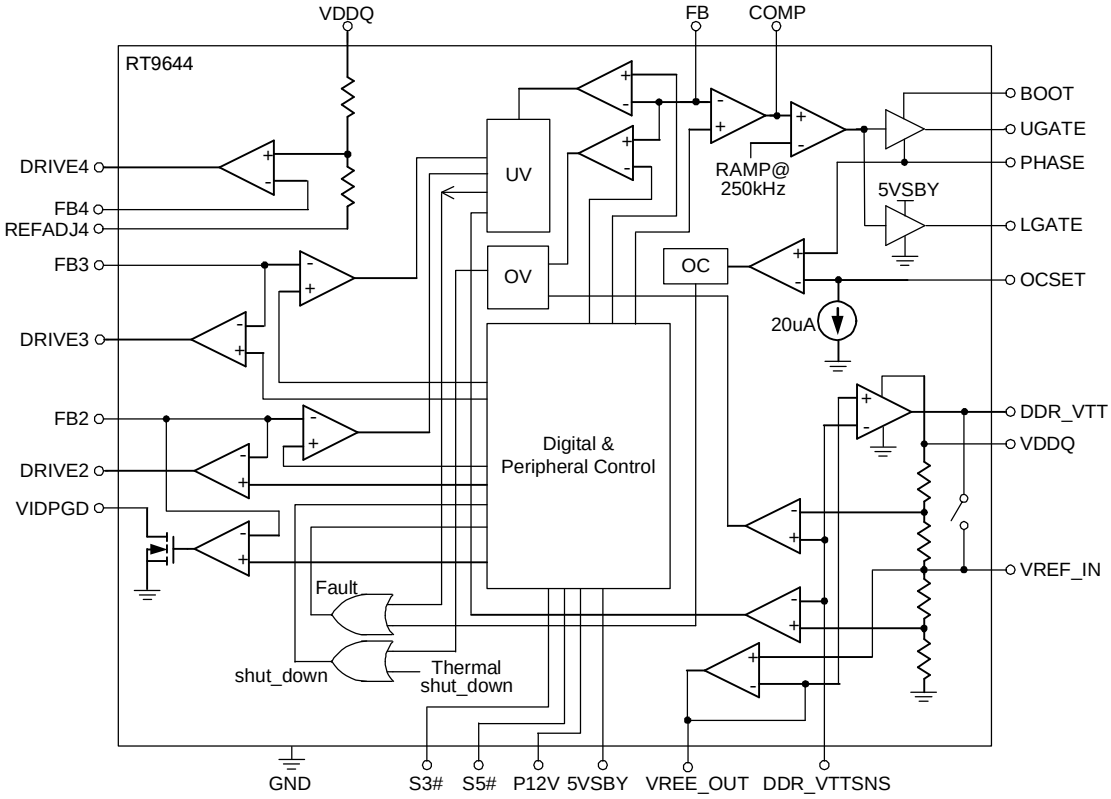
Pin No.		Pin Name	Pin Function
RT9644	RT9644A		
14	14	VREF_IN	A capacitor, C_{SS}, connected between VREF_IN and ground is required. This capacitor and the parallel combination of the Upper and Lower Divider Impedance (RU//RL), sets the time constant for the start up ramp when transitioning from S3/S4/S5 to S0/S1/S2. The soft start capacitance will determine the V_{TT_DDR} soft start ramp by the above RC time constant. $C_{SS} > (C_{VTT} \times V_{DDQ}) / [10 \times 2 \times 1A \times (RU//RL)]$
15	15	FB	FB is the error amplifier negative input that needs proper resistance divider connected to V_{DDQ}. The V_{DDQ} synchronous DC-DC buck is simple voltage control mode. It needs a typical Type 2 compensation network from COMP to FB (or Type 3). The reference voltage of the error amplifier is 0.8V monitored by under and over voltage protection.
16	16	COMP	The COMP is the output to the voltage loop error amplifier. Loop compensation is achieved by connecting an AC network across COMP and FB.
17	18	FB4	In RT9644, the FB4 pin connects the output of the upper V_{GMCH} (V_{GMCHH}) linear regulator to this pin. The voltage at this pin is regulated via the REFADJ4 pin (Pin 20). Generally, the FB4 is connected to V_{GMCHH}, and REFADJ4 = V_{GMCH}. The V_{GMCHH} LDO controller will set the positive input to (V_{DDQ}+REFADJ4)/2 as reference voltage. Then we can have the VGMCHH equal to (V_{DDQ}+V_{GMCH})/2. In RT9644A, the FB4 is the 2nd synchronous DC-DC buck converter error amplifier feedback. There should be the suitable AC compensation RC network. The compensation may be Type 2 even Type 3. The feedback voltage is monitored by the under voltage protection.
18	20	FB3	In RT9644, the FB3 pin connects the output of the lower V_{GMCH} (V_{GMCH}) linear regulator to this pin through a properly sized resistor divider. The voltage at this pin is regulated to 0.8V. This pin is monitored for under-voltage protection. In RT9644A, the pin connects the output of the V_{DAC} linear regulator with proper resister divider.
19	21	DRIVE3	In RT9644, the DRIVE3 pin provides the gate voltage for the lower V_{GMCH} linear regulator pass transistor. Connect this pin to the gate terminal of an external N-MOSFET transistor. In RT9644A, the DRIVE3 pin provides the gate voltage for the V_{DAC} linear regulator pass transistor. Connect this pin to the gate terminal of an external N- MOSFET transistor.
20	--	REFADJ4	This REFADJ4 pin controls the V_{GMCHH} LDO controller reference voltage. To ENSURE that both upper and lower pass transistors dissipate the same power, connecting this REFADJ4 pin to the V_{GMCH} output rail.
21	--	DRIVE4	The DRIVE4 pin provides the gate voltage for the upper V_{GMCH} (V_{GMCHH}) linear regulator. Connect this pin to the gate terminal of an external N-MOSFET transistor.

To be continued

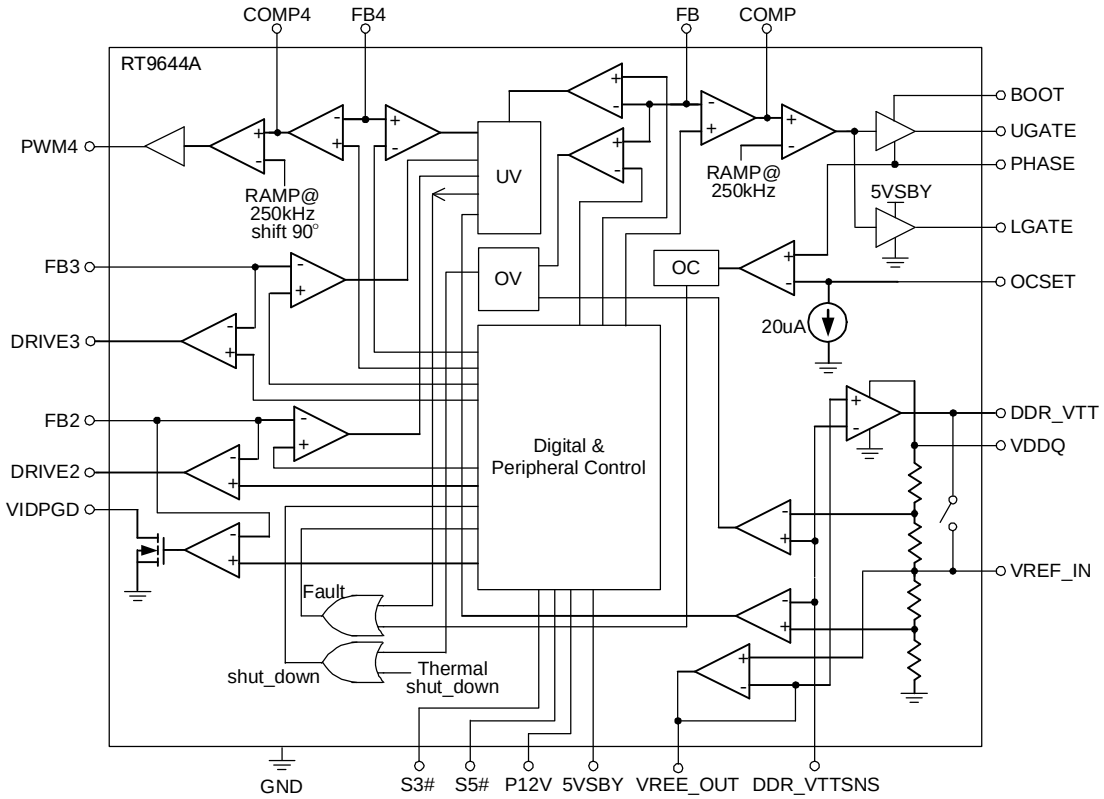
Pin No.		Pin Name	Pin Function
RT9644	RT9644A		
--	17	COMP4	The COMP4 pin provides the compensation AC network for the 2nd synchronous DC-DC buck PWM controller.
--	19	PWM4	The PWM4 pin is the output of the 2nd synchronous DC-DC buck converter used for V_{GMCH}. The PWM4 should be connected to suitable RICHTEK MOSFET driver to drive 2 N-MOSFETs.
22	22	OCSET	V_{DDQ} synchronous DC-DC buck converter has over current protection via the R_{OCSET} to decide the over current criteria. Connect a resistor (R_{OCSET}) from this pin to the drain of the upper N-MOSFET. There is an internal 20μA current sink (I_{OCSET}) from the OCSET pin. We can define the OC trip point via R_{OCSET}, I_{OCSET}, and the upper N-MOSFET on-resistance ($R_{DS(ON)}$) as following equation : $I_{PEAK} = (I_{OCSET} \times R_{OCSET}) / R_{DS(ON)}$
23	23	S5#	This pin accepts the SLP_S5# sleep state signal.
24	24	PHASE	For the V_{DDQ} synchronous DC-DC buck converter, connect the PHASE pin to the upper N-MOSFET's source. This pin is used to monitor the voltage drop across the upper N-MOSFET for over-current protection. The PHASE pin is the return path rail for the upper MOSFET deriver (UGATE).
25	25	BOOT	For the V_{DDQ} synchronous DC-DC buck converter, the BOOT pin provides as power supply to the upper N-MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive a logic-level N-MOSFET.
26	26	UGATE	For the V_{DDQ} synchronous DC-DC buck converter, connect the UGATE pin to the upper N-MOSFET's gate. This pin provides the PWM-controlled gate drive for the upper N-MOSFET. This pin is also monitored by the adaptive shoottthrough protection circuitry to determine when the upper N-MOSFET has turned off. Do not insert any circuitry between this pin and the gate of the upper N-MOSFET, as it may interfere with the internal adaptive shoot-through protection circuitry and render it ineffective.
28	28	LGATE	For the V_{DDQ} synchronous DC-DC buck converter, Connect the LGATE pin to the lower N-MOSFET's gate. This pin provides the PWM-controlled gate drive for the lower N-MOSFET. This pin is also monitored by the adaptive shoottthrough protection circuitry to determine when the lower N-MOSFET has turned off. Do not insert any circuitry between this pin and the gate of the lower N-MOSFET, as it may interfere with the internal adaptive shoot-through protection circuitry and render it ineffective.

Function Block Diagram

RT9644



RT9644A



Absolute Maximum Ratings (Note 1)

- Supply Voltage, 5VSBY ---------- 7V
- Supply Voltage, P12V ---------- 16V
- BOOT, V_{BOOT} – V_{PHASE} ---------- 7V
- UGATE Voltage ---------- V_{PHASE} – 0.3V to V_{BOOT} + 0.3V
- LGATE Voltage ---------- GND – 0.3V to 5VSBY + 0.3V
- Input, Output or I/O Voltage ---------- GND – 0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-28L 6x6 ---------- 2.857W
- Package Thermal Resistance (Note 4)
  VQFN-28L 6x6, θ_{JA} ---------- 35°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –40°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage, 5VSBY ---------- 5V ± 5%
- Supply Voltage, P12V ---------- 12V ± 10%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(5VSBY = 5V, P12V = 12V, T_A = 25°C, unless otherwise specification)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
5VSBY Supply Current						
Nominal Supply Current	I_{CC_S0}	S3# & S5# High, UGATE/LGATE Open	5.5	7	8	mA
	I_{CC_S5}	S5# Low, S3# Don't Care UGATE/LGATE Open	--	700	850	µA
Power-On Reset						
Rising 5VSBY POR Threshold			4	--	4.35	V
Falling 5VSBY POR Threshold			3.6	--	3.95	V
Rising P12V POR Threshold			10	--	10.5	V
Falling P12V POR Threshold			8.8	--	9.75	V
Oscillator and Soft-Start						
PWM Frequency	f_{OSC}		220	250	280	kHz
Ramp Amplitude	ΔV_{OSC}		--	1.5	--	V
Soft-Start Interval	t_{SS}		6.5	8.2	9.5	ms

To be continued

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Reference Voltage						
Reference Voltage V_{REF}			--	0.8	--	V
System Accuracy			-2	-	2	%
VDDQ PWM Controller Error Amplifier						
DC Gain Guaranteed By Design			--	80	--	dB
Gain-Bandwidth Product GBWP			15	--	--	MHz
Slew Rate SR			--	6	--	V/μs
Control I/O (S3# and S5#)						
Low Level Input Threshold			--	--	0.75	V
High Level Input Threshold			2.2	--	--	V
PWM Controller Gate Drivers						
UGATE and LGATE Source IGATE			--	-0.8	--	A
UGATE and LGATE Sink IGATE			--	0.8	--	A
V_{TT} Regulator						
Upper Divider Impedance RU	R_U		--	2.5	--	kΩ
Lower Divider Impedance RL	R_L		--	2.5	--	kΩ
VREF_OUT Buffer Source Current IVREF_OUT			--	--	2	mA
Maximum VTT Load Current	I_{VTT_MAX}	Periodic load applied with 30% duty cycle and 10ms period	-3	--	3	A
Linear Regulators						
DC GAIN Guaranteed By Design			--	80	--	dB
Gain Bandwidth Product GBWP			12	--	--	MHz
Slew Rate SR			--	6	--	V/μs
DRIVEn High Output Voltage		DRIVEn unloaded	9.75	10	--	V
DRIVEn Low Output Voltage		DRIVEn unloaded	--	0.16	0.4	V
DRIVEn High Output Source Current			--	1.2	--	mA
DRIVEn Low Output Sink Current			--	1.2	--	mA
VIDPGOOD						
$V_{TT\_GMCH/CPU}$ Rising Threshold		S0	0.725	0.74	--	V
$V_{TT\_GMCH/CPU}$ Falling Threshold		S0	--	0.7	0.715	V
Protection						
OCSET Current Source	I_{OCSET}		18	20	22	μA
DDR_VTT Current Limit		By Design	–3.3	--	3.3	A
VDDQ OV Level S0/S3	V_{FB}/V_{REF}	S0/S3	--	115	--	%
VDDQ UV Level	V_{FB}/V_{REF}	S0/S3	--	75	--	%
DDR_VTT OV Level	V_{TT}/V_{VREF_IN}	S0	--	115	--	%

To be continued

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
DDR_VTT UV Level	V_{TT}/V_{VREF_IN}	S0	--	85	--	%
V_{GMCH} UV Level	V_{FB4}/V_{REF}	S0	--	75	--	%
$V_{TT\_GMCH/CPU}$ UV Level	V_{FB2}/V_{REF}	S0	--	75	--	%
Thermal Shutdown Limit	TSD	By Design	--	140	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution is highly recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Application Information

Overview

The RT9644/A provides complete control, drive, protection and ACPI compliance for a regulator powering DDR memory systems and the GMCH core and GMCH/CPU termination rails. It is primarily designed for computer applications powered from an ATX power supply.

A 250kHz Synchronous Buck Regulator with a precision 0.8V reference provides the proper Core voltage to the system memory of the computer. An internal LDO regulator with the ability to both sink and source current and an externally available buffered reference that tracks the VDDQ output by 50% provides the VTT termination voltage.

In RT9644, a two-stage LDO controller provides the GMCH core voltage. A third LDO controller is included for the regulation of the GMCH/CPU termination voltage.

In RT9644A, a second 250kHz PWM Buck regulator, which requires an external MOSFET driver, provides the GMCH core voltage. This PWM regulator is 90° out of phase with the PWM regulator used for the Memory core. Two additional LDO controllers are included, one for the regulation of the GMCH/CPU termination rail and the second for the DAC.

ACPI State Transitions

ACPI compliance is realized through the S3# and S5# sleep signals and through monitoring of the 12V ATX bus. Figure 1 and Figure 2 shows how the RT9644 and RT9644A individual regulators are controlled during all state transitions.

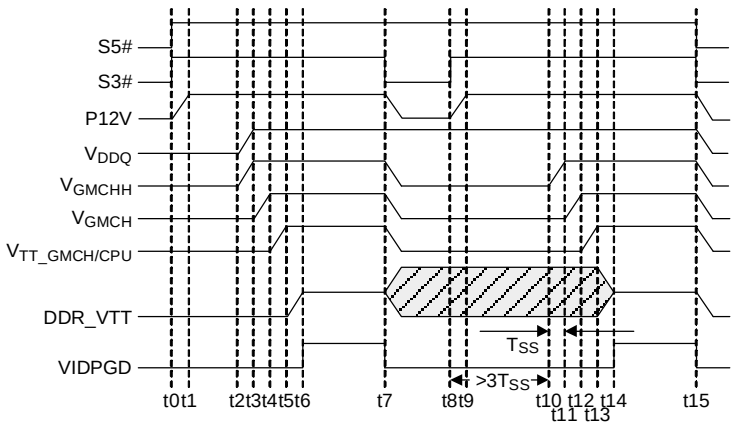


Figure 1. Timing diagram for RT9644

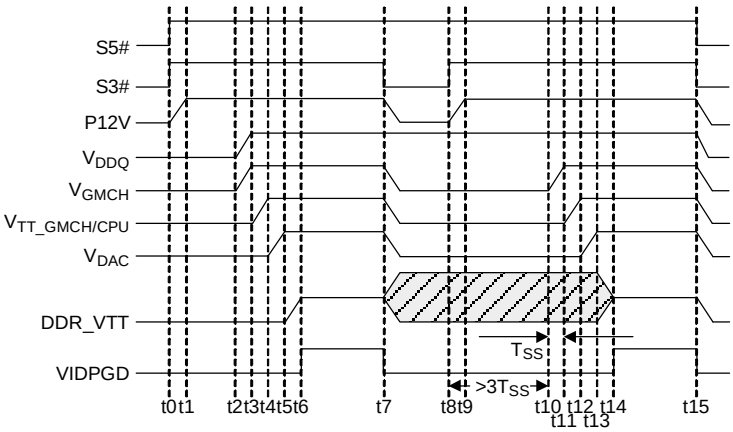


Figure 2. Timing diagram for RT9644A

S5 to S0 Transition

At the onset of a mechanical start, time t0 in Figure 1, the RT9644 receives its bias voltage from the 5V Standby bus (5VSBY). Once the 5VSBY rail has exceeded the POR threshold, the RT9644 will remain in an internal S5 state until both the S3# and S5# signal have transitioned high and the 12V POR threshold has been exceeded by the +12V rail from the ATX, which occurs at time t1.

Once all of these conditions are met, the PWM error amplifier will first be reset by internally shorting the COMP pin to the FB pin. This reset lasts for 3-4 soft-start cycles, Then digital soft-start sequence will begin. Each regulator is enabled and soft-started according to a preset sequence.

At time t2 the V_{DDQ} rail and the upper V_{GMCH} LDO rail of RT9644 are digitally soft-started.

The digital soft-start for the PWM regulator is accomplished by clamping the error amplifier reference input to a level proportional to the internal digital soft-start voltage. As the soft-start voltage slews up, the PWM comparator generates PHASE pulses of increasing width that charge the output capacitor(s).

This method provides a rapid and controlled rising output voltage. The linear regulators, with the exception of the internal DDR_VTT LDO, are soft-started in a similar manner. The error amplifier reference is clamped to the internal digital soft-start voltage. As the soft-start voltage ramps up, the respective DRIVE pin voltages increase, thus enhancing the N-MOSFETs and charging the output

capacitors in a controlled manner.

At time t3, the V_{DDQ} and upper V_{GMCH} LDO output rails are in regulation and the lower V_{GMCH} LDO is soft-started. At time t4, the V_{GMCH} rail is in regulation and the $V_{TT\_GMCH/CPU}$ linear regulator is soft-started. At time t5, the $V_{TT\_GMCH/CPU}$ rail is in regulation DDR_VTT internal regulator is soft-started.

The DDR_VTT LDO soft-starts in a manner unlike the other regulators. When the DDR_VTT regulator is disabled, the reference is internally shorted to the DDR_VTT output. This allows the termination voltage to float during the S3 sleep state. When the RT9644 enables the DDR_VTT regulator or enters S0 state from a sleep state, this short is released and the internal divide down resistors which set the DDR_VTT voltage to 50% of DDR_VTT will provide a controlled voltage rise on the capacitor that is tied to the VREF_IN pin.

The voltage on this capacitor is the reference for the DDR_VTT regulator and the output will track it as it settles to 50% of the V_{DDQ} voltage. The combination of the internal resistors and the VREF_IN capacitor will determine the rise time of the DDR_VTT regulator (see the Functional Pin Description section for proper sizing of the VREF_IN capacitor).

At time t6, a full soft-start cycle has passed from the time that the DDR_VTT regulator was enabled. At this time the VIDPGD comparator is enabled. Once enabled if the $V_{TT\_GMCH/CPU}$ output is within regulation, the VIDPGD pin will be forced to a high impedance state.

S0 to S3 Transition

When S3# goes LOW with S5# still HIGH, the RT9644/A will disable all the regulators except for the VDDQ regulator, which is continually supplied by the 5VDUAL rail.

VIDPGD will also transition LOW. When V_{TT} is disabled, the internal reference for the V_{TT} regulator is internally shorted to the V_{TT} rail. This allows the V_{TT} rail to float. When floating, the voltage on the V_{TT} rail will depend on the leakage characteristics of the memory and MCH I/O pins. It is important to note that the V_{TT} rail may not bleed down to 0V. Figure 1 shows how the individual regulators are affected by the S3 state at time t7.

S3 to S0 Transition

When S3# transits from LOW to HIGH with S5# held HIGH and after the 12V rail exceeds POR, the RT9644/A will initiate the soft-start sequence. This sequence is very similar to the mechanical start soft-start sequencing. The transition from S3 to S0 is represented in Figure 1 and Figure 2 between times t8 and t14.

At time t8, the S3# signal transits to HIGH. This enables the ATX, which brings up the 12V rail. At time t9, the 12V rail has exceeded the POR threshold and the RT9644 enters a reset mode that lasts for 3 soft-start cycles. At time t10, the 3 soft-start cycle reset is ended and the individual regulators are enabled and soft-started in the same sequence as the mechanical cold start sequence, with the exception that the VDDQ regulator is already enabled and in regulation.

S0 to S5 Transition

When the system transits from active state to shutdown (S0 to S5) state, the RT9644/A IC disables all regulators and forces the VIDPGD pin LOW. This transition is represented on Figure 1 and Figure 2 at time t15.

Fault Protection

The RT9644/A monitors the V_{DDQ} regulator for under voltage,over-voltage and over-current protection. The internal DDR_VTT LDO regulator is monitored for under-voltageand over-voltage protection.

All other regulators are monitored for under-voltage protection. An over-voltage protection on either the VDDQ or DDR_VTT regulator and thermal Shutdown protection will cause an immediate shutdown of all regulators.

This can only be cleared by toggling the S5# signal such that the system enters the S5 sleep state and then transitions back to the active, S0, state. If a regulator experiences any other fault condition (an under-voltage or an over-current on VDDQ), all of regulator will be disabled and an internal fault counter will be incremented by 1.

At every fault occurrence, the internal fault counter is incremented by 1 and an internal Fault Reset Counter is cleared to zero. The Fault Reset Counter will Count 9 x Tss period. If the Fault Reset Counter reaches 9 x Tss

period and no other fault occurs, then the Fault Counter is cleared to 0. If a fault occurs prior to the Fault Reset Counter reaching 9 x Tss period, then the Fault Reset Counter is set back to zero.

The RT9644/A will immediately shut down when the Fault Counter reaches a count of 4. When attempting to restart a faulted regulator, the RT9644/A will follow the preset start up sequencing. If a regulator is already in regulation, then it will not be affected by the start up sequencing.

VDDQ Overcurrent Protection

The OCP function monitors output current by using upper MOSFET $R_{DS(ON)}$. The OCP function cycles soft-start function in a hiccup mode. Over-current triggering level can be arbitrarily set by adjusting R_{OCSET}. An Internal 20μA current sink makes a voltage drop across R_{OCSET} from V_{IN}. When V_{PHASE} is lower than V_{OCSET}, OCP function initializes soft-start cycles. The OCP funcion will be triggered as inductor current reach :

$$I_{L(MAX)} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

To prevent OC form tripping in normal operation, R_{OCSET} must be carefully chosen with :

1. Maximum $R_{DS(ON)}$ at highest junction temperature
2. MInimum I_{OCSET} from specification table
3. $I_{L(MAX)} > I_{OUT(MAX)} + \Delta I_L / 2$

   ΔI_L = inductor ripple current

Feedback Compensation

Figure 3 highlights the voltage-mode control loop for a synchronous buck converter. Figure 4 shows the corresponding Bode plot. The output voltage (V_{OUT}) is regulated to the reference voltage. The error amplifier EA output (COMP) is compared with the oscillator (OSC) sawtooth wave to provide a pulse-width modulated (PWM) wave with an amplitude of VIN at the PHASE node. The PWM wave is smoothed by the output filter (L and C_{OUT}).

The modulator transfer function is the small-signal transfer function of V_{OUT}/COMP. This function is dominated by a DC gain and the output filter (L and C_{OUT}), with a double pole break frequency at FP_LC and a zero at FZ_ESR. The DC gain of the modulator is simply the input voltage (VIN) divided by the peak-to-peak oscillator voltage %V_{OSC}.

The break frequency FLC and FESR are expressed as Equation (1) and (2) respectively.

$$F_{P\_LC} = \frac{1}{2p\sqrt{LC_{OUT}}} \quad (1)$$

$$F_{Z\_ESR} = \frac{1}{2p \times ESR \times C_{OUT}} \quad (2)$$

The compensation network consists of the error amplifier EA and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest DC gain, the highest 0dB crossing frequency (FC) and adequate phase margin. Typically, FC in range 1/5 to 1/10 of switching frequency is adequate. The higher FC is, the faster dynamic response is. A phase margin in the range of 45°C to 60°C is desirable. The equations below relate the compensation network poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 4.

$$F_{Z1} = \frac{1}{2p \times R2 \times C1} \quad (3)$$

$$F_{Z2} = \frac{1}{2p \times (R1+R3) \times C3} \quad (4)$$

$$F_{P1} = \frac{1}{2p \times R2 \times \frac{C1 \times C2}{C1+C2}} \quad (5)$$

$$F_{P2} = \frac{1}{2p \times R3 \times C3} \quad (6)$$

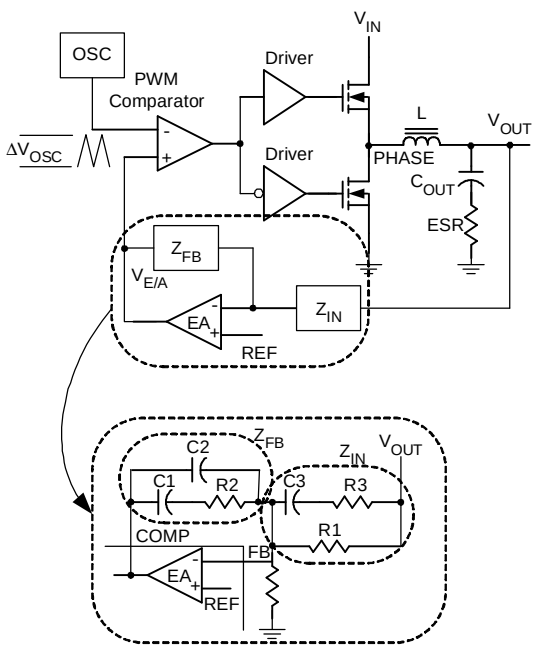


Figure 3

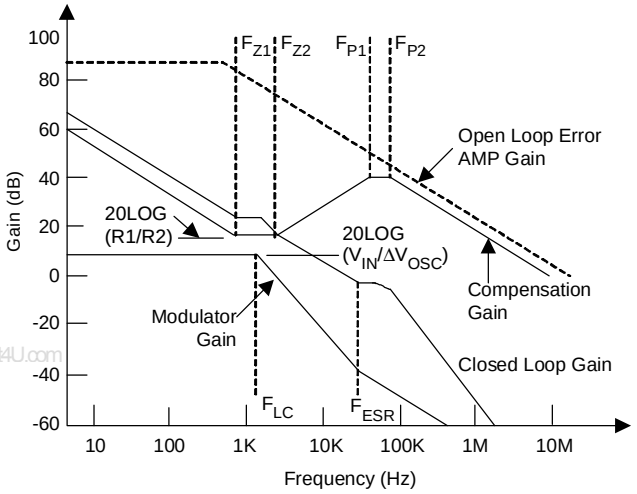


Figure 4

Feedback Loop Design Procedure

Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R2/R1) for desired 0dB crossing frequency (FC).

2. Place 1st zero F_{Z1} below modulator double pole FLC (~75% FLC).

3. Place 2nd zero F_{Z2} at modulator double pole FLC.

4. Place 1st pole F_{P1} at the ESR zero FZ_ESR

5. Place 2nd pole F_{P2} at half the switching frequency.

6. Check gain against error amplifier's open-loop gain.

7. Pick RFB for desired output voltage.

8. Estimate phase margin and repeat if necessary.

Component Selection

Components should be appropriately selected to ensure stable operation, fast transient response, high efficiency, minimum BOM cost and maximum reliability.

Output Inductor Selection

The selection of output inductor is based on the considerations of efficiency, output power and operating frequency. For a synchronous buck converter, the ripple current of inductor (%I_L) can be calculated as follows :

$$\Delta I_L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times f_{OSC} \times L} \quad (7)$$

Generally, an inductor that limits the ripple current between 20% and 50% of output current is appropriate. Make sure that the output inductor could handle the maximum output current and would not saturate over the operation temperature range.

Output Capacitor Selection

The output capacitors determine the output ripple voltage (%V_{OUT}) and the initial voltage drop after a high slew rate load transient. The selection of output capacitor depends on the output ripple requirement. The output ripple voltage is described as Equation (8).

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{1}{8} \times \frac{V_{OUT}}{f_{OSC}^2 \times L \times C_{OUT}} (1-D) \quad (8)$$

For electrolytic capacitor application, typically 90 to 95% of the output voltage ripple is contributed by the ESR of output capacitors. Paralleling lower ESR ceramic capacitor with the bulk capacitors could dramatically reduce the equivalent ESR and consequently the ripple voltage.

Input Capacitor Selection

Use mixed types of input bypass capacitors to control the input voltage ripple and switching voltage spike across the MOSFETs. The buck converter draws pulsewise current from the input capacitor during the on time of upper MOSFET. The RMS value of ripple current flowing through the input capacitor is described as :

$$I_{IN(RMS)} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (9)$$

The input bulk capacitor must be cable of handling this ripple current. Sometime, for higher efficiency the low ESR capacitor is necessarily. Appropriate high frequency ceramic capacitors physically near the MOSFETs effectively reduce the switching voltage spikes.

MOSFET Selection of PWM Buck Converter

The selection of MOSFETs is based upon the considerations of $R_{DS(ON)}$, gate driving requirements, and thermal management requirements. The power loss of upper MOSFET consists of conduction loss and switching loss and is expressed as :

$$P_{UPPER} = P_{COND\_UPPER} + P_{SW\_UPPER} \quad (10)$$
$$= I^2_{OUT} \times R_{DS(ON)} \times D + \frac{1}{2} I_{OUT} \times V_{IN} \times (T_{RISE} + T_{FALL}) \times f_{OSC}$$

where T_{RISE} and T_{FALL} are rising and falling time of V_{DS} of upper MOSFET respectively. $R_{DS(ON)}$ and QG should be simultaneously considered to minimize power loss of upper MOSFET.

The power loss of lower MOSFET consists of conduction loss, reverse recovery loss of body diode, and conduction loss of body diode and is expressed as :

$$P_{LOWER} = P_{COND\_LOWER} + P_{RR} + P_{DIODE} \quad (11)$$
$$= I^2_{OUT} \times R_{DS(ON)} \times (1 - D) + Q_{RR} \times V_{IN} \times f_{OSC} + \frac{1}{2} I_{OUT} \times V_F \times T_{DIODE} \times f_{OSC}$$

where T_{DIODE} is the conducting time of lower body diode. Special control scheme is adopted to minimize body diode conducting time. As a result, the $R_{DS(ON)}$ loss dominates the power loss of lower MOSFET. Use MOSFET with adequate $R_{DS(ON)}$ to minimize power loss and satisfy thermal requirements.

MOSFET Selection of LDO

The main criteria for selection of the LDO pass transistor is package selection for efficient removal of heat.

Select a package and heatsink that maintains the junction temperature below the rating with a maximum expected ambient temperature.

The power dissipated in the linear regulator is:

$P_D = I_{OUT(MAX)} \times (V_{IN} - V_{OUT})$

where $I_{OUT(MAX)}$ is the maximum output current and V_{OUT} is the nominal output voltage of LDO

Layout Consideration

Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. First, place the PWM power stage components. Mount all the power components and connections in the top layer with wide copper areas. The MOSFETs of Buck, inductor, and output capacitor should be as close to each other as possible. This can reduce the radiation of EMI due to the high frequency current loop. If the output capacitors are placed in parallel to reduce the ESR of capacitor, equal sharing ripple current should be considered.

Place the input capacitor directly to the drain of high-side MOSFET. The MOSFETs of linear regulator should have wide pad to dissipate the heat. In multilayer PCB, use one layer as power ground and have a separate control signal ground as the reference of the all signal. To avoid the signal ground is effect by noise and have best load regulation, it should be connected to the ground terminal of output. Furthermore, follows below guide lines can get better performance of IC :

(1). The IC needs a bypassing ceramic capacitor as a R-C filter to isolate the pulse current from power stage and supply to IC, so the ceramic capacitor should be placed adjacent to the IC.

(2). Place the high frequency ceramic decoupling close to the power MOSFETs.

(3). The feedback part should be placed as close to IC as possible and keep away from the inductor and all noise sources.

(4). The components of bootstraps should be closed to each other and close to MOSFETs.

(5).The PCB trace from Ug and Lg of controller to MOSFETs should be as short as possible and can carry 1A peak current.

(6). Place all of the components as close to IC as possible.

(7).VTT LDO must dissipate heat generated,the pin29 should be connected to the internal ground plane through four vias.

Below PCB gerber files are our test board for your reference :

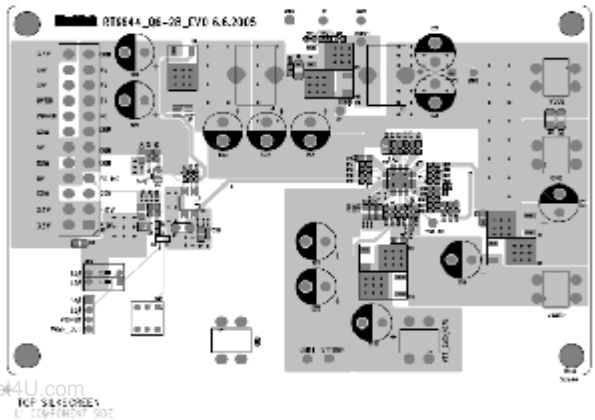


Figure 5. Top Layer for RT9644

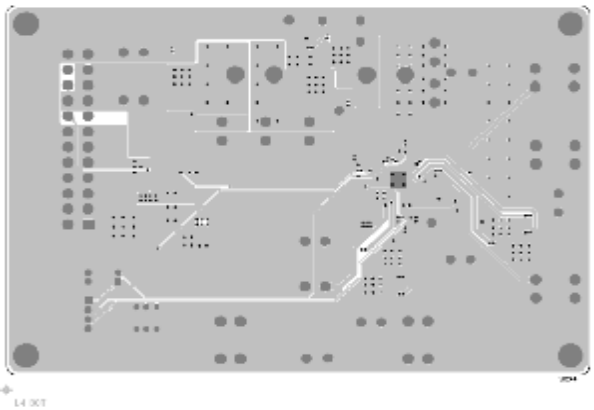


Figure 6. Bottom Layer for RT9644

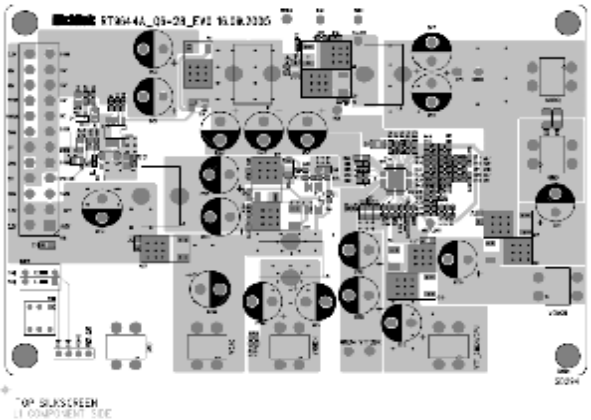


Figure 7. Top Layer for RT9644A

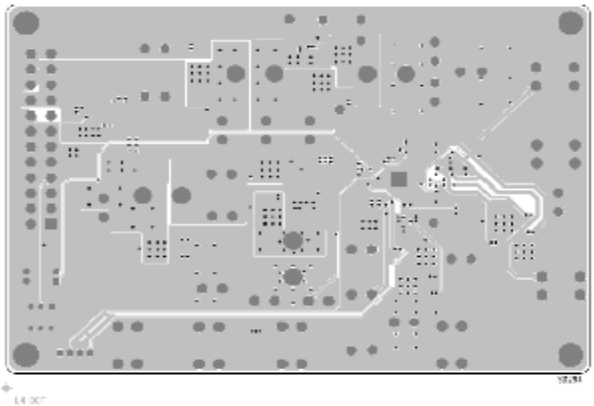
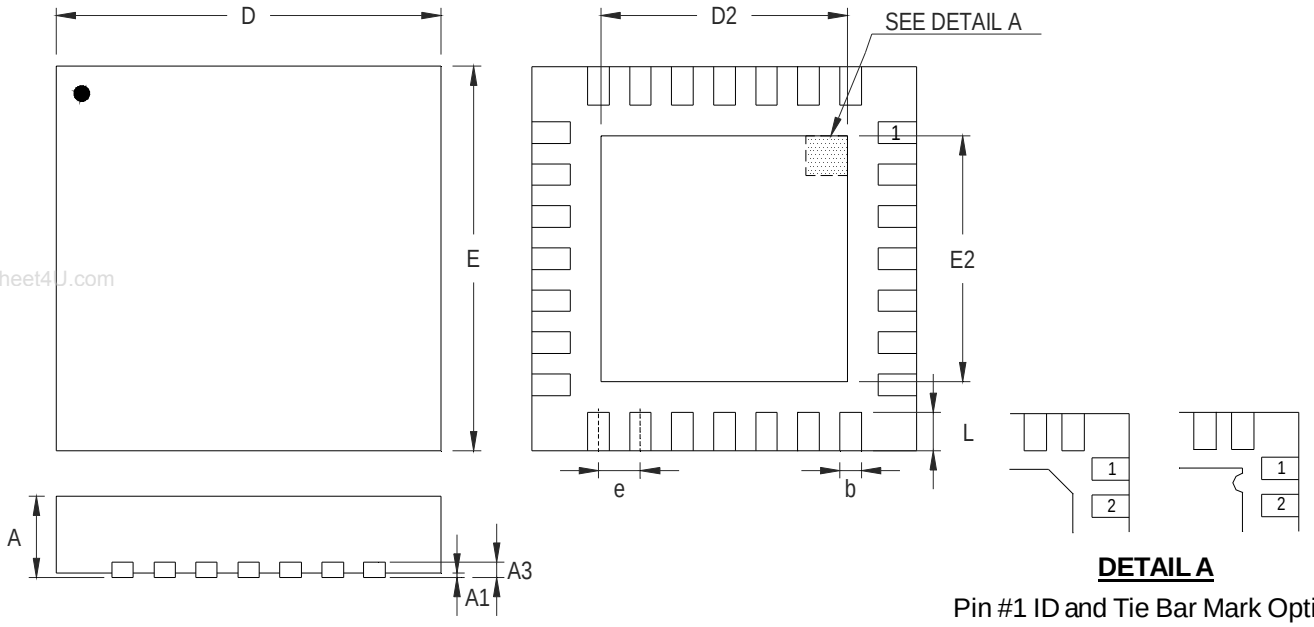


Figure 8. Bottom Layer for RT9644A

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.230	0.350	0.009	0.014
D	5.900	6.100	0.232	0.240
D2	3.500	4.100	0.138	0.161
E	5.900	6.100	0.232	0.240
E2	3.500	4.100	0.138	0.161
e	0.650		0.026	
L	0.500	0.700	0.020	0.028

V-Type 28L QFN 6x6 Package

Richtek Technology Corporation

Headquarter

5F, No. 20, Taiyuen Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation

Taipei Office (Marketing)

8F, No. 137, Lane 235, Paochiao Road, Hsintien City

Taipei County, Taiwan, R.O.C.

Tel: (8862)89191466 Fax: (8862)89191465

Email: marketing@richtek.com