Integrated Multi-Channel DC-DC Converter for TFT LCD Panels

General Description

The RT9913A/B includes a high-performance boost regulator, one linear-regulator controller for VGL, one low dropout linear regulator, a gate pulse modulator (GPM), a voltage detector and a V_{COM} Buffer (Unity- gain OPA) for active-matrix thin-film transistor (TFT) liquid-crystal displays (LCDs).

The boost converter provides the regulated supply voltage for the panel source driver ICs. With integrated 16V N-Channel 0.2Ω MOSFET it allows the use of ultra-small inductors and ceramic capacitors and provides fast transient response to pulsed loads. The VGL linear-regulator controller provides regulated TFT Gate-Off . The low-dropout linear regulator (LDO) using an internal PMOS as the pass device can supply up to 350mA current is suitable for the supply voltage to the T-CON ASIC. And the GPM is controlled by frame signals from timing controller to modulate the Gate-On voltage. Voltage detector monitors the supply voltage to issue a reset signal while the detected voltage is too low. The V_{COM} Buffer (Unity-gain) high-performance operation amplifier) can drive the LCD backplane (V_{COM}) and features high short-circuit current (140mA), fast slew rate (12V/μs), wide bandwidth (12MHz) and rail-to-rail input and output.

Ordering Information

RT9913A/B □ □

- Package Type
  QV : VQFN-24L 4x4 (V-Type)
- Operating Temperature Range
  P : Pb Free with Commercial Standard
- Switching Frequency
  A : 640kHz
  B : 1.2MHz

Note :

RichTek Pb-free products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Features

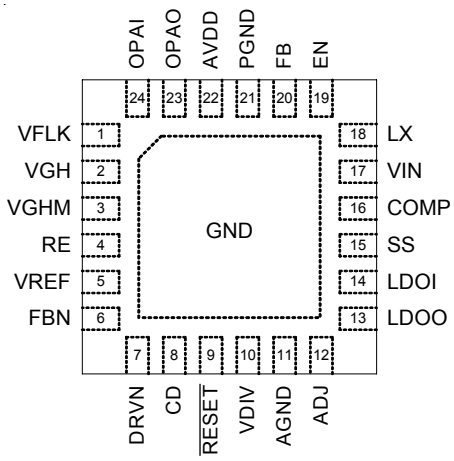
- **2.5V to 5.5V Input Supply Voltage**
- **640kHz/1.2MHz (A/B version) Current-Mode Step-Up Boost Regulator**
  Fast Transient Response to Pulsed Load
  High Accuracy Output Voltage (±2%)
  Built-In 16V, 2.0A, 0.2Ω N-Channel MOSFET
  High Efficiency Up to 90%
  Programmable Soft-Start
  Programmable Over-Current Protection
- **Linear-Regulator Controller for VGL**
- **Low Drop-Out Voltage Linear Regulator**
  Adjustable Output Voltage (2.5V to 3.3V)
  350mA Maximum Output Current
- **On-Chip GPM Controller with Adjustable Falling Time**
  Flicker Compensator
  Power-On Sequence Control
- **Low Voltage Detector**
  Programmable Detecting Voltage and Delay Time
- **Unity-Gain Operation Amplifier for V_{COM} Buffer**
- **Over-Temperature Protection**
- **Thin 24-Lead VQFN Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Marking Information

For marking information, contact our sales representative directly or through a RichTek distributor located in your area, otherwise visit our website for detail.

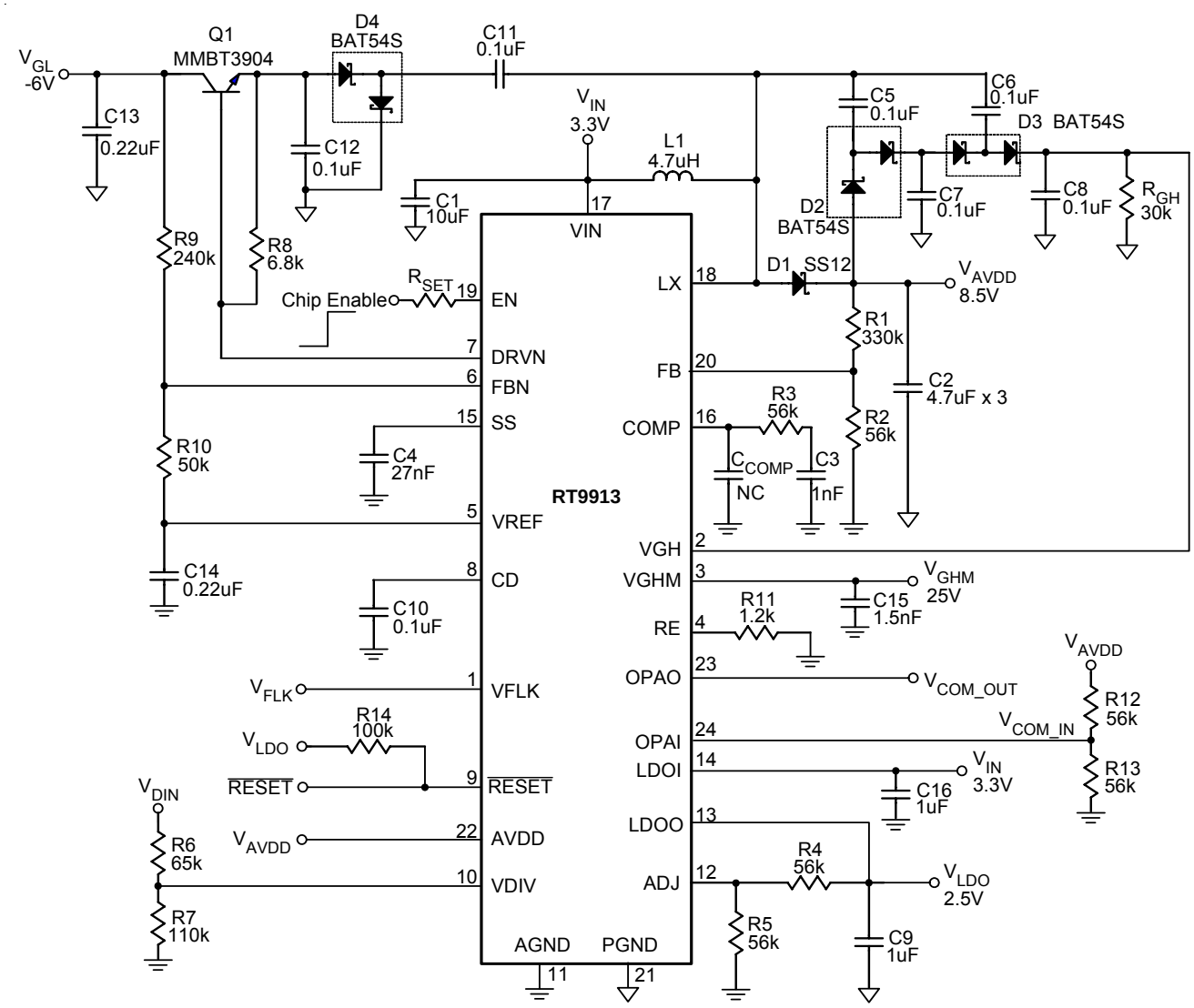
Pin Configurations

(TOP VIEW)



VQFN-24L 4x4

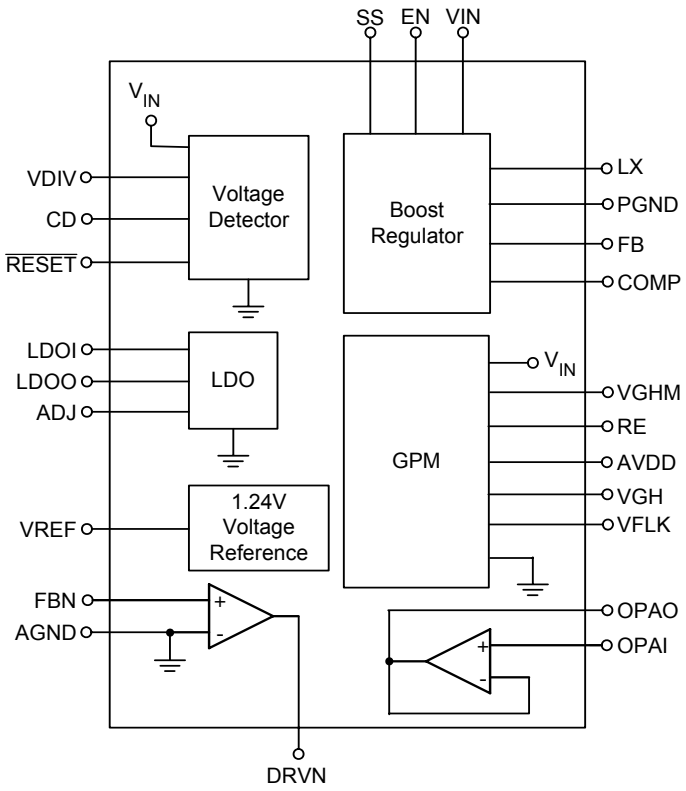
Typical Application Circuit



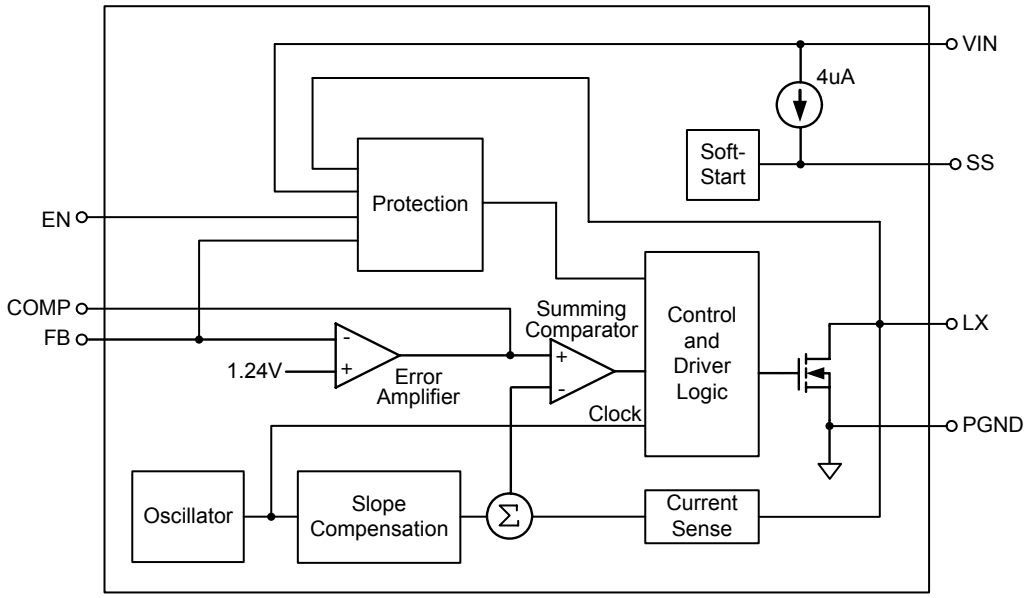
Functional Pin Description

Pin Number	Pin Name	Pin Function
1	VFLK	VFLK is produced by timing controller for charging or discharging VGHM.
2	VGH	Switch input for charge VGHM
3	VGHM	VGHM is the supply voltage for the gate driver ICs.
4	RE	Switch input for discharge VGHM
5	VREF	Internal Reference Bypass Terminal. Connect a 0.22uF ceramic capacitor from the VREF to analog ground (AGND). The source capability is 100uA.
6	FBN	Negative Linear-Regulator Feedback Input. Connect FBN to the center of a resistive voltage-divider between the negative output voltage VGL and the VREF to set the negative linear-regulator output voltage. Place the resistive voltage-divider close to the pin.
7	DRVN	Negative Linear-Regulator Base Drive. Open drain of an internal PMOS. Connect DRVN to the base of the external linear-regulator NPN pass transistor.
8	CD	Pin for external capacitor setting the delay time for voltage detector reset delay time.
9	$\overline{\text{RESET}}$	Voltage Detector open-drain Output for Reset.
10	VDIV	Voltage Detector Divider Input. Connect VDIV to the center of a resistive voltage-divider between the detected voltage input (VDIN) and analog ground (AGND).
11	AGND	Analog Ground.
12	ADJ	Low-Dropout Linear Regulator (LDO) Feedback Input. ADJ regulates to 1.24V nominal. Connect ADJ to the center of a resistive voltage-divider between the LDO output voltage LDOO and the analog ground (AGND) the LDO output voltage. Place the resistive voltage-divider close to the pin.
13	LDOO	Voltage Output of the LDO.
14	LDOI	Voltage Input of the LDO.
15	SS	Soft-Start Control Pin. Connect a soft-start capacitor (C_{SS}) to this pin. The soft-start capacitor is charged with a constant current 4uA.
16	COMP	Compensation Error Amplifier Pin. Connect a compensation network to ground.
17	VIN	Supply Input. The supply voltage powers all the control circuits including the boost converter, negative linear-regulator, gate pulse regulator and voltage detector.
18	LX	Switching pin. Drain of the internal power NMOS for the main step-up regulator.
19	EN	Active-High Enable Control Input and OCP level setting.
20	FB	Main Boost Regulator Feedback Input. FB regulates to 1.24V nominal. Connect FB to the center of a resistive voltage-divider between the main output AVDD and the analog ground (AGND) the boost regulator output voltage. Place the resistive voltage-divider close to the pin.
21	PGND	Power Ground. PGND is the source of the power NMOS.
22	AVDD	VDD for Source Driver Power. It also supplies OP power and GPM level shift voltage.
23	OPAO	Unit-Gain OPA Output Pin.
24	OPAI	Unit-Gain OPA Input Pin.
Exposed Pad	GND	Exposed pad should be soldered to PCB board and connected to GND.

Function Block Diagram



Boost Regulator Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 7V
- VGH-AVDD, VGHM-AVDD ---------- 18V
- LX ---------- –0.3V to 16V
- VGH, VGHM RE ---------- –0.3V to 30V
- AVDD ---------- –0.3V to 16V
- OPAI, OPAO ---------- –0.3V to (AVDD + 0.3V)
- DRVN ---------- (V_{IN} – 16V) to (V_{IN} + 0.3V)
- VFLK, VREF, FBN, CD, RESET_, VDIV, SS, COMP, EN, FB ---------- –0.3V to (V_{IN} + 0.3V)
- LDOI ---------- –0.3V to 7V
- ADJ, LDOO ---------- –0.3V to (LDOI + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-24L 4x4 ---------- 1.786W
- Package Thermal Resistance (Note 4)
  VQFN-24L 4x4, θ_{JA} ---------- 56°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- Junction Temperature ---------- 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 3.3V, V_{OUT} = 8.5V, T_A = 25°C, unless otherwise specification)

Parameter		Symbol	Test Condition	Min	Typ	Max	Units
System Supply							
Input Supply Voltage		V_{IN}		2.5	--	5.5	V
V_{IN} Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} rising	1.8	2.0	2.2	V
			Hysteresis	0.05	0.1	0.15	
V_{IN} Quiescent Current		I_Q	V_{FB} = 1.3V, LX no switching	0.15	0.4	1	mA
			V_{FB} = 1.1V, LX switching	1	2	3.5	mA
Shut Down Current		I_{IN}	V_{IN} = 3.3V	--	1	5	μA
EN Threshold	Logic-High Voltage	V_{IH}		--	--	1.5	V
	Logic-Low Voltage	V_{IL}		0.8	--	--	
Main Boost Regulator							
Operation Frequency		F_{OSC}	RT9913 A	--	640	--	kHz
			RT9913 B	0.9	1.2	1.4	MHz
Maximum Duty Cycle				86	90	94	%

To be continued

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	No load, T_A = 25°C	1.22	1.24	1.26	V
FB Input Bias Current		V_{FB} = 1.5V	-40	--	+40	nA
Transconductance of Error Amplifier	Gm	I_{COMP} = 5μA	--	160	--	μA/V
Voltage Gain of Error Amplifier	A_V		--	700	--	V/V
Feedback Voltage Line Regulation		V_{IN} = 2.5V to 5.5V	--	0.1	0.15	%/V
Output Voltage Load Regulation		V_{IN} = 3.3V, I_{LOAD} = 20 to 200mA	–1	--	0	%
LX ON-Resistance	$R_{LX(ON)}$		50	200	500	mΩ
Current Sense Transresistance			--	0.5	--	A/V
Soft-Start Charge Current	I_{SS}		2	4	6	μA
Thermal Shutdown Temperature	T_{SD}		--	170	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C
Current Limit	I_{LIM}		--	2	--	A
Gate-Off Regulation Controller						
V_{REF} source current capability	I_{REF}		--	100	1000	μA
FBN Regulation Voltage	V_{FBN}		–20	0	20	mV
FBN Effective Load Regulation Error		V_{DRVN} = –10V, I_{DRVN} = 50uA to 1mA	–30	–5	0	mV
FBN Line Regulation Error		I_{DRVN} = 0.1mA, 2.5V<V_{IN}<5.5V	--	1	6	mV
DRVN Source Current	I_{DRVN}		1	4	6	mA
Power-On-Delay Time	T_{VGL}	Refer to V_{FB} > 1V	25	32	39	ms
Low Drop-Out Linear Regulator (LDO)						
Input Voltage	V_{LDOI}		2.5	--	5.5	V
Dropout Voltage	V_{DROP}	V_{IN} = 3.3V, I_{OUT} = 350mA	200	300	500	mV
Feedback Voltage	V_{ADJ}		1.22	1.24	1.26	V
Current Limit	I_{LIM}		350	500	650	mA
Quiescent Current	I_{LDO}		--	60	100	μA
Line Regulation		V_{IN} = 2.8V to 5.5V, I_{OUT} = 100mA, V_{LDO} = 2.5V	--	0.1	0.3	%/V
Load Regulation		I_{OUT} = 1mA to 300mA	0	0.2	0.5	%
Gate Pulse Modulator						
VFLK Input High Voltage	V_{IH_FLK}		1.5	--	--	V
VFLK Input Low Voltage	$V_{IL\ FLK}$		--	--	0.6	V
Power-On-Delay Time (Note 5)	T_{VGHM}	Refer to V_{FB} > 1V	50	64	78	ms

To be continued

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Gate Pulse Modulator							
VGH Switch On-Resistance	RP1			10	30	50	Ω
RE Switch On-Resistance	RN2			10	25	50	Ω
Voltage Detector							
Minimum Operating Voltage				1.6	--	--	V
Detecting voltage adjustment	V_{DIV}			--	1.1	--	V
Detecting voltage accuracy				−2%	--	2%	%
Adjustable delay time-constant	k	t_D = k(Ω)*C10(F)		80k	120k	160k	Ω
V_{COM} Buffer							
Supply Voltage Range	V_{SUP}			AVDD	--	15	V
Supply Current	I_{OP}			--	0.5	0.9	mA
Input Offset Voltage	V_{OS}	V_{COM} = AVDD/2, T_A = 25°C		−15	0	15	mV
Input Bias Current	I_{BIAS}			--	1	50	nA
Output Voltage Swing High	V_{OH}	I_{OUT} = 100μA		AVDD-20	AVDD-5	--	mV
		I_{OUT} = 75mA		AVDD-1.5	AVDD-1.3	--	V
Output Voltage Swing Low	V_{OL}	I_{OUT} = −100μA		--	2	20	mV
		I_{OUT} = −75mA		--	1.5	1.8	V
Short-Circuit Current		To AVDD/2	Source	100	140	180	mA
			Sink	100	140	180	mA
-3dB Bandwidth	F_{3db}			--	12	--	MHz
Gain Bandwidth Product	GBW			--	8	--	MHz
Slew Rate	SR			8	12	16	V/μs

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

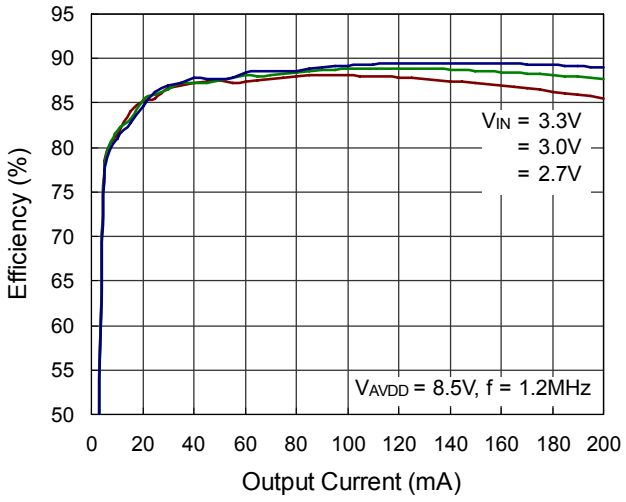
Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

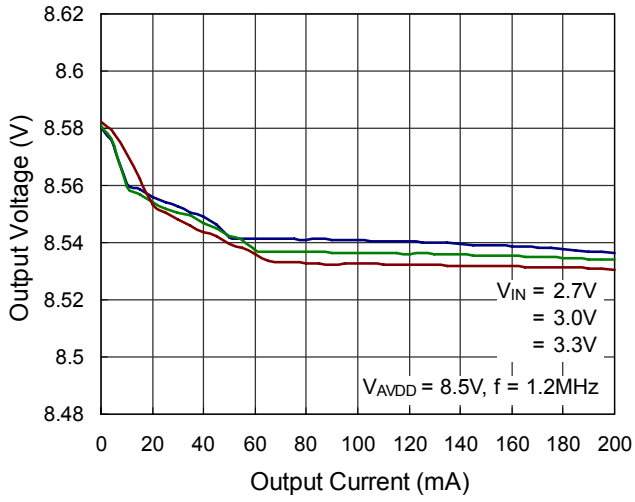
Note 5. It is guaranteed by design.

Typical Application Circuit

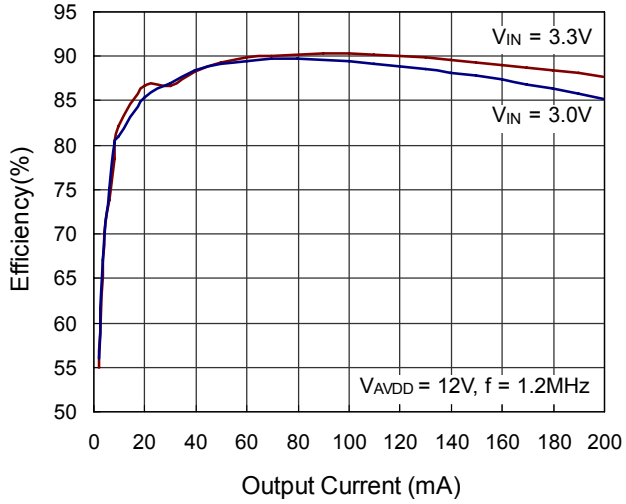
Boost Efficiency vs. Output Current



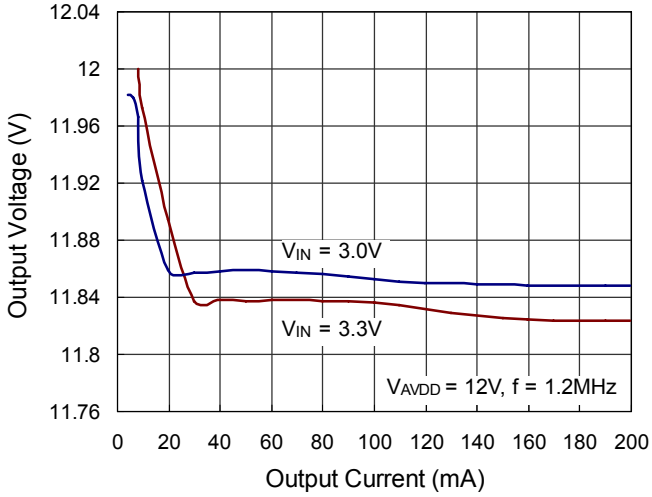
Boost Output Voltage vs. Output Current



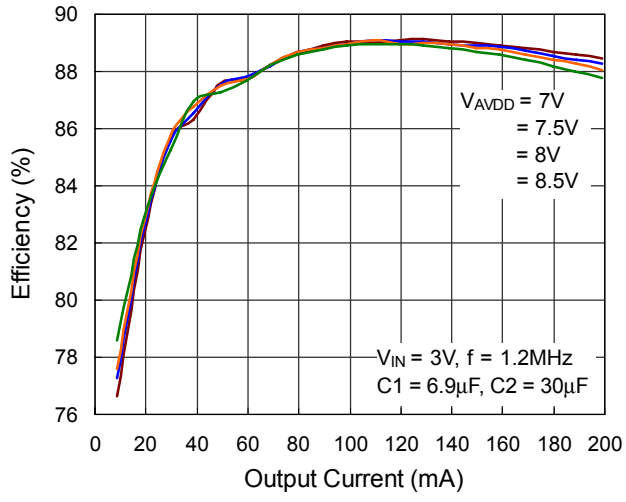
Boost Efficiency vs. Output Current



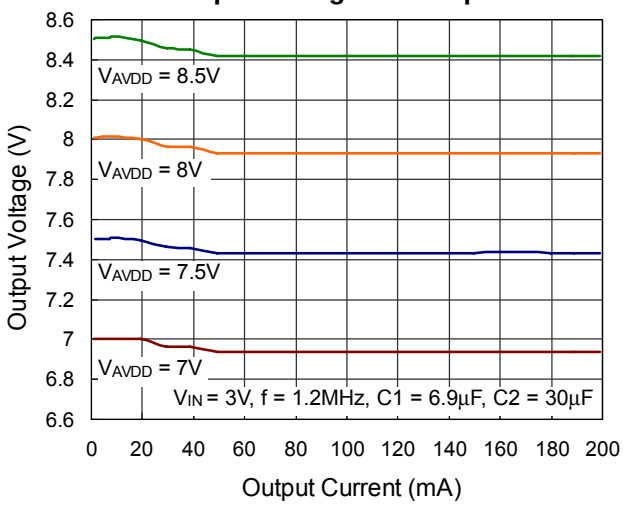
Boost Output Voltage vs. Output Current



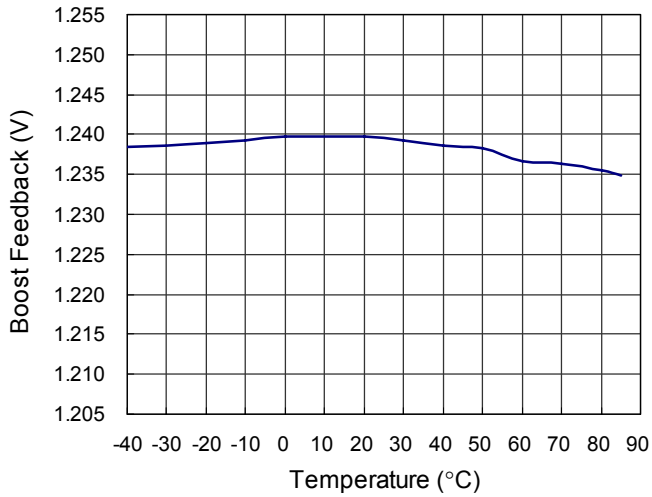
Boost Efficiency vs. Output Current



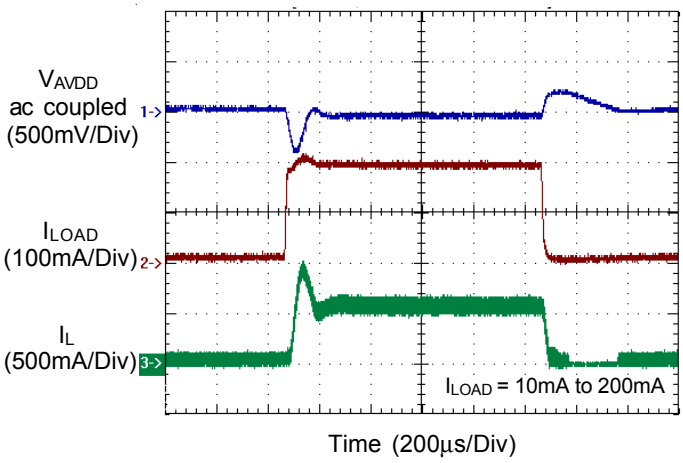
Boost Output Voltage vs. Output Current



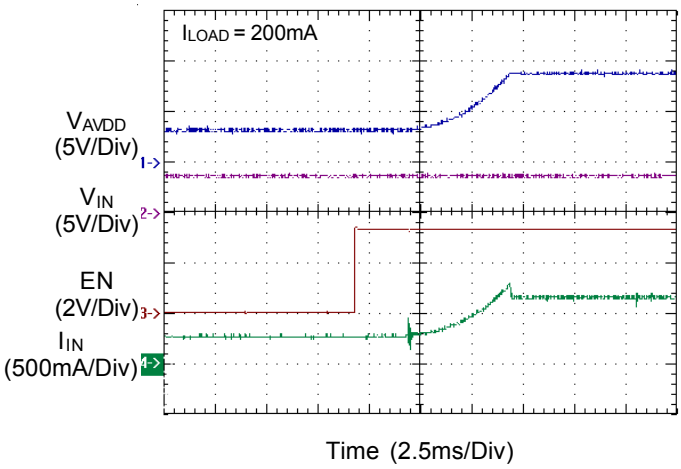
Boost Feedback vs. Temperature



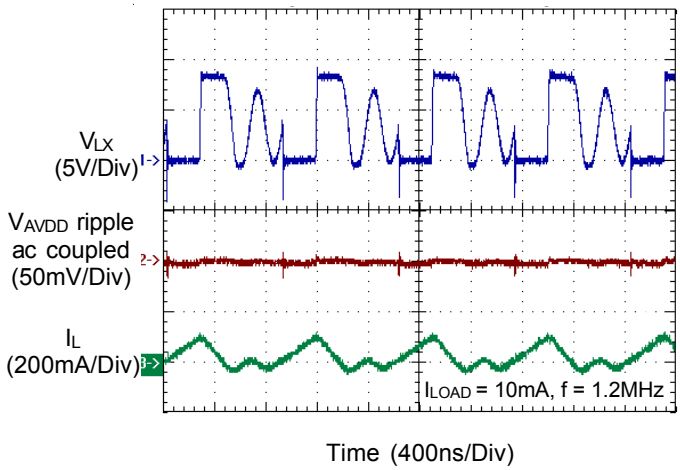
Boost Regulator Load Transient Response



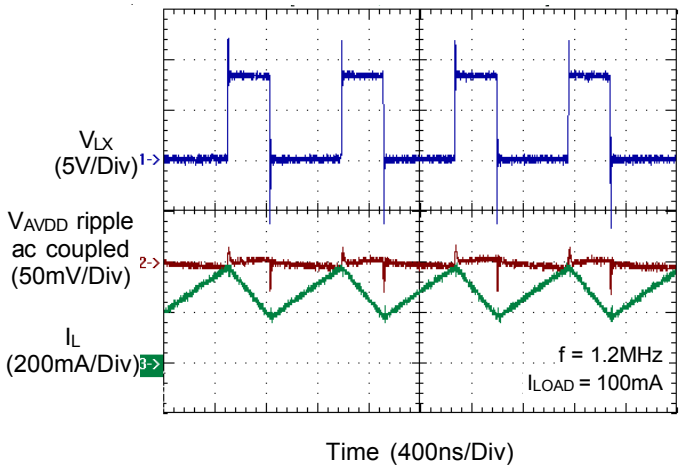
Boost Regulator Soft-Start



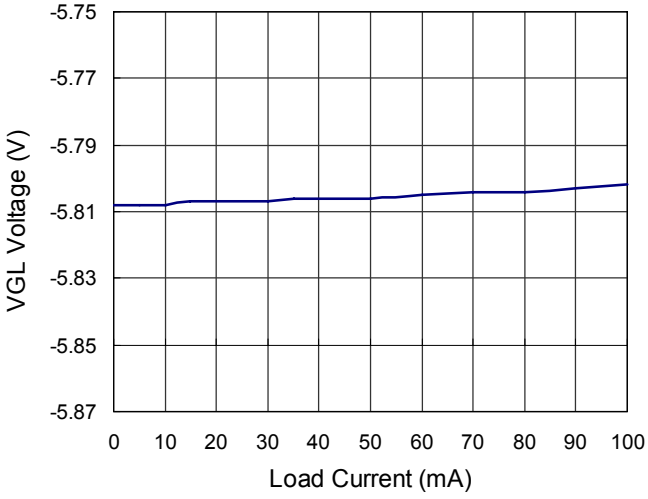
Boost Regulator Stability



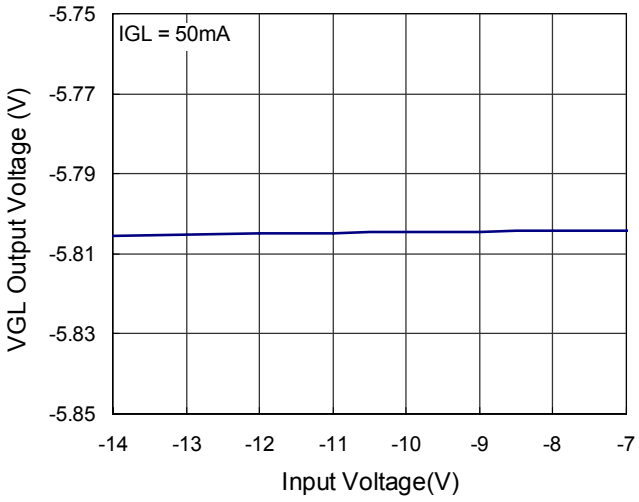
Boost Regulator Stability



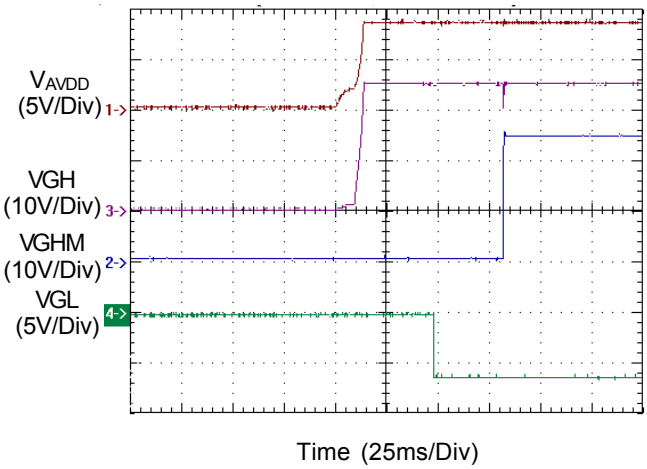
VGL Regulator Load Regulation



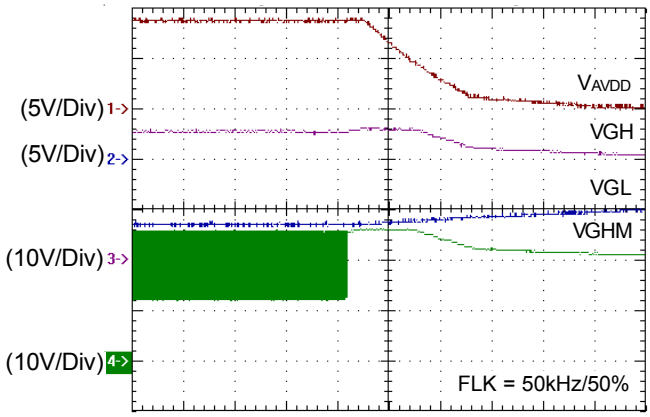
VGL Regulator Line Regulation



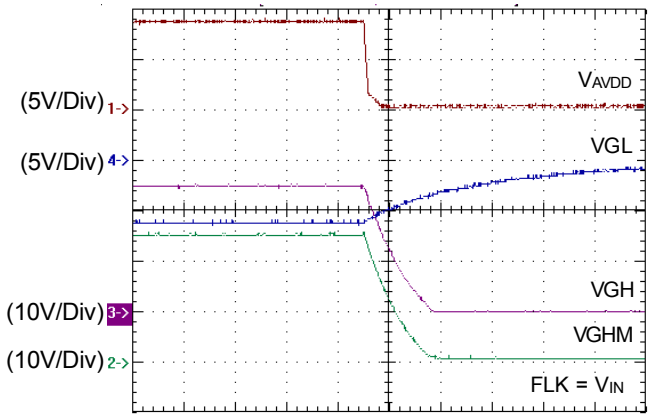
Power On Sequence



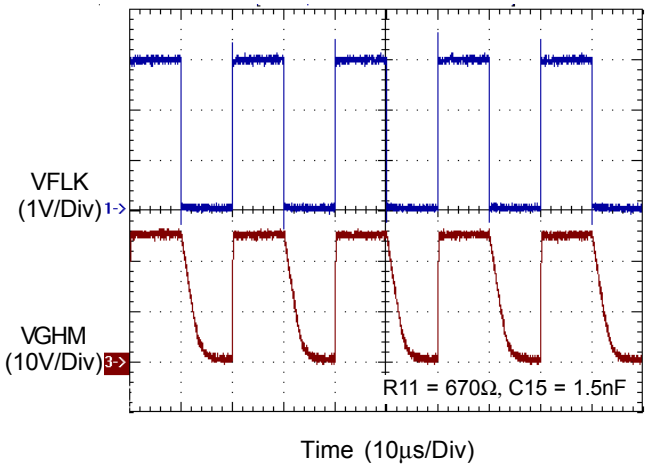
Power Off Sequence with GPM Function



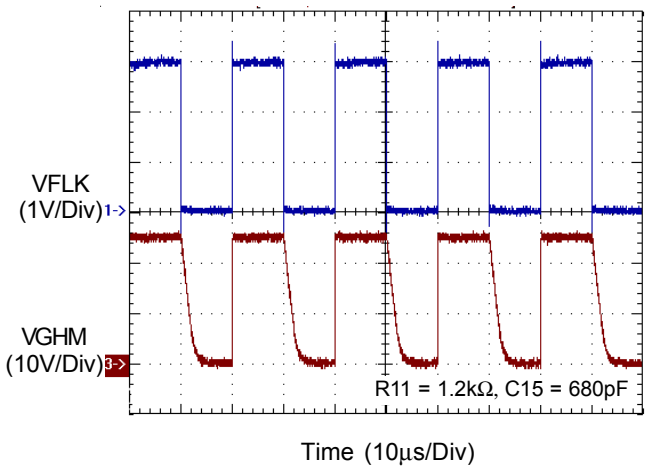
Power Off Sequence



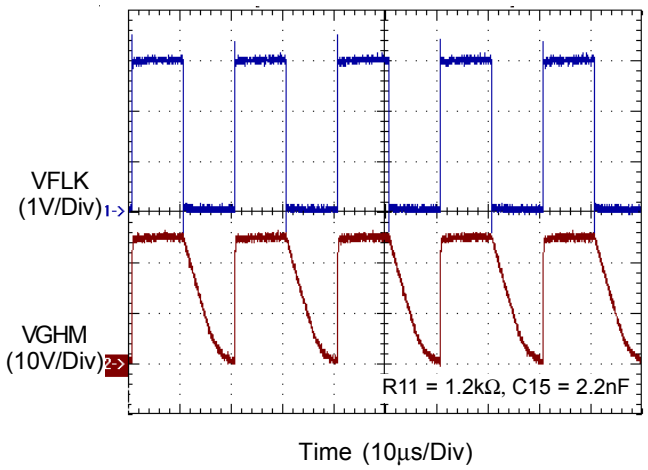
VGHM



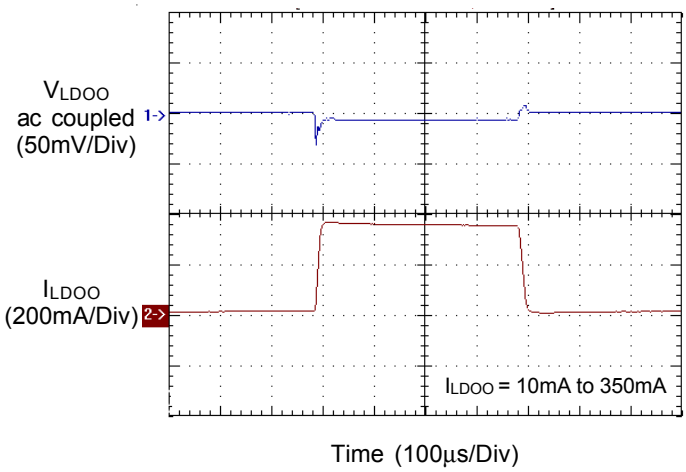
VGHM



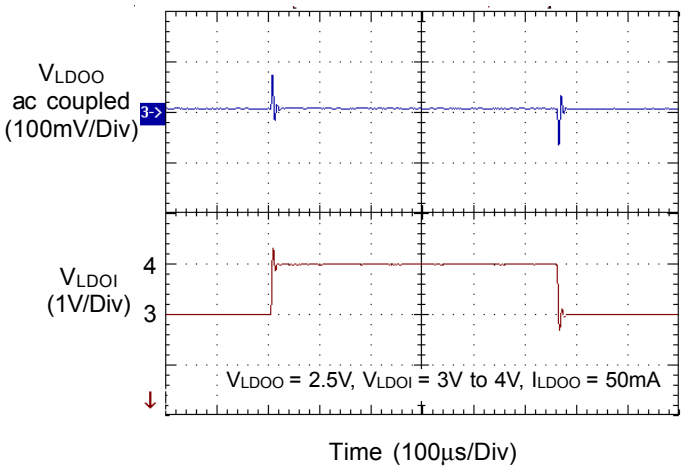
VGHM



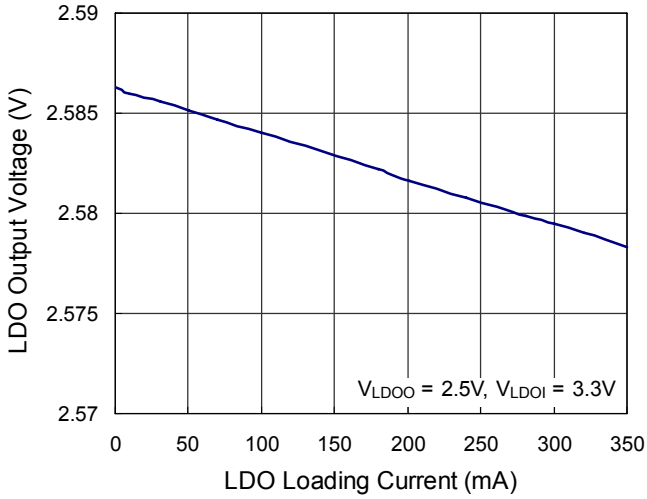
LDO Load Transient



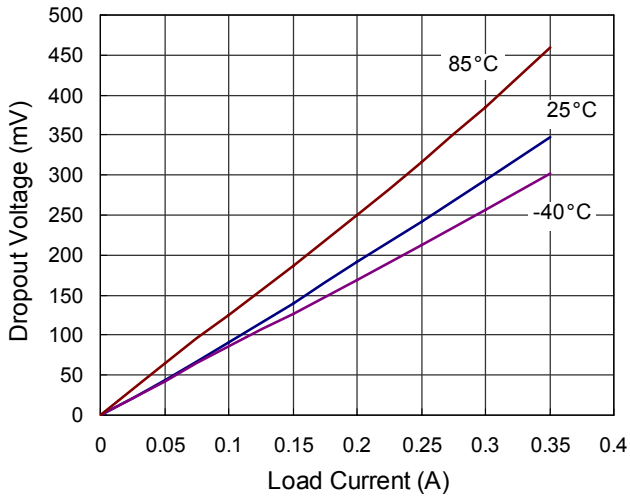
LDO Line Transient



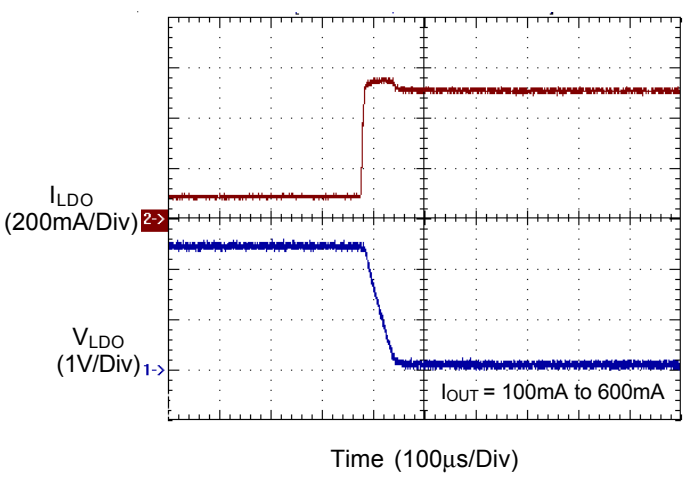
LDO Load Regulation



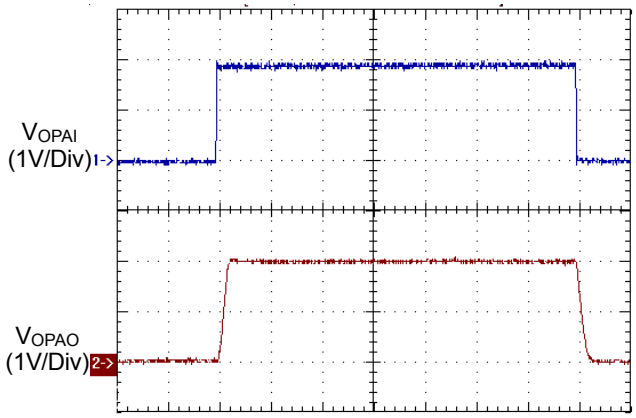
LDO Dropout Voltage



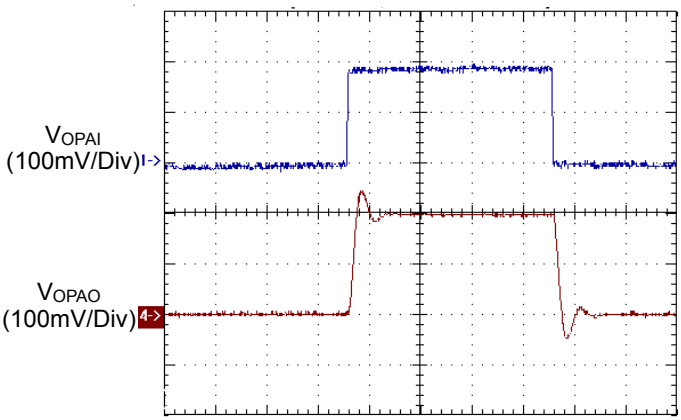
LDO OCP



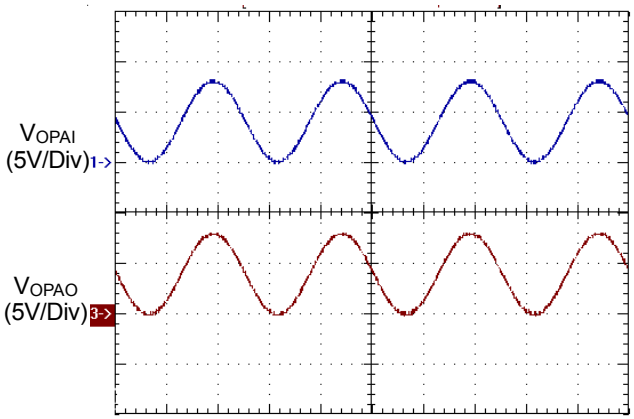
OPA Large-Signal Step Response



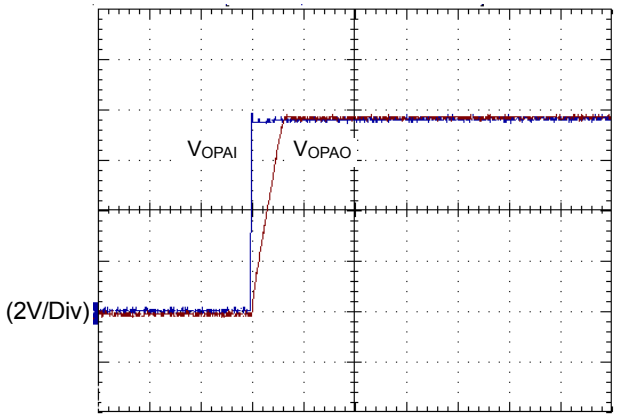
OPA Small-Signal Step Response



OPA Rail-to-Rail Input/Output



OPA Slew Rate



Application Information

The RT9913 contains a high performance boost regulator to generate voltage for output voltage, gate-on driver and negative voltage regulated by linear regulator controller for gate-off driver. It also includes of a high-current rail-to-rail operation amplifier, a gate pulse modulator (GPM), a programmable timing control voltage detector, and a low dropout linear regulator. The following content contains the detailed description and the information of component selection.

Boost Regulator

The boost regulator is a high efficiency current-mode PWM architecture with 1.2MHz or 640kHz operation frequency. It performs fast transient responses to generate gate driver supplies for TFT LCD display. The high operation frequency allows smaller components used to minimize the thickness of LCD panel. To regulate the output voltage is to set resistive voltage-divider sensing at FB pin. The error amplifier varies the COMP voltage by sensing FB pin to regulate the output voltage. For better stability, the slope compensation signal summed with the current-sense signal will be compared with the COMP voltage to determine the current trip point and duty cycle.

Soft-Start

The RT9913 provides soft-start function to minimize the inrush current. When EN pin is connected to high, an internal constant current charges an external capacitor. The rising voltage rate on COMP pin is limited during the charging period and the inductor peak current also limited at the same time. In the meanwhile, the frequency increases slowly at the beginning. When the EN pin is connected to GND, the external capacitor will be discharged for next soft start time.

The soft-start function is implemented by the external capacitor with a 4μA constant current charging to the soft-start capacitor. Therefore, the capacitor should be large enough for output voltage regulation. Typical value for soft-start capacitor range is 27nF. The available soft start capacitor range is from 10nF to 200nF.

Inductor Selection & Maximum output current capability

The minimum inductance value, peak current rating and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient-response time and output voltage ripple. Physical size and cost are also important factors to be considered. The maximum output current, input voltage, output voltage and switching frequency determine the inductor value. Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size but increase the current ripple and peak current.

Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size and cost.

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using the following equation.

$$I_{IN(DC,MAX)} = \frac{I_{AVDD(MAX)} \times V_{AVDD}}{V_{IN(MIN)} \times \eta(MIN)}$$

The expected efficiency at that operating point (η_{MIN}) can be taken from an appropriate curve in the Typical Operating Characteristics. Calculate the ripple current at that operating point and the peak current required for the inductor :

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times (V_{AVDD} - V_{IN(MIN)})}{L \times V_{AVDD} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the LX over-current protection (I_{OCP}) should exceed I_{PEAK} and the inductor DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choosing an inductor with less than 0.1Ω series resistance is suggested.

Diode Selection

To achieve high efficiency, Schottky diode is the recommended diode for lower forward drop voltage and faster switching time. The output diode rating should be large enough for maximum output voltage, average power dissipation and the pulsating diode peak current.

Output Capacitor Selection

For lower output voltage ripple, low-ESR ceramic capacitor is recommended. The output voltage ripple consists of two components: one is the pulsating output ripple current flowing through the ESR, and the other is the capacitive ripple caused by charging and discharging.

$$V_{RIPPLE} = V_{RIPPLE\_ESR} + V_{RIPPLE\_C}$$

$$\cong I_{PEAK} \times R_{ESR} + \frac{I_{PEAK}}{C_{OUT}} \left(\frac{V_{AVDD} - V_{IN}}{V_{AVDD} \times f} \right)$$

Input Capacitor Selection

For better input bypassing, low-ESR ceramic capacitor is recommended for better performance. A 10μF input capacitor is sufficient and it is flexible to reduce the value for a lower output power requirement.

Output Voltage

The regulated output voltage is the following formula :

$$V_{OUT} = 1.24V \times \left(1 + \frac{R1}{R2}\right)$$

The recommended value for R2 should be up to 100kΩ without some sacrificing. To place the resistor-divider as close as possible to the chip can reduce noise sensitivity.

Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisted of R3, C3 and C_{COMP} (As Figure 1). Choose R3 to set high frequency integrator gain for fast transient response and C3 to set the integrator zero to maintain loop stability.

Place C_{COMP} between COMP and GND to add an additional high-frequecncy pole. The value is between 10pF and 47pF. For typical application V_{IN} = 3.3V , V_{OUT} = 8.5V ,C_{OUT} = 4.7μF x 3 , L = 4.7μH, the recommened value for compensation is as below:

R3 = 56kΩ , C3 = 1nF , Ccomp=NC

Over Current Protection

The RT9913 main boost converter has over-current protection to limit peak inductor current. It prevents large current damaging the inductor and diode. During the ON-time, once the inductor current exceeds the current limit, the internal LX switch turns off immediately and shortens the duty cycle. Therefore, the output voltage drops if the over-current condition occurs. Actual current limit is always larger than nominal value because of the internal circuit delay. Current limit is also affected by the input voltage, duty cycle, and inductor value. The following figure shows the different over-current settings and the corresponding R_{SET} resistance while OCP function works and V_{AVDD} falls to 90%.

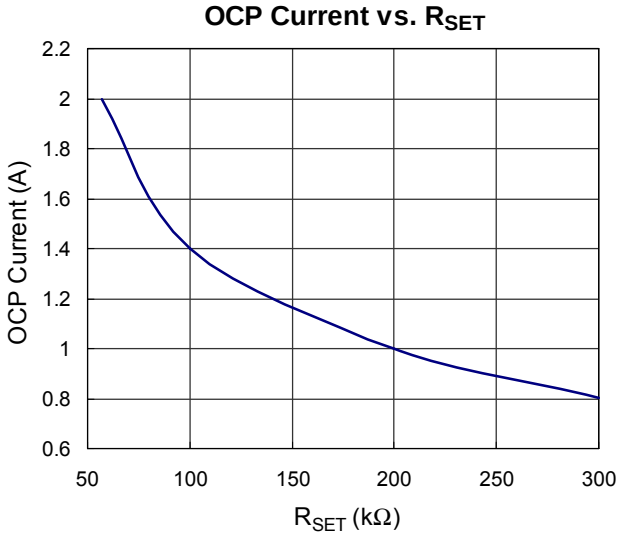


Figure 1. OCP settings versus R_{SET} @ V_{EN} = 2.5V

Over Temperature Protection

The RT9913 main boost converter has thermal protection function to prevent the excessive power dissipation from overheating. When the junction temperature exceeds 170°C, it will shut down the device. Once the device cools down by approximately 20°C, it will start to operate normally. For continuous operation, do not operate over the maximum junction temperature rating around 150°C.

Gate-Low Linear Regulator Controller

The gate-low linear regulator controller is to provide the TFT-LCD gate off voltage. One stage charge pump can provide a negative voltage. Using the gate-low regulator after the produced negative voltage can regulate the exceeded voltage. With a 6.8kΩ base to emitter resistor it can drive an extra NPN pass transistor and at least 4mA source current. V_{GL} can be regulated by the voltage-divider resistor and 0.22μF ceramic output capacitor. The output load current (I_{LOAD}) can be decided by the current gain (β), drive current (I_{DRVN}), base-to-emitter forward voltage drop (V_{BE}) and base-to-emitter resistor (R8) as the following equation :

$$I_{LOAD} = \beta(I_{DRVN} - \frac{V_{BE}}{R8})$$

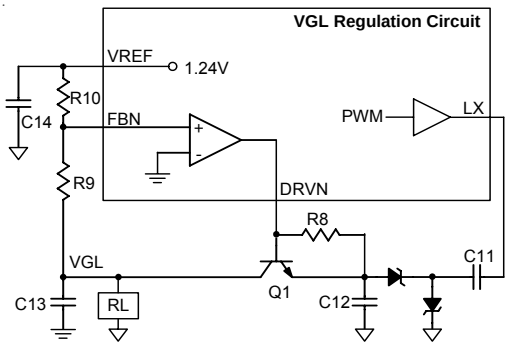


Figure 2

The VGL regulator controls the intermediate charge-pump stage and regulates the final charge-pump's output voltage as the following equation :

$VGL = -V_{REF}(R9/R10)$

Zener Diode for the Negative Regulator

Instead of the gate-low linear regulator controller, bypassing a zener diode(ZD1) after the charge-pump satge can also stable the negative voltage. However, for better efficiency, using the gate-low linear regulator controller is recommended.

$V_{GL} = -(V_{AVDD} - V_D)$

V_D : forward voltage drop of the charge pump diode

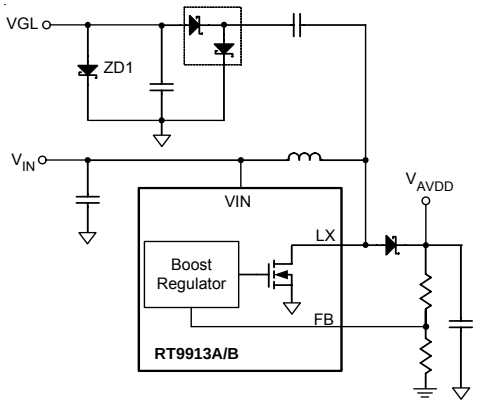


Figure 3

GPM

The GPM function is controlled by frame signals from timing controller to modulate the Gate-On voltage (VGHM). According to the different loading capacitor (C16), the falling slope of the Gate-On voltage is programmable by an external resistor (R11) .The V_{GL} lags 32ms (typ.) behind AVDD and the VGHM lags 64ms (typ.) behind AVDD while power on.

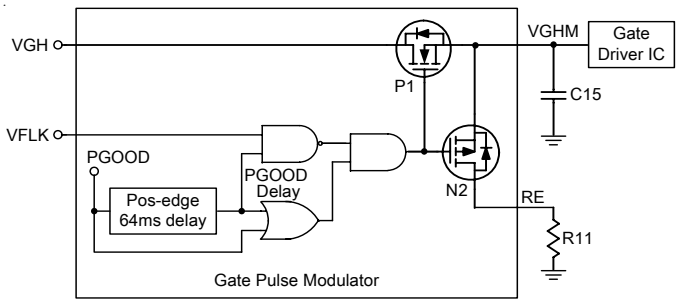


Figure 4

The GPM operation sequence is shown in Figure 5. PGOOD is the logic signal detecting the feedback voltage (V_{FB}). If V_{FB} is below 1V, PGOOD becomes low ; otherwise, PGOOD is high while V_{FB} is above 1V. When PGOOD is high lasting more than 64ms, PGOOD Delay signal is built and then VGHM is controled by V_{FLK} signal.

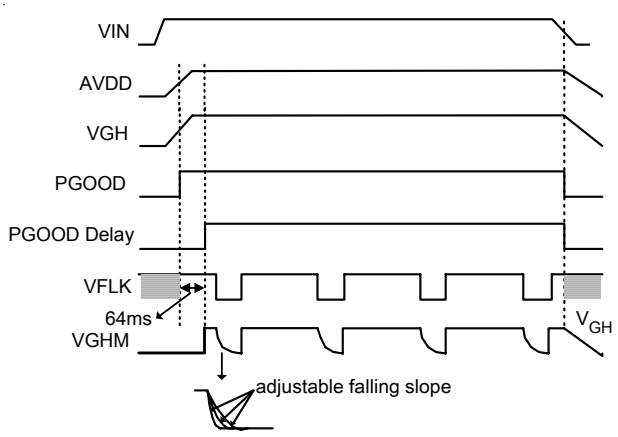


Figure 5

GPM for Power Sequence

The GPM function also achieves the power-on sequence control. The GPM internal delay time (64ms) can be used for VGH built-up delay. The application circuit is shown in Figure 6 connecting input voltage to V_{FLK} and bypassing a 1uF to VGHM .VGH will lag 64ms after V_{AVDD} built.

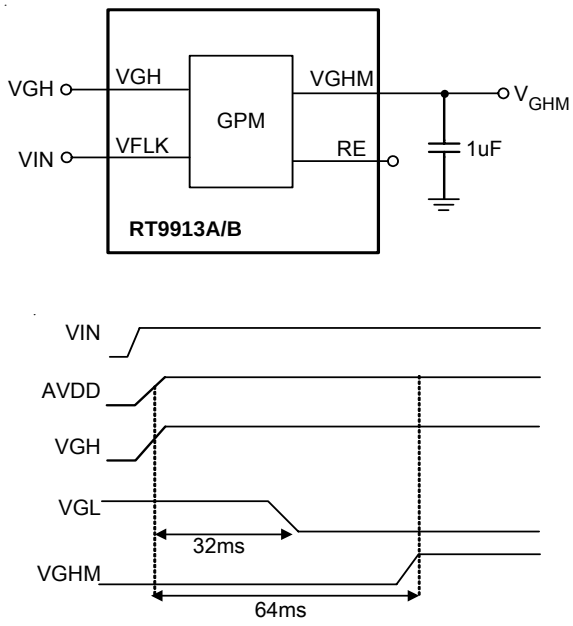


Figure 6

Charge Pumps

The charge pump stages can be achieved by the flying capacitors and the Schottky diodes. According to the application circuit, the positive and negative charge-pump output voltages can be determined by the following equations :

$V_{GH} = 3V_{AVDD} - 2V_D$

V_D : the forward voltage drop of the charge pump diodes

The flying capacitor requires the voltage rating larger than 16V and 0.1uF ceramic capacitors are enough for the low-current applications (10mA) . Besides, Schottky diodes with a current rating should equal to or greater than two times the average charge-pump input current. Note that the voltage difference between VGH (VGHM) and AVDD should not exceed 18V.

Operational Amplifier

The operational amplifier to drive the LCD backplane V_{COM}. The operational amplifier features +/- 140mA output short-circuit current, 12V/μs slew rate, and 12MHz bandwidth.

An internal short-circuit protection circuit is implemented to protect the device from output short circuit. The operational amplifier limits the short circuit current while the output is directly shorted.

LDO

The low-dropout linear regulator (LDO) can supply up to 350mA current while input voltage is 3.3V. It uses an internal PMOS as the pass device. The output current limitation is 500mA. It is suitable for the supply voltage for the T-CON ASIC.

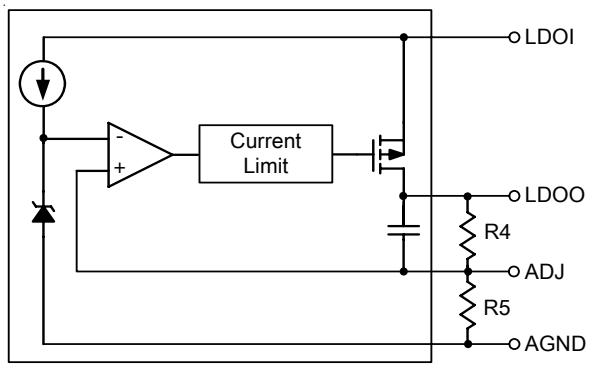


Figure 7

Voltage Detector

The voltage detector monitors the VDIN voltage to generate a reset signal while VDIN is lower than the detecting level. The detecting level is decided by an external resistor divider.

$V_{DET} = V_{REF2}$ (1+R6/R7) = 1.1V x (1+R6/R7)

V_{HYS} = 50mV (1+R6/R7)

The delay time is programmable by an external capacitor (C10) as equation. For example, setting C10 = 100nF can generate 12ms delay for reset signal.

t_D = 120k x C10

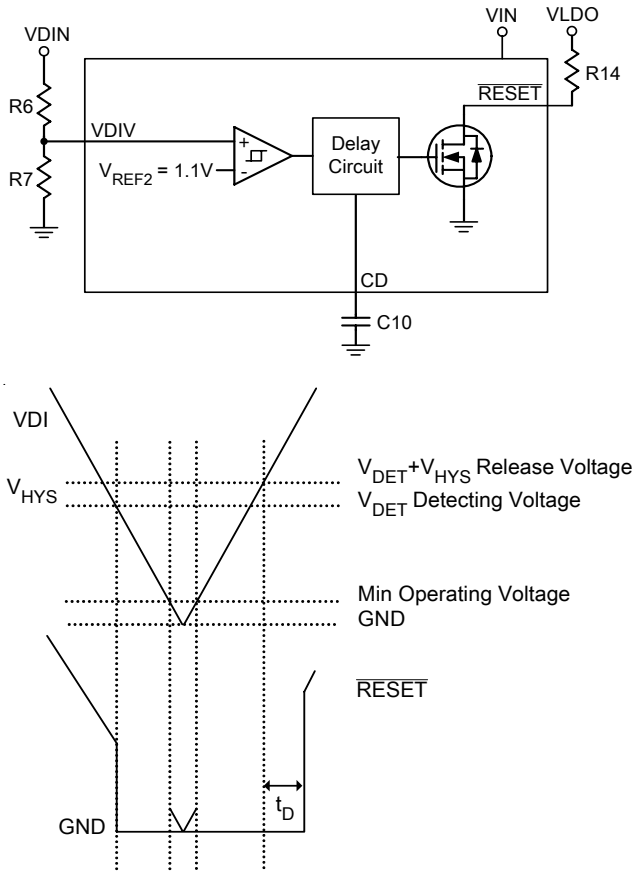


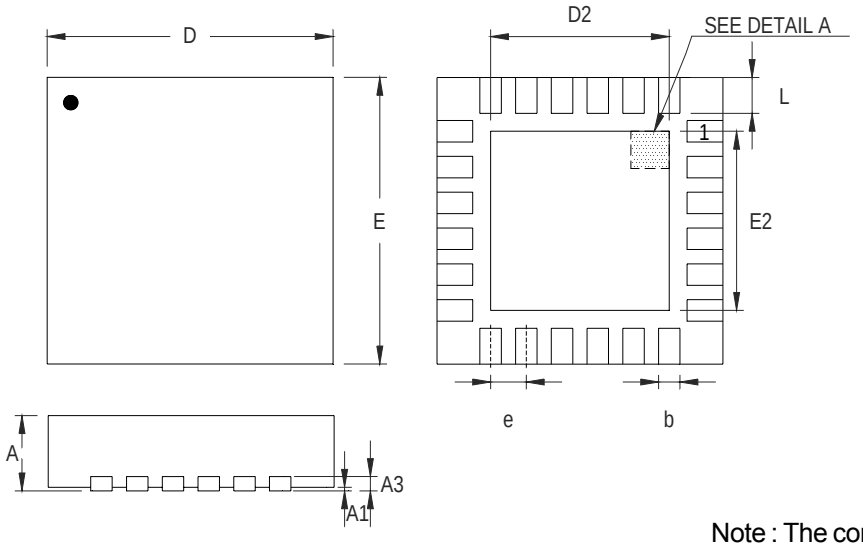
Figure 8

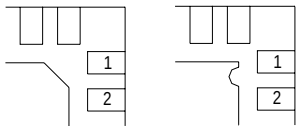
Layout Guideline

For high frequency switching power supplies, the PCB layout is important to get good regulation, high efficiency and stability. The following descriptions are the guidelines for better PCB layout.

- For good regulation place the power components as close as possible. The traces should be wide and short especially for the high-current output loop.
- The current limit setting resistor R_{SET} must be near the EN pin, The trace must be shorter and avoid the trace near any switching nodes.
- The feedback voltage-divider resistors must be near the feedback pin. The divider center trace must be shorter and avoid the trace near any switching nodes.
- The compensation circuit should be kept away from the power loops and be shielded with a ground trace to prevent any noise coupling.
- Minimize the size of the Lx node and keep it wide and shorter. Keep the Lx node away from the FB and analog ground.
- The power ground (PGND) consists input and output capacitor grounds, the components' ground of charge pump and GPM. The PGND should be wide and short connected to a ground plane.
- The analog ground (AGND) consists the grounds of compensation, soft-stat capacitor, FB divider, and OP divider. The AGND should be separated from PGND and connected to the ground of the input capacitor.
- The exposed pad of the chip should be connected to ground plane for thermal consideration.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	2.300	2.750	0.091	0.108
E	3.950	4.050	0.156	0.159
E2	2.300	2.750	0.091	0.108
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 24L QFN 4x4 Package

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