Power Management IC for SSD

General Description

The RT9991 is a 3-CH PMIC for SSD (Solid-State Drive). It integrates 3 synchronous buck converters and one voltage detector.

The RT9991 provides 3 independent enable pins for sequence control and auto discharge when powered off on the power line of a NAND Flash.

The frequency can be up to 1.5MHz for Buck 1and Buck 2, and up to 2MHz for Buck 3, hence allowing the use of smaller sized inductors to meet the space and height limit in handheld applications.

To maximize power utilization, the RT9991 is designed with extremely low quiescent current. The buck converter can consume down to 70µA when operating in standby mode.

The RT9991 is available in a VQFN-32L 5x5 package.

Ordering Information

RT9991☐☐

Package Type
QV : VQFN-32L 5x5 (V-Type)

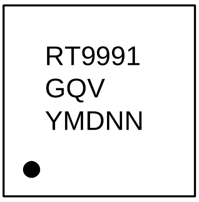
Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



RT9991GQV : Product Number

YMDNN : Date Code

Features

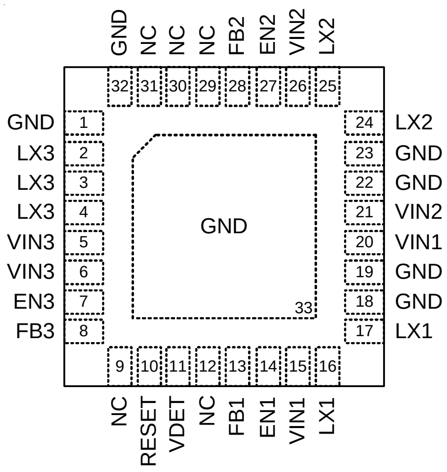
- **Supply Input Voltage Range : 2.8V to 5.5V**
- **Buck 1 / Buck 2**
  - **Adjustable Output Voltage for V_{CORE} or DRAM Cache**
  - **Output Current up to 1A**
  - **Switching Frequency : 1.5MHz**
- **Buck 3**
  - **Adjustable Output Version for NAND Flash**
  - **Output Current up to 3A**
  - **Switching Frequency : 2MHz**
  - **Auto Discharge Function**
- **Voltage Detector**
  - **Programmable Threshold Voltage**
  - **Open-Drain Reset Output**
- **RoHS Compliant and Halogen Free**

Applications

- 1.8/2.5 inch Solid-State Drives
- Portable Devices
- USB-Based Hand-Held Products

Pin Configurations

(TOP VIEW)



VQFN-32L 5x5

Part Status

Part No	Status	Package	Lead Plating System
RT9991GQV	Lifebuy	VQFN-32L 5x5	G : Green (Halogen Free and Pb Free)

The part status values are defined as follows:

Active: Device is in production and is recommended for new designs.

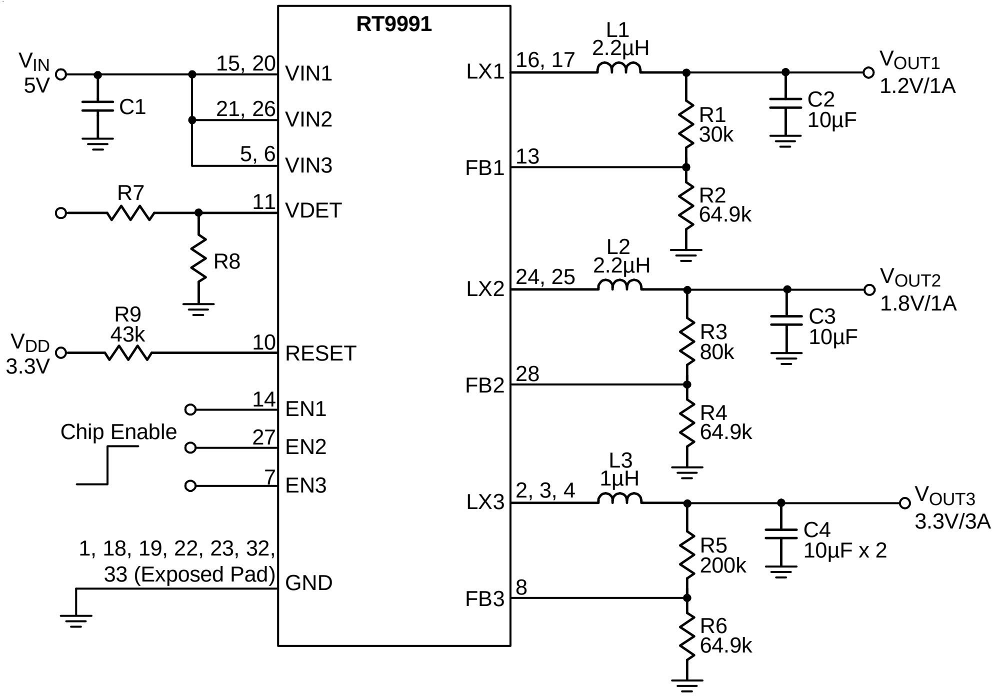
Lifebuy: The device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs.

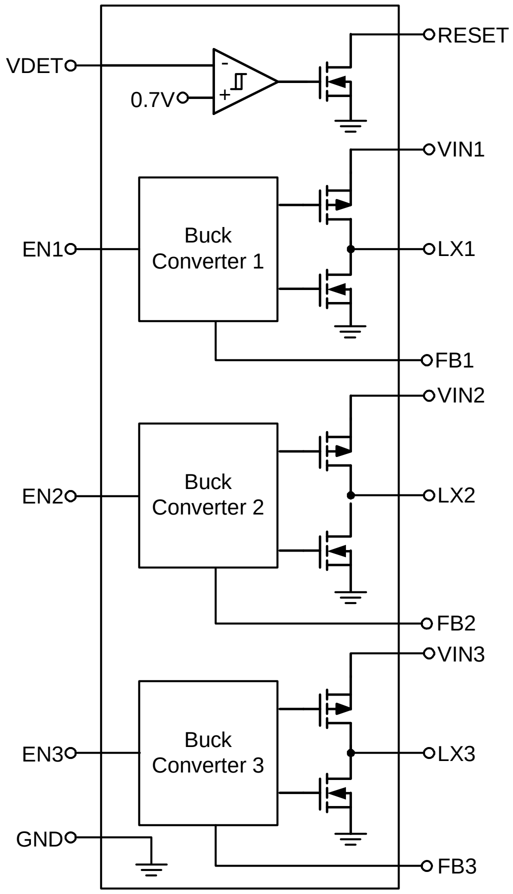
Preview: Device has been announced but is not in production.

EOL: Richtek has discontinued the production of the device.

Typical Application Circuit



Function Block Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 18, 19, 22, 23, 32, 33 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
2, 3, 4	LX3	Buck Converter 3 Switch Output (inductor connection point).
5, 6	VIN3	Buck Converter 3 Power Supply Input.
7	EN3	Buck Converter 3 Chip Enable (Active High).
8	FB3	Buck Converter 3 Feedback Input.
9, 12, 29, 30, 31	NC	No Internal Connection.
10	RESET	Reset Output.
11	VDET	Threshold Voltage Detect Setting.
13	FB1	Buck Converter 1 Feedback Input.
14	EN1	Buck Converter 1 Chip Enable (Active High).
15, 20	VIN1	Buck Converter 1 Power Supply Input.
16, 17	LX1	Buck Converter 1 Switch Output (inductor connection point).
21, 26	VIN2	Buck Converter 2 Power Supply Input.
24, 25	LX2	Buck Converter 2 Switch Output (inductor connection point).
27	EN2	Buck Converter 2 Chip Enable (Active High).
28	FB2	Buck Converter 2 Feedback Input.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} -- –0.3V to 6.5V
- LX Pin Voltage -- –0.3V to (V_{IN} + 0.3V)
- Other Pins Voltage -- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-32L 5x5 -- 2.778W
- Package Thermal Resistance (Note 2)
  VQFN-32L 5x5, θ_{JA} -- 36°C/W
  VQFN-32L 5x5, θ_{JC} -- 6°C/W
- Lead Temperature (Soldering, 10 sec.) -- 260°C
- Junction Temperature -- 150°C
- Storage Temperature Range -- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) -- 2kV
  MM (Machine Mode) -- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} -- 2.8V to 5.5V
- Junction Temperature Range -- –40°C to 125°C
- Ambient Temperature Range -- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Buck Converter 1							
Quiescent Current		I_Q	No Load, No Switching	--	70	–	μA
Shutdown Current		I_{SHDN}	EN = GND	--	0.2	–	μA
Feedback Reference Voltage		V_{FB}		--	0.8	–	V
UVLO Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	--	2.1	–	V
			Hysteresis	--	0.1	–	
EN1 Threshold Voltage	Logic-High	V_{IH}		1.5	--	V_{IN}	V
	Logic-Low	V_{IL}		--	--	0.4	V
Peak Current Limit		I_{LIM}		1.3	1.7	–	A
Oscillator Frequency		f_{OSC}	V_{IN} = 3.6V, I_{OUT} = 300mA	1.2	1.5	1.8	MHz
Start-Up Time			I_{OUT} = 0mA. Time from active EN to 90% of V_{OUT}	--	250	–	μs
P-MOSFET On Resistance		$R_{DS(ON)\_P}$	V_{IN} = V_{GS} = 3.6V, PWM Mode	--	250	–	mΩ
N-MOSFET On Resistance		$R_{DS(ON)\_N}$	V_{IN} = V_{GS} = 3.6V, PWM Mode	--	260	–	mΩ
BUCK CONVERTER 2							
Quiescent Current		I_Q	No Load, No Switching	--	70	–	μA
Shutdown Current		I_{SHDN}	EN = GND	--	0.2	–	μA
Feedback Reference Voltage		V_{FB}		--	0.8	–	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
UVLO Under Voltage Lockout threshold		V_{UVLO}	V_{IN} Rising	--	2.1	--	V
			Hysteresis	--	0.1	--	
EN2 Threshold Voltage	Logic-High	V_{IH}		1.5	--	V_{IN}	V
	Logic-Low	V_{IL}		--	--	0.4	
Peak Current Limit		I_{LIM}		1.3	1.7	--	A
Oscillator Frequency		f_{OSC}	V_{IN} = 3.6V, I_{OUT} = 300mA	1.2	1.5	1.8	MHz
Start-Up Time			I_{OUT} = 0mA Time from active EN to 90% of V_{OUT}	--	250	--	µs
P-MOSFET On Resistance		$R_{DS(ON)\_P}$	V_{IN} = V_{GS} = 3.6V, PWM Mode	--	250	--	mΩ
N-MOSFET On Resistance		$R_{DS(ON)\_N}$	V_{IN} = V_{GS} = 3.6V, PWM Mode	--	260	--	mΩ
Buck Converter 3							
Quiescent Current		I_Q	No Load, No Switching	--	80	--	µA
Shutdown Current		I_{SHDN}	EN = GND	--	0.2	--	µA
Feedback Reference Voltage		V_{FB}			0.8	--	V
UVLO Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	--	2.4	--	V
			Hysteresis	--	0.1	--	
EN3 Threshold Voltage	Logic-High	V_{IH}		1.5	--	V_{IN}	V
	Logic-Low	V_{IL}		--	--	0.4	
Peak Current Limit		I_{LIM}		3.5	3.9	--	A
Oscillator Frequency		f_{OSC}	V_{IN} = 3.6V, I_{OUT} = 300mA	1.6	2	2.4	MHz
Start-Up Time			No Load. Time from active EN to 90% of V_{OUT}	2000	--	--	µs
P-MOSFET On Resistance		$R_{DS(ON)\_P}$	V_{IN} = V_{GS} = 3.6V, PWM Mode	--	110	--	mΩ
N-MOSFET On Resistance		$R_{DS(ON)\_N}$	V_{IN} = V_{GS} = 3.6V, PWM Mode	--	110	--	mΩ
Voltage Detector							
Voltage Detection Threshold			V_{IN} Rising (L to H)	0.693	0.7	0.707	V
			V_{IN} Falling (H to L)	0.673	0.68	0.687	
Voltage Detection Delay Time			V_{Delay} (L to H)	70	100	130	ms
			V_{Delay} (H to L)	5	10	20	µs
Thermal Protections							
Thermal Shutdown Threshold		T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	25	--	°C

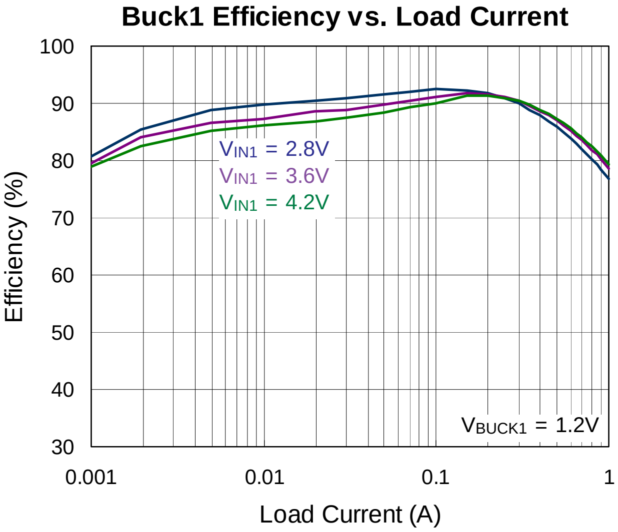
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

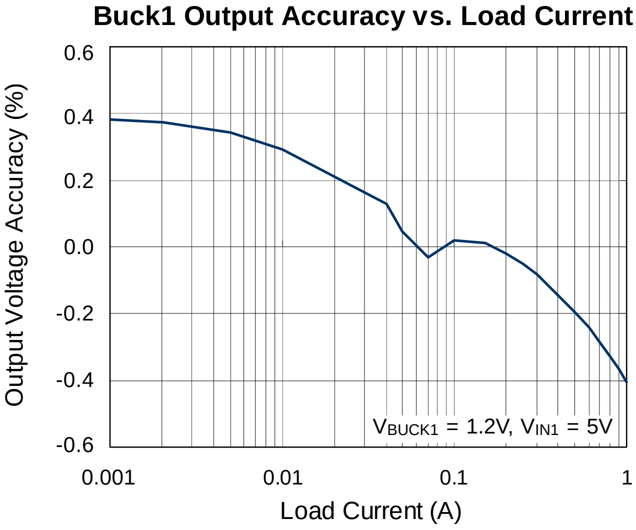
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high-effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

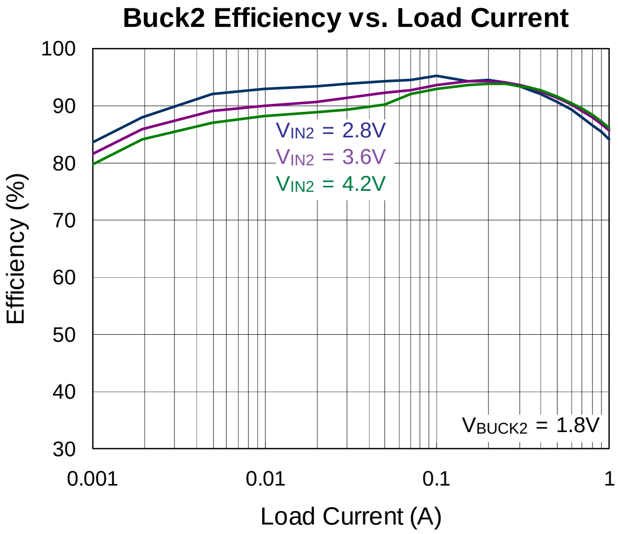
Note 3. Devices are ESD sensitive. Handling precautions are recommended.

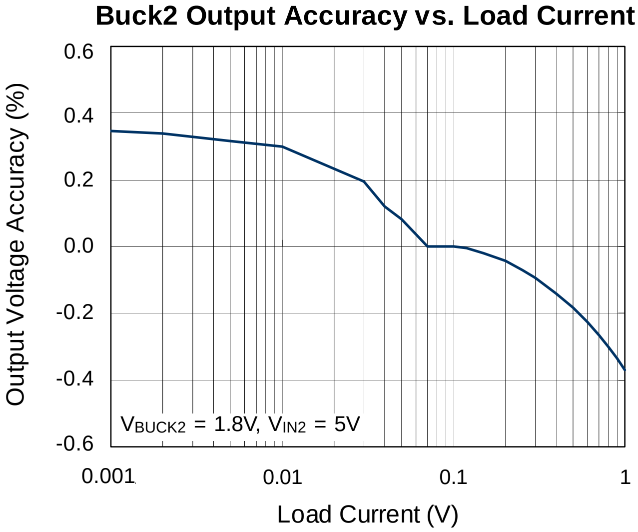
Note 4. The device is not guaranteed to function outside its operating conditions.

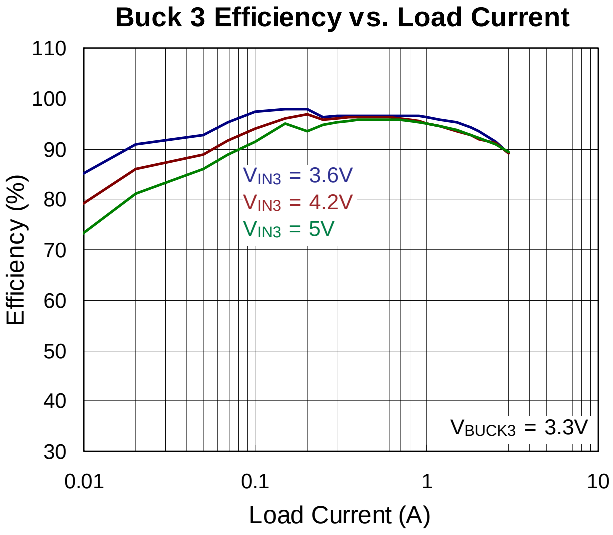
Typical Operating Characteristics

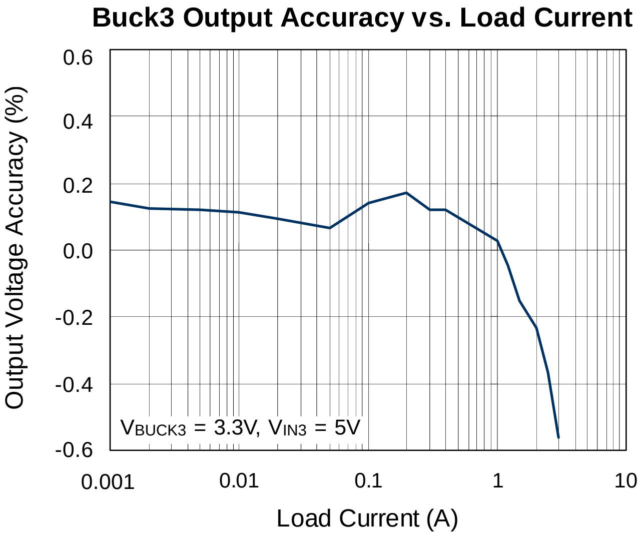


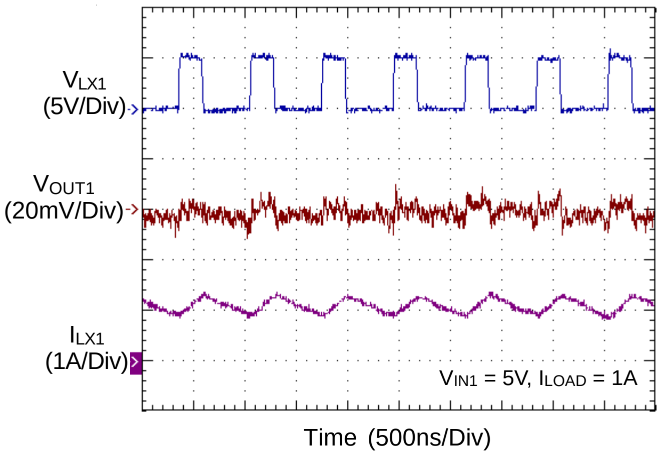


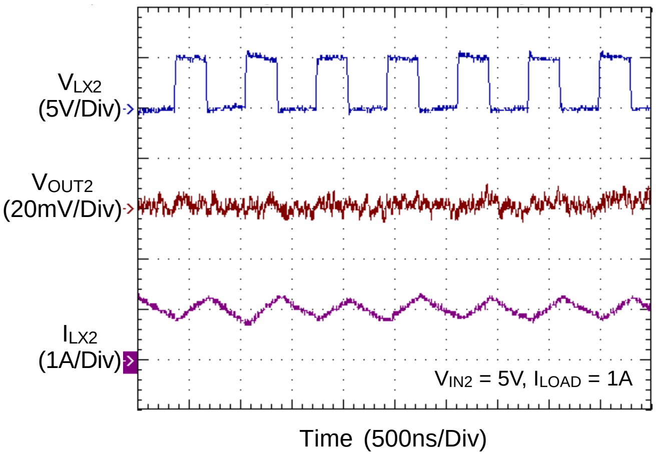


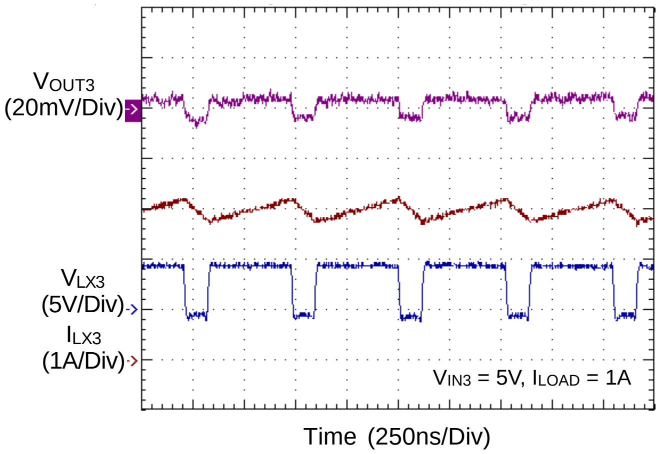


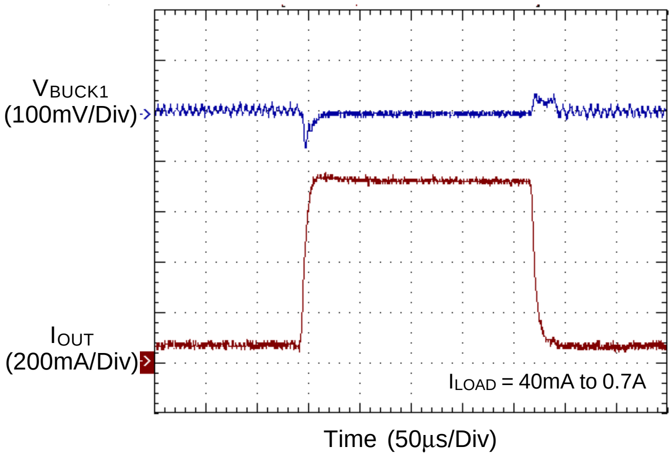


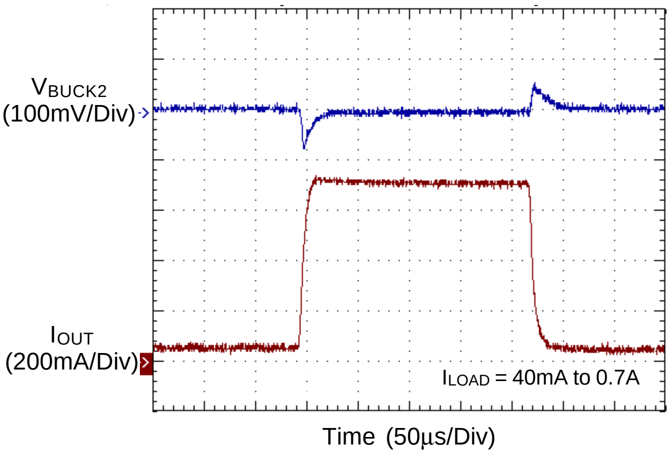


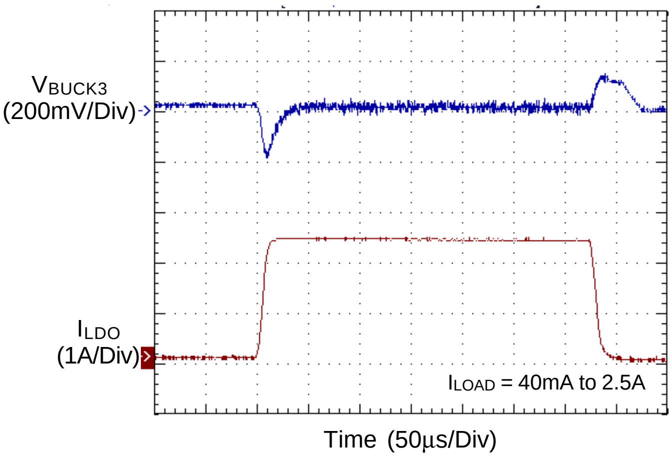

Buck1 Output Ripple


Buck2 Output Ripple


Buck3 Output Ripple


Buck1 Load Transient Response


Buck2 Load Transient Response


Buck3 Load Transient Response

Application Information

The basic RT9991 application circuit is shown in the section Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance, as shown in equation below :

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

where f is the operating frequency and L is the inductance.

Having a lower ripple current reduces not only the ESR losses in the output capacitors, but also the output voltage ripple. Higher operating frequency combined with smaller ripple current is necessary to achieve high efficiency. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4I_{(MAX)}$. The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)} / 2$. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \le \Delta I_L \times \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

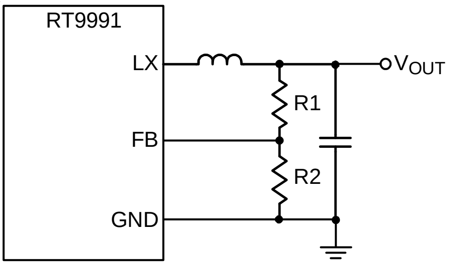
The output ripple is the highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR, but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistakened as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output Voltage Programming

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown below



For adjustable voltage mode, the output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{FB} is the internal reference voltage 0.8V (typ.).

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value.

During this recovery time, V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem.

Chip Enable Operation

If the EN pin for the selected buck is pulled high and the input voltage is greater than the under voltage lockout threshold, the selected buck will be turned on. Buck1 can be turned on/off by the external EN1 pin; Buck2 can be turned on/off by the external EN2 pin; Buck3 can be turned on/off by the external EN3 pin.

Table 1. The RT9991 Power Terminology

Output	Buck 1	Buck 2	Buck 3
State	ON	ON	ON
EN	VIN1 > EN1 > 1.5V	VIN1 > EN2 > 1.5V	VIN1 > EN3 > 1.5V
UVLO	5.5V > VIN1 > 2.1V	5.5V > VIN2 > 2.1V	5.5V > VIN3 > 2.4V
Default Output Voltage	$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$ $V_{FB} = 0.8V$		

Voltage Detector

RESET is an open drain output that indicates whether the VDET voltage is higher than 0.7V or not. RESET is typically pulled up to 3.3V. VDET monitors the input voltage and triggers the RESET output (Figure 1).

RESET is high impedance when the voltage from VDET exceeds the rising threshold 0.7V (typ.). RESET is low when the voltage from VDET falls below the low-battery falling threshold 0.68V (typ.) (Figure 2).

If the voltage detector feature is not required, connect RESET to ground and connect VDET to VIN.

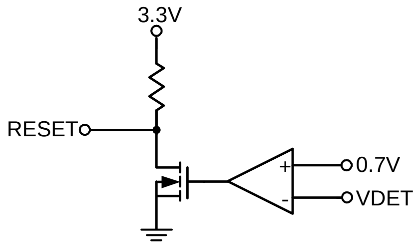


Figure 1. VDET and RESET Circuit

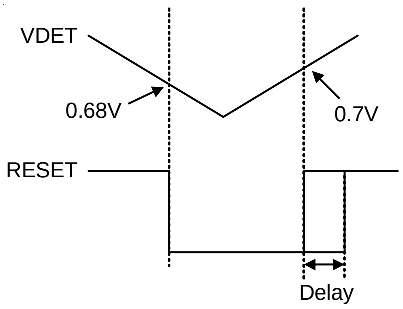


Figure 2. VDET and RESET Comparator Waveform

Choosing the Inductor

The RT9991 includes a current-reversal comparator which monitors inductor current and disables the synchronous rectifier as current approaches zero. This comparator will minimize the effect of current reversal for higher efficiency. For some low inductance values, however, the inductor current may still reverse slightly. This value depends on the speed of the comparator in relation to the slope of the current waveform, given by V_L / L. V_L is the voltage across the inductor (approximately – V_{OUT}) and L is the inductance value.

An inductance value of 2.2μH is a good starting value. As the inductance is reduced from this value, the RT9991 will enter discontinuous conduction mode at progressively higher loads. Ripple at V_{OUT} will increase directly proportionally to the magnitude of inductor ripple. Transient response, however, will improve.

A smaller inductor changes its current more quickly for a given voltage drive than a larger inductor, resulting in faster transient response. A larger inductor will reduce output ripple and current ripple, but at the expense of reduced transient performance and a physically larger inductor package size. For this reason a larger C_{VOUT} will be required for larger inductor sizes.

The input regulator has an instantaneous peak current clamp to prevent the inductor from saturating during transient load or start-up conditions. The clamp is designed so that it does not interfere with normal operation at high loads and reasonable inductor ripple. It is intended to prevent inductor current runaway in case of a shorted output.

The DC winding resistance and AC core losses of the inductor will also affect efficiency, and therefore available output power. These effects are difficult to characterize and vary by application. Some inductors and capacitors that may be suitable for this application are listed in Table below :

Table 2

p/n	Length (mm)	Width (mm)	Height (mm)	Inductance (μH)	RDC (mΩ)	IDC (A)	Supplier
	Max.	Max.	Max.	L	Max.	Max.	
VLF5012ST-1R0N2R5	5	4.8	1.2	1	50	3.3	TDK
VLF5014ST-2R2M2R3	5	4.8	1.4	2.2	73	3	
VLF3010A-1	3	2.8	1	2.2	120	1	
VLF3012A	3	2.8	1.2	2.2	100	1	
VLS2010E	2.1	2.1	1	2.2	228	1	
VLS2012E	2.1	2.1	1.2	2.2	153	1	
NR6045T1R0N	6	6	4.5	1	19	4.2	TAIYO
CB2016T2R2M	2.2	1.8	1.8	2.2	130	1	
NR6020T2R2N	6	6	2	2.2	34	2.7	
NR3015	3	3	1.5	2.2	60	1.48	
LPS4018	3.9	3.9	1.7	3.3	80	2.2	CoilCraft
D53LC	5	5	3	3.3	34	2.26	Toko
DB318C	3.8	3.8	1.8	3.3	70	1.55	
WE-TPC Type M1	4.8	4.8	1.8	3.3	65	1.95	Wurth

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT9991, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For VQFN-32L 5x5 packages, the thermal resistance, θ_{JA}, is 36°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (36°C/W) = 2.778W for VQFN-32L 5x5 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT9991 package, the derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

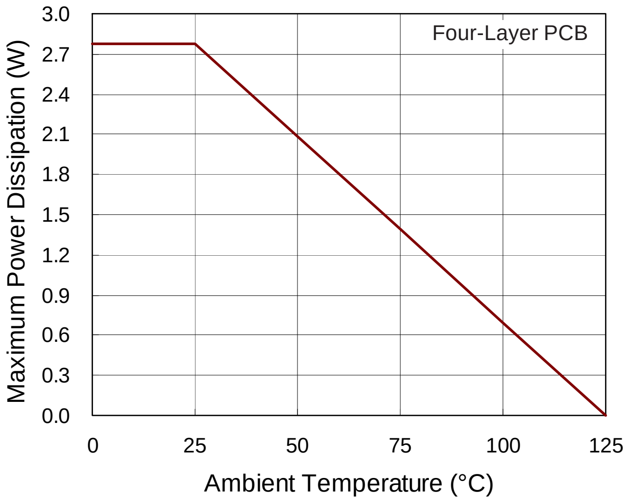


Figure 3. Derating Curve for the RT9991 Package

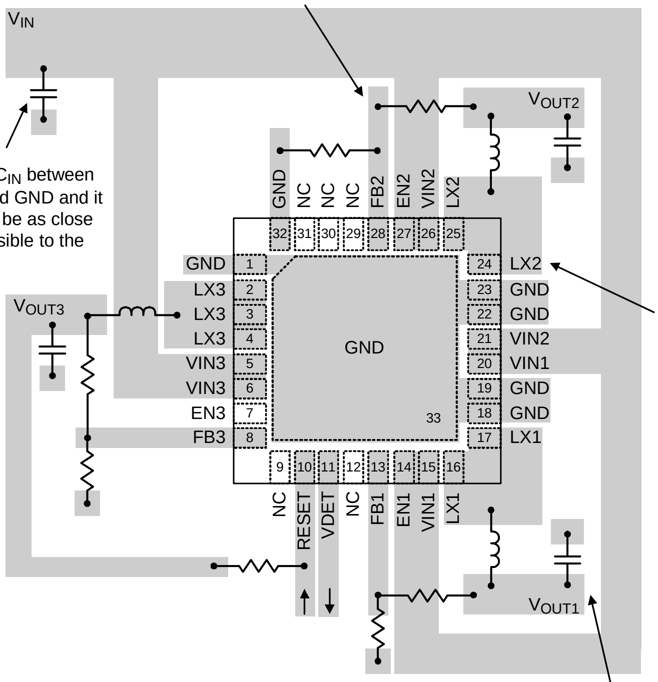
Layout Considerations

Follow the PCB layout guidelines for optimal performance of RT9991.

- Place the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept in a small area.
- Connect feedback network behind the output capacitors.
- Keep the switching area small. Place the feedback components near the RT9991.
- Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.

The feedback resistor divider must be placed as close to the FB pin as possible.

Place C_{IN} between VIN and GND and it should be as close as possible to the IC.

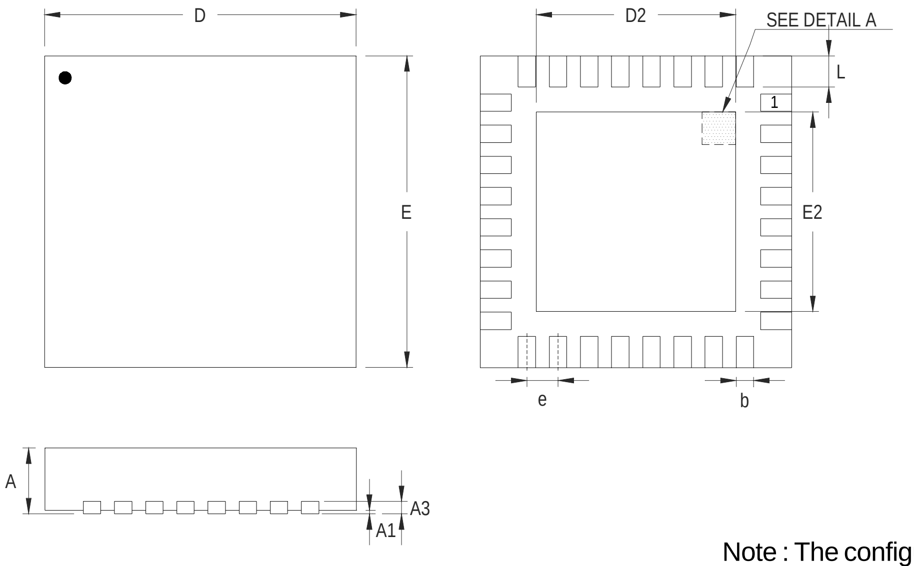


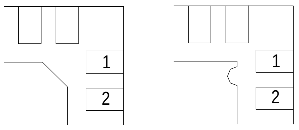
The LX pin should be connected to the inductor by a wide and short trace, Keep sensitive components away from this trace.

The output capacitor must be close to the IC.

Figure 4. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.400	3.750	0.134	0.148
E	4.950	5.050	0.195	0.199
E2	3.400	3.750	0.134	0.148
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 32L QFN 5x5 Package

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