RTC6649 Application Notes

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TABLE OF CONTENT

Revision History

Version	Content	Effective date
V0.1	Initial version	5/11/2010

1. Introduction

RTC6649 power amplifier (PA) is designed to operate in 2.4GHz ISM band. This document contains information of using RTC6649 as the power amplifier of an 802.11b/g/n compatible WLAN system, including application circuit, Bill of Material (BOM), PCB design and layout guideline. Typical performance data and pin definition are also summarized here for reference.

2. Electrical Characteristics Summary

- Operation frequencies : 2.412 ~ 2.482 GHz
- Linear Pout for 11a usage : 25.5 dBm
- Small signal gain : 32 dB
- 2f, 3f harmonics : -68 dBc
- Supply voltage : typical 5.0 V
- Vref1, Vref2 : typical 2.9 V

3. Pin Definition

Pin	Function	Description
1,4,8,13, 15	NC	Not connected
2,3	RF_in	RF input. Input matching network is built on chip
5	VCCB	Power supply for bias circuit
6	Vref1	Bias control voltage for 1st & 2nd stage
7	Vref2	Bias control voltage for 3rd stage
9	PD	Detector output voltage for output power index
10,11	RF_out	RF output.
12	Vcc3	Power supply for power stage-3, connected to pin10 & 11 internally
14	Vcc2	Power supply for power stage-2
16	Vcc1	Power supply for power stage-1

4. Application Circuit

Typical application circuit of RTC6649 for 802.11b/g/n WLAN system is drawn as the following schematic. The circuit can be divided into 6 functional areas: (A) Power Supply path, (B) RF output transmission line, (C) Bias and reference voltages supply, (D) RF input transmission line, (E) power detector output, (F) Grounding Via for exposed pad,

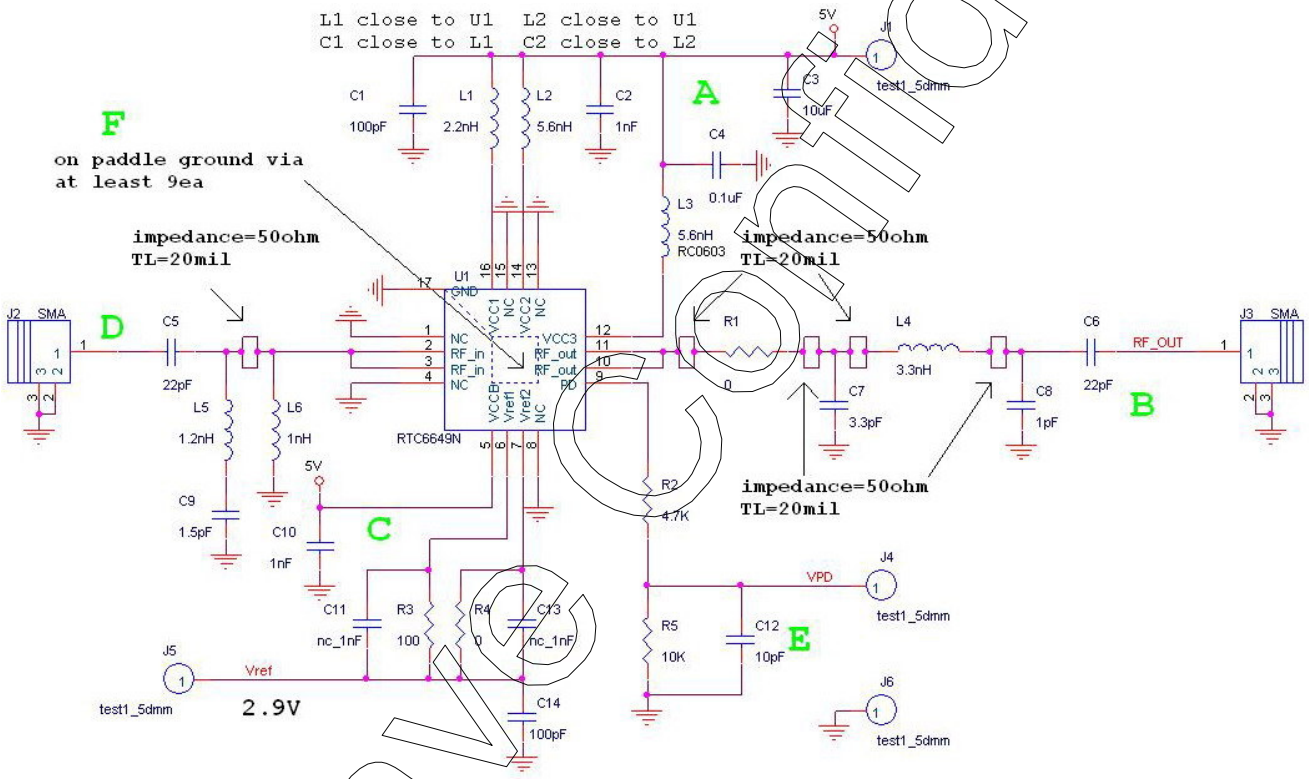


Figure 1: Typical Application Circuit

5. Bill of Material

Item	Qty	Reference Designators	Part Description	Size	Tol.	Manufacturer P/N	Manufacturer	Note
1	2	R1,R4	0 ohm, 1/16W, 1A, LF	0402	±5%	WR04X000PTL	WALSIN	
2	1	R3	100 ohm, 1/16W, 1A, LF	0402	±5%	WR04X101PTL	WALSIN	
3	1	R2	4.7K ohm, 1/16W	0402	±5%	WR04X472JTL	WALSIN	
4	1	R5	10K ohm, 1/16W	0402	±5%	WR04X103JTL	WALSIN	
5	1	C8	1pF,NP0,50V,±0.25pF	0402	±0.25pF	0402N1R0C500LT	WALSIN	
6	1	C9	1.5pF,NP0,50V,±0.25pF	0402	±0.25pF	0402N1R5C500LT	WALSIN	
7	1	C7	3.3pF,NP0,50V,±0.25pF	0402	±0.25pF	0402N3R3C500LT	WALSIN	
8	1	C12	10pF,NP0,50V,±5%	0402	±5%	0402N100J500LT	WALSIN	
9	2	C5,C6	22pF,NP0,50V,±5%	0402	±5%	0402N220J500LT	WALSIN	
10	2	C1,C14	100pF,NP0,50V,±5%	0402	±5%	0402N101J500LT	WALSIN	
11	2	C2,C10	1nF, X7R,50V,±10%	0402	±10%	0402B103K250CT	WALSIN	
12	1	C4	100nF,X7R,50V,±10%	0402	±10%	0402B104K500CT	WALSIN	
13	1	C3	10uF,X5R,6.3V,±10%	0805	±10%	0805X106K6R3CT	WALSIN	
14	1	L6	1nH,±0.3nH,300mA	0402	±0.3nH	HI1005-1C1N0SMT	ACX	
15	1	L5	1.2nH,±0.3nH,300mA	0402	±0.3nH	HI1005-1C1N2SMT	ACX	
16	1	L1	2.2nH,±0.3nH,300mA	0402	±0.3nH	HI1005-1C2N2SMT	ACX	
17	1	L4	3.3nH,±0.3nH,300mA	0402	±0.3nH	HI1005-1C3N3SMT	ACX	
18	1	L2	5.6nH,±0.3nH,300mA	0402	±0.3nH	HI1005-1C5N6SMT	ACX	
19	1	L3	5.6nH,±0.3nH,600mA	0603	±0.2nH	LQW18AN5N6C00	Murata	
20	1	U1	RTC6649_QFN16_3x3	3x3		RTC6649	RichWave	

Table 1: Bill of Material

6. PCB Design

For 802.11a/b/g/n compliant WLAN system, typically 4-layer PCB is used. The stack-up of PCB is very important for decision of the width of 50Ω transmission line.

Typically, PCB manufacturer may provide 4-layer boards with final thickness of 20, 31, 40, 47 and 62 mil. You can select 1 or 2 ounce inner layer copper foil for your board. The PCB manufacturer also have several inner layer cores available using FR4 materials, including 5, 8, 9.5, 14, 18, 21, 28, 35, 39 and 47 mil cores. Between outer layer copper foil and inner core are sheets of prepreg. Several types of prepreg could be selected to stack up the PCB, including type 106, 1080, 2116… etc. The PCB manufacturers have several types of standard stack-up, e.g.

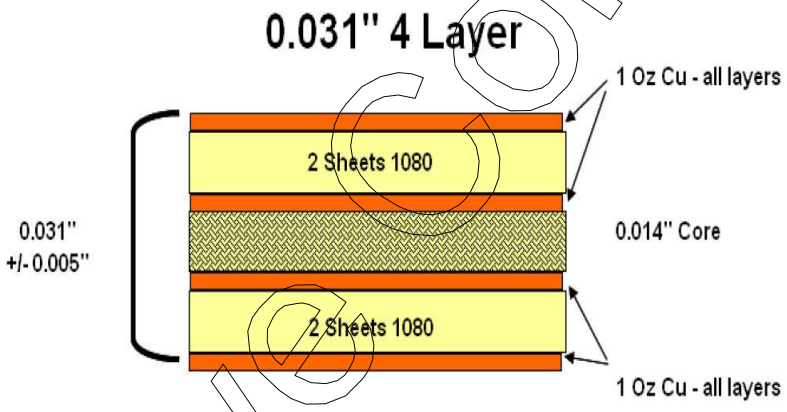


Figure 2: Vendor standard stack-up of 4-layer PCB with 31 mil thickness

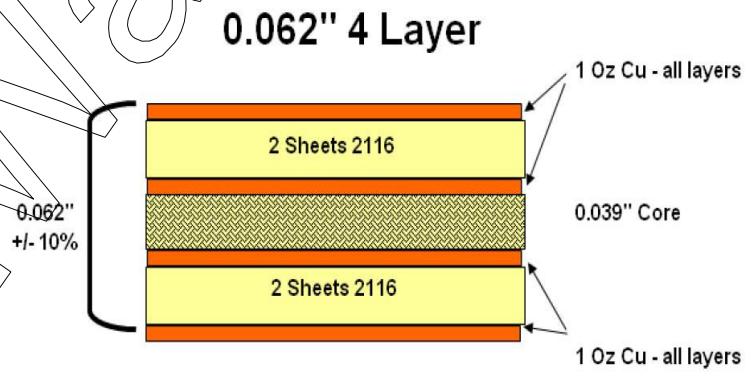


Figure 3: Vendor standard stack-up of 4-layer PCB with 62 mil thickness

To PCB manufacturer, you can choose their “standard” stack-up as above or you can specify your own controlled PCB stack-up. In either case, you should know the spacing between signal layer and ground plane layer. For microstrip line, this information is enough. However, for Coplanar Waveguide (CPW) or Conductor Backed Coplanar Waveguide (CBCPW or CPWG), you should know the gap or spacing between transmission line and the ground copper on the same layer.

As an example, if you specify the following PCB stack-up, you can route the 50Ω transmission line with 15-mill width, and the gap between transmission line and ground plane copper should be 13 ~ 14 mil.

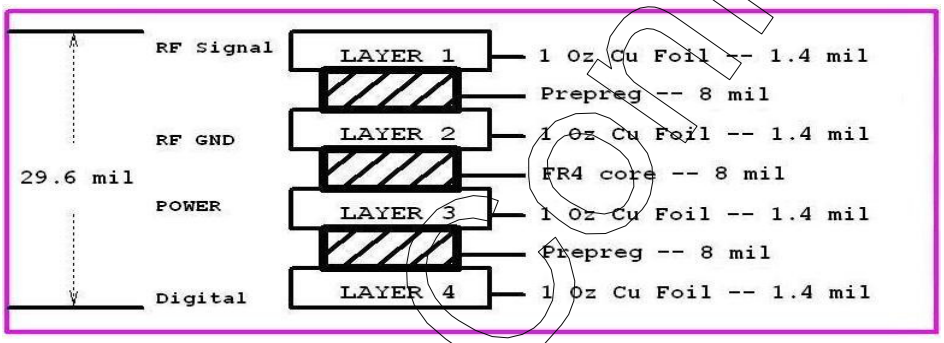


Figure 4: A specific 4-layer PCB stack-up

The impedance calculation of conductor backed CPW is shown below:

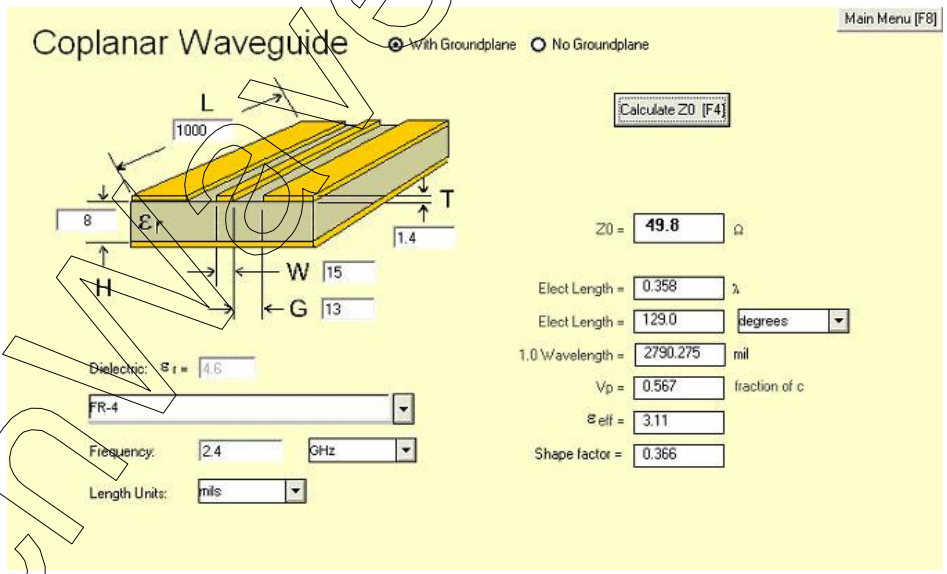


Figure 5: 50Ω transmission line parameter calculation

On the other hand, if you use a 2-layer PCB with the following stack-up, you can route the 50Ω transmission line with 24-mill width, and the gap between transmission line and ground plane copper should be 4 ~ 5 mil.

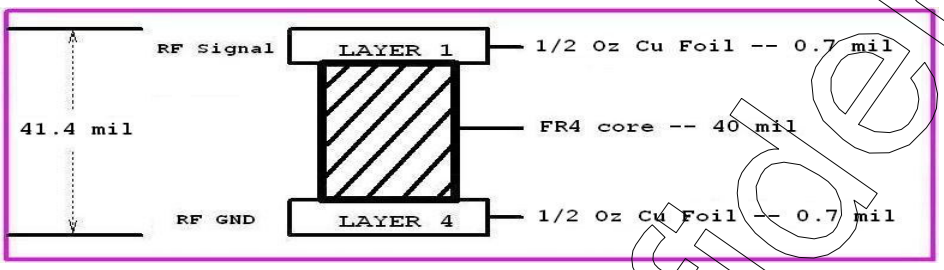


Figure 6: A specific 2-layer PCB stack-up

The impedance calculation of conductor backed CPW is shown below:

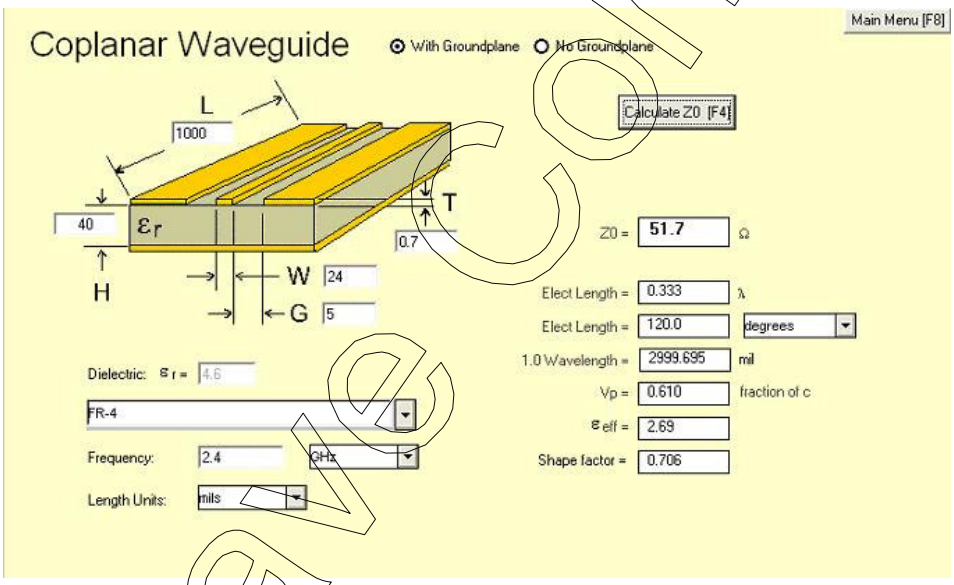


Figure 7: 50Ω transmission line parameter calculation

For other PCB stack-up, please calculate the parameter carefully to get a transmission line with impedance closer to 50Ω.

7. PCB Layout Guideline

7.1 Power Supply Path

The power supply path for PA is the circuit drawn as below:

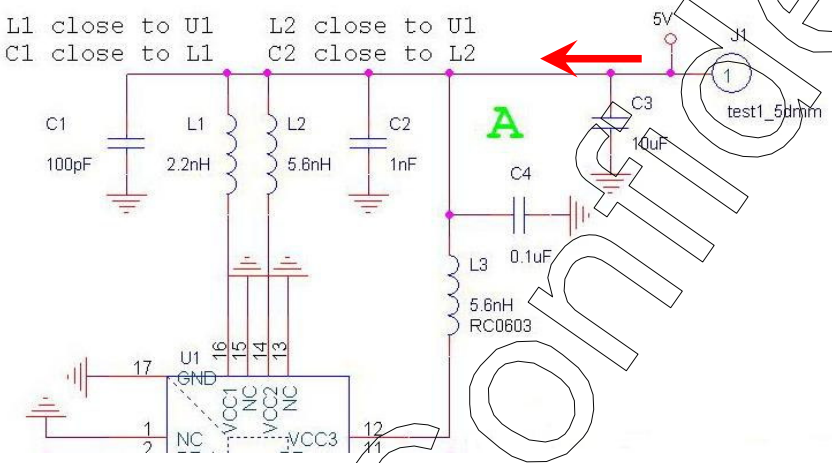


Figure 8: Power supply path schematic

5V supply voltage for PA should be routed with enough width (at lease 30mil is recommended) to the 10uF decoupling main node (C3). From here route the power trace to VCC3(L3), VCC2(L2) and VCC1(L1). Route the power trace from C3 as wide as possible. C1 is the decoupling capacitor for VCC1, put it closer to L1 and L1 closer to PA(U1). C2 is the decoupling capacitor for VCC2, put C2 closer to L2 and L2 closer to PA(U1). The Line width of power trace from L1 and L2 should be greater than 7-mil. Place L1, C1, L2, C2 as close as possible and PCB trace as short as possible.

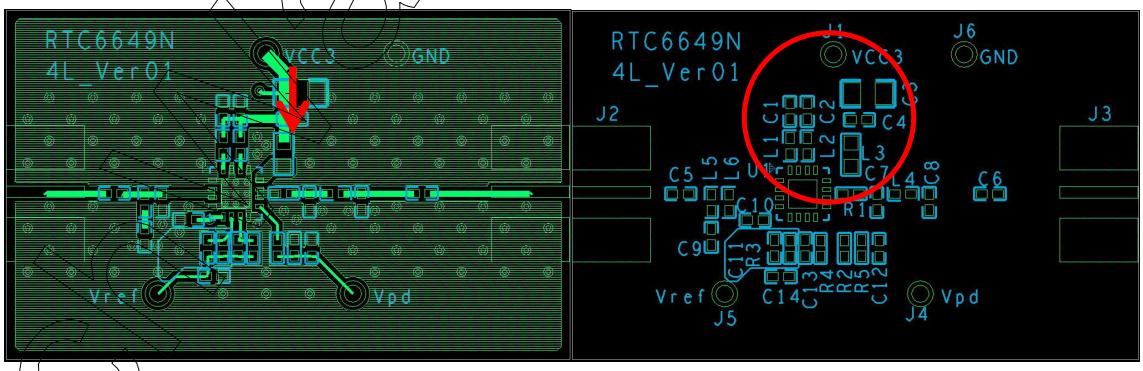


Figure 9: Power supply path layout

7.2 RF Output Transmission Line

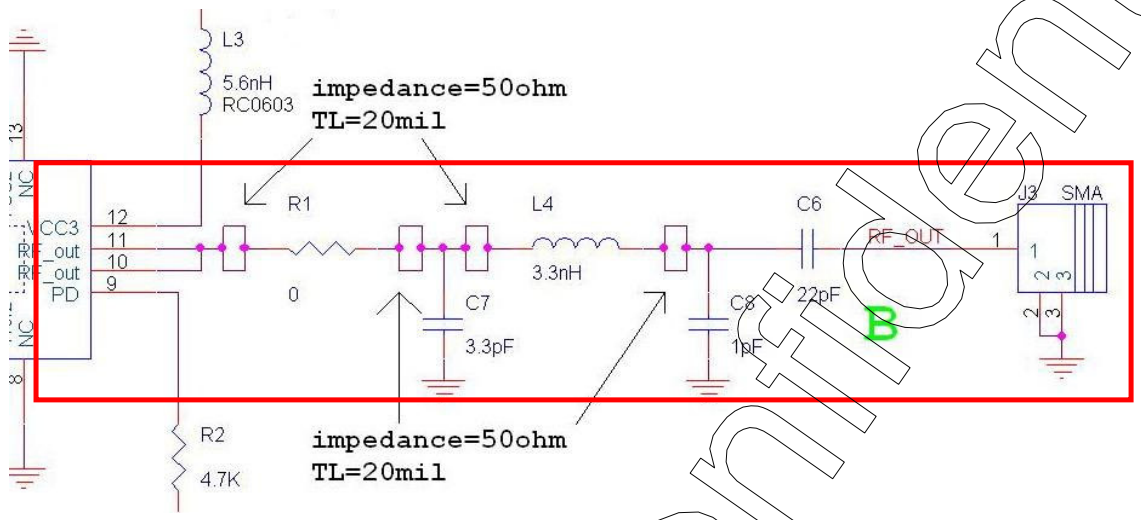


Figure 10: RF output schematic

Route the RF output transmission line with 50Ω impedance. The parameter of transmission line (width & gap) should be carefully calculated as described in section 6. For RTC6649, the output matching R1 should be put at 20mil away from U1 pin-10 & pin-11 (body edge to body edge). Shunt C7 at 20mil TL away from R1 edge and series L4 at 20mil TL away from C7. Also shunt C8 at 20mil TL away from L4 edge. C6 is output DC block.

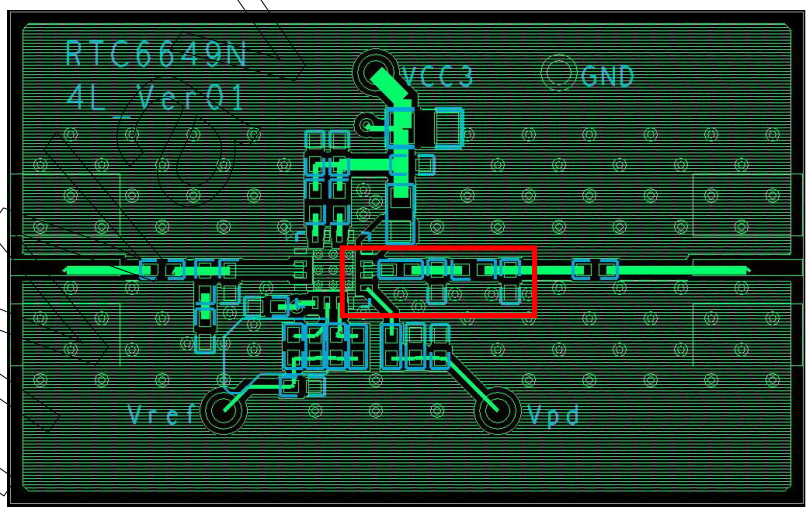


Figure 11: RF output layout

7.3 Bias and Reference Voltage Supplies

This part of circuit includes 3.3V supply voltage for bias circuit, reference voltages for bias control, and the voltage to enable power detector. Schematic is drawn as below:

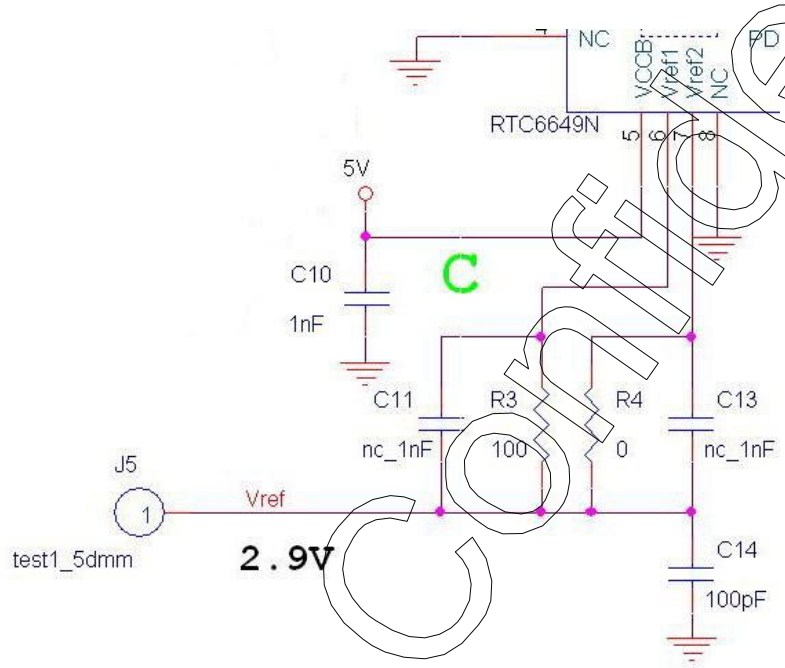


Figure 12: Bias and reference voltage supplies

C10 is the decoupling capacitor of VCCB, put it closer to PA pin-5. R3 and R4 are resistors used for adjusting Vref. Reserve C11 and C13 to adjust burst rising and falling time. C14 is the decoupling capacitor for Vref, put it closer to R3, R4.

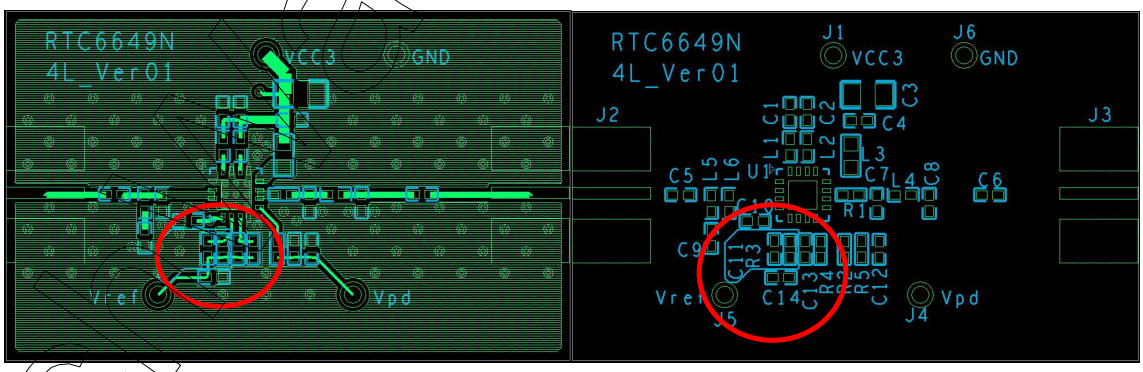


Figure 13: Vref and VCCB PCB layout

7.4 RF Input Transmission Line

Schematic of PA's RF input is drawn in the following figure. C5 is the DC-blocking capacitor of PA input. Route the RF input transmission line with 50Ω impedance. The parameter of transmission line (width & gap) should be carefully calculated as described in section 6.

L5, C9, L6 are notch filter for 3.2GHz Gain rejection. Put L6 at a distance of 20mil TL away from L5.

Put C9 to L5 as close as possible.

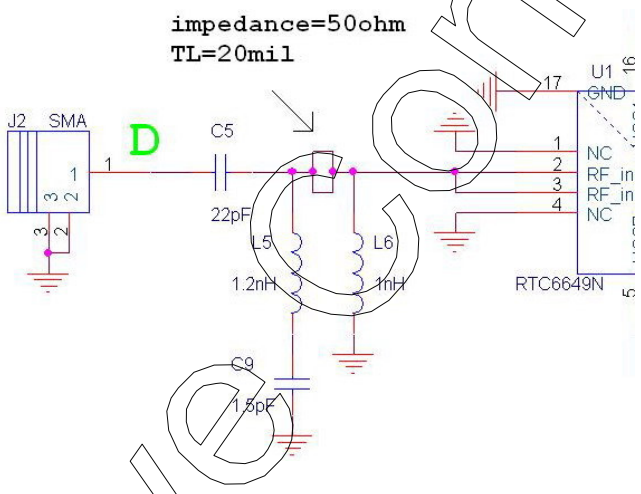


Figure 14: RF input schematic with notch filter circuit

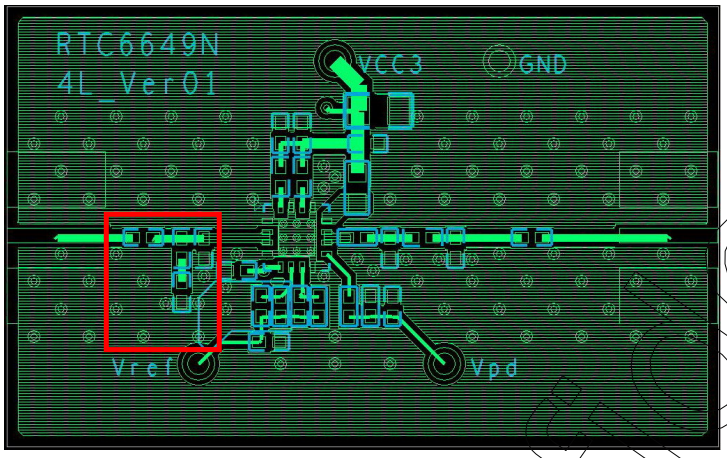


Figure 15: RF input PCB layout with notch filter

RTC6649 is equipped with internal input matching circuit. The internal matching circuit shunt an inductor to GND, lead to no DC leakage to PA input.

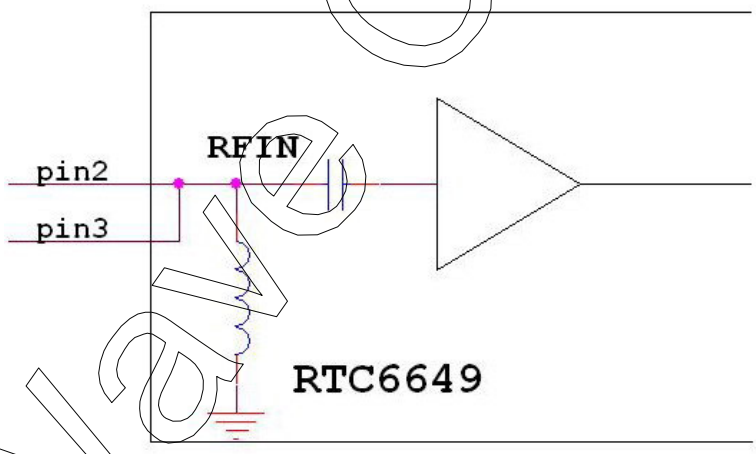


Figure 16: Internal input matching circuit

7.5 Power Detector Output

Pin-9 of PA is power detector output. R5 and C12 construct a LPF to filter RF signal from pin-9. R2 is used to reduce Vpd level.

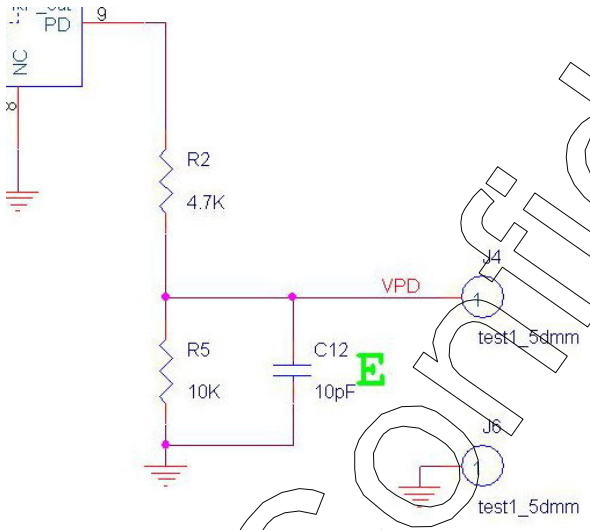


Figure 17: power detector schematic with LPF

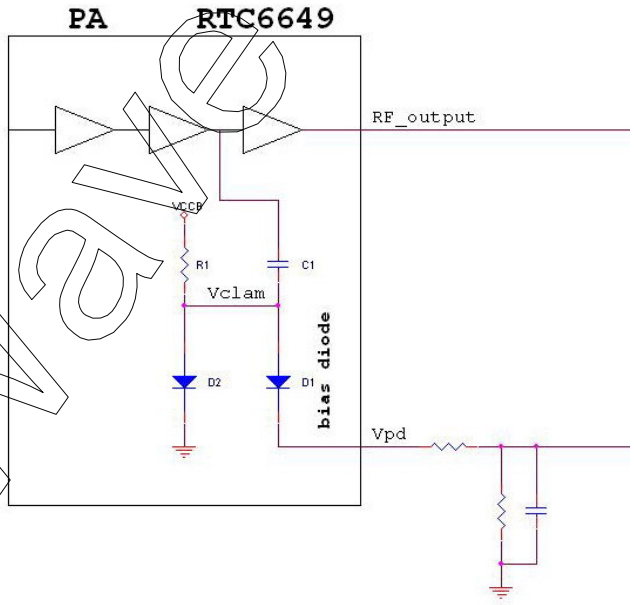


Figure 18: power detector equivalent circuit

7.6 Grounding Via for PA Exposed Pad

As drawing in the following figure, at least 9 pieces of grounding via should be put on the grounding area for PA exposed pad. They are used to make more connection to larger ground planes for better power dissipation, as well as minimize the stray inductance between PA exposed pad and 2nd layer ground plane.

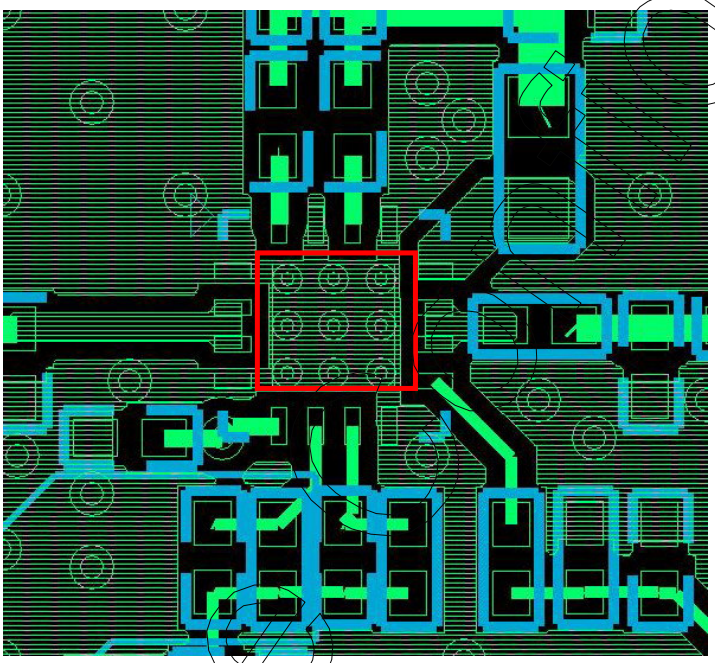


Figure 19: Amount of grounding via

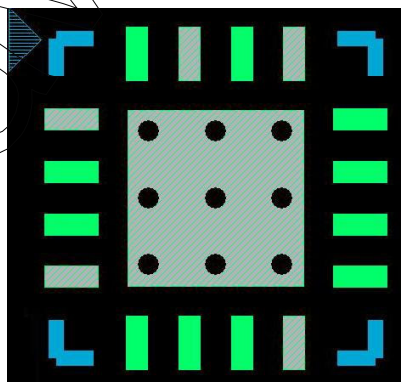


Figure 20: Amount of grounding via

7.7 NC Pin & Layout Guidelines for 2_Layer PCB

Pin 1, 4, 8, 13, 15 are all NC pins. There are no embedded bonding wires connected to these pins. Connect these NC pins to ground is recommended.

For 2-layer PCB, since the spacing between top and bottom layer is larger than the 4-layer PCB, the stray inductance on the ground return path will be higher than 4-layer PCB. Therefore, for 2-layer PCB we should minimize the ground path inductance as possible as we can. As shown in the following schematic, in 2-layer PCB case, these NC pins have to be connected to ground to make an intact ground plane copper.

Please refer to section 6 for 50Ω transmission line parameter calculation.

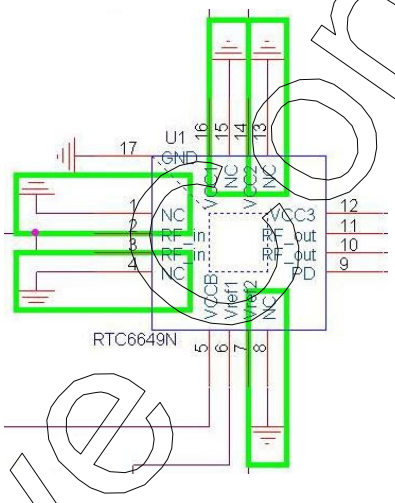


Figure 21: NC pins of RTC6649 connect to GND

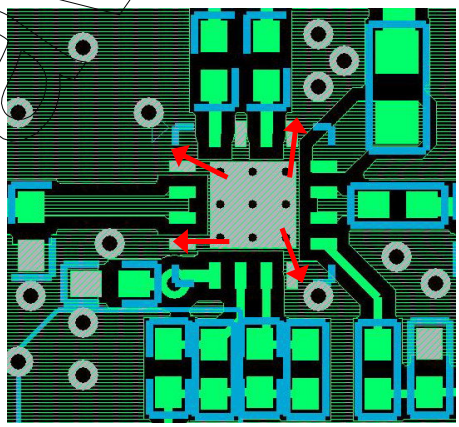
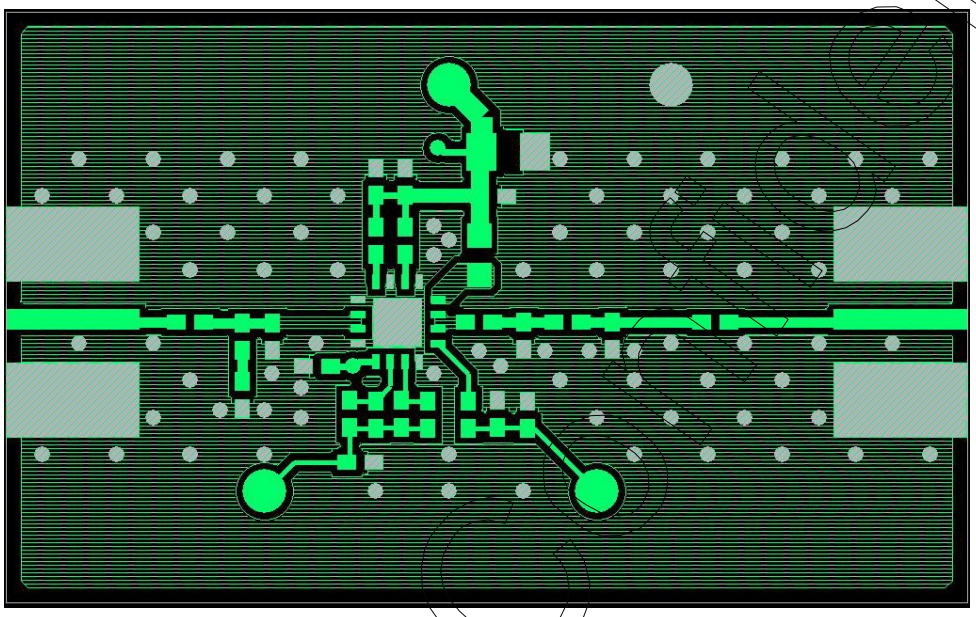


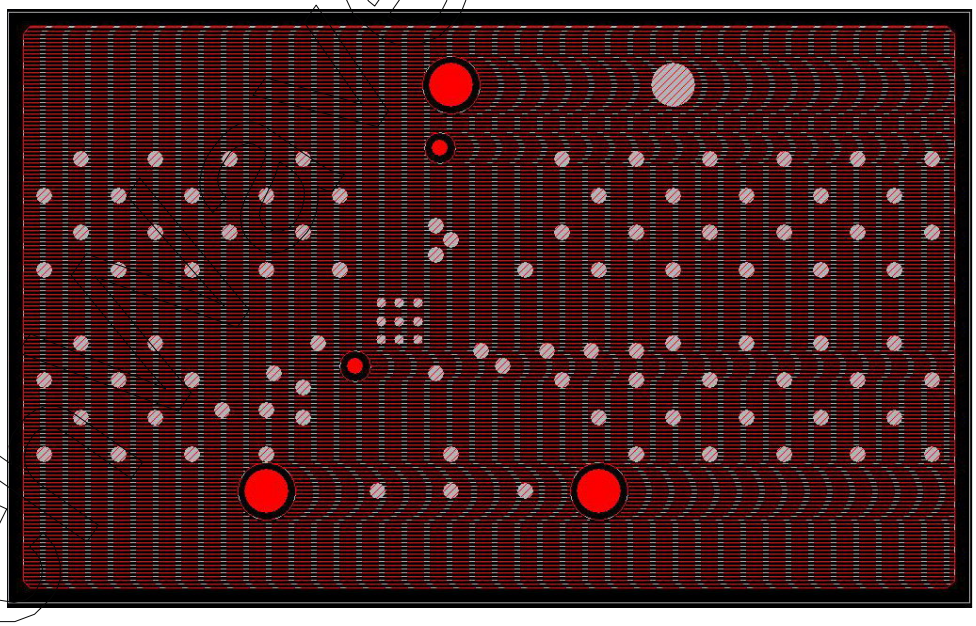
Figure 22: routing NC pins extend ground plan

8. PCB Layout Example for Each Layer

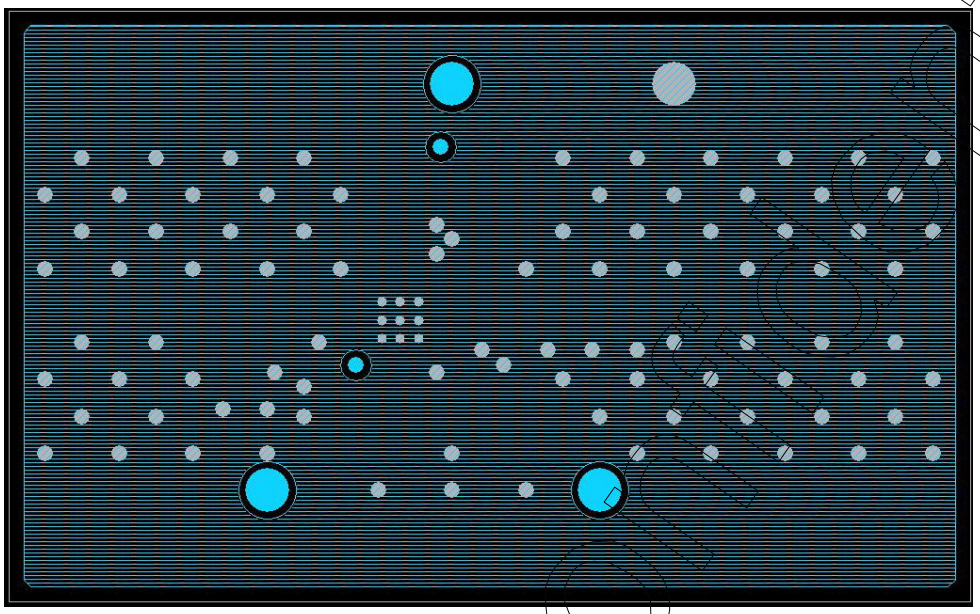
8.1 Top layer



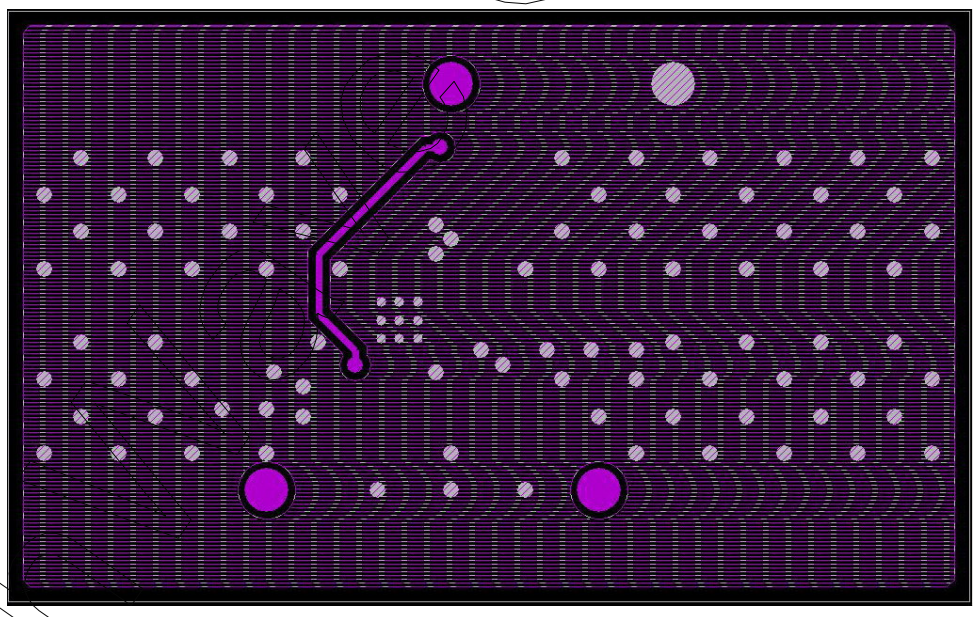
8.2 Bottom layer



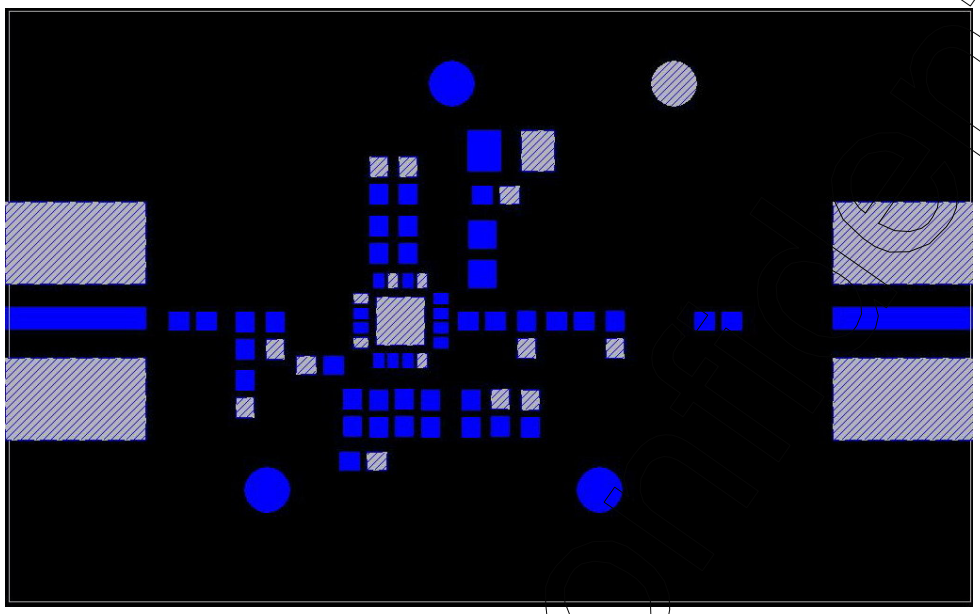
8.3 INT1 layer (layer 2, grounding layer)



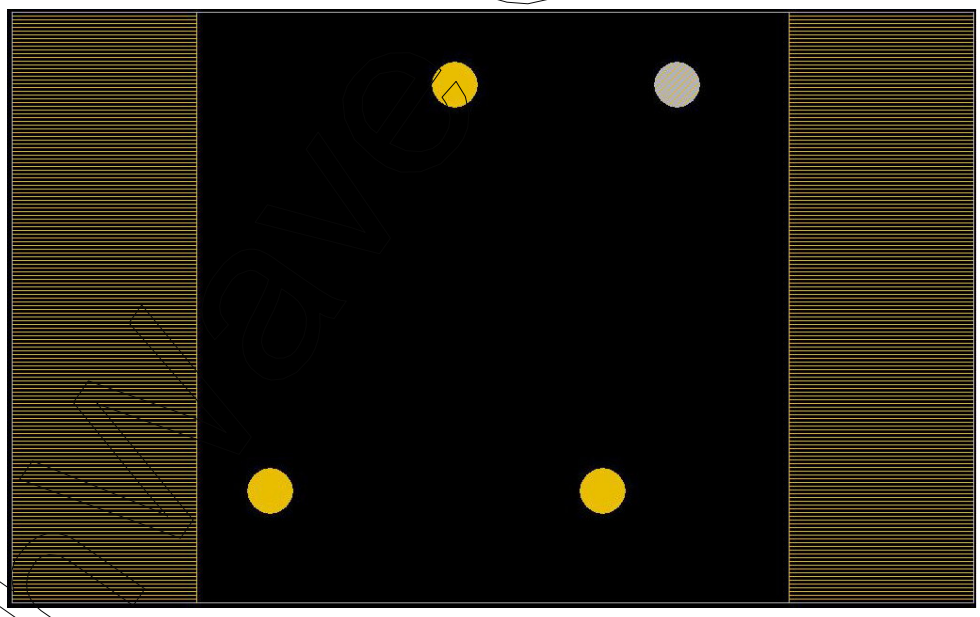
8.4 INT2 layer (layer 3)



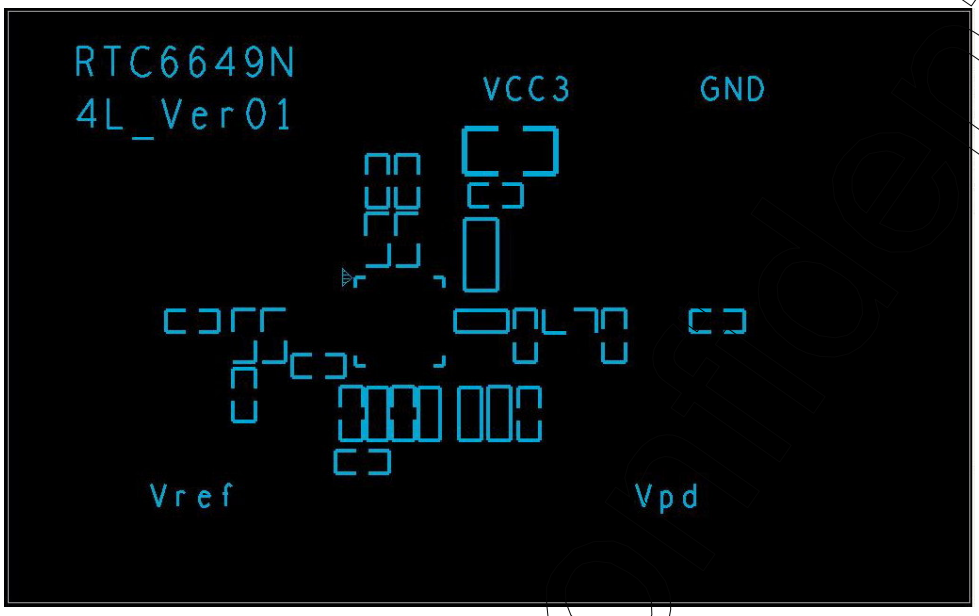
8.5 MASK TOP layer



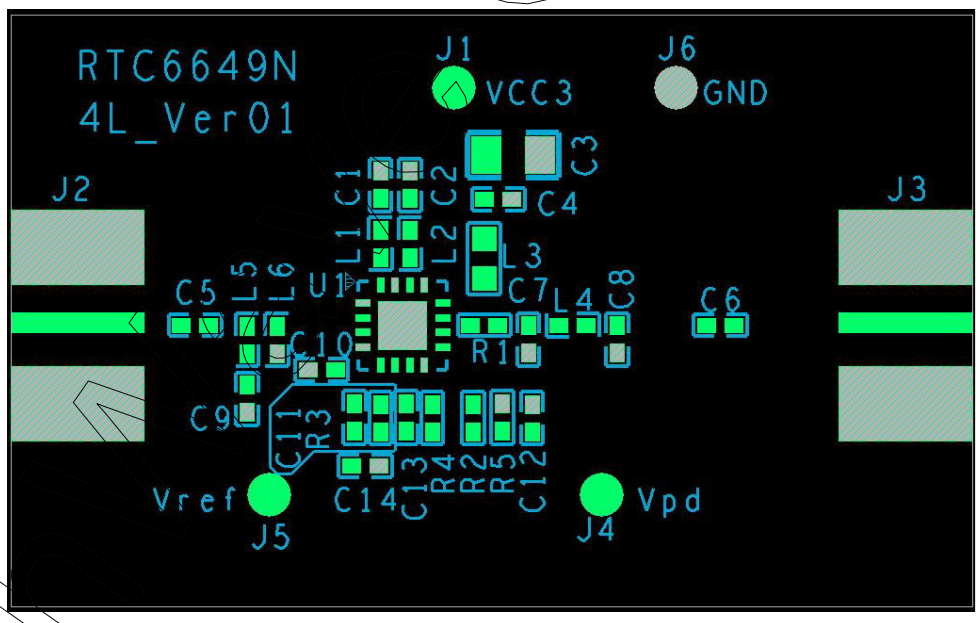
8.6 MASK Bottom layer



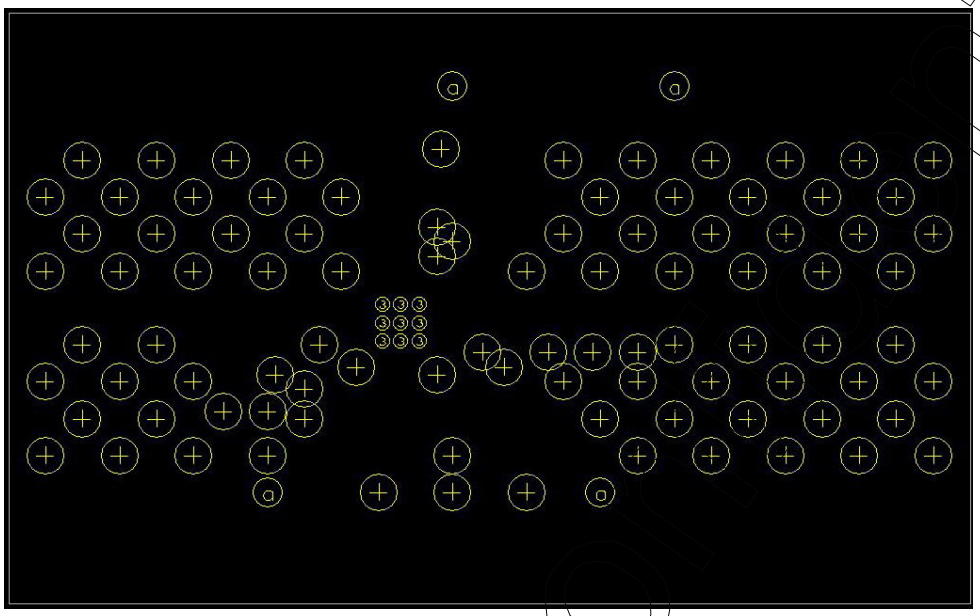
8.7 Silktop layer



8.8 Component layer



8.9 Drill layer



DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILS			
FIGURE	SIZE	PLATED	QTY
◦	8.0	PLATED	9
⊕	13.0	PLATED	93
◦	40.0	PLATED	4