RTD2023L

Flat Panel Display Controller

Fully Technology
Revision
Version 1.00
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Revision History

Version	Date	Block	Register	Description
1.00	2005/5/16			

1. Features

General
- Support DDCCI
- Zoom scaling up and down
- No external memory required.
- Require only one crystal to generate all timing.
- Programmable 3.3V/5V detection reset output.
- 3 channels 8 bits PWM output, and wide range selectable PWM frequency.

Analog RGB Input Interface
- Integrated 8-bit triple-channel 165MHz ADC/PLL
- Embedded programmable Schmitt trigger of HSYNC
- Support Sync On Green (SOG) and various kinds of composite sync modes
- On-chip high-performance hybrid PLLs
- High resolution true 64 phase ADC PLL

Auto Detection /Auto Calibration
- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for Phase/Image position/Color calibration

Scaling
- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement
- Support non-linear scaling from 4:3 to 16:9 or 16:9 to 4:3

Color Processor
- True 10 bits color processing engine
- sRGB compliance
- Advanced Dithering logic for 18-bit panel color depth enhancement
- Content adaptive edge enhancement.
- Dynamic overshoot-smear canceling engine
- Brightness and contrast control
- Programmable 10-bit gamma support

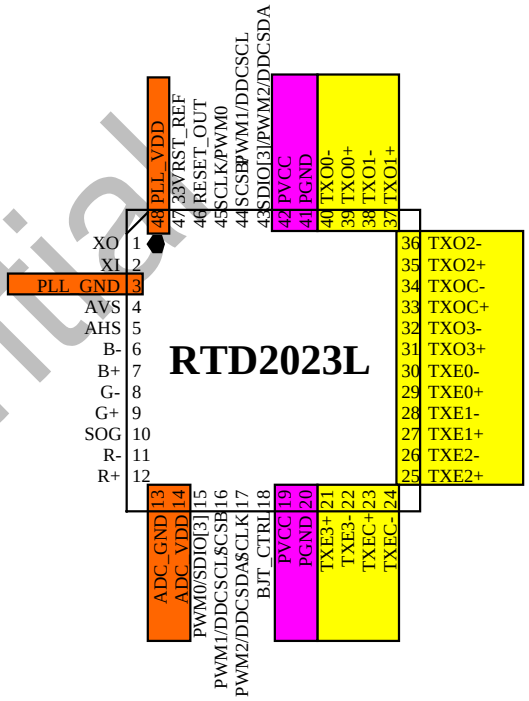
Output Interface
- Fully programmable display timing generator
- Flexible data pair swapping for easier system design.
- Dual/Single LVDS output interface
- Spread-Spectrum DPLL to reduce EMI
- Fixed Last Line output for perfect panel capability

Host Interface
- Support MCU serial bus interface.
- Support MCU dual edge data latch.

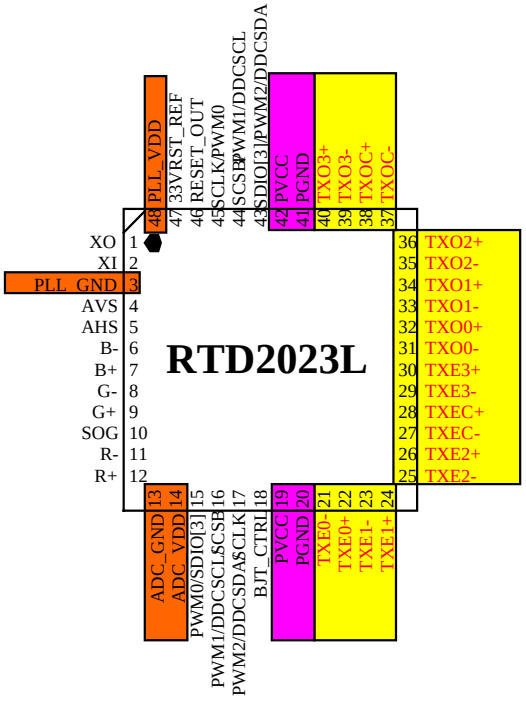
Embedded OSD
- Embedded 12K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1, 2 and 4-bit per pixel
- 16 color palette with 24bit true color selection
- Maximum 8 window with alpha-blending/ gradient/dynamic fade-in/fade-out, bordering/ shadow/3D window type
- Every window can place anywhere on the screen
- Rotary 90,180,270 degree
- Independent row shadowing/bordering
- Programmable blinking effects for each character
- OSD-made internal pattern generator for factory mode
- Support 12x18~4x18 proportional font

Power & Technology
- 1.8V and 3.3V power supplier
- 0.18um CMOS process, 48-pin LQFP package
- Embedded 3.3V to 1.8V voltage regulator (P type) BJT control

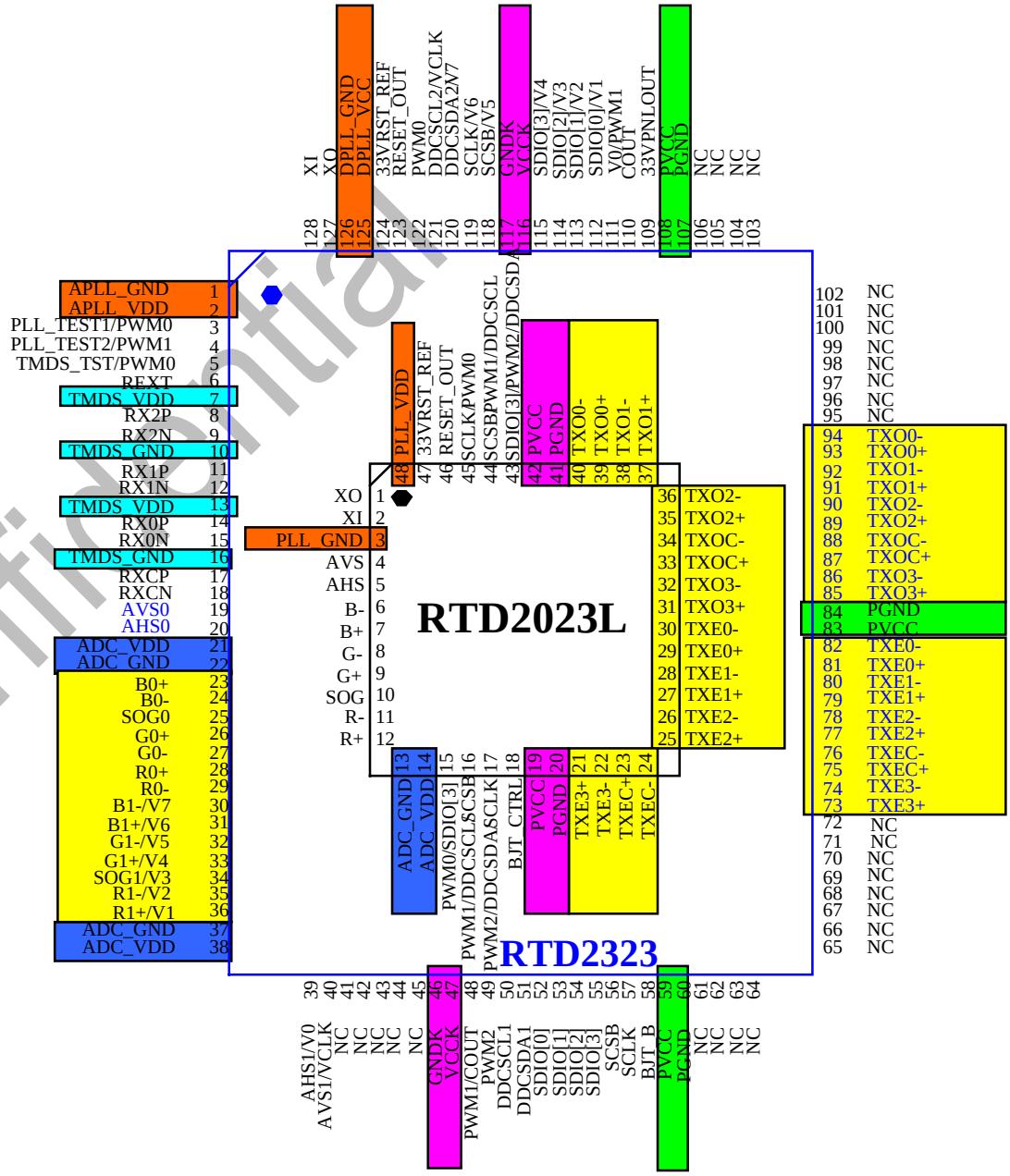
LVDS Mirror



Analog Input with LVDS (when CR8D[7] = 0)



Analog Input with LVDS (when CR8D[7] = 1)



RTD2023L & RTD2323/RTD2523B pin-to-pin Illustration

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

n INPUT PORT

Name	I/O	Pin No	Description	Tolerance	Note
AVS	I	4	ADC vertical sync input Adjustable Schmidt trigger Power from PIN 48	5V	
AHS	I	5	ADC horizontal sync input Power from PIN 48	5V	
B-	AI	6	Negative BLUE analog input	3.3V	
B+	AI	7	Positive BLUE analog input	3.3V	
G-	AI	8	Negative GREEN analog input	3.3V	
G+	AI	9	Positive GREEN analog input	3.3V	
SOG	AI	10	Sync on Green	3.3V	
R-	AI	11	Negative RED analog input	3.3V	
R+	AI	12	Positive RED analog input	3.3V	
ADC_GND	AG	13	ADC Ground		
ADC_VDD	AP	14	ADC Power (1.8V)		

n PLL

Name	I/O	Pin No	Description	Tolerance	Note
XO	AO	1	Crystal OSC output		
XI	AI	2	Reference clock input from external crystal or from single-ended CMOS/TTL OSC	3.3V	
PLL_GND	AG	3	Ground for display digital PLL		
PLL_VDD	AP	48	Power for digital PLL (3.3V)		

n Host interface

Name	I/O	Pin No	Description	Tolerance	Note
SDIO[3]	I/O	43/15	Serial control I/F data in (Open drain)	5V	
SCSB	O	44/16	Serial control I/F chip select (Open drain)	5V	
SCLK	O	45/17	Serial control I/F clock (Open drain)	5V	

n Pad/Digital Power & Ground

Name	I/O	Pin No	Description	Tolerance	Note
Pad 1.8V Power	P	19/42	PVCC (1.8V)		
Pad 1.8V Ground	G	20/41	PGND		

n DDC Channel & PWM

Name	I/O	No	Description	Tolerance	Note
PWM0	O	15/45	Open drain	5V	
DDCSCL/PWM1	I/O	16/44	Open drain	5V	
DDCSDA/PWM2	I/O	17/43	Open drain	5V	

n MISC

Name	I/O	No	Description	Tolerance	Note
BJT_B	O	18	Embedded regulator P type BJT control pin out	3.3V	
RESET_OUT	O	46	Reset out Open drain	5V	
33VRST_REF	I	47	Reference 3.3V for Reset Out		

n LVDS Display Interface

Name	I/O	No	Description	Tolerance	Note
TXE3+ / TXE0-	O	21	(CR8D[7] = 0) / (CR8D[7] = 1)	1.8V	
TXE3- / TXE0+	O	22		1.8V	
TXEC+ / TXE1-	O	23		1.8V	
TXEC- / TXE1+	O	24		1.8V	
TXE2+ / TXE2-	O	25		1.8V	
TXE2- / TXE2+	O	26		1.8V	
TXE1+ / TXEC-	O	27		1.8V	
TXE1- / TXEC+	O	28		1.8V	
TXE0+ / TXE3-	O	29		1.8V	
TXE0- / TXE3+	O	30		1.8V	
TXO3+ / TXO0-	O	31		1.8V	
TXO3- / TXO0+	O	32		1.8V	
TXOC+ / TXO1-	O	33		1.8V	
TXOC- / TXO1+	O	34		1.8V	
TXO2+ / TXO2-	O	35		1.8V	
TXO2- / TXO2+	O	36		1.8V	
TXO1+ / TXOC-	O	37		1.8V	
TXO1- / TXOC+	O	38		1.8V	
TXO0+ / TXO3-	O	39		1.8V	
TXO0- / TXO3+	O	40		1.8V	

2. Chip Data Path Block Diagram

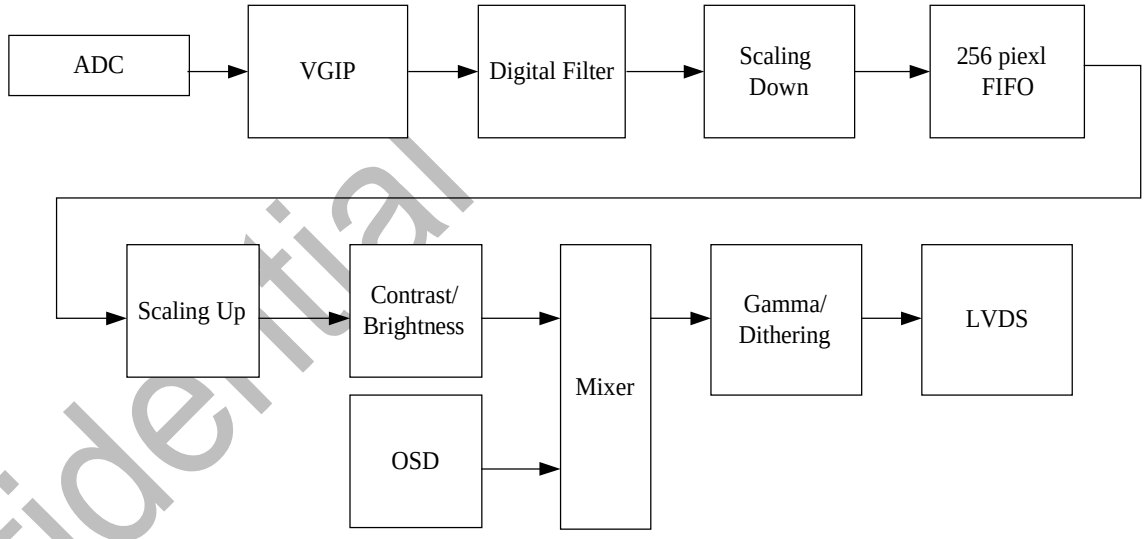


Figure 1

3. Architecture

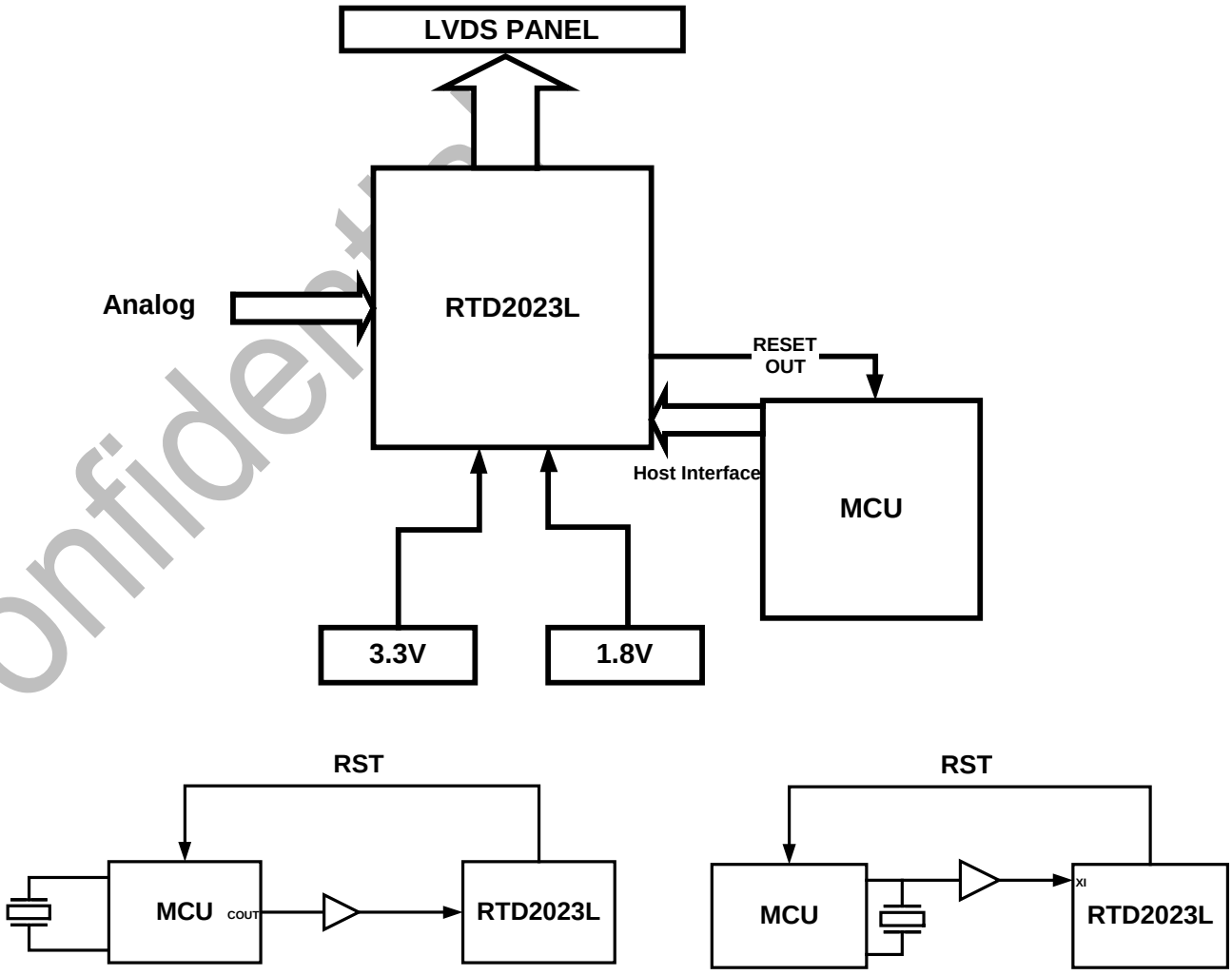


Figure 2

4. Functional Description

4.1 Input

Analog Input

RTD 2023L integrates three ADC's (analog-to-digital converters), one for each color (red, green, and blue). The sync-processor can deal with Separate-Sync, Composite-Sync, and Sync-On-Green. And the PLL can generate very low jitter clock from HS to sample the analog signal to digital data. Input data is latched within a capture window defined in registers refer to VS and HS leading edge.

Input Capture Window

Inside RTD, there are four registers IPH_ACT_STA, IPH_ACT_WID, IPV_ACT_STA & IPV_ACT_LEN to define input capture window for the selected input video on either A or B input port while programmed analog input mode. The horizontal sync (IHS) & vertical sync (IVS) signals are used from the selected port to determine the capture window region.

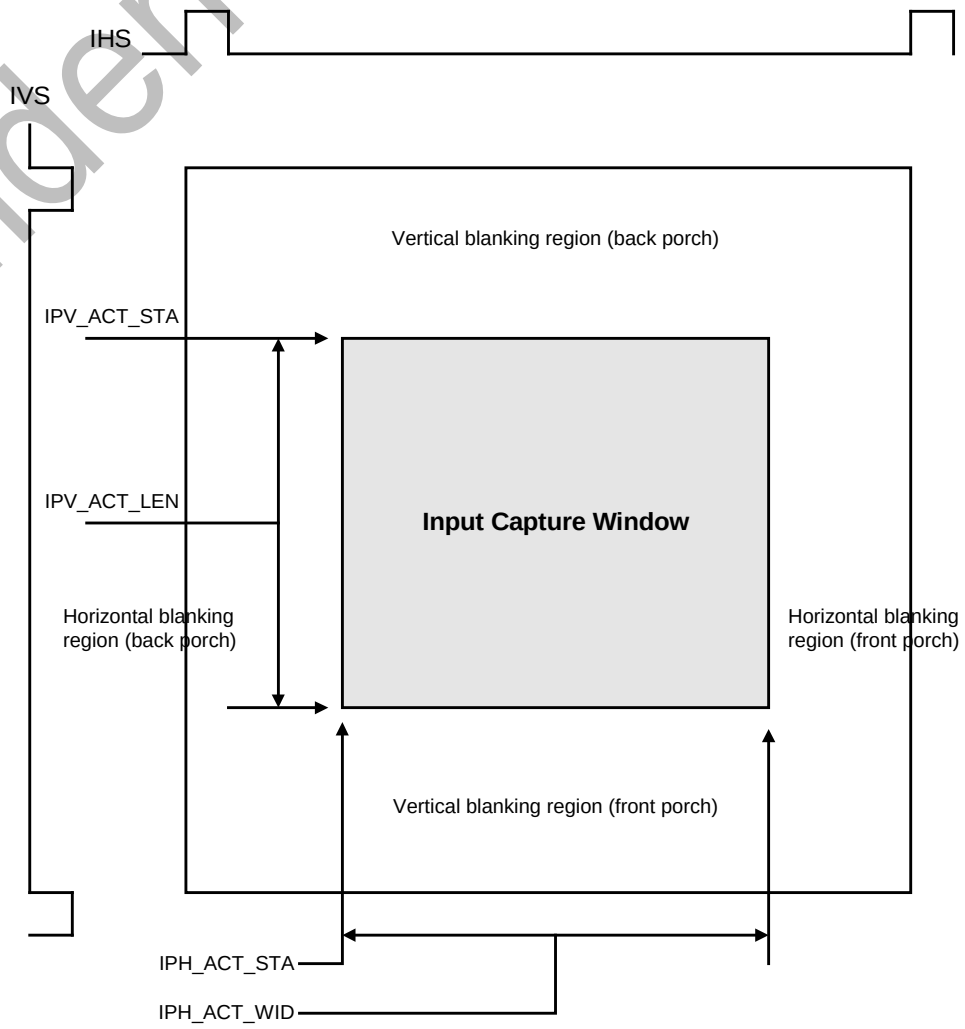


Figure 2 Input Capture Window

4.2 Output Timing

Display Output Timing

The display output port sends single/double pixel data transfer and synchronized display timing to an external device. The display port also support display panel with 6-bit per color, turn on the dithering function to enhance color depth.

In single pixel output mode, single pixel data (24-bit RGB) is transferred to display port A on each active edge of DCLK, the rate of DCLK is also equal to display pixel clock. The sync & enable signals are also sent to display port on each active edge of DCLK.

In double pixel output mode, double pixel data (48-bit RGB) is transferred to display port A & B on each active edge of DCLK and the rate of DCLK is equal to half display pixel clock at this moment. The sync & enable signals are also sent to display port on each active edge of DCLK.

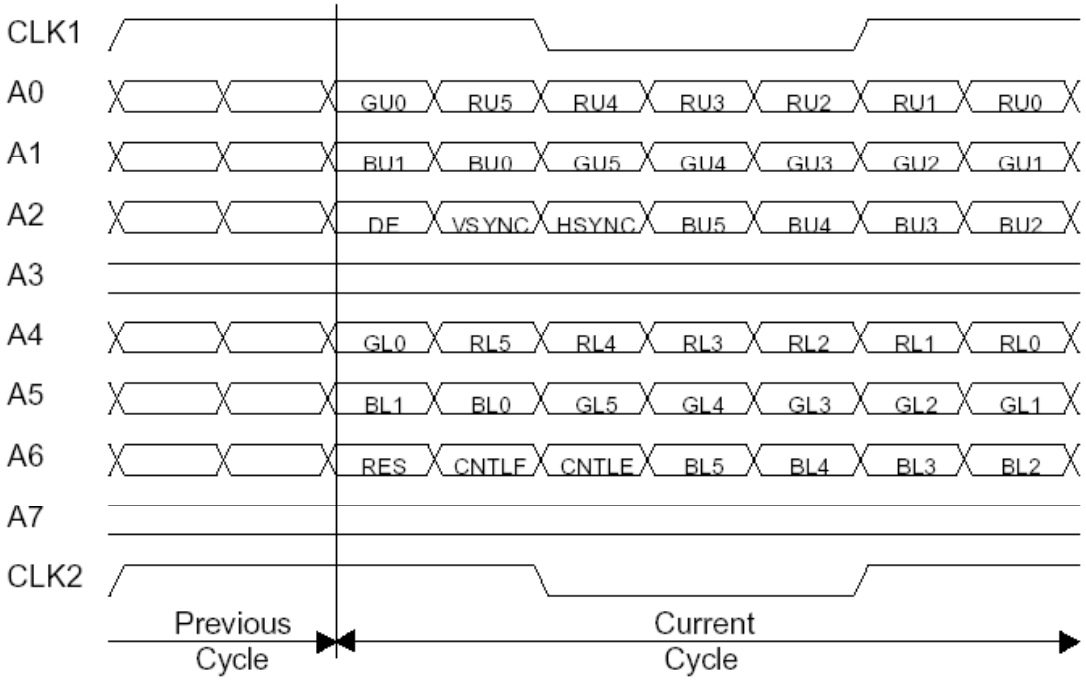


Figure 4 LVDS 18bit Display Timing

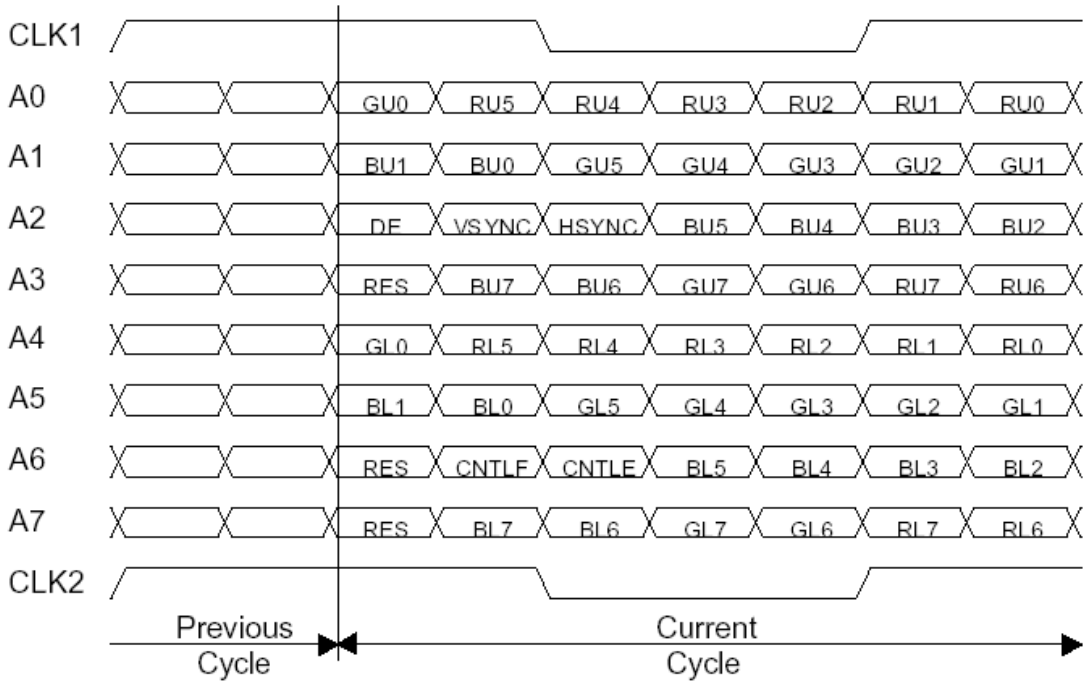


Figure 5 LVDS 24 bit Display Timing

Display Active Window

These registers to define the **display active window** shown below in application of frame sync mode. Refer to the register description for detail.

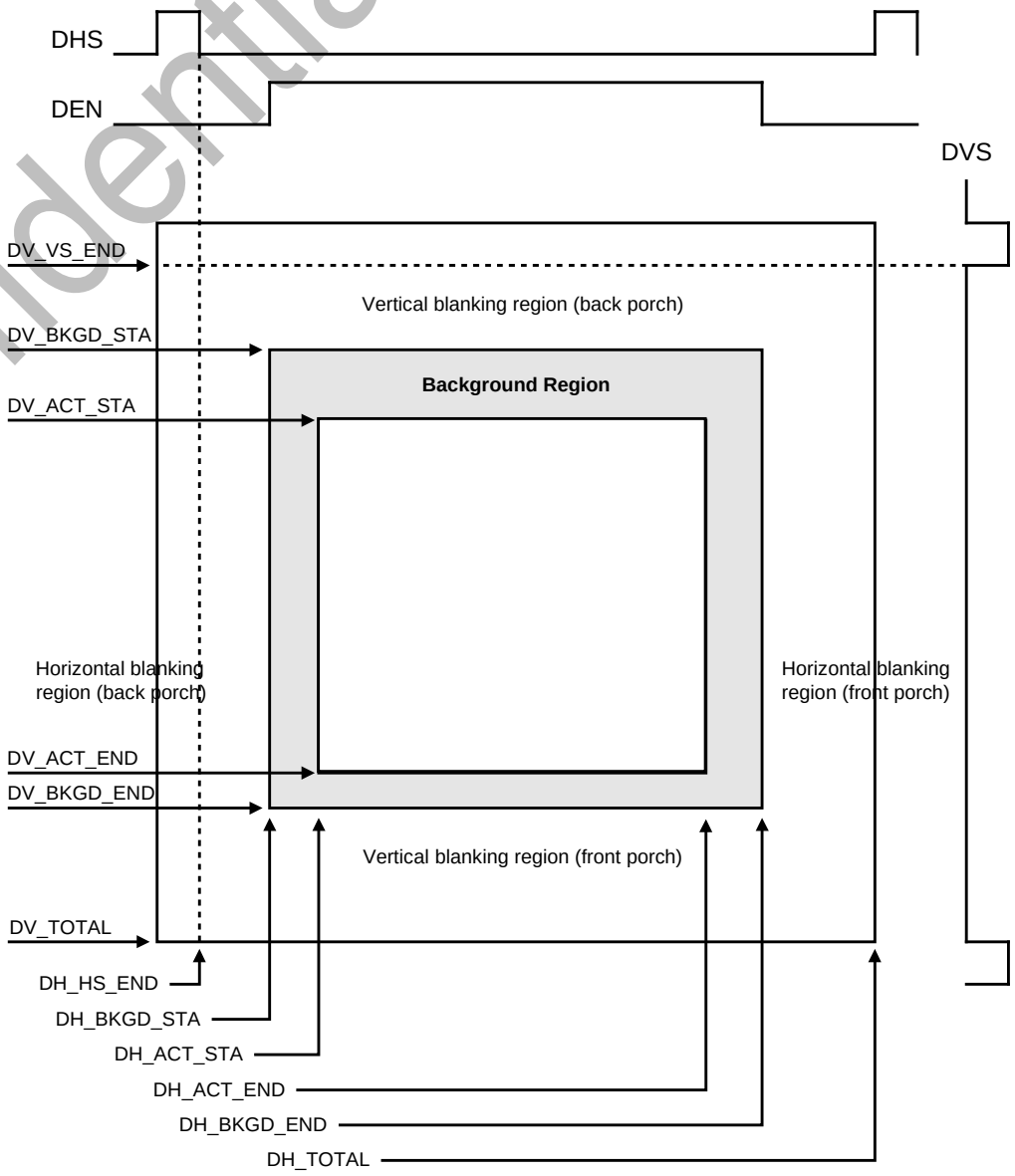


Figure 6 Display Active Window Diagram

4.3 Color Processing

Digital color R & G & B independent channel contrast, brightness, gamma, dithering controls are built in RTD. The contrast control is performed a multiply value from 0 to 2 for each R/G/B channel. The brightness control is used to set an offset value from –512 to +511 also for each R/G/B channel. Also RTD2023L provided 10 bit gamma and a high performance dithering function.

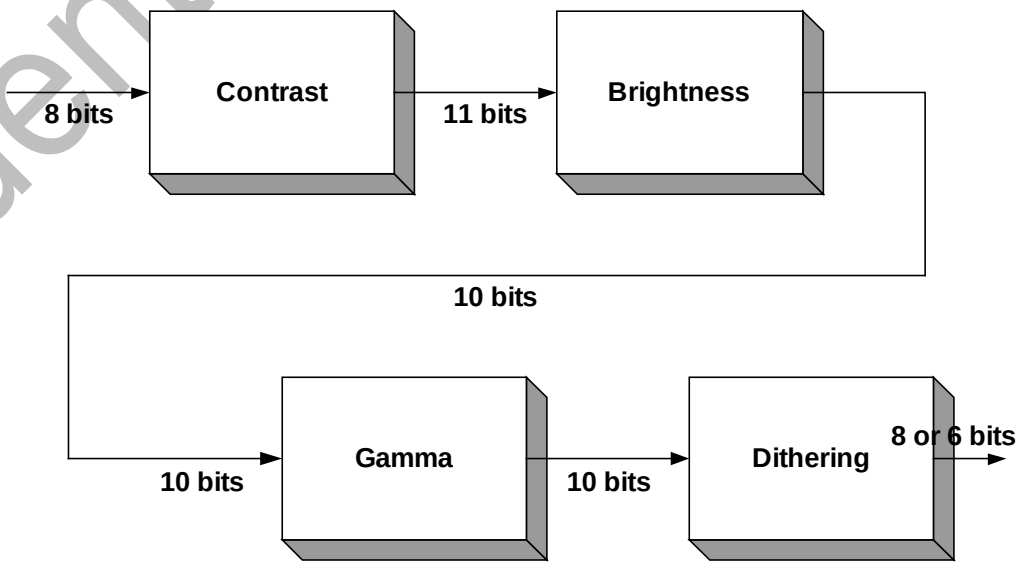


Figure 7 Color Processing Block Diagram

4.4 OSD & Color LUT

Build-In OSD

The detailed function-description of build-in OSD, please refer to the application note for RTD embedded OSD.

Color LUT & Overlay Port

The following diagram presents the data flow among the gamma correction, dithering, overlay MUX, OSD LUT and output format conversion blocks.

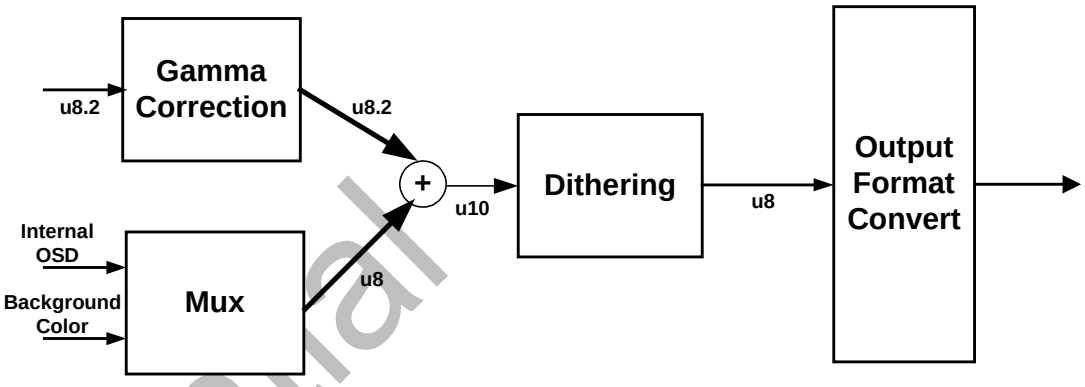


Figure 8 OSD color look-up table data path diagram

4.5 Auto-Adjustment

There are two main independent auto-adjustment functions supported by RTD, including auto-position & auto-tracking. The operation procedure is as following;

Auto-Position

1. Define the RGB color noise margin: When the value of color channel R or G or B is greater than these noise margins, a valid pixel is found.
2. Define the threshold-pixel for vertical boundary search
3. Define the boundary window of searching for horizontal boundary search.
4. Start auto-function.
5. The result can be read from register.

Auto-Tracking

1. Setting the control-registers for the function (auto-phase, auto-balance) according to the Control-Table.
2. Define the Diff-Threshold
3. Define the boundary window of searching for tracking window.
4. Start auto-function.
5. The result can be read from register

4.6 PLL System

Inside the RTD, there are four PLL systems for display clock and ADC sample clock (PLL1, PLL2, M2PLL, DPLL).

DCLK PLL

DPLL frequency = F_IN * DPM / DPN * Divider.

F_IN is input crystal frequency. DPM and DPN is in ***DPLL_M*** and ***DPLL_N***. Divider is in ***DPLL_N***, and it divide PLL frequency by 1, 2, 4 or 8.

According to parameter DPN, you must set LPF Mode in ***DPLL_WD***. If LPF Mode is 1, the charge pump current, Ich, must be DPM/17.6, while Ich must be DPM/1.67 if LPF Mode is 0. The charge pump current Ich is in ***DPLL_CRNT***.

Spread-Spectrum function is also build in DCLK to reduce EMI. You can control the SSP_I, SSP_W, and FMDIV to fine-tune the EMI.

M2PLL

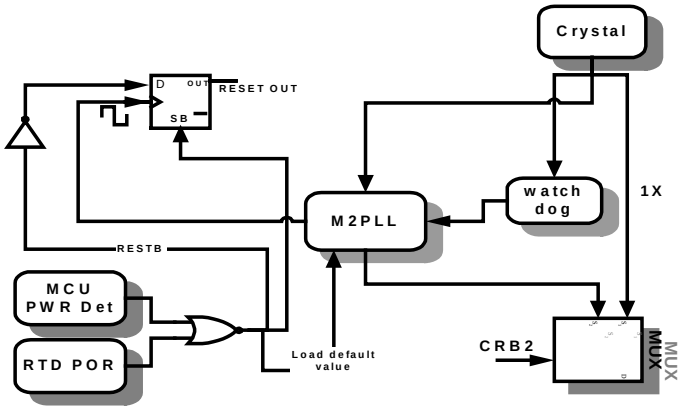


Figure 9 M2PLL System Block Diagram

M2PLL is a PLL used to double the input Xtal clock. You can change M2PLL M & N code to double the Xtal clock (M2PLL M code: CRB2[7:4], M2PLL N code:CRB2[1]). And user can use only one Xtal to share between MCU and Scalar.

ADC Pixel Sampling PLL

The input pixel sampling PLL of RTD2023L compose of PLL1 and PLL2 and DDS, the hybrid PLL system inherently has a process-independent advantages comparing with pure analog PLL, DDS synthesizer is in charge of the phase-frequency control, PLL1 provided a high frequency to get a larger bandwidth letting the system fast locking, PLL2 finally synthesize the desired pixel sampling clock. The block diagram shown below describes our high-performance tracking system.

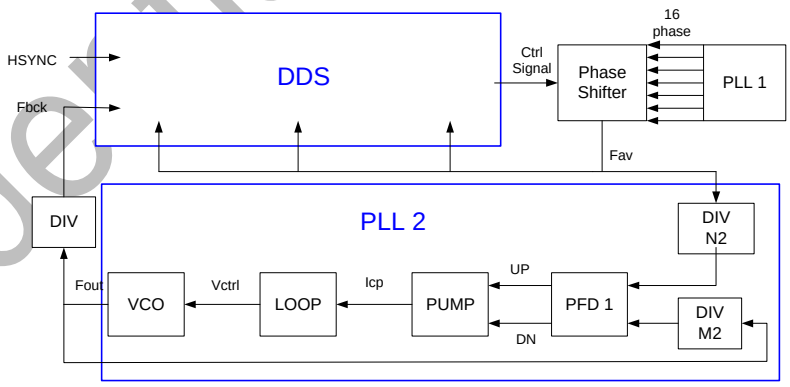


Figure 10 APLL System Block Diagram

4.7 Host Interface

Serial Interface(Double Data Rate):

Any transaction should start from asserted the SCSB low and stop after the SCSB goes high.

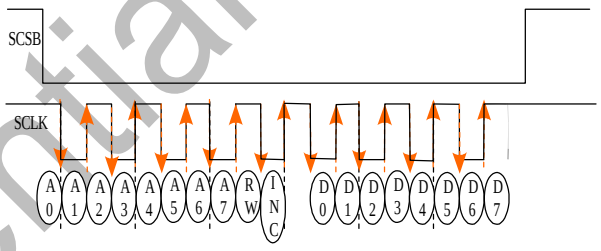


Figure 11 Serial Port Read with Dual edge data latch

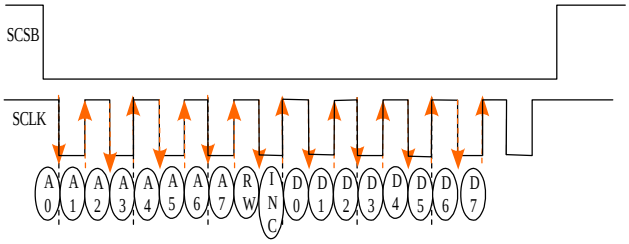


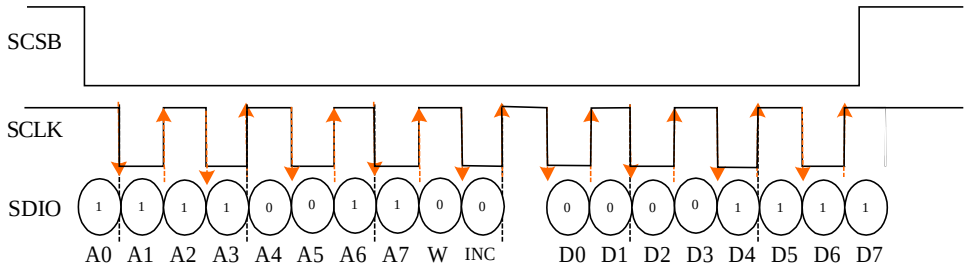
Figure 12 Serial Port Write with Dual edge data latch

A0	A1	A2	A3	A4	A5	A6	A7	R/W	INC	D0	D1	D2	D3	D4	D5	D6	D7

Serial port data alignment

Host Interface Determination:

After the hardware reset signal, the MCU must be send write command data (write address **0xCF**, **no address increment**, the data **0xF0**) to determine the interface port.



4.8 Reset Output

We have the RESET_OUT function, and also reserve the RESET_IN function. By the bounding of internal pins we can select two kinds of reset function. First of all is only reset-out, we can output the reset signal to MCU, and the MCU can reset the RTD by firmware. The second is RTD output reset and also reset itself. Notice that the reset output is positive polarity, besides, the reset output is open-drain pin, please don't forget to attach a **pull-up resistor (10K).**

The reset function for 3.3V operating voltage detection is determined by **33VRST_REF** voltage, No matter 5V or 3.3V MCU is been used, divider the input voltage on 33VRST_REF to 2.2V for internal power sensing circuit detecting, the divider resistor should be 10K level avoiding current leakage.

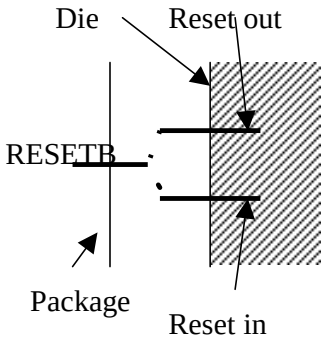


Figure 13 Three kinds of RESET function

4.9 The Programmable Schmitt Trigger of HSYNC

To get better waveform of the input HSYNC, we have a programmable Schmitt Trigger circuit. For different HSYNC amplitude and polarity, we can select different setting of the threshold voltage. The $\mathbf{V_t^+}$ and the $\mathbf{V_t^-}$ can be selected by register CR97

We can select the old mode or the new mode. When using the new mode we can directly determine the positive threshold voltage (1.4V, 1.6V… 2.6V), and we can choose the hysterias from the $\mathbf{V_t^+}$ to determine the $\mathbf{V_t^-}$ (0.6V, 0.8V, 1.0V, 1.2V). We also can finely tune the voltage by minus 0.1V. For application, we can select different threshold voltage by the polarity of the HSYNC. The control register is CR97

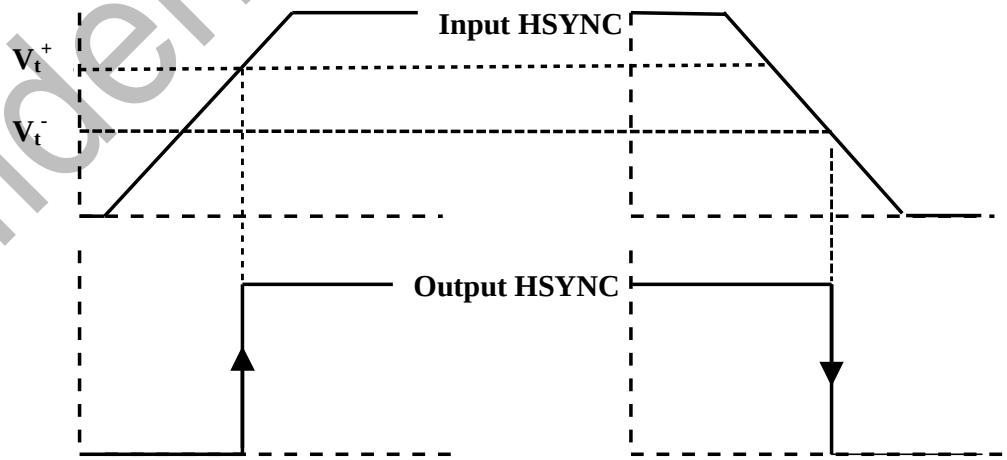


Figure 14 The Schmitt Trigger Behavior Diagram

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5. Register description

Global event flag

Reading unimplemented registers will return 0.

Address: 00 **ID_REG** **Default: 11**

Bit	Mode	Function
7:0	R	**MSB 4 bits:** 0001-product code **LSB 4 bits:** 0001 rev. code

Address: 01 **HOSTCTRL** **Default: 02**

Bit	Mode	Function
7:3	--	**Reserved to 0**
2	R/W	**Power Down Mode Enable** 0: Normal (Default) 1: Enable power down mode Turn off ADC R/G/B/Banggap/DPLL/LVDS/PLL1/PLL2/SOG/SYNC PROC
1	R/W	**Power Saving Mode Enable** 0: Normal 1: Enable power saving mode (Default) Turn off ADC R/G/B/DPLL/LVDS/PLL1/PLL2
0	R/W	**Software Reset Whole Chip (Low pulse at least 8ms)** 0: Normal (Default) 1: Reset (All registers are reset to default except HOST_CTRL& M2PLL , the only difference with Hardware-Reset is power on latch won't not work)

Address: 02 **STATUS0 (Status0 Register)** **Default: 00h**

Bit	Mode	Function
7	R	**ADC_PLL Non-Lock:** If the ADC_PLL non-lock occurs, this bit is set to "1".
6	R	**Input VSYNC Error** If the input vertical sync occurs within the programmed active period, this bit is set to "1".
5	R	**Input HSYNC Error** If the input horizontal sync occurs within the programmed active period, this bit is set to "1".
4:3	--	**Reserved**
2	R	**ADC Input Vertical/Horizontal Sync Occurs** Input V or H sync edge occurs; this bit is set to "1".

1	R	**Input Overflow Status** (Frame Sync Mode) If an overflow in the input data capture buffer occurs, this bit is set to "1".[2]
0	R	**Line Buffer Underflow status** (Frame Sync Mode) If an underflow in the line-buffer occurs, this bit is set to "1".

Write to clear status.

Address: 03 **STATUS1 (Status1 Register)** **Default: 00h**

Bit	Mode	Function
7	R	**Line Buffer Overflow Status**[3] 1: Line Buffer overflow has occurred since the last status cleared
6	R	**Line Buffer Underflow Status** 1: Line Buffer underflow has occurred since the last status cleared
5	R	**DENA Stop Event Status** 1: If the DENA stop event occurred since the last status cleared
4	R	**DENA Start Event Status** 1: If the DENA start event occurred since the last status cleared
3	R	**DVS Start Event Status** 1: If the DVS start event occurred since the last status cleared
2	R	**IENA Stop Event Status** 1: If the IENA stop event occurred since the last status cleared
1	R	**IENA Start Event Status** 1: If the IENA start event occurred since the last status cleared
0	R	**IVS Start Event Status** 1: If the IVS start event occurred since the last status cleared

Write to clear status.

Address: 04 **Reserved** **Default: 00h**

[2] Only the first event of input overflow/underflow will be recorded at the same time.

[3] Both input overflow/underflow status will be recorded whenever it happens.

Input Video Capture

Capture Format

Address: 05 **VGIP_CTRL (Video Graphic Input Control Register)** **Default: 00h**

<table>
<tr><th>Bit</th><th>Mode</th><th>Function</th></tr>
<tr><td>7</td><td>R/W</td><td>8 bit Random Generator
0: Disable(Default)
1: Enable</td></tr>
<tr><td>6</td><td>R/W</td><td>Input Test Mode:
0: Disable (Default)
1: Video8 input will go through RGB channel, AVS=>IVS, AHS=>IHS, VCLK=>ICLK</td></tr>
<tr><td>5</td><td>R/W</td><td>VGIP Double Buffer Ready
0: Not Ready to Apply
1: Ready to Apply
I When the list table of CR05 [4] is set, then enable CR05 [5], finally, hardware will auto load these value into RTD2023L as the trigger event happens and clear CR05 [5] to 0.</td></tr>
<tr><td>4</td><td>R/W</td><td>VGIP Double Buffer Mode Enable(Each register describe below has its own double buffer)
0: Disable (Original- Write instantly by MCU write cycles)
1: Enable (Double Buffer Function Write Mode)
<table>
<tr><th>Register</th><th>Trigger Event</th></tr>
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		00: Embedded ADC (ADC_HS)(Default) 01: Reserved 10: Reserved 11: Reserved
1	R/W	**Input graphic/video mode** 0: From analog input (input captured by 'Input Capture Window') (Default) 1: From digital input (captured start by 'enable signal', but sill stored in 'capture window size')
0	R/W	**Input Video Run Enable** 0: No data is transferred (Default) 1: Sampling input pixels

Address: 06 **VGIP_SIGINV (Input Control Signal Inverted Register)** **Default: 00h**

Bit	Mode	Function
7	R/W	**Safe Mode** 0: Normal (Default) 1: Safe Mode Enable, mask 1 frame IVS of every 2 frame IVS, slow down input frame rate.
6	R/W	**IVS Sync with IHS Control (avoid VS bouncing)** 0: Enable (Default) 1: Disable
5:4	--	**Reserved**
3	R/W	**Input VS Signal Polarity Inverted** 0: Not inverted (VS = positive polarity) (Default) 1: Inverted (VS = negative polarity)
2	R/W	**Input HS Signal Polarity Inverted** 0: Not inverted (HS = positive polarity) (Default) 1: Inverted (HS = negative polarity)
1	R/W	**Input ENA Signal Polarity Inverted** 0: Not inverted (input high active) (Default) 1: Inverted (while input low active)
0	R/W	**Input Clock Polarity** 0: Rising edge latched (Default) 1: Falling edge latched

Address: 07 **VGIP_DELAY_CTRL** **Default: 00h**

Bit	Mode	Function
7	R	**6-Iclk-delay HS level latched by VS rising edge**
6	R	**HS level latched by VS rising edge**

5	R	**HS level latched by 6-Iclk-delay VS rising edge**
4	R/W	**Add one clock delay to IHS delay** 0: Disable (Default) 1: Enable
3	R/W	**HSYNC Synchronize Edge** 0: HSYNC is synchronized by the positive edge of the input clock 1: HSYNC is synchronized by the negative edge of the input clock (HSYNC source is selected by **CR48[0]** and then synchronized)
2	R/W	**VSYNC Synchronize Edge** 0: latch VS by the negative edge of input HSYNC(Default) 1: latch VS by the positive edge of input HSYNC
1:0	R/W	**Input Clock Delay Control:** 00: Normal (Default) 01: 1ns delay 10: 2ns delay 11: 3ns delay

Address: 08 **Reserved** **Default: 00h**

Input Frame Window (All capture window setting unit is 1)

Address: 09 **IPH_ACT_STA_H(Input Horizontal Active Start)** **Default: 00h**

Bit	Mode	Function
7:3	--	**Reserved to 0**
2:0	R/W	**Input Video Horizontal Active Start** -- High Byte [10:8]

Address: 0A **IPH_ACT_STA_L (Input Horizontal Active Start Low)** **Default:00h**

Bit	Mode	Function
7:0	R/W	**Input Video Horizontal Active Start** -- Low Byte [7:0]

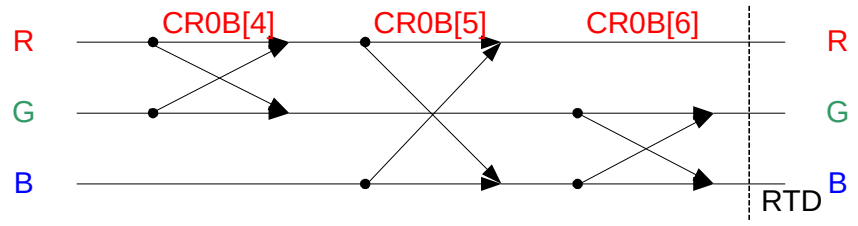
- In analog mode, the number of pixel clocks from the leading edge of HS to the first pixel of the active line.

  Target = IPH_ACT_STA(>=2) +2,

- In digital mode, the **IPH_ACT_STA** is actually the same as it set.

Address: 0B **IPH_ACT_WID_H (Input Horizontal Active Width High)** **Default: 00h**

Bit	Mode	Function
7	--	**Reserved**
6	R/W	**ADC input G/B Swap** 0: No Swap 1: Swap
5	R/W	**ADC input R/B Swap** 0: No Swap 1: Swap
4	R/W	**ADC input R/G Swap** 0: No Swap 1: Swap
3	R/W	**Double Clock Input** 0: Single Clock 1: Double Clock
2:0	R/W	**Input Video Horizontal Active Width** – High Byte [10:8]



Address: 0C **IPH_ACT_WID_L (Input Horizontal Active Width Low)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Input Video Horizontal Active Width** -- Low Byte [7:0]

This register defines the number of active pixel clocks to be captured.

(Horizontal Active Start + Horizontal Active Width) < 2047

Address: 0D **IPV_ACT_STA_H (Input Vertical Active Start High)** **Default: 00h**

Bit	Mode	Function
7:3	--	**Reserved**
2:0	R/W	**Input Video Vertical Active Start** – High Byte [10:8]

Address: 0E **IPV_ACT_STA_L (Input Vertical Active Start Low)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Input Video Vertical Active Start** – Low Byte [7:0]

The numbers of lines from the leading edge of selected input video VSYNC to the first line of the active window.

The value above should be larger than 1.

Address: 0F **IPV_ACT_LEN_H (Input Vertical Active Lines)** **Default: 00h**

Bit	Mode	Function
7	R	**SAV/EAV two-bit error (write to clear)**
6	R	**SAV/EAV one-bit error (write to clear)**
5	--	**Reserved**
4:3	R	**The number of input HS between 2 input VS. LSB bit [1:0]**
2:0	R/W	**Input Video Vertical Active Lines** – High Byte [10:8]

Address: 10 **IPV_ACT_LEN_L (Input Vertical Active Lines)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Input Video Vertical Active Lines** – Low Byte [7:0]

This register defines the number of active lines to be captured.

Address: 11 **IVS_DELAY (Internal Input-VS Delay Control Register)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Input VS delay count by Input HSYNC [7:0]** It's IVS delay for capture and digital filter, not for auto function

Address: 12 **IHS_DELAY (Internal Input-HS Delay Control Register)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Input HS delay count by Input clock [7:0]** It's IHS delay for capture and digital filter, not for auto function

Address: 13 **VGIP_HV_DELAY** **Default: 00h**

Bit	Mode	Function

7:6	R/W	**Input HS delay count by input clock for Auto function** 00: No delay 01: 32 pixels 10: 64 pixels 11: 96 pixels
5:4	R/W	**Input VS delay count by input HSYNC for Auto function** 00: No delay 01: 3 line 10: 7 line 11: 15 line
3:2	--	**Reserved to 0**
1	R/W	**Input VS delay count by Input HSYNC[8]**
0	R/W	**Input HS delay count by Input clock[8]**

FIFO Window

Address: 14 **DRL_H_BSU (Display Read High Byte Before Scaling-Up)** **Default: 00h**

Bit	Mode	Function
7	--	**Reserved**
6:4	R/W	**Display window read width before scaling up:** High Byte [10:8]
3	--	**Reserved**
2:0	R/W	**Display window read length before scaling up:** High Byte [10:8]

Address: 15 **DRW_L_BSU (Display Read Width Low Byte Before Scaling-Up)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Display window read width before scaling up:** Low Byte [7:0]

Address: 16 **DRL_L_BSU (Display Read Length Low Byte Before Scaling-Up)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Display window read length before scaling up:** Low Byte [7:0]

- The setting above should be use 2 as unit

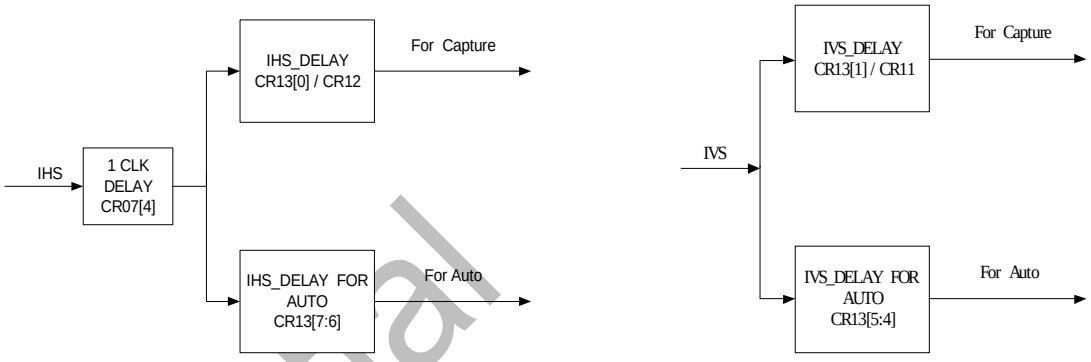


Figure 15 IHS_DELAY Path Diagram

Digital Filter

Address: 17 **DIGITAL_FILTER_CTRL** **Default: 00h**

Bit	Mode	Function
7:5	R/W	**Access Port Write Enable** 000: disable 001: phase access port 010: negative smear access port 011: positive smear access port 100: negative ringing access port 101: positive ringing access port 110: mismatch access port 111: B/G/R channel digital filter enable
4:3	R/W	**Two condition occur continuous** (ringing to smear) 00: disable(hardware is off , depend on firmware) 01: only reduce ringing condition 10: only reduce smear condition 11: no adjust (hardware is on, but do nothing)
2:0	--	**Reserved to 0**

Address: 18 **DIGITAL_FILTER_PORT** DIGITAL_FILTER_CTRL[7:5] = 111 **Default: 00h**

Bit	Mode	Function
7	R/W	**G EN** : function enable 0: function disable 1: function enable
6	R/W	**B EN** : function enable 0: function disable

		1: function enable
5	R/W	**R EN** : function enable 0: function disable 1: function enable
4	R/W	**Initial value**: 0: raw data 1: extension
3:0	--	**Reserved to 0**

DIGITAL_FILTER_PORT DIGITAL_FILTER_CTRL[7:5] = 000 ~ 110 **Default: 00h**

Bit	Mode	Function
7	R/W	**EN**: function enable 0: function disable 1: function enable
6:4	R/W	**THD_OFFSET** Threshold value of phase and mismatch or offset value of smear and ringing
3:2	R/W	**DIV:** divider value 00: 0 01: 1 10: 2 11: 3
1:0	--	**Reserved to 0**

THD_OFFSET define:

The THD value define of phase enhance function

Bit6~4	000	001	010	011	100	101	110	111
Value	112	128	144	160	176	192	208	224

The offset value define of smear and ringing reduce function

Bit6~4	000	001	010	011	100	101	110	111
Value	no use	16	32	48	64	80	96	112

The THD value define of mismatch enhance function

Bit6~4	000	XX1
Value	1	2

Scaling Up Function

Address: 19 **SCALE_CTRL0 (Scale Control Register)** **Default: 00h**

Bit	Mode	Function

7:6	--	**Reserved**
5	R	**Display Line Buffer Ready** 0: Busy 1: Ready
4	R/W	**Enable Full Line buffer:** 0: Disable (Default) 1: Enable
3	R/W	**Vertical Line Duplication** 0: Disable 1: Enable
2	R/W	**Horizontal pixel Duplication** 0: Disable 1: Enable
1	R/W	**Enable the Vertical Filter Function:** 0: By pass the vertical filter function block (Default) 1: Enable the vertical filter function block
0	R/W	**Enable the Horizontal Filter Function:** 0: By pass the horizontal filter function block (Default) 1: Enable the horizontal filter function block

- When using H/V duplication mode, FIFO window width set original width, but FIFO width height should be 2X the original height.

Address: 1A **SF_ACCESS_Port (Scaling Factor Access Port)** **Default: 00h**

Bit	Mode	Function
7	R/W	**Enable scaling-factor access port**
6:5	--	**Reserved to 0**
4:0	R/W	**Scaling factor port address**

- When disable scaling factor access port, the access port pointer will reset to 0

Address: 1B-00 **HOR_SCA_H (Horizontal Scale Factor High)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Bit [19:16] of horizontal scale factor**

Address: 1B-01 **HOR_SCA_M (Horizontal Scale Factor Medium)**

Bit	Mode	Function
7:0	R/W	**Bit [15:8] of horizontal scale factor**

Address: 1B-02 **HOR_SCA_L (Horizontal Scale Factor Low)**

Bit	Mode	Function

7:0	R/W	**Bit [7:0] of horizontal scale factor**

Address: 1B-03 **VER_SCA_H (Vertical Scale Factor High)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Bit [19:16] of vertical scale factor**

Address: 1B-04 **VER_SCA_M (Vertical Scale Factor Medium)**

Bit	Mode	Function
7:0	R/W	**Bit [15:8] of vertical scale factor**

Address: 1B-05 **VER_SCA_L (Vertical Scale Factor Low)**

Bit	Mode	Function
7:0	R/W	**Bit [7:0] of vertical scale factor**

This scale-up factor includes a 20-bit fraction part to present a vertical scaled up size over the stream input. For example, for 600-line original picture scaled up to 768-line, the factor should be as follows:

$(600/768) \times 2^{20} = 0.78125 \times 2^{20} = 819200 = C8000h = 0Ch, 80h, 00h.$

Address: 1B-06 **Horizontal Scale Factor Segment 1 Pixel** **Default: 00h**

Bit	Mode	Function
7:3	--	**Reserved**
2:0	R/W	Bit [10:8] of Scaling Factor Segment 1 pixel

Address: 1B-07 **Horizontal Scale Factor Segment 1 Pixel** **Default: 00h**

Bit	Mode	Function
7:0	R/W	Bit [7:0] of Scaling Factor Segment 1 pixel

Address: 1B-08 **Horizontal Scale Factor Segment 2 Pixel** **Default: 00h**

Bit	Mode	Function
7:3	--	**Reserved**
2:0	R/W	Bit [10:8] of Scaling Factor Segment 2 pixel

Address: 1B-09 **Horizontal Scale Factor Segment 2 Pixel** **Default: 00h**

Bit	Mode	Function
7:0	R/W	Bit [7:0] of Scaling Factor Segment 2 pixel

Address: 1B-0A **Horizontal Scale Factor Segment 3 Pixel** **Default: 00h**

Bit	Mode	Function
7:3	--	**Reserved**
2:0	R/W	Bit [10:8] of Scaling Factor Segment 3 pixel

Address: 1B-0B **Horizontal Scale Factor Segment 3 Pixel** **Default: 00h**

Bit	Mode	Function
7:0	R/W	Bit [7:0] of Scaling Factor Segment 3 pixel

Address: 1B-0C **Horizontal Scale Factor Delta 1** **Default: 00h**

Bit	Mode	Function
7:5	--	**Reserved**
4:0	R/W	Bit [12:8] of Horizontal Scale Factor delta 1

Address: 1B-0D **Horizontal Scale Factor Delta 1** **Default: 00h**

Bit	Mode	Function
7:0	R/W	Bit [7:0] of Horizontal Scale Factor delta 1

Address: 1B-0E **Horizontal Scale Factor Delta 2** **Default: 00h**

Bit	Mode	Function
7:5	--	**Reserved**
4:0	R/W	Bit [12:8] of Horizontal Scale Factor delta 2

Address: 1B-0F **Horizontal Scale Factor Delta 2** **Default: 00h**

Bit	Mode	Function
7:0	R/W	Bit [7:0] of Horizontal Scale Factor delta 2

Address: 1B-10 **Horizontal Filter Coefficient Initial Value** **Default: C4h**

Bit	Mode	Function
7:0	R/W	Accumulate Horizontal filter coefficient initial value

Address: 1B-11 **Vertical Filter Coefficient Initial Value** **Default: C4h**

Bit	Mode	Function
7:0	R/W	Accumulate Vertical filter coefficient initial value

Address: 1C **FILTER_CTRL (Filter Control Register)** **Default: 00h**

Bit	Mode	Function
7	R/W	**Enable Filter Coefficient Access** 0: Disable (Default) 1: Enable
6	R/W	**Select H/V User Defined Filter Coefficient Table for Access Channel** 0: 1st coefficient table (Default) 1: 2nd coefficient table
5	R/W	**Select Horizontal user defined filter coefficient table** 0: 1st Horizontal Coefficient Table (Default) 1: 2nd Horizontal Coefficient Table
4	R/W	**Select Vertical user defined filter coefficient table** 0: 1st Vertical Coefficient Table (Default) 1: 2nd Vertical Coefficient Table
3:0	--	**Reserved to 0**

- The User Defined Filter Coefficient Table can be modified on-line. Only the non-active coefficient-table can be

modified, and then switch it to active.

Address: 1D **FILTER_PORT (User Defined Filter Access Port)** **Default: 00h**

Bit	Mode	Function
7:0	W	**Access port for user defined filter coefficient table**

- When enable filter coefficient accessing, the first write byte is stored into the LSB(bit[7:0]) of coefficient #1 and the second byte is into MSB (bit[8:11]). Therefore, the valid write sequence for this table is c0-LSB, c0-MSB, c1-LSB, c1-MSB, c2-LSB, c2-MSB … c63-LSB & c63-MSB, totally 64 * 2 cycles. Since the 128 taps is symmetric, we need to fill the 64-coefficient sequence into table only.

Address: 1E **OSD_REFERENCE__DEN** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Position Of Reference DEN for OSD[7:0]**

Address: 1F **NEW_DV_CTRL** **Default: 00h**

Bit	Mode	Function
7	R/W	**New Timing Enable** 0: Disable 1: Enable
6	R/W	**Line Compensation Enable** 0: Disable 1: Enable
5	R/W	**Pixel Compensation Enable** 0: Disable 1: Enable
4	R/W	**Reserved to 0**
3:0	R/W	**DCLK_Delay[11:8]**

Address: 20 **NEW_DV_DLY** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**DCLK_Delay[7:0]**

When CR 1F[7]=1, CR1F[3:0] & CR20 can't be 0, when compensation pixel is smaller than 1 total line, just turn on pixel compensation, otherwise users should turn on line compensation

Address: 21 Reserved

Scaling Down Control

Address: 22 **SCALE_DOWN_CTRL (Scale Down Control Register)** **Default: 00h**

Bit	Mode	Function
7	R	**Bist for FiFo ok** 0: Fail 1: Ok
6	R	**Bist for Line Buffer one ok** 0: Fail 1: Ok
5	R	**Bist for Line Buffer two ok** 0: Fail 1: Ok
4	R/W	**Fifo Bist Function Start (Auto clear to 0 when finish)** 0: Finish 1: Start
3	R/W	**Line Buffer Bist Function Start (Auto clear to 0 when finish)** 0: Finish 1: Start
2	R/W	**Vertical Scale-Down Compensation** 0: Disable (Default) 1: Enable
1	R/W	**Horizontal scale down function enable:** 0: Disable scale down function (Default) 1: Enable scale down function
0	R/W	**Vertical scale down function enable:** 0: Disable scale down function (Default) 1: Enable scale down function

Address: 23 **H_SCALE_DOWN_H (Horizontal scale down factor register)**

Bit	Mode	Function
7:3	R/W	**Horizontal Scale Down Initial Select** [4:0]
2:0	R/W	**Horizontal Scale Down Factor:** High Byte [18:16]

- Scale Down Initial Point Select: for example, if the value is 20, we select the initial point is 40/64

Address: 24 **H_SCALE_DOWN_M (Horizontal scale down factor register)**

Bit	Mode	Function
7:0	R/W	**Horizontal Scale Down Factor:** Low Byte [15:8]

Address: 25 **H_SCALE_DOWN_L (Horizontal scale down factor register)**

Bit	Mode	Function
7:0	R/W	**Horizontal Scale Down Factor:** Low Byte [7:0]

- First left side point is always latched, then the remaining points interpolates by the shrinking ratio.
- Horizontal scaling down factor should be (Xi / Xm))* (2^{17}) truncate.
- The largest scale down ratio is 1/4 (integer part 2 bits)
- Meanwhile, Xi = horizontal input width; Xm = horizontal memory write width

Address: 26 **V_SCALE_DOWN_H (Vertical scale down factor register)**

Bit	Mode	Function
7:6	--	**Reserved to 0**
5:0	R/W	**Vertical Scale Down Factor:** High Byte [13:8]

Address: 27 **V_SCALE_DOWN_L (Vertical scale down factor register)**

Bit	Mode	Function
7:0	R/W	**Vertical Scale Down Factor:** Low Byte [7:0]

- Vertical scaling down factor = (Yi / Ym)*(2^{12}) truncate.
- The largest scale down ratio is 1/4 (integer part 2 bits)
- Meanwhile, Yi = vertical input width; Ym = vertical memory write width

Display Format

Address: 28 **VDIS_CTRL (Video Display Control Register)** **Default: 20h**

Bit	Mode	Function
7	R/W	**Force Display Timing Generator Enable: (Should be set when in Free-Run mode)** 0: wait for input IVS trigger 1: force enable
6	R/W	**Display Data Output Inverse Enable** 0: Disable (Default) 1: Enable (only when data bus clamp to 0)
5	R/W	**Display Output Force to Background Color** 0: Display output operates normally 1: Display output is forced to the color as selected by background color (CR6D) (Default)
4	R/W	**Display 18 bit RGB Mode Enable** 0: All individual output pixels are full 24-bit RGB (Default) 1: All individual output pixels are truncated to 18-bit RGB
3	R/W	**Frame Sync Mode Enable** 0: Free running mode (Default) 1: Frame sync mode
2	R/W	**Display Output Double Port Enable** 0: Single port output (Default) 1: Double port output
1	R/W	**Display Output Run Enable** 0: DHS, DVS, DEN & DATA bus are clamped to "0" (Default) 1: Display output normal operation.
0	R/W	**Display Timing Run Enable** 0: Display Timing Generator is halted, Zoom Filter halted (Default) 1: Display Timing Generator and Zoom Filter enabled to run normally

Steps to disable output: First set CR28[1]=0, set CR28[6], then set CR28[0]=0 to disable output.

Address: 29 **VDISP_SIGINV (Display Control Signal Inverted)** **Default: 00h**

Bit	Mode	Function
7	R/W	**DHS Output Format Select (only available in Frame Sync)** 0: The first DHS after DVS is active (Default) 1: The first DHS after DVS is inactive
6	R/W	**Display Data Port Even/Odd Data Swap:**

		0: Disable (Default) 1: Enable
5	R/W	**Display Data Port Red/Blue Data Swap** 0: Disable (Default) 1: Enable
4	R/W	**Display Data Port MSB/LSB Data Swap** 0: Disable (Default) 1: Enable
3	R/W	**Skew Display Data Output** 0: Non-skew data output (Default) 1: Skew data output
2	R/W	**Display Vertical Sync (DVS) Output Invert Enable:** 0: Display Vertical Sync output normal active high logic (Default) 1: Display Vertical Sync output inverted logic
1	R/W	**Display Horizontal Sync (DHS) Output Invert Enable:** 0: Display Horizontal Sync output normal active high logic (Default) 1: Display Horizontal Sync output inverted logic
0	R/W	**Display Data Enable (DEN) Output Invert Enable:** 0: Display Data Enable output normal active high logic (Default) 1: Display Data Enable output inverted logic

Address: 2A **DH_TOTAL_H (Display Horizontal Total Pixels)**

Bit	Mode	Function
7:4	--	**Reserved to 0**
3:0	R/W	**Display Horizontal Total Pixel Clocks**: High Byte[11:8]

Address: 2B **DH_TOTAL_L (Display Horizontal Total Pixels)**

Bit	Mode	Function
7:0	R/W	**Display Horizontal Total Pixel Clocks:** Low Byte[7:0]

Real DH_Total (Target value)= DH_Total (Register value)+ 4

Address: 2C **DH_HS_END (Display Horizontal Sync End)**

Bit	Mode	Function
7:0	R/W	**Display Horizontal Sync End[7:0]:** Determines the width of DHS pulse in DCLK cycles

Address: 2D **DH_BKGD_STA_H (Display Horizontal Background Start)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Display Horizontal Background Start**: High Byte [11:8]

Address: 2E **DH_BKGD_STA_L (Display Horizontal Background Start)**

Bit	Mode	Function
7:0	R/W	**Display Horizontal Background Start**: Low Byte [7:0]

Determines the number of DCLK cycles from leading edge of DHS to first pixel of Background region.

Real DH_BKGD_STA (Target value)= DH_BKGD_STA (Register value)+ 10

Address: 2F **DH_ACT_STA_H (Display Horizontal Active Start)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Display Horizontal Active Region Start**: High Byte [11:8]

Address: 30 **DH_ACT_STA_L (Display Horizontal Active Start)**

Bit	Mode	Function
7:0	R/W	**Display Horizontal Active Region Start**: Low Byte [7:0]

Determines the number of DCLK cycles from leading edge of DHS to first pixel of Active region.

Real DH_ACT_STA (Target value)= DH_ACT_STA (Register value)+ 10

Address: 31 **DH_ACT_END_H (Display Horizontal Active End)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Display Horizontal Active End**: High Byte [11:8]

Address: 32 **DH_ACT_END_L (Display Horizontal Active End)**

Bit	Mode	Function
7:0	R/W	**Display Horizontal Active End**: Low Byte [7:0]

Determines the number of DCLK cycles from leading edge of DHS to the pixel of background region.

Real DH_ACT_END (Target value)= DH_ACT_END (Register value)+ 10

Address: 33 **DH_BKGD_END_H (Display Horizontal Background End)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Display Horizontal Background end**: High Byte [11:8]

Address: 34 **DH_BKGD_END_L (Display Horizontal Background End)**

Bit	Mode	Function
7:0	R/W	**Display Horizontal Background end**: Low Byte [7:0]

Real DH_BKGD_END (Target value) = DH_BKGD_END (Register value)+ 10

Address: 35 **DV_TOTAL_H (Display Vertical Total Lines)**

Bit	Mode	Function
7:4	--	**Reserved to 0**
3:0	R/W	**Display Vertical Total**: High Byte [11:8]

Address: 36 **DV_TOTAL_L (Display Vertical Total Lines)**

Bit	Mode	Function
7:0	R/W	**Display Vertical Total:** Low Byte [7:0]

CR35, CR36 use as watch dog reference value in ***frame sync*** mode, the event should be the line number of display HS is equal to DV Total.

Address: 37 **DVS_END (Display Vertical Sync End)**

Bit	Mode	Function
7:5	--	**Reserved**
4:0	R/W	**Display Vertical Sync End[4:0]:** Determines the duration of DVS pulse in lines

Address: 38 **DV_BKGD_STA_H (Display Vertical Background Start)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Display Vertical Background Start:** High Byte [11:8] Determines the number of lines from leading edge of DVS to first line of background region.

Address: 39 **DV_BKGD_STA_L (Display Vertical Background Start)**

Bit	Mode	Function
7:0	R/W	**Display Vertical Background Start:** Low Byte [7:0]

Address: 3A **DV_ACT_STA_H (Display Vertical Active Start)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Display Vertical Active Region Start:** High Byte [11:8] Determines the number of lines from leading edge of DVS to first line of active region.

Address: 3B **DV_ACT_STA_L (Display Vertical Active Start)**

Bit	Mode	Function
7:0	R/W	**Display Vertical Active Region Start:** Low Byte [7:0]

Address: 3C **DV_ACT_END_H (Display Vertical Active End)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Display Vertical Active Region End:** High Byte [11:8]

Address: 3D **DV_ACT_END_L (Display Vertical Active End)**

Bit	Mode	Function
7:0	R/W	**Display Vertical Active Region End**: Low Byte [7:0]

Determine the number of lines from leading edge of DVS to the line of following background region.

Address: 3E **DV_BKGD_END_H (Display Vertical Background End)**

Bit	Mode	Function
7:4	--	**Reserved to 0**
3:0	R/W	**Display Vertical Background end:** High Byte [11:8]

Address: 3F **DV_BKGD_END_L (Display Vertical Background End)**

Bit	Mode	Function
7:0	R/W	**Display Vertical Background End:** Low Byte [7:0]

Determine the number of lines from leading edge of DVS to the line of start of vertical blanking.

Frame Sync Fine Tune

Address: 40 **IVS2DVS_DEALY_LINES (IVS to DVS Lines)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**IVS to DVS Lines:** (Only for FrameSync Mode) The number of input HS from IVS to DVS. Should be double buffer by CR05[5:4]

Address: 41 **IV_DV_DELAY_CLK_ODD (Frame Sync Delay Fine Tuning)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Frame Sync Mode Delay Fine Tune [7:0] "00" to disable** **Applied to all fields when Interlaced_FS_Delay_Fine_Tuning is disabled (CR43[1] = 0)** **Only for odd-field when Interlaced_FS_Delay_Fine_Tuning is enabled (CR43[1] = 1)**

In Frame Sync Mode , CR40[7:0] represents output VS delay fine-tuning. For example, it delays the number of (CR41 [7:0] *16 + 16) input clocks. Fill 00h, means 0, fill 01h, and means 32

Address: 42 **IV_DV_DELAY_CLK_EVEN (Frame Sync Delay Fine Tuning)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Frame Sync Mode Delay Fine Tune [7:0] "00" to disable** **Only for even-field when Interlaced_FS_Delay_Fine_Tuning is enabled (CR43[1] = 1)**

Address: 43 **FS_DELAY_FINE_TUNING** **Default: 00h**

Bit	Mode	Function
7:3	R/W	**Frame Sync Mode Fine Tune[4:0]:** Reference to **Fine Tune Delay Mode Select**
2	R/W	**Fine Tune Delay Mode Select** 0: 0/32 -- 2/32 -- 4/32 -- 6/32 ~~~ 62/32 1: 0/32 -- 4/32 -- 8/32 --12/32 ~~~ 124/32
1	R/W	**Interlaced_FS_Delay_Fine_Tuning** 0: Disable (Default) 1: Enable
0	--	**Reserved**

Address: 44 **LAST_LINE_H** **Default: 00h**

Bit	Mode	Function
7	R/W	**Last-line-width / DV-Total Selector :** 0: CR44 [3:0] and CR45 indicate last-line width counted by display clock (Default) 1: CR44 [3:0] and CR45 indicate DHS total number between 2 DVS.
6	R/W	**DV sync with 4X clock** 0: Disable 1: Enable

5	R/W	**BIST Test Enable** 0: Disable 1: Enable (Auto clear when finish)
4	R/W	**BIST Test Result** 0: Fail 1: Ok
3:0	R	**DV Total or Last Line Width[11:8] Before Sync in Frame Sync Mode**

Address: 45 **LAST_LINE_L**

Bit	Mode	Function
7:0	R	**DV Total or Last Line Width[7:0] Before Sync in Frame Sync Mode**

Display Fine Tune

Address: 46 **DIS_TIMING (Display Clock Fine Tuning Register)** **Default: 00h**

Bit	Mode	Function
7	R/W	**Reserved to 0**
6:4	R/W	**Display Output Clock Fine Tuning Control:** 000: DCLK rising edge correspondents with output display data 001: 1ns delay 010: 2ns delay 011: 3ns delay 100: 4ns delay 101: 5ns delay 110: 6ns delay 111: 7ns delay
3:0	--	Reserved

Sync Processor

Address: 47 **SYNC_SELECT** **Default: 00h**

Bit	Mode	Function
7	R/W	**Sync Processor Power Down (Stop Crystal Clock In)** 0: Normal Run (Default) 1: Power Down
6	R/W	**De-composite type Selection** 0:SOY(Default) 1:CS/SOG
5	R/W	**De-composite circuit enable** 0: Disable (Default) 1: Enable
4	R/W	**Input HS selection** 0 : HS_RAW(SS/CS) (Default) 1: SOG/SOY
3	--	**Reserved to 0**
2	R/W	**ADC HS/VS Source** 0: HS/VS (Default) 1: Test Mode VS & HS input from PWM1 & PWM2
1	R/W	**Measured by Crystal clock (Result showed in CR59) (in Digital Mode)** 0: Input Active Region (Vertical IDEN start to IDEN stop) (measure at IDEN STOP) (Default) 1: Display Active Region(Vertical DEN start to DEN stop) (measure at DEN STOP) The function should work correctly when IVS or DVS occurs.
0	R/W	**HSYNC & VSYNC Measured Mode** 0: HS period counted by crystal clock & VS period counted by HS (Analog mode) (Default) 1: H resolution counted by input clock & V resolution counted by ENA (Digital mode) (Get the correct resolution which is triggered by enable signal, ENA)

Address: 48 **SYNC_INVERT** **Default: 00h**

Bit	Mode	Function
7	R/W	**COAST Signal Invert Enable:** 0: Not inverted (Default) 1: Inverted
6	R/W	**COAST Signal Output Enable:** 0: Disable (Default)

		1: Enable
5	R/W	**HS_OUT Signal Invert Enable:** 0: Not inverted (Default) 1: Inverted
4	R/W	**HS_OUT Signal Output Enable:** 0: Disable (Default) 1: Enable
3	R/W	**CS_RAW Inverted Enable** 0: Normal (Default) 1: Invert
2	R/W	**CLAMP Signal Output Enable** 0: Disable (Default) 1: Enable
1	R/W	**HS Recovery in Coast** 0: Disable (Default) (SS/SOY) 1: Enable (CS or SOG)
0	R/W	**HSYNC Synchronize source** 0: AHS (Default) 1: Feedback HS

Address: 49 **SYNC_CTRL (SYNC Control Register)** **Default: 00h**

Bit	Mode	Function
7	R/W	**CLK Inversion to latch Feedback HS for Coast Recovery** **(Coast Recovery means HS feedback to replace input HS)** 0: Non Inversion (Default) 1: Inversion
6	R/W	**Select HS_OUT Source Signal** 0: Bypass (SeHs)(Use in Separate Mode) 1: Select De-Composite HS out(DeHs) (In Composite mode)
5	R/W	**Select ADC_VS Source Signal** 0: VS_RAW 1: DeVS
4	R/W	**CLK Inversion to latch HS_OUT for Clamp** 0: Non Inversion (Default) 1: Inversion
3	R/W	**Inversion of HS to measure Vsync** 0: Non Inversion (Default)

		1: Inversion
2	R/W	**HSYNC Measure Source(ADC_HS)** 0: Select ADC_HS (Default) 1: Select SeHS or DeHS by CR49[6]
1:0	R/W	**Measure HSYNC/VSYNC Source Select:** 00: Reserved 01: Reserved 10: ADC_HS1/ADC_VS (Default) 11: Reserved

Y-Pb-Pr Control

Address: 4A **DETECT_HSYNC_PERIOD_MSB** **Default: 00h**

Bit	Mode	Function
7:0	R	**Detected_Hsync_Period[10:3] MSB** Hsync period counted by crystal-clock.

Address: 4B **DETECT_HSYNC_PERIOD_LSB**

Bit	Mode	Function
7	R	**Hysnc_Period_Detect_Reset_Status (Write Clear)**
6	R	**The toggling of polarity of YPbPr Field happens** 0: No toggle 1: Toggle
5:3	R	**The number of input HS between 2 input VSYNC**. LSB bit [2:0] for YPbPr
2:0	R	**Detected_Hsync_Period[2:0] LSB** Hsync period counted by crystal-clock.

Address: 4C **VSYNC_COUNTER_LEVEL_MSB** **Default: 03h**

Bit	Mode	Function
7:6	--	**Reserved**
5	R/W	**ADC/Video switch** 0: ADC (Default) 1: Video8 (Should power on ADC Band-Gap CRE8[3])
4	R/W	**SOY De-Composite** 0: Auto period de-composite (Default) 1: Force period de-composite
3	R/W	**Pop up Detected_Hsync_Period** 0: no pop up

		1: pop up result (CR4A[7:0], CR4B[2:0])
2:0	R/W	**Vsync counter level count [10:8] MSB** Vsync detection counter start value.

Address: 4D **VSYNC_COUNTER_LEVEL_LSB** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Vsync counter level count [7:0] LSB**

Address: 4E **SYNC_POLARITY_PERIOD_COUNT** **Default: 50h**

Bit	Mode	Function
7:0	R/W	**Sync polarity period count number [8:1]**

Address: 4F **STABLE COUNT** **Default: 00h**

Bit	Mode	Function
7	---	**Reserved to 0**
6	R	**HSYNC Polarity Change (write clear)** flag will be cleared when this byte being accessed
5	R/W	**Vsync measure invert Enable** 0: Disable (Default) 1: Enable
4	R/W	**Pop Up Stable Period and Polarity Value** 0: No Pop Up (Default) 1: Pop Up Result, (CR50[3:0],CR51)
3	R/W	**Stable Period Tolerance** 0: ±2 crystal clks (Default) 1: ±4 crystal clks
2	R/W	**Stable Count** 0 : 32 lines (Default) 1 : 64 lines
1	R/W	**Polarity measure method** 0 : High / Low compare (Default) 1 : Fix-Length (The length is decided by CR4E].)
0	R/W	**Stable Measure Start** 0 : Stop (Default) 1 : Start (Clear CR4F[6], CR50 and CR51)

Address: 50 **STABLE_PERIOD_H**

Bit	Mode	Function
7	R	**HS Overflow(16-bits)**Only by cleared when set CR4F[0]=1
6	R	**Stable Period Change** Flag will be cleared when this byte being accessed or clear when CR4F[0]=1

5	R	**Stable Polarity Change** Flag will be cleared when this byte being accessed or clear when CR4F[0]=1
4	R	**Stable Flag** 0: Period or polarity can't get continuous stable status. 1: Both polarity and period are stable.
3	R	**Stable Polarity (on line monitor)** 0: Negative 1: Positive Compare each line's polarity; if we get continuous N lines with the same one, the polarity is updated as the stable polarity. N is determined by CR4F [2]. Detect method is determined by CR4F [1].
2:0	R	**Stable Period[10:8]** Compare each line's period, if we get continuous N lines with the same one, the period is updated as the stable period. N is determined by CR4F [2].

Address: 51 **STABLE_PERIOD_L**

Bit	Mode	Function
7:0	R	**Stable Period[7:0]** Compare each line's period, if we get continuous N lines with the same one, the period is **updated** as the stable period. N is determined by CR4E[2]

Address: 52 **MEAS_HS_PER_H (HSYNC Period Measured Result)** **Default: 8'b000xxxxx**

Bit	Mode	Function
7	R/W	**On Line Auto Measure Enable** 0: Disable (Default) 1: Enable
6	R/W	**Pop Up Period Measurement Result** 0: No Pop Up (Default) 1: Pop Up Result
5	R/W	**Start a HS & VS period / H & V resolution & polarity measurement (on line monitor)** 0: Finished/Disable (Default) 1: Enable to start a measurement, auto cleared after finished
4	R	**Over-flow bit of Input HSYNC Period Measurement** 0: No Over-flow occurred 1: Over-flow occurred
3:0	R	**Input HSYNC Period Measurement Result:** High Byte[11:8]

Address: 53 **MEAS_HS_PERIOD_L (HSYNC Period Measured Result)**

Bit	Mode	Function

7:0	R	**Input HSYNC Period Measurement Result:** Low Byte[7:0]

- This result is expressed in terms of crystal clocks.
- When measured digitally, the result is expressed as the number of input clocks between 2 input HS signals

Address: 54 **MEAS_VS_PERIOD_H (VSYNC Period Measured Result)**

Bit	Mode	Function
7	R	**Input VSYNC Polarity Indicator** 0: negative polarity (high period is longer than low one) 1: positive polarity (low period is longer than high one)
6	R	**Input HSYNC Polarity Indicator** 0: negative polarity (high period is longer than low one) 1: positive polarity (low period is longer than high one)
5	R	**Time-Out bit of Input VSYNC Period Measurement (No VSYNC occurred)** 0: No Time Out 1: Time Out occurred
4	R	**Over-flow bit of Input VSYNC Period Measurement** 0: No Over-flow occurred 1: Over-flow occurred
3:0	R	**Input VSYNC Period Measurement Result:** High Byte[11:8]

Address: 55 **MEAS_VS_PERIOD_L (VSYNC Period Measured Result)**

Bit	Mode	Function
7:0	R	**Input VSYNC Period Measurement Result:** Low Byte[7:0]

- This result is expressed in terms of input HS pulses.
- When measured digitally, the result is expressed as the number of input ENA signal within a frame.

Address: 56 **MEAS_HS_VS_HIGH_PERIOD_H (HSYNC&VSYNC High Period Measured Result)**

Bit	Mode	Function
7:4	R	**Input VSYNC High Period Measurement Result: High Byte[11:8]**
3:0	R	**Input HSYNC High Period Measurement Result: High Byte[11:8]**

Address: 57 **MEAS_HS_HIGH_PERIOD_L (HSYNC High Period Measured Result)**

Bit	Mode	Function
7:0	R	**Input HSYNC High Period Measurement Result: Low Byte[7:0]**

This result is expressed in terms of crystal clocks. When measured digitally, the result is expressed as the number of input clocks inside the input enable signal

Address: 58 **MEAS_VS_HIGH_PERIOD_L (VSYNC High Period Measured Result)**

Bit	Mode	Function
7:0	R	**Input VSYNC High Period Measurement Result:** Low Byte[7:0]

This result is expressed in terms of input HS pulses

Address: 59 **MEAS_ACTIVE_REGION_H (Active Region Measured by CRSTL_CLK Result)**

Bit	Mode	Function
7:0	R/W	**Active Region Measured By Crystal Clock** **1st read: Measurement Result:** High Byte[23:16] **2nd read: Measurement Result:** High Byte[15:8] **3rd read: Measurement Result:** High Byte[8:0] Read pointer is auto increase, if write, the pointer is also reset to 1st result.

Address: 5A **CLAMP_START (Clamp Signal Output Start)** **Default: 10h**

Bit	Mode	Function
7:0	R/W	**Start of Output Clamp Signal Pulse[7:0]:** Determine the number of input double-pixel between the select edge (CR5C[6]) of input HSYNC and the start of the output CLAMP signal.

Address: 5B **CLAMP_END (Clamp Signal Output End)** **Default: 14h**

Bit	Mode	Function
7:0	R/W	**End of Output Clamp Signal Pulse[7:0]:** Determine the number of input double-pixel between the select edge (CR5C[6]) of input HSYNC and the end of the output CLAMP signal.

Address: 5C **Clamp_CTRL0** **Default:00h**

Bit	Mode	Function
7	R/W	**Clamp Mask Enable** 0: Disable (Disable) 1: Enable
6	R/W	**CLAMP_Trigger_Edge_Inverse** 0: Trailing edge (Disable) 1: Leading edge
5:0	R/W	**Mask Line Number before VS [5:0]**

Address: 5D **CLAMP_CTRL1** **Default: 00h**

Bit	Mode	Function
7	R/W	**Sync Processor Test Mode** 0: Normal (Default) 1: Enable Test Mode; (switch 70ns-ck to the time-out & polarity counters)
6	R/W	**Select Clamp Mask as De VS** 0: Disable 1: Enable
5:0	R/W	**Mask Line Number after VS [5:0]**

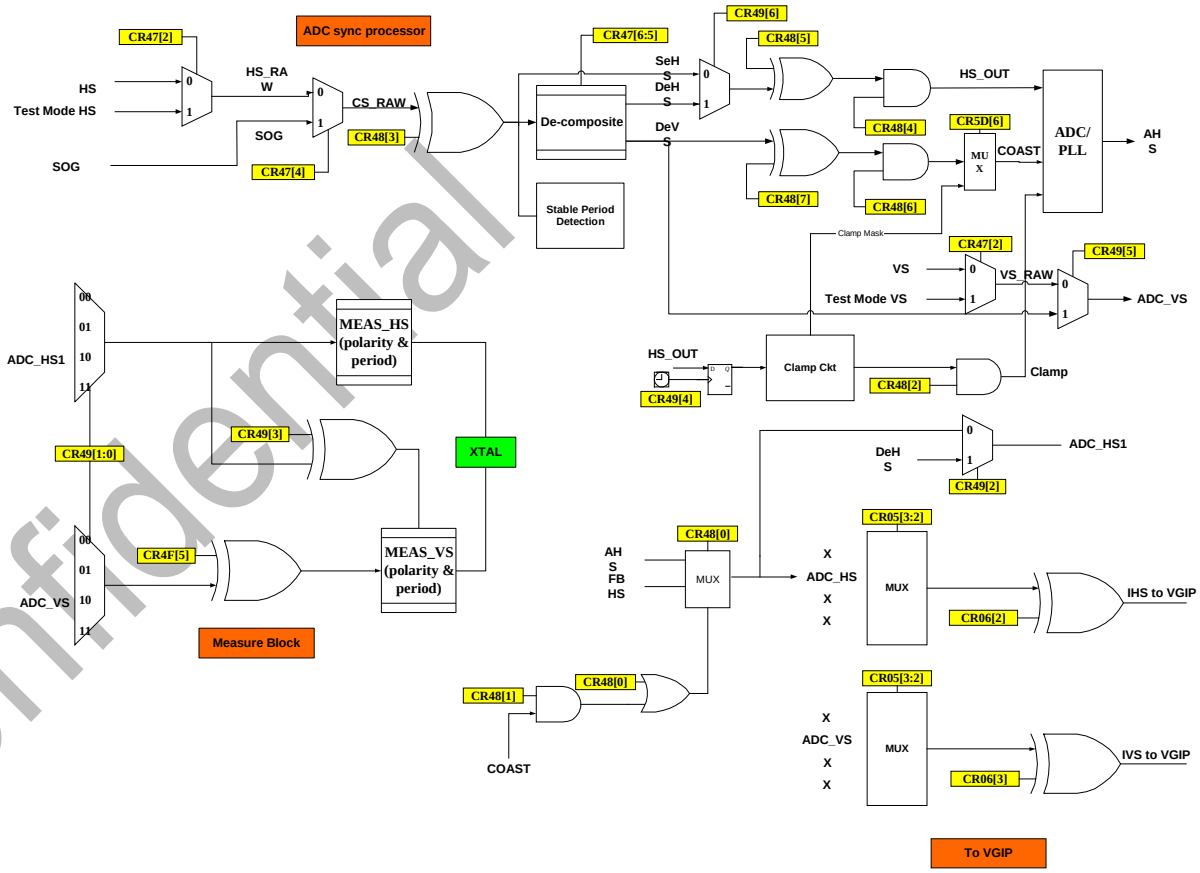


Figure 16 Sync processor

Color Processor Control

Address: 5E **COLOR_CTRL (Color Control Register)** **Default: 00h**

Bit	Mode	Function
7:2	--	**Reserved to 0**
1	R/W	**Enable Contrast Function:** 0: disable the coefficient (Default) 1: enable the coefficient
0	R/W	**Enable Brightness Function:** 0: disable the coefficient (Default) 1: enable the coefficient

Address: 5F **Reserved**

Bit	Mode	Function
7:0	--	**Reserved**

Brightness Coefficient:

Address: 60 **BRI_RED_COE (Brightness Red Coefficient)**

Bit	Mode	Function
7:0	R/W	**Brightness Red Coefficient:** Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 61 **BRI_GRN_COE (Brightness Green Coefficient)**

Bit	Mode	Function
7:0	R/W	**Brightness Green Coefficient: Valid range:** Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 62 **BRI_BLU_COE (Brightness Blue Coefficient)**

Bit	Mode	Function
7:0	R/W	**Brightness Blue Coefficient:** Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Contrast Coefficient:

Address: 63 **CTS_RED_COE (Contrast Red Coefficient)**

Bit	Mode	Function
7:0	R/W	**Contrast Red Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 64 **CTS_GRN_COE (Contrast Green Coefficient)**

Bit	Mode	Function
7:0	R/W	**Contrast Green Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65 **CTS_BLU_COE (Contrast Blue Coefficient)**

Bit	Mode	Function
7:0	R/W	**Contrast Blue Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Gamma Control

Address: 66 **GAMMA_PORT**

Bit	Mode	Function
7:0	W	**Access port for gamma correction table**

- The input data sequence is {g0[9:2]}, {g0[1:0], 1'b0, d0[4:0]}, {3'b0, d1[4:0]}; {g2[9:2]}, {g2[1:0], 1'b0, d2[4:0]}, {3'b0, d3[4:0]}; … ; {g254[9:2]}, {g254[1:0] , 1'b0, d254[4:0]}, {3'b0, d255[4:0]} for full gamma table.
- The input data sequence is {g0[9:2]}, {g0[1:0], 1'b0, d0[4:0]}, {g2[9:2]}, {g2[1:0] , 1'b0, d2[4:0]} … , {g254[9:2]}, {g254[1:0] ,1'b0, d254[4:0] } for compact gamma table.
- For compact gamma table, d1[4:0]=d0[4:0], d3[4:0]=d2[4:0], … , d(2n+1)[4:0]=d(2n)[4:0].
- g(n) is 10bit gamma coefficient, and d(n) is g(n+1) – g(n) with 5bit.
- If n is even, Gamma-port output is g(n) + d(n)*(2bit LSB brightness output)/4.
- If n is odd, Gamma-port output is g(n-1) + d(n-1) + d(n)*(2bit LSB brightness output)/4.
- Gamma can be only accessed when DCLK exists.
- The latest stage of d[n] can't let gamma curve exceed 255.

Address: 67 **GAMMA_CTRL** **Default: 00h**

Bit	Mode	Function
7	R/W	**Enable Access Channels for Gamma Correction Coefficient:** 0: disable these channels (Default) 1: enable these channels

6	R/W	**Gamma table enable** 00: by pass (Default) 01: enable
5:4	R/W	**Color Channel of Gamma Table** 00: Red Channel (Default) 01: Green Channel 10: Blue Channel 11: Red/Green/Blue Channel (R/G/B Gamma are the same)
3:1	--	**Reserved to 0**
0	R/W	**Gamma Access Type** 0: access compact gamma table (Default) 1: access full gamma table

- Access Gamma_Access register will reset GAMMA_PORT index.

Address: 68 **GAMMA_BIST (Color Control Register)** **Default: 00h**

Bit	Mode	Function

7	R/W	**Test_mode**
		0: Disable, dither_out = dither_result[9:2]; // truncate to integer number (Default)
		1: Enable, dither_out = dither_result[7:0]; // propagate decimal part for test

6:4	--	**Reserved to 0**
3:2	R/W	**Gamma BIST select** 00: BIST Disable (Default) 01: Red LUT 10: Green LUT 11: Blue LUT
1	R/W	**Gamma BIST_Progress** 0: BIST is done (Default) 1: BIST is running
0	R	**Gamma BIST Test Result** 0: SRAM Fail 1: SRAM OK

Dithering Control

Address: 69 **DITHERING_SEQUENCE_TABLE**

Bit	Mode	Function
7:6	W	Dithering Sequence Table (SR3)
5:4	W	Dithering Sequence Table (SR2)
3:2	W	Dithering Sequence Table (SR1)
1:0	W	Dithering Sequence Table (SR0)

- There are three set of dithering sequence table, each table contains 32 elements, s0, s1, … , s31.

Each element has 2 bit to index one of 4 dithering table.

- Input data sequence is {sr3,sr2,sr1,sr0}, {sr7,sr6,sr5,sr4}, … , {sr31,sr30,sr29,sr28}, {sg3,sg2,sg1,sg0}, … , {sg31,sg30,sg29,sg28}, {sb3,sb2,sb1,sb0}, … , {sb31,sb30,sb29,sb28} for red, green and blue channel.
- R + (2R+1) * C choose sequence element, where R is Row Number / 2, and C is Column Number / 2.

Address: 6A **DITHERING_TABLE_ACCESS (Dithering Table Access Port)**

Bit	Mode	Function
7:4	W	Access port for dithering table D00/D02/ D10/D12/D20/D22/D30/D32
3:0	W	Access port for dithering table D01/D03/ D11/D13/D21/D23/D31/D33

- Red, green, blue each channel has 4 dithering table, each table is 2x2 elements, and one element has 4 bit for 10B/8B, the elements should fill 0 to 3, for 10B/6B, the elements should fill 0 to 15.
- Input data sequence is [Dr00 Dr01],[Dr02,Dr03], … , [Dr30,Dr31],[Dr32,Dr33], [Dg00,Dg01],[Dg02,Dg03], … , [Dg30,Dg31],[Dg32,Dg33], [Db00,Db01],[Db02,Db03], … , [Db30,Db31],[Db32,Db33].

D00	D01	D10	D11	D20	D21	D30	D31
D02	D03	D12	D13	D22	D23	D32	D33

Address: 6B **DITHERING_CTRL** **Default: 00h**

Bit	Mode	Function
7	R/W	**Enable Access Dithering Sequence Table** 0: disable (Default) 1: enable
6	R/W	**Enable Access Dithering Table** 0: disable (Default) 1: enable
5	R/W	**Enable Dithering Function** 0: disable (Default) 1: enable
4	R/W	**Temporal Dithering** 0: Disable (Default) 1: Enable
3	R/W	**Dithering Table Value Sign** 0: unsigned 1: signed (2's complement)
2	R/W	**Dithering Mode** 0: New (Default) 1: Old
1	R/W	**Vertical Frame Modulation** 0: Disable (Default) 1: Enable
0	R/W	**Horizontal Frame Modulation**

		0: Disable (Default) 1: Enable

- {Dithering sequence + Frame Number (if temporal dithering)} mod 4 determine which dithering table to use

Overlay/Color Palette/Background Color Control

Address: 6C **OVERLAY_CTRL (Overlay Display Control Register)** **Default: 00h**

Bit	Mode	Function
7:6	--	**Reserved to 0**
5	R/W	**Background color access enable** 0: Disable(Reset CR6D Write Pointer to R) 1: Enable
4:2	R/W	**Alpha blending level (Also enable OSD frame control register 0x003 byte 1[3:2])** 000: Disable (Default) 001 ~111: 1/8~ 7/8
1	R/W	**Overlay Sampling Mode Select:** 0: single pixel per clock (Default) 1: dual pixels per clock (The OSD will be zoomed 2X in horizontal scan line)
0	R/W	**Overlay Port Enable:** 0: Disable (Default) 1: Enable **Turn off overlay enable and switch to background simultaneously when auto switch to background.**

Address: 6D **BGND_COLOR_CTRL (Background color control)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Background color RGB 8-bit value[7:0]**

- There are 3 bytes color select of background R, G, B, once we enable Background color access channel(CR6C[5] and the continuous writing sequence is R/G/B

Address: 6E **OVERLAY_LUT_ADDR (Overlay LUT Address)** **Default: 00h**

Bit	Mode	Function
7	--	**Reserved to 0**
6	R/W	**Enable Overlay Color Plate Access:** 0: Disable (Default) 1: Enable
5:0	R/W	**Overlay 16x24 Look-Up-Table Write Address [5:0]**

- Auto-increment while every accessing “Overlay LUT Access Port”.

Address: 6F **COLOR_LUT_PORT (LUT Access Port)**

Bit	Mode	Function
7:0	W	**Color Palette 16x24 Look-Up-Table access port [7:0]**

- Using this port to access overlay color plate which addressing by the above registers.

- The writing sequence into LUT is [R0, G0, B0, R1, G1, B1, … R15, G15, and B15] and the address counter will be automatic increment and circular from 0 to 47.

Image Auto Function

Address: 70 **H_BOUNDARY_H**

Bit	Mode	Function
7	--	**Reserved**
6:4	R/W	**Horizontal Boundary Start:** High Byte [10:8]
3:0	R/W	**Horizontal Boundary End:** High Byte [11:8]

Address: 71 **H_BOUNDARY_STA_L**

Bit	Mode	Function
7:0	R/W	**Horizontal Boundary Start:** Low Byte [7:0]

Address: 72 **H_BOUNDARY_END_L**

Bit	Mode	Function
7:0	R/W	**Horizontal Boundary End:** Low Byte [7:0]

Address: 73 **V_BOUNDARY_H**

Bit	Mode	Function
7	--	**Reserved**
6:4	R/W	**Vertical Boundary Start:** High Byte [10:8]
3:0	R/W	**Vertical Boundary End:** High Byte [11:8]

Vertical boundary search should be limited by Vertical boundary start.

Address: 74 **V_BOUNDARY_STA_L**

Bit	Mode	Function
7:0	R/W	**Vertical Boundary Start:** Low Byte [7:0]

Address: 75 **V_BOUNDARY_END_L**

Bit	Mode	Function
7:0	R/W	**Vertical Boundary End:** Low Byte [7:0]

Address: 76 **RED_NOISE_MARGIN (Red Noise Margin Register)**

Bit	Mode	Function
7:2	R/W	**Red pixel noise margin setting register**
1:0	--	**Reserved to 0**

Address: 77 **GRN_NOISE_MARGIN (Green Noise Margin Register)**

Bit	Mode	Function
7:2	R/W	**Green pixel noise margin setting register**

1:0	--	**Reserved to 0**

Address: 78 **BLU_NOISE_MARGIN (Blue Noise Margin Register)**

Bit	Mode	Function
7:2	R/W	**Blue pixel noise margin setting register**
1:0	--	**Reserved to 0**

Address: 79 **DIFF_THRESHOLD**

Bit	Mode	Function
7:0	R/W	**Difference Threshold**

Address: 7A **AUTO_ADJ_CTRL1** **Default: 00h**

Bit	Mode	Function
7	R/W	**Field_Select_Enable:** Auto-Function only active when Even or Odd field. 0: Disable (Default) 1: Enable
6	R/W	**Field_Select:** Select Even or Odd field. Active when **Field_Select_Enable(CR7A[7])**. 0: Active when ODD signal is "0" (Default) 1: Active when ODD signal is "1"
5	R/W	**Even or Odd pixel be measured** 0: Even 1: Odd
4	R/W	**Measure only Even or Odd pixel enable** 0: Disable (Default) 1: Enable
3:2	R/W	**Vertical boundary search:** 00: 1 pixel over threshold (Default) 01: 2 pixel over threshold 10: 4 pixel over threshold 11: 8 pixel over threshold
1:0	R/W	**Color Source Select for Detection:** 00: B color (Default) 01: G color 10: R color 11: ALL (when using "ALL" mode, the result SOD value will be right shift 1 bit) Measure ALL R/G/B can be done in three frames

Address: 7B **HW_AUTO_PHASE_CTRL0** **Default: 00h**

Bit	Mode	Function
7:3	**R/W**	**Number of Auto-Phase Step** (Valut+1)

		(How many times (steps reference CR7B[2:0]) jumps when using Hardware Auto)
2:0	**R/W**	**Hardware Auto Phase Step** 000: Step =1 (Default) 001 Step =2 010: Step =4 011: Step =8 1xx: Step =16

Address: 7C **HW_AUTO_PHASE_CTRL1** **Default: 00h**

Bit	Mode	Function
7	**R/W**	**Hardware Auto Phase Select Trigger** 0: IVS 1: Vertical Boundary End
6	**R/W**	**Low Pass Filter (121-LPF)** 0: Disable (Default) 1: Enable
5:0	**R/W**	**Initial phase of Auto-Phase** (0~63) For High Freq: the phase sequence is 0,1,2……..,63 (Default) For Low Freq: the phase sequence is 0,2,4,6,8……,126

Address: 7D **AUTO_ADJ_CTRL1** **Default: 00h**

Bit	Mode	Function
7	R/W	**Measure Digital Enable Info when boundary search active** 0: Normal Boundary Search (Default) 1: Digital Enable Info Boundary Search.(Digital mode)
6	R/W	**Hardware / Software Auto Phase Switch** 0: Software (Default) 1: Hardware
5	R/W	**Color Max or Min Measured Select:** 0: MIN color measured (Only when Balance-Mode, result must be complemented) (Default) 1: MAX color measured
4	R/W	**Accumulation or Compare Mode** 0: Compare Mode (Default) 1: Accumulation Mode
3	R/W	**Mode Selection For SOD** 0: SOD Edge Mode (Original TYPE II MODE I) (Default) 1: SOD Edge + Pulse Mode
2	--	**Reserved to 0**

1	R/W	**Function (Phase/Balance) Selection** 0: Auto-Balance (Default) 1: Auto-Phase
0	R/W	**Start Auto-Function Tracking Function:** 0: stop or finished (Default) 1: start

Control Table/ Function	Sub-Function	CR7D.6	CR7D.5	CR7D.4	CR7D.3	CR7D.1	CR7C
Auto-Balance	**Max pixel**	X	1	0	0	0	X
	Min pixel	X	0	0	0	0	X
Auto-Phase Type	**Mode1**	1	1	1	0	1	Th
	Mode2	1	1	1	1	1	Th
Accumulation	**All pixel**	1	1	1	0	0	0

Table 1 Auto-Tracking Control Table

Address: 7E **VER_START_END_H (Active region vertical start Register)**

Bit	Mode	Function
7:4	R	**Active region vertical START measurement result:** bit[11:8]
3:0	R	**Active region vertical END measurement result:** bit[11:8]

Address: 7F **VER_START_L (Active region vertical start Register)**

Bit	Mode	Function
7:0	R	**Active region vertical start measurement result:** bit[7:0]

Address: 80 **VER_END_L (Active region vertical end Register)**

Bit	Mode	Function
7:0	R	**Active region vertical end measurement result:** bit[7:0]

Address: 81 **HOR_START_END_H (Active region horizontal start Register)**

Bit	Mode	Function
7:4	**R**	**Active region horizontal START measurement result:** bit [11:8]
3:0	R	**Active region horizontal END measurement result:** bit[11:8]

Address: 82 **HOR_START_L (Active region horizontal start Register)**

Bit	Mode	Function
7:0	R	**Active region horizontal start measurement result:** bit[7:0]

Address: 83 **HOR_END_L (Active region horizontal end Register)**

Bit	Mode	Function
7:0	R	**Active region horizontal end measurement result:** bit[7:0]

Address: 84 **AUTO_PHASE_3 (Auto phase result byte3 register)**

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[31:24]

Address: 85 **AUTO_PHASE_2 (Auto phase result byte2 register)**

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[23:16]

Address: 86 **AUTO_PHASE_1 (Auto phase result byte1 register)**

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[15:8]

Address: 87 **AUTO_PHASE_0 (Auto phase result byte0 register)**

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[7:0] The measured value of R or G or B color max or min. (Auto-Balance)

Address: 88 **Reserved to 0**

Address: 89 **Reserved**

Address: 8A **Reserved**

Embedded Timing Controller

Address: 8B **TCON_ADDR _PORT** **Default: 00h**

Bit	Mode	Function
7:0	**R/W**	**Address port for embedded TCON access**

Address: 8C **TCON_DATA _PORT** **Default: 00h**

Bit	Mode	Function
7:0	**R/W**	**Data port for embedded TCON access**

Address: 00 **TC_CTRL1 (Timing Controller control register1)** **Default: 01**

Bit	Mode	Function
7	R/W	**Enable Timing Controller Function (Global)** 0: Disable (Default) 1: Enable **Reset all TCON pins after Enable TCON function is set and ties low.**
6	R/W	**TCON [n] Toggle Function Reset** 0: Not reset (Default) 1: reset by DVS
5	R/W	Set to 0
4	--	**Reserved**
3:2	--	**Reserved**
1:0	R/W	**Display Port Configuration:** 00: Reserved 01: HZ (Default) 10: LVDS 11: Reserved

Address: 01 **LVDS Location Pin Driving Control** **Default: 04h**

Bit	Mode	Function
7:5	--	**Reserved to 0**
4	R/W	**Pin 15/16/17 or Pin 43/44/45 drive current setting** 0: 4mA 1: 6mA
3	R/W	**LVDS PLL Lock edge** 0: Positive (Default) 1: Negative

2:1	R/W	**Display Port Driving Current Control** ***LVDS : (Pin 21-40)*** 00: 2.5mA 01: 3mA 10: 3.5mA (Default) 11: 4mA
0	--	**Reserved to 0**

Address: 02~07 Reserved

TCON Horizontal/Vertical Timing Setting

Address: 08 TCON [0]_VS_LSB (TCON [0] Vertical Start LSB Register)

Bit	Mode	Function
7:0	W	**Line number [7:0] at which TCON control generation begins**

Address: 09 TCON [0]_VS_MSB (TCON [0] Vertical Start/End MSB Register)

Bit	Mode	Function
7	--	**Reserved**
6:4	W	**Line number [10:8] at which TCON control generation ends**
3	--	**Reserved**
2:0	W	**Line number [10:8] at which TCON control generation begins**

Address: 0A TCON [0]_VE_LSB (TCON [0] Vertical End LSB Register)

Bit	Mode	Function
7:0	W	**Line number [7:0] at which TCON control generation ends**

Address: 0B TCON [0]_HS_LSB (TCON [0] Horizontal Start LSB Register)

Bit	Mode	Function
7:0	W	**Pixel count [7:0] at which TCON goes active**

Address: 0C TCON [0]_HS_MSB (TCON [0] Horizontal Start/End MSB Register)

Bit	Mode	Function
7	--	**Reserved**
6:4	W	**Pixel count [10:8] at which TCON goes inactive**
3	--	**Reserved**
2:0	W	**Pixel count [10:8] at which TCON goes active**

To be triggered on rising edge of the DCLK

Address: 0D TCON [0]_HE_LSB (TCON [0] Horizontal End LSB Register)

Bit	Mode	Function
7:0	W	**Pixel count [7:0] at which TCON goes inactive**

If the register number is large than display format, the horizontal component is always on.

Real TCON_HS = TCON_HS-4, Real TCON_HS = TCON_HS-4

Address: 0E TCON [0]_CTRL (TCON [0] Control Register) Default: 00h

Bit	Mode	Function
7	R/W	**TCON [n] Enable** (Local) 0: Disable (TCON [n] output clamp to '0') (Default) 1: Enable
6	R/W	**Polarity Control** 0: Normal output (Default) 1: Inverted output
5:4	--	**Reserved to 0**
3	R/W	**Toggle Circuit Enable/Disable** 0: Normal TCON output (Default) 1: Toggle Circuit enable When using toggle circuit enable mode, the TCON[n] will be 1 clock earlier than TCON[n-1] and then toggling together, finally output will be 1 clock delay comparing to toggling result.
2:0	R/W	**TCON [5] (TCON Combination Select)** 000: Normal TCON output (Default) 001~111: Reserved **TCON [6] & TCON [7] (TCON Combination Select)** 000: Normal TCON output (Default) 001: Select TCON [n] "AND" with TCON [n-1] 010: Select TCON [n] "OR" with TCON [n-1] 011: Select TCON [n] "XOR" with TCON [n-1] 100: Select TCON [n-1] rising edge as toggle trigger signal (when toggle enable) 101: Select TCON [n-1] rising edge as toggle trigger signal, then "AND" (when toggle enable) 110: Select TCON [n-1] rising edge as toggle trigger signal, then "OR" (when toggle enable) 111: Select TCON [n] and TCON [n-1] on alternating frames. **TCON [9] (TCON Combination Select)** 000: Normal TCON output (Default) 001: Select TCON [9] "AND" with TCON [7] 010: Select TCON [9] "OR" with TCON [7] 011: Select TCON [9] "XOR" with TCON [7] 100: Select TCON [7] rising edge as toggle trigger signal (when toggle enable) 101: Select TCON [7] rising edge as toggle trigger signal, then "AND" (when toggle enable) 110: Select TCON [7] rising edge as toggle trigger signal, then "OR" (when toggle enable) 111: Select TCON [9] and TCON [7] on alternating frames.

TCON [5] /TCON [6]/TCON[7]/TCON[9] Control Registers Address Map

Address	Data(# bits)	Default
32,31,30	TCON [5]_VS_REG (11)	
35,34,33	TCON [5]_HS_REG (11)	
36	TCON [5]_CTRL_REG	00
37	Reserved	
3A,39,38	TCON [6]_VS_REG (11)	
3D,3C,3B	TCON [6]_HS_REG (11)	
3E	TCON [6]_CTRL_REG	00
3F	Reserved	
42,41,40	TCON [7]_VS_REG (11)	
45,44,43	TCON [7]_HS_REG (11)	
46	TCON [7]_CTRL_REG	00
47	Reserved	
52,51,50	TCON [9]_VS_REG (11)	
55,54,53	TCON [9]_HS_REG (11)	
56	TCON [9]_CTRL_REG	00
57	Reserved	

Control For LVDS

Address: 78 LVDS_CTRL0 Default: 00h

Bit	Mode	Function
7	--	**Reserved to 0**
6	--	**Reserved to 0**
5	R/W	**Power up LVDS even-port** 0: Power down (Default) 1: Normal
4	R/W	**Power up LVDS odd-port** 0: Power down (Default) 1: Normal
3:2	R/W	**Watch Dog Model** 00: Enable Watch Dog(Default)

		01: Keep PLL VCO = 1V 1x: Disable Watch Dog
1	--	**Reserved to 0**
0	R	**Watch Dog Control Flag** (Write to clear) 0: Watch dog not active (Default) 1: Watch dog active, Reset PLL and set VCO = 1V

Address: 79 LVDS_CTRL1 Default: 14h

Bit	Mode	Function
7	--	**Reserved to 0**
6	--	**Reserved to 0**
5:3	R/W	**STSTL [2:0]: select test attribute** 000: WD 001: VCOM 010: IB40U (Default) 011: IBVOCM 100: PLLTST-fbak 101: PLLTST-fin 110: LVTST-CKDIN 111: LVTST-LVDSIN[6]
2:0	R/W	**RSDS / LVDS Output Common Mode** (Default: 100b)

Address: 7A LVDS_CTRL2 Default: 03h

Bit	Mode	Function
7:6	--	**Reserved to 0**
5:4	--	**Reserved**
3	--	**Reserved to 0**
2:0	R/W	**Bias Generator Adjust** (011)

Address: 7B LVDS_CTRL3 Default: 1Ch

Bit	Mode	Function
7:6	--	**Reserved to 0**
5:3	R/W	**SIL [2:0]**: PLL charge pump current (I=5uA+5uA*code) (Default: 011)
2:1	R/W	**SRL [1:0]**: PLL resistor (Default: 10)
0	R/W	**BMTS**: Bit-Mapping Table Select 0: Table 1 (Default) 1: Table 2

LVDS	Bit 1	Bit 0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 6	Bit 5
TXE0	ER1	ER0	EG0	ER5	ER4	ER3	ER2	ER1	ER0	EG0	ER5
TXE1	EG2	EG1	EB1	EB0	EG5	EG4	EG3	EG2	EG1	EB1	EB0
TXE2	EB3	EB2	DEN	VS	HS	EB5	EB4	EB3	EB2	DEN*6	VS*5
TXE3	ER7	ER6	RSV	EB7	EB6	EG7	EG6	ER7	ER6	RSV*7	EB7
TXO0	OR1	OR0	OG0	OR5	OR4	OR3	OR2	OR1	OR0	OG0	OR5
TXO1	OG2	OG1	OB1	OB0	OG5	OG4	OG3	OG2	OG1	OB1	OB0
TXO2	OB3	OB2	DEN	VS	HS	OB5	OB4	OB3	OB2	DEN*2	VS*1
TXO3	OR7	OR6	RSV	OB7	OB6	OG7	OG6	OR7	OR6	RSV*3	OB7

TABLE 1 Bit-Mapping 6bit(5~0)+2bit(7~6)

LVDS	Bit 1	Bit 0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 6	Bit 5
TXE0	ER3	ER2	EG2	ER7	ER6	ER5	ER4	ER3	ER2	EG2	ER7
TXE1	EG4	EG3	EB3	EB2	EG7	EG6	EG5	EG4	EG3	EB3	EB2
TXE2	EB5	EB4	DEN	VS	HS	EB7	EB6	EB5	EB4	DEN*6	VS*5
TXE3	ER1	ER0	RSV	EB1	EB0	EG1	EG0	ER1	ER0	RSV*7	EB1
TXO0	OR3	OR2	OG2	OR7	OR6	OR5	OR4	OR3	OR2	OG2	OR7
TXO1	OG4	OG3	OB3	OB2	OG7	OG6	OG5	OG4	OG3	OB3	OB2
TXO2	OB5	OB4	DEN	VS	HS	OB7	OB6	OB5	OB4	DEN*2	VS*1
TXO3	OR1	OR0	RSV	OB1	OB0	OG1	OG0	OR1	OR0	RSV*3	OB1

TABLE 2 Bit-Mapping 6bit(7~2)+2bit(1~0)

Address: 7C **LVDS_CTRL4** **Default: 80h**

Bit	Mode	Function
7:6	R/W	**E_RSV**: even port reserve signal select 11: Always '1' 10: Always '0' 01: Reserved 00: PWM_0
5:4	R/W	**E_DEN**: even port data enable signal select 11: Always '1' 10: Always '0' 01: TCON [9] 00: DENA
3:2	R/W	**E_VS**: even port VS signal select 11: Always '1' 10: Always '0' 01: TCON [7] 00: DVS
1:0	R/W	**E_HS**: even port HS signal select 11: Always '1'

		10: Always ‘0’ 01: TCON [5] 00: DHS

Address: 7D LVDS_CTRL5 Default: 80h

Bit	Mode	Function
7:6	R/W	**O_RSV**: odd port reserve signal select 11: Always ‘1’ 10: Always ‘0’ 01: Reserved 00: PWM_1
5:4	R/W	**O_DEN**: odd port data enable signal select 11: Always ‘1’ 10: Always ‘0’ 01: TCON [9] 00: DENA
3:2	R/W	**O_VS**: odd port VS signal select 11: Always ‘1’ 10: Always ‘0’ 01: TCON [7] 00: DVS
1:0	R/W	**O_HS**: odd port HS signal select 11: Always ‘1’ 10: Always ‘0’ 01: TCON [5] 00: DHS

Address: 7E Reserved

Pin Share

Address: 8D **PIN_SHARE_CTRL0** **Default: 00h**

Bit	Mode	Function
7	R/W	**Pin 21/22/23/24/25/26/27//28/29/30/31/32/33/34/35/36/37/38/39/40 (LVDS Mirror)** 0: TXE3+/TXE3-/ TXEC+/TXEC-/ TXE2+/TXE2-/ TXE1+/TXE1-/ TXE0+/TXE0-/ TXO3+/TXO3-/ TXOC+/TXOC-/ TXO2+/TXO2-/ TXO1+/TXO1-/ TXO0+/TXO0- (Default) 1: TXE0-/TXE0+/ TXE1-/TXE1+/ TXE2-/TXE2+/ TXEC-/TXEC+/ TXE3-/TXE3+/ TXO0-/TXO0+/ TXO1-/TXO1+/ TXO2-/TXO2+/ TXOC-/TXOC+/ TXO3-/TXO3+/
6	R/W	**Pin 16/17 or 44/43 (DDC or PWM selection)** 0: DDCSCL / DDCSDA (Default) 1: PWM1 / PWM2
5	R/W	**Test Mode Enable** 0: Disable (Default) 1: Enable
4	R/W	**Test Mode for DCLK Input** 0: Disable (Default) 1: Test Mode for DCLK input from PWM0 (Pin 15 or 45) VSYNC input from PWM1 (Pin 16 or 44) HSYNC input from PWM2 (Pin 17or 43)
3:2	R/W	**Test Mode LVDS_1 (Even Port) Control: (Pin 21-30)** 00: TTLO 01: TTLI 10: LVDS 11: DIFFTST
1:0	R/W	**Test Mode LVDS_2 (Odd Port) Control: (Pin 31-40)** 00: TTLO 01: TTLI 10: LVDS 11: DIFFTST

Address: 8E **PIN_SHARE_CTRL1** **Default: 00h**

Bit	Mode	Function
7	R/W	**Test Mode TLLO Output Port Select (Even Data or Odd Data Output)** 0: EVEN (default) 1: ODD
6:4	R/W	**CR8D[3:2] = 00 (TTL0) : (Pin21-30)** 000: ADC_CLK, RAW_VS, INPUT_RED[7:0]

		001: ADC_CLK, RAW_HS, INPUT_GREEN[7:0] 010: ADC_CLK, EN_FLAG, INPUT_BLUE[7:0] 011: ADC_CLK, SOG_IN, COAST, DECOMP_HS, CLAMP, COAST, HS_FB, AVIDEO_F, 2'b00 100: DCLK, DVS, DHS, DEN, ODDX, 1'b0, TCON[3:0] 101: DRED[7:0], DITHER_R[1:0] 110: DBLU[7:0], DITHER_B[1:0] 111: MCU_ADR_INC, MADR[7:0], 1'b0
3	R/W	**Reserved**
2:0	R/W	**CR8D[1:0] = 00 (TTLO) : (Pin31-40)** 000: VGIP_CLK, IVS_DLY, SD_RED[7:0] 001: SD_DEN, SD_ACT, SD_GREEN[7:0] 010: SD_DEN, SD_ACT, SD_BLUE[7:0] 011: VGIP_CLK, IVS_DLY, IHS_DLY, IFD_ODD, IENA, AUTO_HS, AUTO_VS AUTO_FIELD, 2'b00 100: ADC_CLK, SOG_IN, COAST, DECMP_HS, CLAMP, COAST, HS_FB, PHASE_ERROR, FAV4, MSB_2 101: DCLK, DVS, DHS, DEN, ODDX, DCLK_16, SDMOUT_TST[3:0] 110: DGRN[7:0],DITHER_G[1:0] 111: MCUWR, MCURD, MIN[7:0] **CR8D[1:0] = 01 (TTLI): (Pin31-40)** 000: Pin40 (TEST_CLK for ADC) 001~111: Reserved

Address: 8F **PIN_SHARE_CTRL2**

(PLL_TEST Output Signal Select, CR8D [3:2]=2'b11 or CR8D [1:0]= 2'b11) **Default: 00h**

Bit	Mode	Function
7	R/W	**Pin21 & Pin22 (ADC clock from PPL2)** 0:Disable (Default) 1:Enable
6	R/W	**Pin23 & Pin24 (PLL1 Clock)** 0:Disable (Default) 1:Enable
5	R/W	**Pin25 & Pin26 (DPLL Status)** 0:Disable (Default) 1: Enable
4	R/W	**Pin27 & Pin28 (PLL2 Phase0 Clock)**

		0:Disable (Default) 1: Enable
3	R/W	**Pin31 & Pin32 (DPLL clock)** 0:Disable (Default) 1: Enable
2	R/W	**Pin33 & Pin34 (PLL1 Status)** 0:Disable (Default) 1: Enable
1	R/W	**Pin35 & Pin36 (FAV clock from PLL1)** 0:Disable (Default) 1: Enable
0	R/W	**Pin37 & Pin38 (PLL2 Status)** 0:Disable (Default) 1: Enable

Embedded OSD

Address: 90 **OSD_ADDR_MSB (OSD Address MSB 8-bit)**

Bit	Mode	Function
7:0	R/W	**OSD MSB 8-bit address**

Address: 91 **OSD _ADDR_LSB (OSD Address LSB 8-bit)**

Bit	Mode	Function
7:0	R/W	**OSD LSB 8-bit address**

Address: 92 **OSD_DATA_PORT (OSD Data Port)**

Bit	Mode	Function
7:0	W	**Data port for embedded OSD access**

Refer to the embedded OSD application note for the detailed.

Address: 93 **OSD_SCRAMBLE** **Default: 05**

Bit	Mode	Function
7	R/W	**BIST Start** 0: stop (Default) 1: start (auto clear)
6	R	**BIST Result** 0: fail (Default) 1: success
5	R	**MCU writes data when OSD ON status (Queue 1 byte data)** 0: MCU writes data to OSD but not to real position (There is one level buffer here) 1: MCU doesn't write data, or data has been written to real position
4	R	**Double_Buffer_Write_Status** 0: double buffer write out is finish, or data write to double buffer is not ready, or no double buffer function. 1: after data write to dbuf and before dbuf write out, such that double buffer is busy.
3	--	**Reserved to 0**
2:0	R/W	**Double buffer depth (Default=6)** **000~101=>1~6**

Address: 94 **OSD_TEST**

Bit	Mode	Function
7:0	R/W	**Testing Pattern**

Reset Out

Address: 95 **POWER_ON_RESET_REGULATOR** **Default: 14**

Bit	Mode	Function
7:6	R/W	**Negative Threshold Value For Power on Reset** 00:1.8V(Default) 01:2.0V 10:2.2V 11:2.4V
5:4	R/W	**Negative Threshold Value For MCU Power Detecting** 00: 1.2V 01: 1.3333V (Default) 10: 1.4666V 11: 1.6V
3	--	Reserved
2:0	--	Reserved

Address: 96 **EBD_REGLATOR_VOL** **Default: 88**

Bit	Mode	Function
7:5	R/W	**Digital Core Regulator Voltage Value[2:0] (Supply current depends on PNP BJT)** 000 to 111 => 2.2V to 1.5V (Default 100=>1.8V)
4:3	R/W	**Band-gap Voltage Of Regulator Adjust** Default: 01
2	R/W	**Reserved to 0**
1	--	**Reserved**
0	--	**Reserved to 0**

Schmitt Trigger Control

Address: 97 **HS_SCHMITT_TRIGGE_CTRL** **Default: 41h**

Bit	Mode	Function
7	R/W	**HSYNC Schmitt Power Down (Only for Schmitt trigger new mode)** 0: Power down (Default) 1: Normal
6	R/W	**Threshold Select (For new mode only)** 0: Category 2 1: Category 1 (Default)
5	R/W	**Schmitt Trigger Mode**

		0: Old mode (Default) 1: New mode
4	R/W	**Threshold Voltage Fine Tune (only for Schmitt trigger new mode)** 0: 0V (Default) 1: -0.1V
3:2	R/W	**Positive Threshold Voltage**
1:0	R/W	**Negative Threshold Voltage**

- There are 3 mode of the HSYNC Schmitt trigger.
  1. Old mode 1: original HSYNC Schmitt trigger.
     bit[6:5]=00 **è** V_t^+ = 1.4V, V_t^- = 1.1V
  2. Old mode 2: The easy HSYNC Schmitt trigger.
     bit[6:5]=10 **è**

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Bit[1:0]	V_t^+	V_t^-
01	2.6V	1.8V
10	2.2	1.4V
11	1.8V	1.3V

  3. New mode: Fully programmable Schmitt trigger.
     The following table will determine the Schmitt Trigger positive and negative voltage:

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bit[6]=1 Category 1				bit[6] = 0 Category 2			
bit[3:2]	V_t^+	bit[1:0]	V_t^-	bit[3:2]	V_t^+	bit[1:0]	V_t^-
00	1.1V	00	0.2V	00	1.4V	00	0.5
01	1.2V	01	0.5V	01	1.5V	01	0.75
10	1.4V	10	0.75V	10	1.6V	10	1.1
11	1.5V	11	1.1V	11	1.8V	11	1.4

- After we get the threshold voltage by the table, we still can fine tune it:
  Final Positive Threshold Voltage = V_t^+ - 0.1* bit[4]
  Final Negative Threshold Voltage = V_t^- - 0.1* bit[4]

Phase-Lock-Loop (PLL)

DDS Setting for ADC

Address: 98 **PLL_DIV_CTRL** **Default: 04h**

Bit	Mode	Function
7	R/W	**PFD Selection** 0: New PFD fine (Default) 1: New PFD coarse (the resolution will be 1/2 of the PFD fine mode)
6	R/W	**DDS Tracking Edge** 0: HS positive edge (Default) 1: HS negative edge
5	R/W	**DDS Reset Enable** 0: Normal function (Default) 1: DDS circuit's reset will be asserted, for test only
4	R/W	**Test Mode**: (for production test) 0: Normal (Default) 1: Test Mode
3	R/W	**HS output synchronized by** 0: phase 32 (Default) 1: phase 0
2:1	R/W	**Delay Compensation Mode** 00: Mode 0 01: Mode 1 10: Mode 2 (Default) 11: Mode 3
0	R/W	**Clock select for DIV** 0: phase 0 (phase-0 of PLL2) (Default) 1: internal CLK (Fav)

Address: 99 **I_CODE_L** **Default: 47h**

Bit	Mode	Function
7:3	R/W	**Old/New mode:** I_Code [9:5] (Default: 01000)
2	R/W	**Old mode:** I_Code [4] (Default=1) **New mode:** I-code control mechanism 0: new linear mode, PE*(2+NEW_I[12])*2^(NEW_I+2) 1: old mode, P-code = P-code_2011 – 1 (Default)
1:0	R/W	**Old mode:** I_Code [3:2] (Default: 11) **New mode**: P-code protection mode 00 => No protection 01 => 1 bit protection

		10 => 2 bits protection 11 => 3 bits protection (Default)

Address: 9A **I_CODE_M** **Default: 00h**

Bit	Mode	Function
7:6	R/W	**Old mode :**I_Code [15:14] (Default: 00)
5	R/W	**Old mode :**I_code [13] (Default:0) **New mode :**I_code calibrated setting
4	R/W	**Old mode :**I_Code [12] (Default:0) **New mode :**P_code calibrated setting
3	R/W	**Old mode :**I_Code [11]
2	R/W	**I_Code [10] or PFD type selection** 0: Old PFD (Default) 1: New PFD
1	R/W	**Old mode :**I_Code [1] (Default: 0) **New mode :** P-code mapping curve 0: choose the new P-code mapping curve (PE*2+NEW_I[12])* 2^{NEW_P+2} 1: choose the old P-code mapping curve
0	R/W	**Old mode:** I_Code [0] (Default: 0) **New mode:** I-code multiplication factor 0: choose the new I-code multiplication factor = $2^{(NEW\_I[9:5]+2)}$ 1: choose the old I-code multiplication factor

I CONTROL =(I-CODE control mechanism)*(I-code multiplication factor)

Address: 9B **P_CODE** **Default: 18h**

Bit	Mode	Function
7	R/W	**Phase Swallow Down Enable** 0: Swallow Up (Default) 1: Swallow Down
6:5	R/W	**I_Code[17:16]** Default: 00b
4:0	R/W	**P_Code[4:0]** Default: 18h

Address: 9C **PFD_CALIBRATED_RESULTS** **Default: 8'b 00xxxxxx**

Bit	Mode	Function
7	--	**Reserved to 0**
6	R/W	**PFD Calibration Enable** Overwrite 0 to 1 return a new PFD calibrated value.
5:0	R	**PFD Calibrated Results[5:0]**

Address: 9D **PE_MEARSURE** **Default: 00h**

Bit	Mode	Function
7:6	--	**Reserved to 0**
5	R/W	**PE Measure Enable** 0: Disable (Default) 1: Start PE Measurement, clear after finish.
4:0	R	**PE Value Result [4:0]**

Address: 9E **PE_MAX_MEASURE** **Default: 00h**

Bit	Mode	Function
7	---	**Reserved to 0**
6	R/W	**PE Max. Measure Enable** 0: Disable (Default) 1: Start PE Max. Measurement
5	R/W	**PE Max. Measure Clear** 0: clear after finish (Default) 1: write '1' to clear PE Max. Value
4:0	R	**PE Max Value[4:0]**

Address: 9F **FAST_PLL_CTRL** **Default: 00h**

Bit	Mode	Function
7	--	**Reserved to 0**
6	R/W	**Enable APLL Setting** 0: Disable (Default) 1: Enable (Auto clear when finished) When CR9F[5] enabled, enable this bit will write PLL2M/N, PLLDIV and DDS SUM_I at the end of input vertical data enable
5	R/W	**Enable Fast PLL Mechanism** 0: Disable (Default) 1: Enable
4	--	**Reserved to 0**
3	R/W	**DDS I_SUM Setting Updated Enable** 0: Disable (Default) 1: Enable (Auto clear when finished)
2	R/W	**Measure I_SUM** 0: Disable 1: Enable (Auto clear after finish)
1	R/W	**Enable Port A0** 0: Disable Port A0 Access 1: Enable Port A0 Access

		When this bit is 0, port address will be reset to 00, and will auto increase when read or write
0	R/W	**Select I_SUM for Read** 0: Select SUM_I_PRE [31:0] for read 1: Select SUM_I_NOW [31:0] for read

Address: A0 **FAST_PLL_ISUM**

Bit	Mode	Function
7:0	R/W	**I_SUM (Auto Increase)** **1st I_SUM[31:24]** **2nd I_SUM[23:16]** **3rd I_SUM[15:8]** **4th I_SUM[7:0]**

ADC PLL1

Address: A1 **PLL1_M (M Parameter Register)** **Default: 0Fh**

Bit	Mode	Function
7:0	R/W	**PLL1M[7:0] (PLL1 DPM value – 2)**

Address: A2 **PLL1_N (N Parameter Register)** **Default: 80h**

Bit	Mode	Function
7	R/W	**PLL1PWDN (PLL1 Power Down)** 0: Normal Run 1: Power Down (Default)
6:4	---	**Reserved to 0**
3:0	R/W	**PLL1N[3:0] (PLL1 DPN value – 2)**

- PLL1_N modify to only 4-bit.
- Assume PLL1_M=0x0B, P1M=0x0B+2=13; PLL1_N=0x03, P1N=0x03+2=5; F_IN = 24.576MHz. F_PLL1 = F_IN x P1M / P1N = 24.576 x 13 / 5 = 63.8976MHz
- If the target frequency is F_ADC, the constraint of F_PLL1 is *(15/16)*F_ADC < F_PLL1 < F_ADC*

Address: A3 **PLL1_CRNT (PLL1 Current/Resistor Register)** **Default: 33h**

Bit	Mode	Function
7	R/W	**Reserved to 0**
6:4	R/W	**PLL1VR[2:0] (PLL1 Loop Filter Resister Control)** 000: 20K 001: 21K 010: 22K 011: 23K (Default) 100: 24K 101: 25K 110: 26K 111: 27K
3:0	R/W	**PLL1SI[3:0] (PLL1 Charger Pump Current IchDpll) (Default: 0011b)** Icp = 2.5uA+2.5uA*bit[0]+5uA*bit[1]+10uA*bit[2]+20uA*bit[3]

- **Keep Icp/PLL1 DPM constant**

Address: A4 **PLL1_WD (PLL1 Watch Dog Register)** **Default: 0Eh**

Bit	Mode	Function
7	R	**PLL1STATUS (PLL1 WD Status)** 0: Normal (Default) 1: Abnormal
6	R/W	**PLL1WDRST (PLL1 WD Reset)** 0: Normal (Default) 1: Reset

5	R/W	**PLL1WDSET (PLL1 WD Set)** 0: Normal (Default) 1: Set
4:3	R/W	**PLL1WDVSET[1:0] (PLL1 WD Voltage Set)** 00: 2.46V 01: 1.92V(Default) 10: 1.36V 11: 1.00V
2	R/W	**PLL1UPDN (PLL1 Frequency Tuning Up/Down)** 0: Freq Down 1: Freq Up (Default)
1	R/W	**PLL1MSBSTOP (PLL1 Frequency Tuning Enable)** 0: Disable 1: Enable (Default)
0	---	**Reserved to 0**

ADC PLL2

Address: A5 **PLL2_M (M Parameter Register)** **Default: 3Eh**

Bit	Mode	Function
7:0	R/W	**PLL2_M[7:0] (PLL2 DPM value – 2) (Default 3E)**

Address: A6 **PLL2_N (N Parameter Register)** **Default: 3Dh**

Bit	Mode	Function
7:0	R/W	**PLL2_N[7:0] (PLL2 DPN value – 2) (Default 3D)**

- Assume PLL2_M=0x0A, P2M=0x0A+2=12; PLL2_N=0x04, P2N=0x04+2=6; F_IN =65 MHz .
- F_PLL2 = F_IN x P2M x 2 / P2N /2 = 65 x 12 x 2 / 6 / 2 = 130 MHz
- the constraint of F_PLL2 is that *P2N =(int)(F_IN / 10)*

Address: A7 **PLL2_CRNT (PLL2 Current/Resistor Control)** **Default: 6Fh**

Bit	Mode	Function
7:5	**R/W**	**PLL2VR[2:0] (PLL2 Loop Filter Resister Control)** 000: 15K 001: 16K 010: 17K 011: 18K 100: 19K 101: 20K 110: 21K 111: 22K
4:0	**R/W**	**PLL2SI[4:0] (PLL2 Charger Pump Current Ich)** Icp = 2.5uA+2.5uA*bit[0]+5uA*bit[1]+10uA*bit[2]+20uA*bit[3]+30uA*bit[4]

l Keep Icp/DPM constant

Address: A8 **PLL2_WD (PLL2 Watch Dog Register)** **Default: 09h**

Bit	Mode	Function
7	R	**PLL2STATUS (PLL2 WD Status)** 0: Normal (Default) 1: Abnormal
6	R/W	**PLL2WDRST (PLL2 WD Reset)** 0: Normal (Default) 1: Reset
5	R/W	**PLL2WDSET (PLL2 WD Set)** 0: Normal (Default) 1: Set
4:3	R/W	**PLL2WDVSET[1:0] (PLL2 WD Voltage Set)** 00: 2.46V 01: 1.92V(Default) 10: 1.36V 11: 1.00V
2:1	R/W	**ADCKMODE[1:0] (ADC Input Clock Select Mode)** 00 : Single Clock Mode (Default) 01 : Single Inverse-Clock Mode 10 : External Clock Mode 11 : Dual Clock Mode (1x and 2x Clock)
0	R/W	**PLL2PWDN (PLL2 Power Down)** 0: Normal Run 1: Power Down (Default)

Address: A9 **PLLDIV_H** **Default: 05h**

Bit	Mode	Function
7	**---**	**Reserved to 0**
6	**R/W**	**Phase_Select_Method** 0: Manual (Default) 1: Look-Up-Table
5	**R/W**	**PLL2PH0PATH** 0: Short Path (Default) 1: Long Path (Compensate PLL_ADC path delay)
4	**R/W**	**PLL2D2** 0:ADC CLK=1/2 VCO CLK (Default) 1:ADC CLK=1/4 VCO CLK

3:0	**R/W**	**PLL Divider Ratio Control. High-Byte [11:8]. (Default: 5h)**

Address: AA **PLLDIV_L** **Default: 3Fh**

Bit	Mode	Function
7:0	R/W	**PLL Divider Ratio Control. Low-Byte [7:0].** PLLDIV should be double buffered when PLLDIV_LO changes and IDEN_STOP occurs.

- This register determines the horizontal total pixels. PLL derives the sampling clock and data output clock (DCLK) from input HSYNC. *The real operation Divider Ratio = PLLDIV+1*
- The default value of PLLDIV is 053Fh(=1343, VESA timing standard, 1024x768 60Hz, Horizontal time).
- CR A9 & AA will filled in when Control-Register AA is written.

Address: AB **PLLPHASE_CTRL0 (Select Phase to A/D)** **Default: 30h**

Bit	Mode	Function
7	R/W	**PLL2D2X control** (Default=0)
6	R/W	**PLL2D2Y control** (Default=0)
5	R/W	**PLL2X (PLL2 X Phase control)** (Default=1)
4	R/W	**PLL2Y (PLL2 X Phase control)** (Default=1)
3:0	R/W	**PLL2SCK[4:1] (PLL2 32 Phase Pre-Select Control)** (Default=0h)

Address: AC **PLLPHASE_CTRL1 (Select Phase to A/D)** **Default: 00h**

Bit	Mode	Function
7	R/W	**PLL2SCK[0] (PLL2 32 Phase Pre-Select Control)** (Default=0)
6	R/W	**MSB of 128 phase** (Only for ADC CLK=1/4 VCO CLK) (Default=0)
5:0	R/W	**Phase Select the index of Look-Up-Table[5:0]** (Default=0)

- **When Phase_Select_Method=1, Phase is selected by CR[AC]-Bit[6:0].**
- **When Phase_Select_Method=0, PLL2D2X, PLL2D2Y, PLL2X, PLL2Y, PLL2SCLK[4:0] Should be double buffered when PLL2SCK[0] is updated**

Address: AD **PLL2_PHASE_INTERPOLATION** **Default: 51h**

Bit	Mode	Function
7:6	R/W	**PLL2 Phase Interpolation Control Load (Default: 01)**
5:3	R/W	**PLL2 Phase Interpolation Control Source (Default: 010)**
2:1	R/W	**PLL2 Add Phase Delay** 00: Original phase selected by X,Y and 16-phase pre-select 01-11: Add 1-3 delay to Original phase selected by X,Y and 32-phase pre-select
0	R/W	**DPLL Clock to SSCG** 0: DPLLVCO/4 1: (DPLLVCO+Phase_Swallow)/4 (Defalult)

Phase	[XY^^^^^]	Phase	[XY ^^^^^]	Phase	[XY ^^^^^]	Phase	[XY ^^^^^]
0	[11 00000]	**16**	[01 10000]	**32**	[10 00000]	**48**	[00 10000]
1	[11 00001]	**17**	[01 10001]	**33**	[10 00001]	**49**	[00 10001]
2	[11 00010]	**18**	[01 10010]	**34**	[10 00010]	**50**	[00 10010]
3	[11 00011]	**19**	[01 10011]	**35**	[10 00011]	**51**	[00 10011]
4	[11 00100]	**20**	[01 10100]	**36**	[10 00100]	**52**	[00 10100]
5	[11 00101]	**21**	[00 10101]	**37**	[10 00101]	**53**	[00 10101]
6	[11 00110]	**22**	[00 10110]	**38**	[10 00110]	**54**	[00 10110]
7	[11 00111]	**23**	[01 10111]	**39**	[10 00111]	**55**	[00 10111]
8	[11 01000]	**24**	[01 11000]	**40**	[10 01000]	**56**	[00 11000]
9	[11 01001]	**25**	[01 11001]	**41**	[10 01001]	**57**	[00 11001]
10	[01 01010]	**26**	[10 11010]	**42**	[10 01010]	**58**	[11 11010]
11	[01 01011]	**27**	[10 11011]	**43**	[10 01011]	**59**	[11 11011]
12	[01 01100]	**28**	[10 11100]	**44**	[00 01100]	**60**	[11 11100]
13	[01 01101]	**29**	[10 11101]	**45**	[00 01101]	**61**	[11 11101]
14	[01 01110]	**30**	[10 11110]	**46**	[00 01110]	**62**	[11 11110]
15	[01 01111]	**31**	[10 11111]	**47**	[00 01111]	**63**	[11 11111]

DISPLAY PLL

Address: AE **DPLL_M (DPLL M Divider Register)** **Default: 2Ch**

Bit	Mode	Function
7:0	R/W	**DPLLM[7:0] (DPLL DPM value – 2)**

Address: AF **DPLL_N (DPLL N Divider Register)** **Default: 83h**

Bit	Mode	Function
7	R/W	**DPLLPWDN (DPLL Power Down)** 0: Normal Run 1: Power Down (Default)
6	R/W	**DPLLFREEZE (DPLL Output Freeze)** 0: Normal (Default) 1: Freeze
5:4	R/W	**DPLLO[1:0] (DPLL Output Divider)** 00: Div1 (Default) 01: Div2 10: Div4 11: Div8
3:0	R/W	**DPLLN[3:0] (DPLL DPN value – 2) (Default: 3h)**

- Assume DPLL_M=7Dh, DPM=7Dh+2=127; DPLL_N=0Ah, DPN=0Ah+2=12; Divider=1/4, F_IN = 24.576MHz.

F_DPLL = F_IN*DPM / (DPN *Divider) = 24.576*127 / (12*4) = 65.024MHz.

- If LPF_Mode = 1, suppose DPM=110, DPN = 12, Icp = [000100] = 6.25uA, DPLL=225MHz, then DPM / Icp =17.6. Please keep the ratio as constant.
- If LPF_Mode = 0, suppose DPM=46, DPN = 5, Icp = [101010] =27.5uA, DPLL=226MHz, then DPM / Icp = 1.67. Please keep the ratio as constant.

Address: B0 **DPLL_CRNT (DPLL Current/Resistor Register)** **Default: C8h**

Bit	Mode	Function
7:6	R/W	**DPLLVR[1:0] (DPLL Loop Filter Resister Control)** 00: 16K (LPF Mode = 0), 46K (LPF Mode = 1) 01: 18K (LPF Mode = 0), 53K (LPF Mode = 1) 10: 20K (LPF Mode = 0), 60K (LPF Mode = 1) 11: 22K (LPF Mode = 0), 67K (LPF Mode = 1) (Default)
5:4	--	**Reserved to 0**
3:0	R/W	**DPLLSI[3:0] (DPLL Charger Pump Current IchDpll) (Default: 1000b = 9uA)** Icp=(8uA*Bit[3] + 4uA*Bit[2] + 2uA*Bit[1] + 1uA*Bit[0] + 1uA)

- Keep Icp/DPM constant

Address: B1 **DPLL_WD (Watch Dog Register)** **Default: 16h**

Bit	Mode	Function
7	R	**DPLLSTATUS (DPLL WD Status)** 0: Normal 1: Abnormal
6	R/W	**DPLLWDRST (DPLL WD Reset)** 0: Normal (Default) 1: Reset
5	R/W	**DPLLWDSET (DPLL WD Set)** 0: Normal (Default) 1: Set
4:3	R/W	**DPLLWDVSET[1:0] (DPLL WD Voltage Set)** 00: 0.587V 01: 0.74V 10: 0.88V (Default) 11: 1.17V
2	R/W	**DPLLUPDN (DPLL Frequency Tuning Up/Down)** 0: Freq Up 1: Freq Down (Default)
1	R/W	**DPLLSTOP (DPLL Frequency Tuning Enable)** 0: Disable 1: Enable (Default) Turn on before CRBB[0].

0	R/W	**DPLLLPFMODE (DPLL LPF Mode)** 0: DPN<=5 è LPFMode=0 Ich=9.06A DPM=46 DPN=5 (Default) 1: DPN>=5 è LPFMode=1 Ich=3.1uA DPM=110 DPN=12

MULTIPLY PLL FOR INPUT CYRSTAL

Address: B2 **MULTI_PLL_CTRL0** **Default: 62h**

Bit	Mode	Function
7:4	R/W	**M2PLL M Code[3:0]-2 (DPM)** **Default=8 => 0110**
3	R/W	**M2PLL Power Down** 0: Normal Run (Default) 1: Power Down
2	R/W	**M2PLL Output Freeze** 0: Normal (Default) 1: Freeze i.e.: when output is frozen, the internal PLL is still operating
1	R/W	**M2PLL N Code** 0: N=1 1: N=2 (Default)
0	R	**M2PLL WD Status** 0: Normal 1: Abnormal

Address: B3 **MULTI_PLL_CTRL1** **Default: 94h**

Bit	Mode	Function
7:6	R/W	**M2PLL Loop Filter Resistor Control** 00: 15K 01: 18K 10: 21K(Default) 11: 24K
5:4	R/W	**M2PLL Loop Filter Charge Current Control(Default:01)** Icp=5uA+5uA*bit[4]+10uA*bit[5] i.e.: Keep Icp/DPM constant
3:2	R/W	**M2PLL WD Voltage** 00: 0.80V 01: 1.0V (Default) 10: 1.2V 11: 1.4V
1	R/W	**M2PLL_WDRST**

		0: Normal (Default) 1: Reset (M2PLL Function as a Normal PLL, regardless WD)
0	R/W	**M2PLL_WDSET** 0: Normal (Default) 1: Set (Free Run by WD asserts VCO Voltage)

Address: B4 **DPLL_OTHER** **Default: 04h**

Bit	Mode	Function
7:3	--	**Reserved**
2	R/W	**DPLL VCO RON (Increase VCO_OP Phase Margin)** 0: Disable 1: Enable (Default)
1	R/W	**DPLL VCO START (PLL_TestPin2 I/O Mode Select)** 0: Disable (Default) 1: Enable
0	R/W	**DPLL BPN (DPLL dividend enable)** 0: CRAE[3:0]DPLL_N dividend enable (Default) 1: N dividend disable

DCLK Spread Spectrum

Address: B5 **DCLK_FINE_TUNE_OFFSET_MSB** **Default: 00h**

Bit	Mode	Function
7	---	Reserved
6	R/W	**DPLL Reference Frequency Select** 0: Original Crystal Clock (Default) 1: Clock After M2PLL
5	R/W	**Only Even / Odd Field Mode Enable** 0: Disable (Default) 1: Enable
4	R/W	**Even / Odd Field Select** 0: Even (Default) 1: Odd
3:0	R/W	**DCLK Offset** [11:8] in Fixed Last Line DVTOTAL & DHTOTAL

Address: B6 **DCLK_FINE_TUNE_OFFSET_LSB** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**DCLK Offset** [7:0] in Fixed Last Line DVTOTAL & DHTOTAL

Address: B7 **SPREAD_SPECTRUM** **Default: 00h**

Bit	Mode	Function
7:4	R/W	**DCLK Spreading range** (0.0~7.5%) The bigger setting, the spreading range will bigger, but not uniform
3	R/W	**Spread Spectrum FMDIV** (SSP_FMDIV)//(0) 0: 33K 1: 66K
2	R/W	**Spread Spectrum Setting Ready for Writing** (Auto Clear) 0: Not ready 1: Ready to write
1:0	R/W	**Frequency Synthesis Select** (F & F-N*dF) 00~11: N=1~4

- The following control register will be written after CRB7[2] is applied, be ready the following bits before applying CRB7[2]
  1. DCLK spreading range (CRB7[7:4])
  2. Spread spectrum FMDIV (CRB7[3])
  3. DCLK offset setting (CRB5[3:0] & CRB6)
  4. Frequency synthesis select (CRB7[1:0])

Address: B8 **FIXED_LAST_LINE_MSB**

Bit	Mode	Function
6:4	R/W	**Fixed Last Line Length** [11:8]
3:0	R/W	**Fixed DVTOTAL** [11:8]

Address: B9 **FIXED_LAST_LINE_DVTOTAL_LSB**

Bit	Mode	Function
7:0	R/W	**Fixed DVTOTAL** [7:0]

Address: BA **FIXED_LAST_LINE_ LENGTH_LSB**

Bit	Mode	Function
7:0	R/W	**Fixed Last Line Length** [7:0]

- Fixed last line value can't be zero, and can't smaller than DH_Sync width.

Address: BB **FIXED_LAST_LINE_CTRL** **Default: 00h**

Bit	Mode	Function
7:4	--	**Reserved to 0**
3	R/W	**Enable New Design Function in Fixed Last Line Mode** 0: Disable (Default) 1: Enable

2	R/W	**DDS Spread Spectrum Test Enable** 0: Disable (Default) 1: Enable
1	R/W	**Enable the Fixed DVTOTAL & Last Line DHTOTAL Function** 0: Disable (Default) 1: Enable
0	R/W	**Enable DDS Spread Spectrum Output Function** 0: Disable (Default) 1: Enable

Procedure:

- First, we have set M/N code and then we need to tune DCLK OFFSET to achieve frame-sync, every step of offset frequency is DCLK/ 2^{15} .
- When we finished the frame-sync, we turn on CR BB[1] to let the system running in to free-run mode, at this time, the CRB8,CRB9,CRBA are the reference DV and DH total and Fixed last Line Length.
- But the free-run mode DVS' should be close to frame-sync mode DVS to achieve pseudo-frame-sync(actually, it is free run mode now)
- Then we use CRB7 [1:0] (F-N*dF) to keep DVS' and DVS very closely to achieve pseudo-frame-sync.

Notice:

- In RTD2523, when all the setting above is ready, then we open spread spectrum function, the DCLK OFFSET will shift, please keep the DCLK OFFSET keeps steady when we open spread spectrum function.
- In Real free-run mode, the DV_TOTAL refers to CR32/CR33, and in Fixed-Last-Line mode, the free-run timing DV_TOTAL refers to CRB8/CRB9, at this time CR35/36 serve for Vsync-timeout watch dog reference.

Address: BC~D9 **Reserved**

Watch Dog

Address: DA **WATCH_DOG_CTRL** **Default: 00h**

Bit	Mode	Function
7:6	--	**Reserved to 0**
5	R/W	**Auto switch when Display Vsync timeout** 0: Disable (Default) 1: Enable
4	R/W	**Auto switch when ADC-PLL non-lock** 0: Disable (Default) 1: Enable
3	R/W	**Auto switch when overflow or underflow** 0: Disable (Default) 1: Enable
2	R/W	**Auto switch event happen action (for timing)** 0: Disable (Default) 1: Free Run
1	R/W	**Auto switch event happen action (for data)** 0: Disable (Default) 1: Background **Turn off overlay enable and switch to background simultaneously.**
0	R	**Display Vsync timeout flag (status with CRDA [5])** 0: Vsync is present 1: Vsync Timeout The line number of Display HS is equal to Display Vertical Total; this bit is set to “1”. Write to clear status.

Address: DB **Reserved**

Embedded ADC

Address: DC **ADC_ RGB_CTRL** **Default: (56h)**

Bit	Mode	Function
7:6	R/W	**PGA (00: Ash=0.9 01: Ash=1.0 10: Ash=1.1 11: Ash=1.2) (Default: 01)**
5:4	R/W	**PGA (00: Aref=0.9 01: Aref=1.0 10: Aref=1.1 11: Aref=1.2)(Default: 01)**
3	R/W	**ADC source select (Need to select corresponding ADC_OUT_SOG 0 or 1)** 0 : Input0 (Default) 1 : Input1
2	R/W	**ADC input mode selection** 0 : Single Ended 1 : Differential (Default)
1:0	R/W	**Bandwidth Adjustment** 00 : 75M 01 : 150M 10 : 300M (Default) 11 : 500M

Address: DD **ADC_ RED_CTRL** **Default: (40h)**

Bit	Mode	Function
7	R/W	**RED channel clamp mode selection** 0: Low clamp (Default) 1: Middle clamp
6:4	R/W	**Red channel Clamp Voltage** 0~700mV, Step=100mV (Default: 100)
3	R/W	**RED channel Offset Depends on Gain** 0: RGB Dependent, YPbPr Independent (Default) 1: RGB Independent, YPbPr Independent
2:0	R/W	**Red Channel ADC Fine Tune Delay** (Step=90ps) (Default: 000)

Address: DE **ADC_GRN_CTRL** **Default: (40h)**

Bit	Mode	Function
7	R/W	**GREEN channel clamp mode selection** 0: Low clamp (Default) 1: Middle clamp
6:4	R/W	**GREEN channel Clamp Voltage** 0~700mV, Step=100mV(Default:100)
3	R/W	**GREEN channel Offset Depends on Gain** 0: RGB Dependent, YPbPr Independent(Default) 1: RGB Independent, YPbPr Independent
2:0	R/W	**Green Channel ADC Fine Tune Delay** (Step=90ps) (Default:000)

Address: DF **ADC_BLU_CTRL** **Default: (40h)**

Bit	Mode	Function
7	R/W	**BLUE channel clamp mode selection** 0: Low clamp(Default) 1: Middle clamp
6:4	R/W	**BLUE channel Clamp Voltage** 0~700mV, Step=100mV (Default:100)
3	R/W	**BLUE channel Offset Depends on Gain** 0: RGB Dependent, YPbPr Independent(Default) 1: RGB Independent, YPbPr Independent
2:0	R/W	**Blue Channel ADC Fine Tune Delay** (Step=90ps) (Default: 000)

Address: E0 **RED_GAIN** **Default: (80h)**

Bit	Mode	Function
7:0	R/W	**Red Channel Gain Adjust**

Address: E1 **GRN_GAIN** **Default: (80h)**

Bit	Mode	Function
7:0	R/W	**Green Channel Gain Adjust**

Address: E2 **BLU_GAIN** **Default: (80h)**

Bit	Mode	Function
7:0	R/W	**BLUE Channel Gain Adjust**

Address: E3 **RED_OFFSET** **Default: (80h)**

Bit	Mode	Function
7:0	R/W	**Red Channel Offset Adjust**

Address: E4 **GRN_OFFSET** **Default: (80h)**

Bit	Mode	Function
7:0	R/W	**Green Channel Offset Adjust**

Address: E5 **BLU_OFFSET** **Default: (80h)**

Bit	Mode	Function
7:0	R/W	**BLUE Channel Offset Adjust**

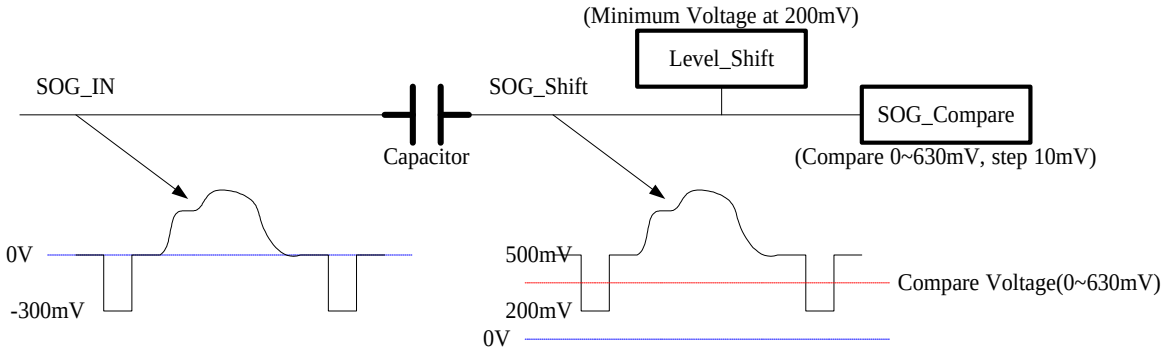
Address: E6 **SOG Control** **Default: (20h)**

Bit	Mode	Function
7:6	--	**Reserved to 0**
5:0	R/W	**SOG Reference Control** 0~630mV, Step=10mV (Default: 100000)

Address: E7 **Reserved** **Default: (20h)**

Bit	Mode	Function
7:0	--	**Reserved to 20h**

- The lowest voltage of SOG_IN is clamped to about 200mV.
- SOG reference control set the threshold voltage to extract the sync signal from G. The threshold voltage maps the value 0~63 to 0~630 mV.



Address: E8 **ADC_POWER_CTRL** **Default: (08h)**

Bit	Mode	Function
7:6	---	**Reserved to 0**
5	R/W	**SOG Power On** 0 : Power Down(Default) 1 : Power On
4	--	**Reserved to 0**
3	R/W	**Band-gap Power On** 0 : Power Down 1 : Power On (Default)

2	R/W	**Red Channel ADC Power On** 0 : Power Down (Default) 1 : Power On
1	R/W	**Green Channel ADC Power On** 0 : Power Down (Default) 1 : Power On
0	R/W	**Blue Channel ADC Power On** 0 : Power Down (Default) 1 : Power On

- Note that Band-gap power can only turn off just in the power down mode, or the chip may run abnormally.
- When in power saving mode, only R/G/B channel will be power down, it doesn't include the SOG & band-gap.

Address: E9 **ADC_CLOCK** **Default: (01h)**

Bit	Mode	Function
7	R/W	**Input Clock Polarity** 0: Negative (Default) 1: Positive
6	R/W	**Output Clock Polarity** 0: Normal (Default) 1: Inverted
5:4	R/W	**ADC_Out Pixel Extra Delay** 00: 1.05ns (Default) 01: 1.39ns 10: 1.69ns 11: 1.97ns
3	R/W	**1x or 2x from APLL (For better clock duty cycle)** 0: 1X (Default) 1: 2X
2	R/W	**Single Ended or Differential clock from APLL** 0: Differential (Default) 1: Single Ended
1:0	R/W	**Duty Stablizer** (Default: 01)

Address: EA **ADC_TEST** **Default: (04h)**

Bit	Mode	Function
7	R/W	**Clock Input** **0: from APLL/3.3V(Default)** **1: from TTL/1.8V**
6:4	R/W	**Test Output Selection(PAD : SOGIN)** 000:X/X(Hi-Z) Normal SOG Mode (Default) 001:GND/GND 010:VRBIR/VREFN 011:VCMI/VCMO 100:VRTIR/VREFP 101:VMID/GND 110:VOFFSET/GND 111:VDD/VDD
3:2	R/W	**SOG Resistor** 00: Poly R=100K, external C=47nF 01: Poly R=500K, external C=10nf (Default)

		10: MOS R=1M, external C=4.7nF 11: MOS R=5M, external C=1nF
1:0	R/W	**Clock Output Divider** 00 : 1/1 (Default) 01 : 1/2 10 : 1/3 11 : 1/4

Address: EB **ADC_IBIAS2** **Default: (53h)**

Bit	Mode	Function
7:6	R/W	**APLL_IB60U[1:0]** Bias Current of APLL_IB60U 00:48uA 01:60uA (Default) 10:72uA 11:84uA
5:4	R/W	**ADC_SF[1:0]** Bias Current of ADC_SF 00:15u 01:20u (Default) 10:25u 11:30u
3	R/W	**ADC_REF** Bias Current of ADC_REF 0:60u (Default) 1:80u
2:0	R/W	**ADC_OP[2:0]** Bias Current of ADC_OP 000:5u 001:10u 010:15u 011:20u (Default) 100:25u 101:30u 110:35u 111:40u

Address: EC **ADC_VBIAS0** **Default: (21h)**

Bit	Mode	Function
7	R/W	**Resistor Reference** (REFIO) 0:Ref. To Internal R (Default) 1:Ref. To External R=2K
6:4	R/W	**ADC_VBIAS0[6:4]** Band gap Voltage 000:0.890 001:0.841 010:0.792 (Default) 011:0.742 100:0.693 101:0.644 110:0.594 111:0.545
3:2	R	**Temperature sensor 0~120 (70+38*1.2)** 00: 30 degree 01: 30-60 degree 10: 60-90 degree 11: 120 degree

1:0	R/W	**ADC_VBIAS0[1:0]** Band gap Voltage 00:0.775 01:0.792 (Default) 10:0.810 11:0.829

Address: ED **ADC_VBIAS1** **Default: (0Dh)**

Bit	Mode	Function
7	---	**Reserved to 0**
6	R/W	**R Channel Clamp to -300mV** 0: 0mV (Default) 1: -300mV
5	R/W	**G Channel Clamp to -300mV** 0: 0mV (Default) 1: -300mV
4	R/W	**B Channel Clamp to -300mV** 0: 0mV (Default) 1: -300mV
3	R/W	**Vcmo with Lower VDD Ratio //(1)** 0:Lower,1.068 1:Normal, 1.122 (Default)
2	R/W	**Vcmo from VBG or from VDD //(1)** 0:from VBG (constant) 1:from VDD (Default)
1:0	R/W	**Vcmo Voltage[1:0] //(01)** 00:0.90 01:1.00 (Default) 11:1.05 11:1.10

Address: EE **PTNPOS_H** **Default: 00h**

Bit	Mode	Function
7	**R/W**	**Enable Test** 0: Finish (and result sequence is R-G-B) (Default) 1: Start
6:4	**R/W**	**Test Pattern V Position Register [10:8]** Assign the test pattern digitized position in line after V_Start.
3	--	**Reserved to 0**
2:0	**R/W**	**Test Pattern H Position Register [10:8]** Assign the test pattern digitized position in pixel after H_Start.

Address: EF **PTNPOS_V_L**

Bit	Mode	Function
7:0	R/W	**Test Pattern V Position Register [7:0]** Assign the test pattern digitized position in line after V_Start..

Address: F0 **PTNPOS_H_L**

Bit	Mode	Function
7:0	R/W	Test Pattern H Position Register [7:0] Assign the test pattern digitized position in line after H_Start..

Use PTNPOS to assign the pixel position after HSYNC leading edge that input signal digitized. Each time the

PTNPOS is written, the digitized results will be loaded into PTNRD, PTNGD and PTNBD. For test issue, make the input signal a fixed pattern before PTNPOS is written. Then the same digitized output will be got.

Address: F1 **PTNRD**

Bit	Mode	Function
7:0	R	**Test Pattern Digitized Result.**

- The test pattern digitized result after HSYNC leading edge about PTNPOS pixel.
- The 1st time read result is Red, the second read result is Green, and the third read result is Blue
- The read pointer should be reset when 1. PTNRD is written 2. Enable Test starts.
- The read back Test Pattern Digitized Result value address should be auto-increase, the sequence is shown above

Cyclic-Redundant-Check

Address: F2 **OP_CRC_CTRL (Output CRC Control Register)** **Default: 00h**

Bit	Mode	Function
7:1	--	**Reserved to 0**
0	R/W	**Output CRC Control:** 0: Stop or finish (Auto-stop after checked a completed display frame) (Default) 1: Start

CRC function = X^24 + X^7 + X^2 + X + 1.

Address: F3 **OP _CRC_BYTE (Output CRC Checksum)**

Bit	Mode	Function
7:0	R/W	1st read=> Output CRC-24 bit 23~16 2nd read=> Output CRC-24 bit 15~8 3rd read=> Out put CRC-24 bit 7~0

- The read pointer should be reset when 1. OP_CRC_BYTE is written 2. Output CRC Control starts.
- The read back CRC value address should be auto-increase, the sequence is shown above

DDC Special Function Access (DDC/CI)

Address: F4 **DDC_SET_SLAVE** **Default: 6E**

Bit	Mode	Function
7:1	R/W	**DDC Slave Address** to decode
0	--	**Reserved to 0**

Address: F5 **DDC_SUB_IN**

Bit	Mode	Function
7:0	R	**DDC Sub-Address Received**

Address: F6 **DDC_DATA_IN**

Bit	Mode	Function
7:0	R/W	**Read: DDC Data Received (16-bytes buffer)** **Write: DDC Data Received (16-bytes buffer)** Every Read/Write access, the buffer index is auto-decreased/increased.

Address: F7 **DDC_CTRL** **Default: 00h**

Bit	Mode	Function
7	--	**Reserved**
6	--	**Reserved**
5	--	**Reserved**
4	--	**Reserved**
3	R/W	**Auto reset DDC_DATA Buffer** 0: disable 1: enable In host (pc) write enable, when DDC write (No START after DDC_SUB), reset DDC_DATA buffer.
2	R/W	**Reset DDC_DATA buffer** 0: Finish 1: Reset
1	R/W	**DDC_DATA buffer write enable** 0: host (pc) write enable 1: slave (mcu) write enable Both PC and MCU can read DDC_DATA buffer, but only one can write DDC_DATA buffer.
0	--	**Reserved**

Address: F8 **DDC_STATUS**

Bit	Mode	Function

7	R	**DDC_DATA_BUFFER Full** If DDC_DATA buffer is full, this bit is set to "1". (On-line monitor) The DDC_DATA buffer Full status will be on-line-monitor the condition, once it becomes full, it kept high, if it is not-full, then it goes low.
6	R	**DDC_DATA_BUFFER Empty** If DDC_DATA buffer is empty, this bit is set to "1". (On-line monitor) The DDC_DATA buffer Empty status will be on-line-monitor the condition, once it becomes empty, it kept high, if it is not-empty, then it goes low.
5	--	**Reserved to 0**
4	R	If **DDC_STOP** signal occurs, this bit is set to "1" . Write clear
3	R	If **DDC_DATA_OUT** loaded to serial-out-byte, this bit is set to "1". Write clear
2	R	If **DDC_DATA_IN** latched, this bit is set to "1" . Write clear
1	R	If **DDC_SUB** latched, this bit is set to "1" Write clear
0	R	If **DDC_SLAVE** latched, this bit is set to "1" Write clear

Address: F9 **Reserved** **Default: 00h**

Address: FA **DDC_ENABLE (DDC Channel Enable Register)** **Default: 04h**

Bit	Mode	Function
7-5	--	**Reserved**
2	R/W	**DDC De-bounce Enable** 0: Disable 1: Enable (with crystal/4)
1:0	--	**Reserved**

Address: FB~FF **Reserved**

Embedded OSD

Addressing and Accessing Register

ADDRESS	BIT							
	7	6	5	4	3	2	1	0
High Byte	A15	A14	A13	A12	A11	A10	A9	A8
Low Byte	A7	A6	A5	A4	A3	A2	A1	A0

Figure 1. Addressing and Accessing Registers

Date	BIT							
Byte 0	D7	D6	D5	D4	D3	D2	D1	D0
Byte 1	D7	D6	D5	D4	D3	D2	D1	D0
Byte 2	D7	D6	D5	D4	D3	D2	D1	D0

Figure 2. Data Registers

All kind of registers can be controlled and accessed by these 2 bytes, and each address contains 3-byte data, details are described as follows:

Write mode: **[A15:A14] select which byte to write**

-00: Byte 0 -01:Byte 1 -10: Byte 2 –11: All

****All data are sorted by these three Bytes (Byte0~Byte2)***

[A13] Auto Load (Double Buffer)

[A12] Address indicator

-0: Window and frame control registers.

-1: Font Select and font map SRAM

[A11:A0] Address mapping

- Font Select and font map SRAM address: 000~EFF **3.75k*3byte**

-Frame control register address: 000~0xx **(Latch)**

-Window control register address: 100~1xx **(Latch)**

**** Selection of SRAM address or Latch address selection is determined by A12!***

Example:

Bit [15:14]=00

-All data followed are written to byte0 and address increases.

Byte0 à Byte0 à Byte0… (Address will auto increase)

Bit [15:14] =01

-All data followed are written to byte1 and address increases.

Byte1 à Byte1 à Byte1… (Address will auto increase)

Bit [15:14] =11

- Address will be increased after each 3-byte data written.

Byte0 à Byte1 à Byte2 à Byte0 à Byte1 à Byte2… (Address will auto increase)

Window control registers

- Windows all support shadow/border/3D button
- Window0, 5, 6, 7 support gradient functions.
- Window 4, 5, 6, 7 start/end resolution are 1line(pixel), Window 0, 1, 2, 3 start/end resolution are 4line(pixel),
- All window start and end position include the ***special effect (border/shadow/3D button)*** been assigned
- Font comes after windows by 10 pixels, so you should compensate 10 pixels on windows to meet font position

Window 0 Shadow/Border/Gradient

Address: 100h

Byte 0

Bit	Mode	Function
7:6	--	Reserved
5:3	W	Window 0 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 0 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 0 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color

3:0	W	Window 0 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 0 start position

Address: 101h

Byte 0

Bit	Mode	Function
7:2	W	Window 0 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 0 vertical start [2:0] line
4:0	W	Window 0 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 0 vertical start [10:3] line

Start position must be increments of four.

Window 0 end position

Address: 102h

Byte 0

Bit	Mode	Function
7:2	W	Window 0 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 0 vertical end [2:0] line
4:0	W	Window 0 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 0 vertical end [10:3] line

- End position must be increments of four.

Window 0 control

Address: 103h

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7	--	Reserved

6:4	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
3:0	W	Window 0 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7	W	Reserved
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 0 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 0 Enable 0: Disable 1: Enable

Window 1 Shadow/Border/Gradient

Address: 104h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 1 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 1 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 1 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 1 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 1 start position

Address: 105h

Byte 0

Bit	Mode	Function
7:2	W	Window 1 horizontal start [5:0]
3:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 1 vertical start [2:0] line
4:0	W	Window 1 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 1 vertical start [10:3] line

Start position must be increments of four.

Window 1 end position

Address: 106h

Byte 0

Bit	Mode	Function
7:2	W	Window 1 horizontal end [5:0]
2:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 1 vertical end [2:0] line
4:0	W	Window 1 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 1 vertical end [10:3] line

End position must be increments of four.

Window 1 control

Address: 107h

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7:4	--	Reserved
3:0	W	Window 1 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 1 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 1 Enable 0: Disable 1: Enable

Window 2 Shadow/Border/Gradient

Address: 108h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 2 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 2 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 2 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 2 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 2 start position

Address: 109h

Byte 0

Bit	Mode	Function
7:2	W	Window 2 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 2 vertical start [2:0] line
4:0	W	Window 2 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 2 vertical start [10:3] line

Start position must be increments of four.

Window 2 end position

Address: 10Ah

Byte 0

Bit	Mode	Function
7:2	W	Window 2 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 2 vertical end [2:0] line
4:0	W	Window 2 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function

7:0	W	Window 2 vertical end [10:3] line

End position must be increments of four.

Window 2 control

Address: 10Bh

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7:4	--	Reserved
3:0	W	Window 2 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 2 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 2 Enable 0: Disable 1: Enable

Window 3 Shadow/Border/Gradient

Address: 10Ch

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 3 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 3 shadow/border height in line unit

		000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 3 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 3 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 3 start position

Address: 10Dh

Byte 0

Bit	Mode	Function
7:2	W	Window 3 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 3 vertical start [2:0] line
4:0	W	Window 3 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 3 vertical start [10:3] line

Start position must be increments of four.

Window 3 end position

Address: 10Eh

Byte 0

Bit	Mode	Function
7:2	W	Window 3 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 3 vertical end [2:0] line
4:0	W	Window 3 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 3 vertical end [10:3] line

End position must be increments of four.

Window 3 control

Address: 10Fh

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7:4	--	Reserved
3:0	W	Window 3 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 3 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 3 Enable 0: Disable 1: Enable

Window 4 Shadow/Border/Gradient

Address: 110h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 4 shadow/border width or 3D button thickness in pixel unit

		000~111: 1 ~ 8 pixel
2:0	W	Window 4 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4 shadow color index in 16-color LUT For 3D window, it is the left-top/ bottom border color
3:0	W	Window 4 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4 start position

Address: 111h

Byte 0

Bit	Mode	Function
7:2	W	Window 4 horizontal start [5:0]
2:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 4 vertical start [2:0] line
4:0	W	Window 4 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 4 vertical start [10:3] line

Window 4 end position

Address: 112h

Byte 0

Bit	Mode	Function
7:2	W	Window 4 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 4 vertical end [2:0] line
4:0	W	Window 4 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 4 vertical end [10:3] line

Window 4 control

Address: 113h

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7:4	--	Reserved
3:0	W	Window 4 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4 Enable 0: Disable 1: Enable

Window 5 Shadow/Border/Gradient

Address: 114h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 5 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel

2:0	W	Window 5 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 5 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 5 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 5 start position

Address: 115h

Byte 0

Bit	Mode	Function
7:2	W	Window 5 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function

7:5	W	Window 5 vertical start [2:0] line
4:0	W	Window 5 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 5 vertical start [10:3] line

Window 5 end position

Address: 116h

Byte 0

Bit	Mode	Function
7:2	W	Window 5 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 5 vertical end [2:0] line
4:0	W	Window 5 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 5 vertical end [10:3] line

Window 5 control

Address: 117h

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7	--	Reserved
6:4	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
3:0	W	Window 5 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7	W	Reserved
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 5 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 5 Enable 0: Disable 1: Enable

Window 6 Shadow/Border/Gradient

Address: 118h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 6 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 6 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

PS: This is for non-rotary, rotate 270, rotate 90 and 180.

Byte 1

Bit	Mode	Function

7:4	W	Window 6 shadow color index in 16-color LUT For 3D window, it is the left-top/ bottom border color
3:0	W	Window 6 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 6 start position

Address: 119h

Byte 0

Bit	Mode	Function
7:2	W	Window 6 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 6 vertical start [2:0] line
4:0	W	Window 6 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 6 vertical start [10:3] line

Window 6 end position

Address: 11Ah

Byte 0

Bit	Mode	Function
7:2	W	Window 6 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 6 vertical end [2:0] line
4:0	W	Window 6 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 6 vertical end [10:3] line

Window 6 control

Address: 11Bh

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7	--	Reserved
6:4	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
3:0	W	Window 6 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7	W	Reserved
6	W	Gradient function 0: Disable 1: Enable

5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 6 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 6 Enable 0: Disable 1: Enable

Window 7 Shadow/Border/Gradient

Address: 11Ch

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 7 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 7 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

PS: This is for non-rotary, rotate 270, rotate 90 and 180.

Byte 1

Bit	Mode	Function
7:4	W	Window 7 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 7 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function

7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 7 start position

Address: 11Dh

Byte 0

Bit	Mode	Function
7:2	W	Window 7 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 7 vertical start [2:0] line
4:0	W	Window 7 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 7 vertical start [10:3] line

Window 7 end position

Address: 11Eh

Byte 0

Bit	Mode	Function
7:2	W	Window 7 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 7 vertical end [2:0] line
4:0	W	Window 7 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 7 vertical end [10:3] line

Window 7 control

Address: 11Fh

Byte 0

Bit	Mode	Function
7:0	--	Reserved

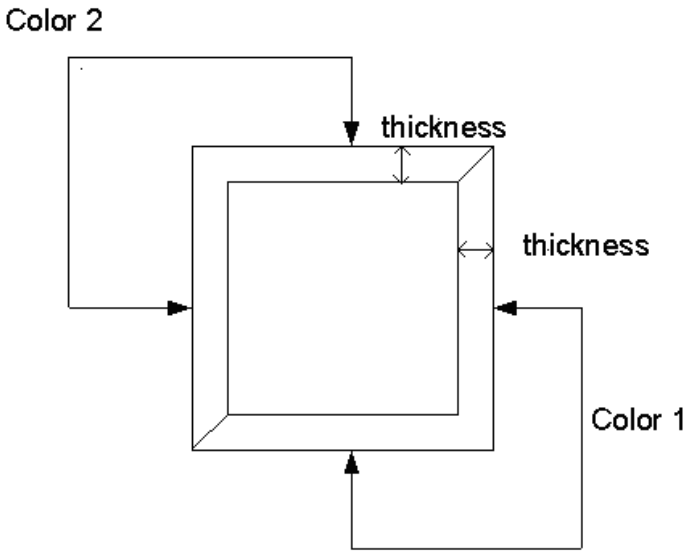
Byte 1

Bit	Mode	Function
7	--	Reserved
6:4	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
3:0	W	Window 7 color index in 16-color LUT

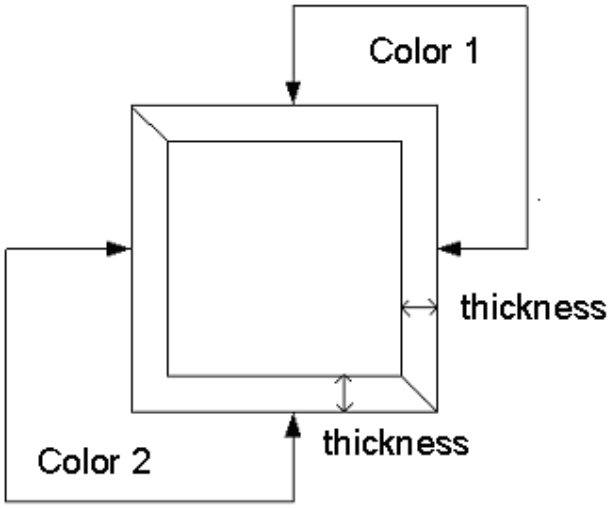
Byte 2 default: 00h

Bit	Mode	Function
7	W	Reserved
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 7 Type

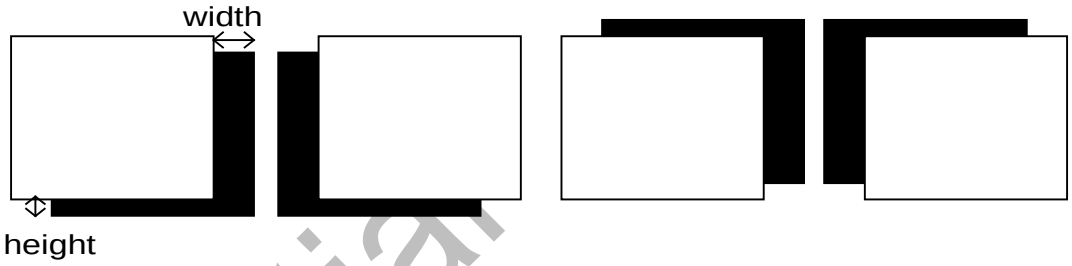
		000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 7 Enable 0: Disable 1: Enable



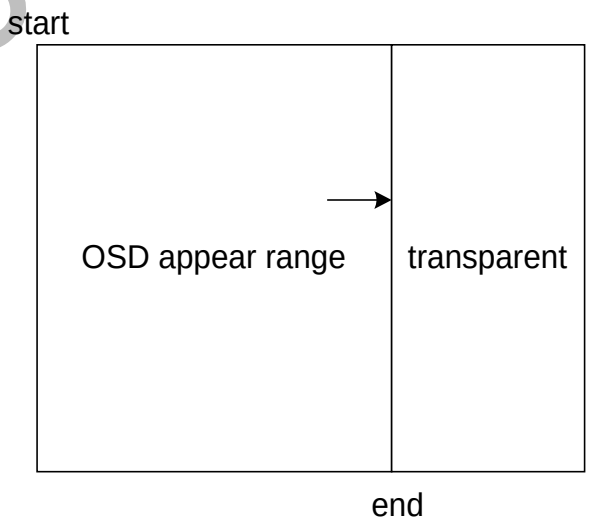
3D Button Type 1



3D Button Type 2



Shadow in all direction



Window mask fade/in out function

Frame control registers

Address: 000h

Byte 0

Bit	Mode	Function
7:0	W	Vertical Delay [10:3] The bits define the vertical starting address. Total 2048 step unit: 1 line

Vertical delay minimum should set 1

Byte 1

Bit	Mode	Function
7:0	W	Horizontal Delay [9:2] The bits define the horizontal starting address. Total 1024 step unit:4 pixels

Horizontal delay minimum should set 2

Byte 2

Bit	Mode	Function
7:6	W	Horizontal Delay bit [1:0]
5:3	W	Vertical Delay [2:0]
2:1	W	Display zone, for smaller character width 00: middle 01: left 10: right 11: reserved
0	W	OSD enable 0: OSD circuit is inactivated 1: OSD circuit is activated

When OSD is disabled, Double Width (address 0x002 Byte1[1]) must be disabled to save power.

PWM Duty Width

Address: 001h

Byte 0 Default: 00h

Bit	Mode	Function
7:0	W	PWM_0 8bits decides the output duty width and waveform of PWM at PWM channel

Byte 1 Default: 00h

Bit	Mode	Function
7:0	W	PWM_1 8bits decides the output duty width and waveform of PWM at PWM channel

Byte 2 Default: 00h

Bit	Mode	Function
7:0	W	PWM_2 8bits decides the output duty width and waveform of PWM at PWM channel

Address: 002h

Byte 0 Default: 00h

Bit	Mode	Function
7:0	W	First stage clock divider N[7:0] N=0-255, 1st F= F/2(N+1)

Byte 1 Default: 00h

Bit	Mode	Function
7	W	PWM0 First stage clock divider Enable 0: Disable 1: Enable
6	W	PWM1 First stage clock divider Enable 0: Disable 1: Enable
5	W	PWM2 First stage clock divider Enable 0: Disable 1: Enable
4	W	Enable PWM Output
3:2	W	Crystal Clock Divider 00: Crystal 01: Crystal/2

		10: Crystal/4 11: Crystal/8
1:0	--	Reserved

Byte 2 Default: 00h

Bit	Mode	Function
7:0	--	Reserved

Address: 003h

Byte 0 default: xxxx_xxx0b

Bit	Mode	Function
7	--	Reserved
6	W	Enable Window 7 Mask OSD-Appear-Range Control for Fade In/Out
5	W	Window 7 Mask 0: Mask area appears 1: Mask area transparent
4	W	OSD vertical start input signal source select 0: Select DVS as OSD VSYNC input 1: Select ENA as OSD VSYNC input
3:0	--	Reserved

Byte 1

Bit	Mode	Function
7:4	W	Char shadow/border color
3: 2	W	Alpha Blending Type 00: Disable alpha blending 01: Only window blending 10: All blending 11: Window and Character background blending
1	W	Double width enable (For all OSD including windows and characters) 0: Normal 1: Double
0	W	Double Height enable (For all OSD including windows and characters) 0: Normal 1: Double

Byte 2

Bit	Mode	Function
7:6	W	**Font downloaded swap control** 0x: No swap

		10: CCW 11: CW
5:2	--	Reserved
1	W	**Global Blinking Enable** 0: Disable 1: Enable
0	W	**Rotation** 0: Normal (data latch 24 bit per 24 bit) 1: Rotation (data latch 18 bit per 24 bit)

Bit	7	6	5	4	3	2	1	0
Firmware	A	B	C	D	E	F	G	H
CW	A	E	B	F	C	G	D	H
CCW	E	A	F	B	G	C	H	D

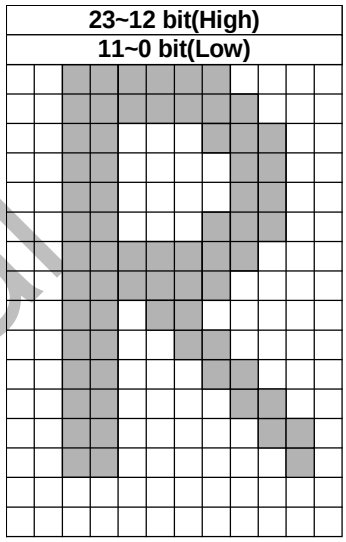


Figure 3 Non-rotated memory alignments

23 **6**

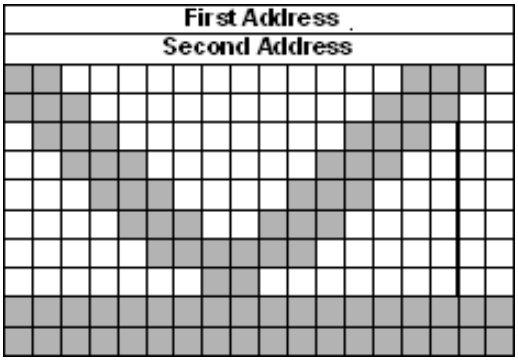


Figure 4 Rotated memory alignments

Base address offset

Address: 004h

Byte 0

Bit	Mode	Function
7:0	W	Font Select Base Address[7:0]

Byte 1

Bit	Mode	Function
7:4	W	Font Select Base Address[11:8]
3:0	W	Font Base Address[3:0]

Byte 2

Bit	Mode	Function
7:0	W	Font Base Address[11:4]

OSD SRAM (Map and font registers)

R0	R1	R2	….			Rn	End					
C01	C02	B03	C04	…		C11	C12	C13	…			
…												
…												
…			Cn1	Cn2	…		1-bit font start		…			
…												
…			2-bit font start			…						
…												
4-bit font start			…									
…												
…												

11.25k bytes SRAM

1. Row Command

R0	R1	R2	R3	R….	Rn	End

Row Command R0~Rn represent the start of new row. Each command contains 3 bytes data which define the length of a row and other attributes. OSD End Command represent the end of OSD. R0 is set in address 0 of SRAM.

2. Character/Blank Command (Font Select)

Character Command is used to select which character font is show. Each command contains three bytes which specify its attribute and 1,2 or 4bit per pixel. Blank Command represents blank pixel to separate the preceding character and following character. Use two or more Blank Command if the character distance exceeds 255 pixel.

The Font Select Base Address in Frame Control Register represents the address of the first character in Row 0, that is, C01 in the above figure. The following character/blank is write in the next address. C11 represents the first character in Row1, C12 represents the second character in Row1, and so on.

The address of the first character Cn1 in Row n = Font Select Base Address + Row 0 font base length + Row 1 font base length + …+Row n-1 font base length.

3. Font

User fonts are stored as bit map data. For normal font, one font has 12x18 pixel, and for rotation font, one has 18x12 pixel. One pixel use 1, 2 or 4 bits.

For 12x18 font,

One 1-bit font requires 9 * 24bit SRAM

One 2-bit font requires 18 * 24bit SRAM

One 4-bit font requires 36 * 24bit SRAM

For 18x12 font,

One 1-bit font requires 12 * 24bit SRAM

One 2-bit font requires 24 * 24bit SRAM

One 4-bit font requires 48 * 24bit SRAM

Font Base Address in Frame Control Register point to the start of 1-bit font.

For normal (12x18) font:

1-bit Font, if CS = 128, Real Address of Font = Font Base Address + 9 * 128

2-bit Font, if CS = 128, Real Address of Font = Font Base Address + 18 * 128

4-bit Font, if CS = 128, Real Address of Font = Font Base Address + 36 * 128

For rotational (18x12) font:

1-bit Font, if CS = 128, Real Address of Font = Font Base Address + 12 * 128

2-bit Font, if CS = 128, Real Address of Font = Font Base Address + 24 * 128

4-bit Font, if CS = 128, Real Address of Font = Font Base Address + 48 * 128

where CS is Character Selector in Character Command.

Note that Row Command, Font Select and Font share the same OSD SRAM.

When we download the font, we have to set the Frame control 002h byte1 [1:0] to set the method of hardware bit swap. If the OSD is Counter-Clock-Wise rotated, we have to set to 0x01 (the 8 bits of every byte of font SRAM downloaded by firmware will be in a sequence of "7 5 3 1 6 4 2 0" (from MSB to LSB) and should be rearranged to "7 6 5 4 3 2 1 0" by hardware). If it is Clock-Wise rotated, we have to set to 0x10 (the 8 bits of every byte of font SRAM downloaded by firmware will be in a sequence of "6 4 2 0 7 5 3 1" (from MSB to LSB) and should be rearranged to "7 6 5 4 3 2 1 0" by hardware). After we finish the downloading or if we don't have to rotate the OSD, we have to set it to 0x00.

Row Command

Byte 0

Bit	Mode	Function
7	W	1: Row Start Command 0: OSD End Command Each row must start with row-command, last word of OSD map must be end-command
6:5	W	Reserved
4:2	W	Character border/shadow 000: None 001: Border 100: Shadow (left-top) 101: Shadow (left-bottom) 110: Shadow (right-top) 111: Shadow (right-bottom)
1	W	Double character width 0: x1 1: x2
0	W	Double character height 0: x1 1: x2

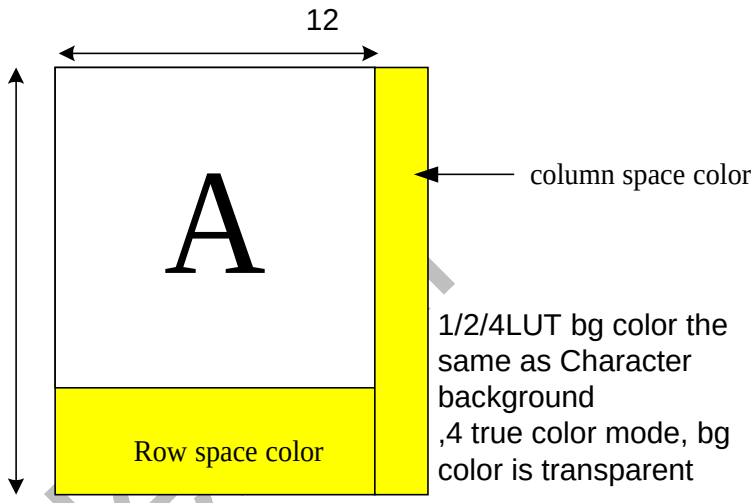
Byte 1

Bit	Mode	Function
7:3	W	Row height (1~32)
2:0	W	Column space 0~7 pixel column space When Char is doubled, so is column space.

Notice:

When character height/width is doubled, the row height/column space definition also twice. If the row height is larger than character height, the effect is just like space between rows. If it is smaller than character height, it will drop last several bottom line of character.

When using 1/2/4LUT font, column space and font smaller than row height, the color of column space and row space is the same as font background color, only 4 bit true color font mode, the color is transparent



Byte 2

Bit	Mode	Function
7:0	W	Row length unit: font base

Character Command (For blank)

Byte 0

Bit	Mode	Function
7	W	0
6	W	Blinking effect 0: Disable 1: Enable
5:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Blank pixel length

At least 3 pixels, and can't exceed 255 pixels.

Byte 2

Bit	Mode	Function
7:5	W	Reserved
4	W	Reserved
3:0	W	Blank color – select one of 16-color LUT (0 is special for transparent)

Character Command (For 1-bit RAM font)

Byte 0

Bit	Mode	Function
7	W	1
6	W	Character Blinking effect 0: Disable 1: Enable
5:4	W	00 (Font type 00: 1-bit RAM Font 01: 4-bit RAM Font 1x: 2-bit RAM Font)
3:0	W	Character width (only for 1-pixel font, doubled when specifying double-width in Row/Blank command register) For 12x18 font: 0100: 4-pixel 0101: 5-pixel 0110: 6-pixel 0111: 7-pixel 1000: 8-pixel 1001: 9-pixel 1010: 10-pixel 1011:11-pixel 1100: 12-pixel For 18x12 Font (rotated) 0000: 4-pixel 0001: 5-pixel 0010: 6-pixel 0011: 7-pixel 0100: 8-pixel 0101: 9-pixel 0110: 10-pixel 0111: 11-pixel 1000: 12-pixel 1001:13-pixel 1010:14-pixel 1011:15-pixel 1100: 16-pixel 1101:17-pixel 1110:18-pixel

When using border/shadow/ effect, the width of the 1-bit font should at least 6 pixel.

Byte 1

Bit	Mode	Function
7:0	W	Character Select [7:0]

Byte 2

Bit	Mode	Function
7:4	W	Foreground color Select one of 16-color from color LUT
3:0	W	Background color Select one of 16-color from color LUT (0 is special for transparent)

Character command (For 2-bit RAM Font)

Byte 0

Bit	Mode	Function
7	W	1
6	W	MSB of Foreground color 11, Background 00
5	W	1
4	W	MSB of Foreground color 10, Foreground 01
3:1	W	Foreground color 11 Select one of 8 color from color LUT Add Byte0 [6] as MSB for 16-color LUT.
0	W	Background color 00 Bit[2] Select one of 8 color from color LUT

Byte 1

Bit	Mode	Function
7:0	W	Character Select [7:0]

Byte 2

Bit	Mode	Function
7:6	W	Background color 00 Bit[1:0] Select one of 8 color from color LUT While 0 is special for transparent Add Byte0 [6] as MSB for 16-color LUT. Once we fill 0000 or 1000(MSB follow Byte0[6]), BG appears transparent.
5:3	W	Foreground color 10 Select one of 8 color from color LUT Add Byte0 [4] as MSB for 16-color LUT.
2:0	W	Foreground color 01 Select one of 8 color from color LUT Add Byte0 [4] as MSB for 16-color LUT.

Character command (For 4-bit RAM font)

Byte 0

Bit	Mode	Function
7	W	1
6	W	Character Blinking effect 0: Disable 1: Enable
5:4	W	01

		(Font type 00: 1-bit RAM Font 01: 4-bit RAM Font 1x: 2-bit RAM Font)
3:0	W	(for Byte1[7] = 0) select one color from 16-color LUT as background (for Byte1[7] = 1) Red color level MSB 4 bits for 8 bits color level (LSB 4 bits are 1111)

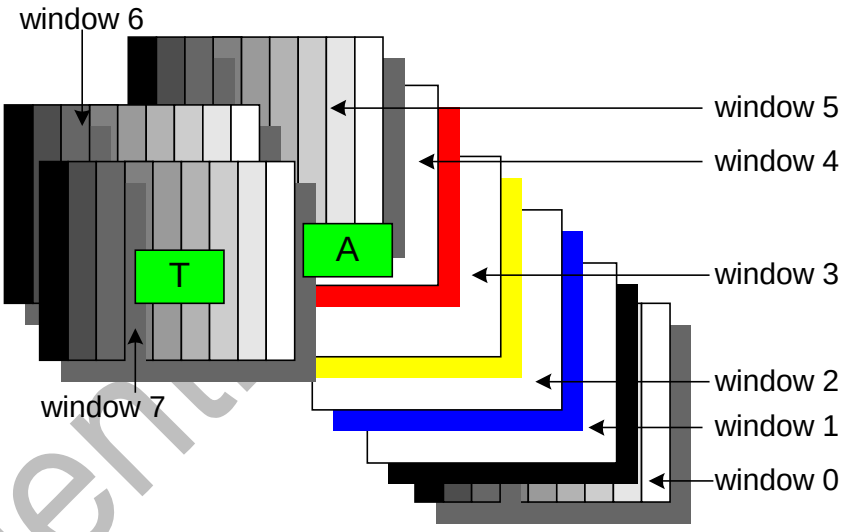
Byte 1

Bit	Mode	Function
7	W	0: 4bit Look Up Table, 0000'b is transparent. 1: 3bit specify R,G,B pattern, color level defined in Byte0[3:0],Byte2. One mask bit defines foreground or background.
6:0	W	Character Select [6:0]

- When 4-bit look-up table mode，color of column space is the same as background.
- When 4-bit look-up table mode and pixel value is 0000, and byte0[3:0]=0000 means transparent.
- When true color mode and pixel value is 0000，it is transparent。

Byte 2

Bit	Mode	Function
7:4	W	(for Byte1[7] = 1) Green color level MSB 4 bits for 8 bits color level (LSB 4 bits are 1111)
3:0	W	(for Byte1[7] = 1) Blue color level MSB 4 bits for 8 bits color level (LSB 4 bits are 1111)



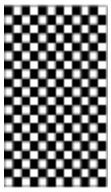
Display Priority

We have four windows with gradient and four windows without gradient, the window priority is as above, character should be always on the top layer of the window.

Pattern gen.

Use OSD to replace display pattern generator.

Chess Board: make a font as below



If we want to fill to the full 1280x1024 screen with character, we need 1280*1024 pixels. Required character is:

Using 12*18 font

1280/12 = 106.7 -> 107

1024/18 = 56.9 -> 57

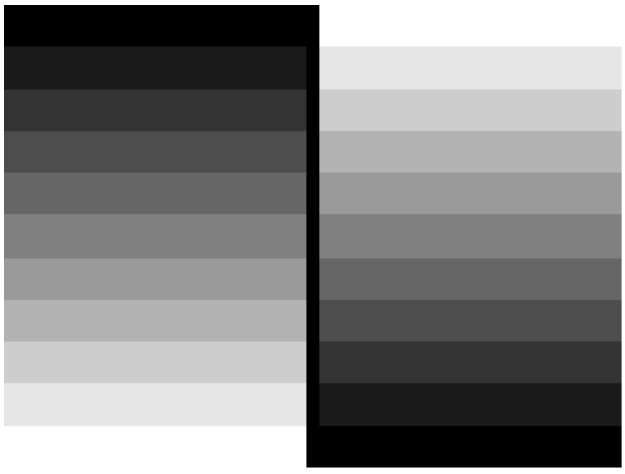
107*57 = 6099 character

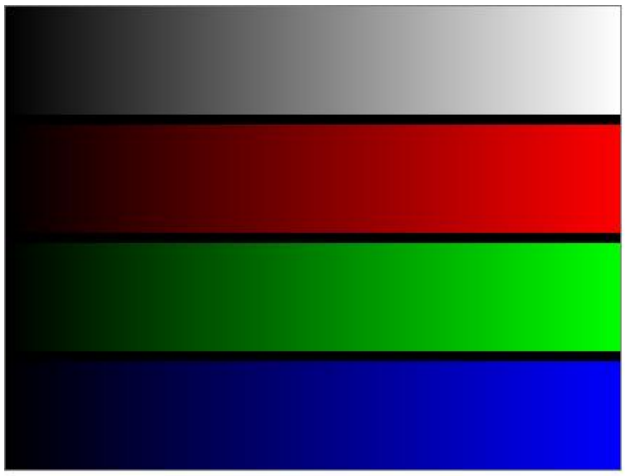
The required number of character map is larger than RAM size. We must turn on double width or double height function to reduce the half of character map.

So the basic unit to chessboard is 2x2 pixel. You can use larger chessboard instead of 2x2 pixels unit, such as 4x4 and so on.

Gray level

We can display 256 gray level by gradient window, 8 and 16 gray level by character map. 32 and 64 gray level is not supported.





6.Electric Specification

DC Characteristics

Table 2 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Voltage on VDD	V_{VDD}	-1		4.6	V
Voltage on Input (5V tolerant)	V_{IN}	-1		5.5	V
Voltage on Output or I/O or NC	V_{IO}	-1		4.6	V
Electrostatic Discharge	V_{ESD}			±2.5	kV
Latch-Up	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	ºC
Storage temperature (plastic)	T_{STG}	-55		125	ºC
Thermal Resistance (Junction to Air)	θ_{JA}			18	ºC/W

Table 3 DC Characteristics/Operating Condition

(0℃<TA<70℃; VDD = 3.3V ± 0.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	VDD	3.0	3.3	3.6	V
Supply Current(All function on at 135M)	I_{VDD}		255.2		mA
● digital supply	I_{DVCC}		244		
● DCLK PLL supply	I_{AVCC}		5.2		
● MCLK PLL supply	I_{PVCC}		6		
Supply Current(Power Saving)	I_{VDD}		7.2		mA
● digital supply	I_{DVCC}		5.6		
● DCLK PLL supply	I_{AVCC}		0.6		
● MCLK PLL supply	I_{PVCC}		1		
Output High Voltage	V_{OH}	2.4		VDD	V
Output Low Voltage	V_{OL}	GND		0.5	V
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V
I/O Pull-up resistance	R_{PU}	100		300	Ω
I/O Pull-down resistance	R_{PD}	50		150	Ω
Input Leakage Current(VI=VCC or GND)	I_{LI}	-10		+10	μA
Output Leakage Current(VO=VCC or GND)	I_{LO}	-20		+20	μA

AC Characteristics

Input Signal

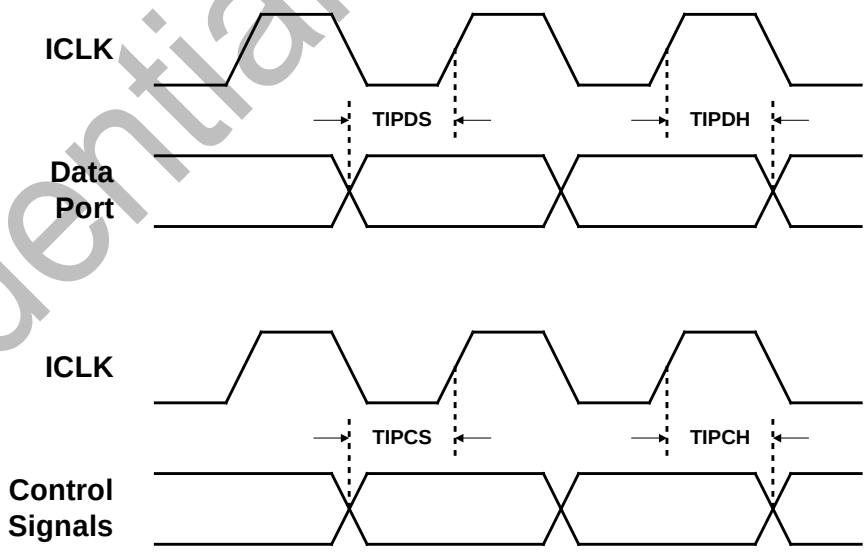


Figure 3 Input Signal Timing

Symbol	Parameter	Min	Max	Unit
TIPCS	Input control signals setup time for	2		ns
TIPCH	Input control signals hold time for ICLK	1		ns
TIPDS	Input data setup time for ICLK	2		ns
TIPDH	Input data hold time for ICLK	1		ns

Output Signal

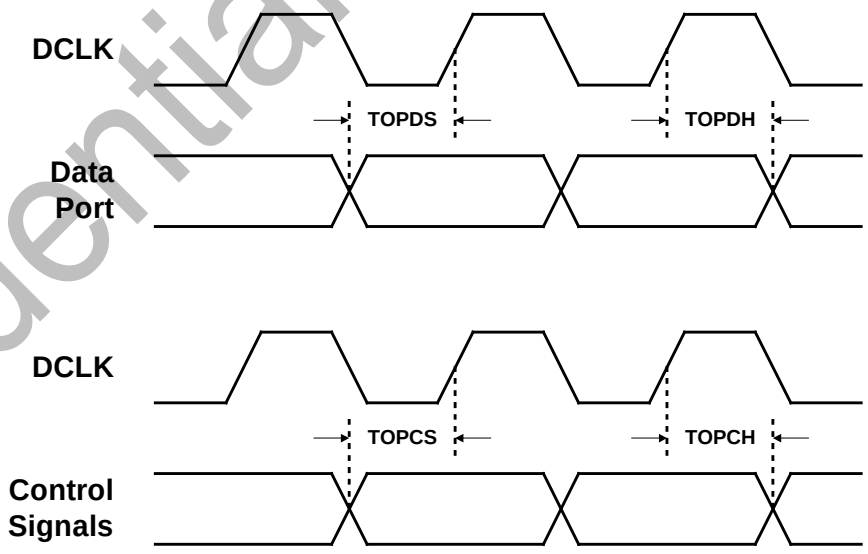


Figure 4 Output Signal Timing

Symbol	Parameter	Min	Max	Unit
TOPCS	Output control signals setup time for	4		ns
TOPCH	Output control signals hold time for	1		ns
TOPDS	Output data setup time for DCLK	4		ns
TOPDH	Output data hold time for DCLK	1		ns

Serial Port Signal

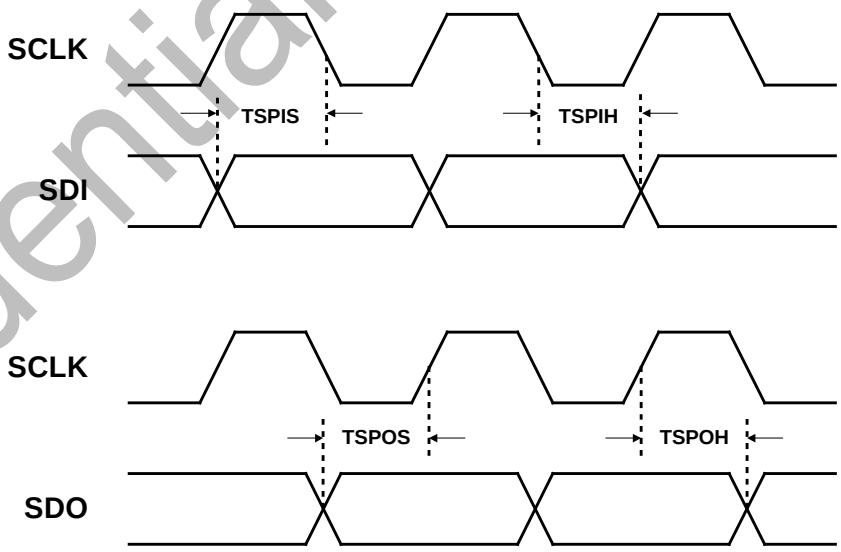
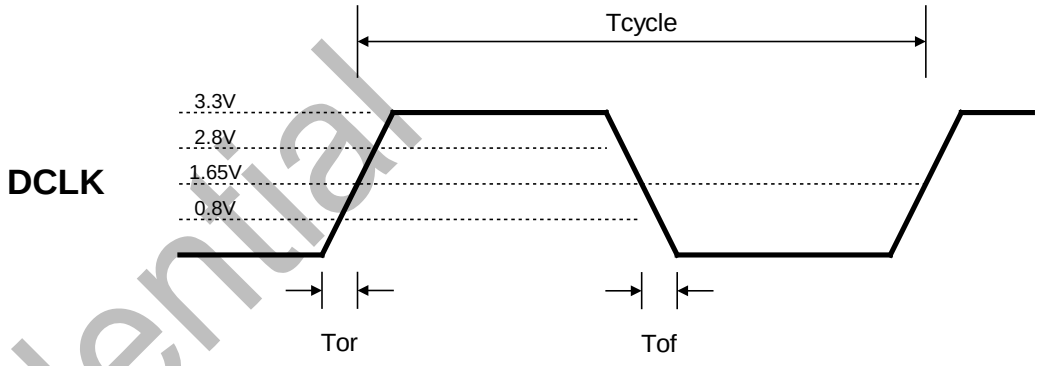


Figure 5 Serial Port Signal Timing

Symbol	Parameter	Min	Max	Unit
TSPIS	Serial port input signal setup time for	2		ns
TSPIH	Serial port input signal hold time for	8		ns
TSPOS	Serial port output signal setup time for	1/3		TCK
TSPOH	Serial port output signal for SCLK	1/2		TCK

1.44.4 PLL

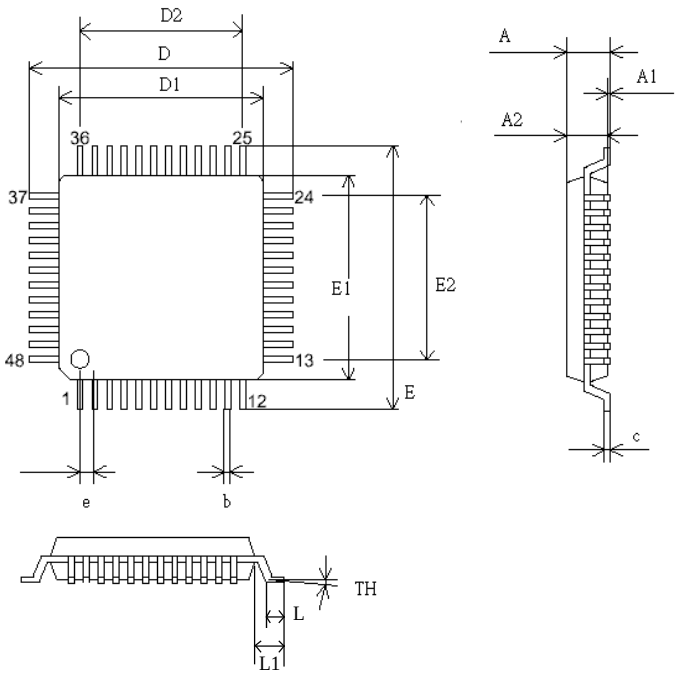


Electrical Characteristics

Characteristics	Symbol	Conditions	Mix	Type	Max	Unit
Output rise time (20pf Load)	Tor	From 0.8V to 2.0V,Vdd=3.3V			2.0	ns
Output fall time (20pf Load)	Tof	From 2.0V to 0.8V,Vdd=3.3V			2.0	ns
Duty cycle (20pf Load, at 1.5V)	Tduty	DCLK	45	50	55	%
Clock Skew (20pf Load, at 1.5V)	Tskw1	DCLK to DCLK			250	ps
Jitter, Absolute (20pf Load)	Tj1	DCLK			300	ps

7. Mechanical Specification

48 Pin LQFP



SYMBOL	MILLIMETER			INCH		
	MIN.	TYPICAL	MAX.	MIN.	TYPICAL	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
c	0.09		0.20	0.004		0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.0196 BSC		
TH	0o	3.5o	7o	0o	3.5o	7o
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1		1.00			0.0393	

TITLE: LQFP-48 (7.0x7.0x1.6mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL		
APPROVE	DOC. NO.	
	VERSION	02
CHECK	DWG NO	PKGC-065
	DATE	
REALTEK SEMICONDUCTOR CORP.		