

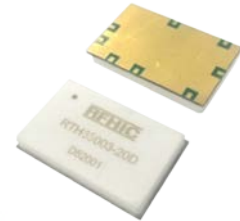


## Product Features

- GaN on SiC Chip on Board
- Surface Mount Hybrid Type
- 2-Stage Doherty Amplifier
- High Efficiency
- No Matching circuit needed

## Applications

- RF Sub-Systems
- Base Station
- RRH
- 4G/ LTE system
- Small cell



Package Type : SP-1E

## Description

Accommodating the future of 4G/LTE small cells, RFHIC introduces RTH35003-20D amplifier fabricated using an advanced high power density Gallium Nitride (GaN) semiconductor process.

## Electrical Specifications @ $V_{ds}=30V$ , $T_a=25^\circ C$

PARAMETER	UNIT	MIN	TYP	MAX	CONDITION
Frequency Range	MHz	3520	3540	3560	$Z_S = Z_L = 50 \text{ ohm}$
Power Gain		21	24	-	
Gain Flatness	dB	-1.5	-	+1.5	-
Input Return Loss		-	-14	-9	
Pout @ Average	dBm	-	35.1	-	3.236W
Pout @ Saturation	dBm	42.6	43.5	-	Pulse Width=20us, Duty cycle 10%
ACLR @ BW 20MHz 2FA LTE (PAPR 7.5dB)	dBc	-	-29	-25	Non DPD
		-	-53	-	With DPD
Doherty Efficiency	%	-	46	-	$T_c=25^\circ C$
Total Efficiency		35	38	-	
Drive Amp. Idq	mA	-	40	-	-
Carrier Amp. Idq		-	110	-	-
Peaking Amp. Idq		-	0	-	-
Supply Voltage	V	-4.9	-2.8	-2.0	Vgd
		-4.9	-2.8	-2.0	Vgc
		-4.9	-4.8	-3.0	Vgp
		-	30	-	Vds

### Caution

The drain voltage must be supplied to the device after the gate voltage is supplied

Turn on → Turn on the Gate voltage supply and last turn on the Drain voltage supplies

Turn off → Turn off the Drain voltage and last turn off the Gate voltage

### Note

1. ACLR Measured Pout=35.1dBm @  $f_c \pm 40\text{MHz} / 38.06\text{MHz}$   
LTE 20MHz 2FA PAPR=7.5dB @ 0.01% probability on CCDF

## Mechanical Specifications

PARAMETER	UNIT	TYPICAL	RATING
Mass	g	6.0	$\pm 1.0$
Dimension	mm	32 x 20 x 4.2	$\pm 0.15$

## Absolute Maximum Ratings

PARAMETER	UNIT	RATING	SYMBOL	CONDITION
Gate-Source Voltage	V	-10 ~ 0	V <sub>gd</sub> V <sub>gc</sub> V <sub>gp</sub>	T <sub>c</sub> =25°C
Drain-Source Voltage	V	50	V <sub>ds</sub>	T <sub>c</sub> =25°C
Gate Current	mA	1.2 2.1 4	Drive Carrier Peaking	T <sub>c</sub> =25°C
Power Dissipation	W	6.1	P <sub>D</sub>	T <sub>c</sub> =85°C
Operating Junction Temperature	°C	225	T <sub>J</sub>	-
Operating Case Temperature	°C	-30 ~ 85	T <sub>C</sub>	-
Storage Temperature	°C	-40 ~ 100	T <sub>STG</sub>	-
Soldering Temperature <sup>*1</sup>	°C	260	T <sub>s</sub>	30s Max.
RF Input Level (Pulse)	dBm	35	Pin	T <sub>c</sub> =25°C

\*1 Reflow cycle limit : 1time

## Operating Voltages & Input level

PARAMETER	UNIT	MIN	TYP	MAX	SYMBOL
Drain Voltage 1	V	29.5	30	30.5	V <sub>ds1</sub>
Drain Voltage 2	V	29.5	30	30.5	V <sub>ds2</sub>
Gate Voltage (on-stage)	V	-4.9	V <sub>gd</sub> <sup>*2</sup>	-2.0	V <sub>gd</sub>
Gate Voltage (on-stage)	V	-4.9	V <sub>gc</sub> <sup>*3</sup>	-2.0	V <sub>gc</sub>
Gate Voltage (on-stage)	V	-4.9	V <sub>gp</sub> <sup>*4</sup>	-3.0	V <sub>gp</sub>
Gate Voltage (off-stage)	V	-	-8	-	V <sub>gd</sub>
Gate Voltage (off-stage)	V	-	-8	-	V <sub>gc</sub>
Gate Voltage (off-stage)	V	-	-8	-	V <sub>gp</sub>
RF Input Level (Pulse)	dBm	-	-	30	Pin

\*2 V<sub>gd</sub>(Pin#1) set : Lower V<sub>gd</sub> of Δ-0.15V at Drive amp. Idq 80mA±5%

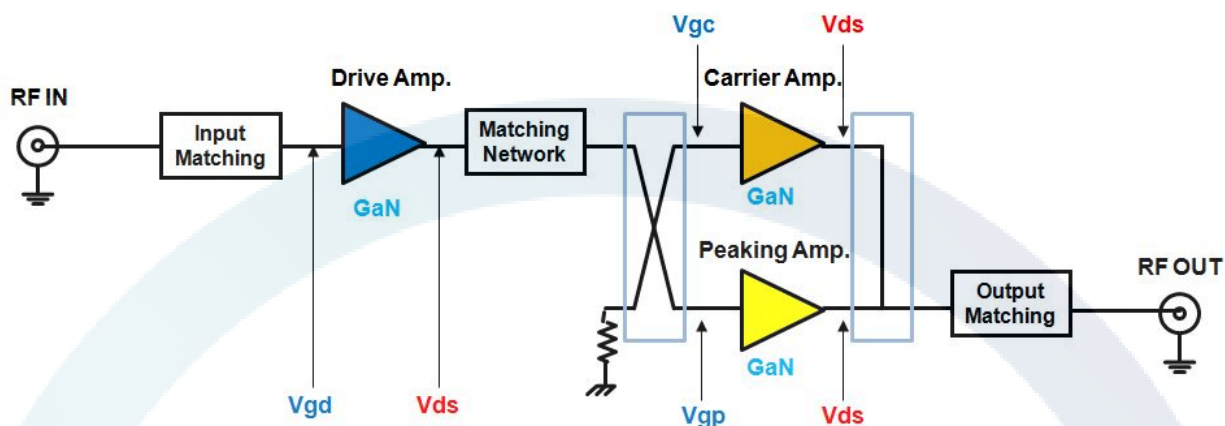
\*3 V<sub>gc</sub>(Pin#13) set: Carrier Idq 110mA±5%

\*4 V<sub>gp</sub>(Pin#5) set: Lower V<sub>gp</sub> of Δ-1.7V at Peaking Idq 100mA±5%

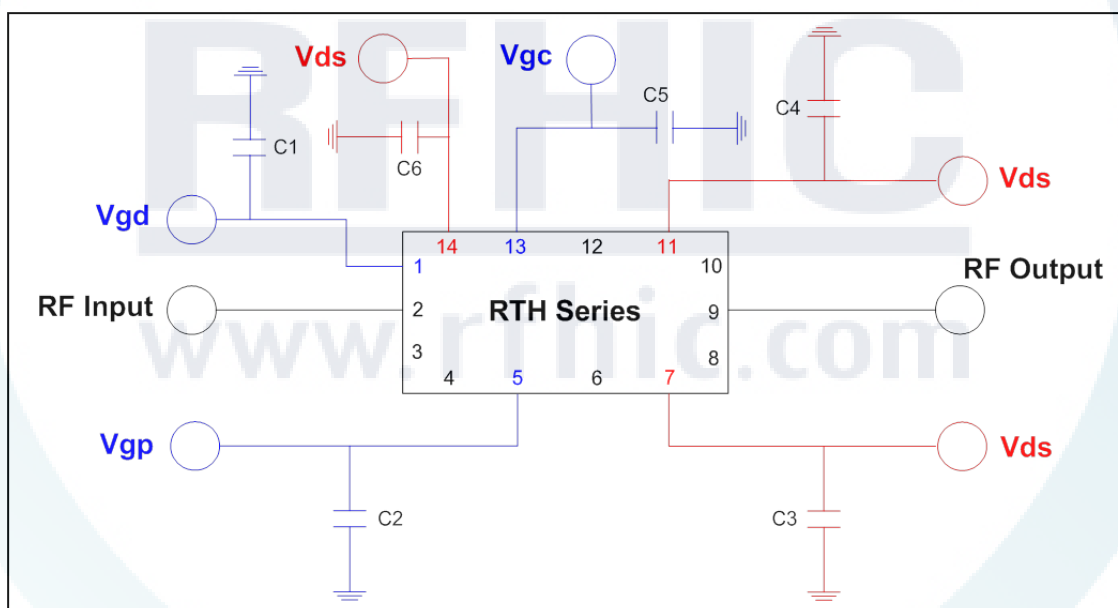
## ESD Level

PARAMETER	STANDARD	RESULT
HBM	JESD22-A114E	Class 1A/ passed Voltage 500V
MM	JESD22-A115C	Class A/ passed Voltage 100V

## Block Diagram



## Application Circuit



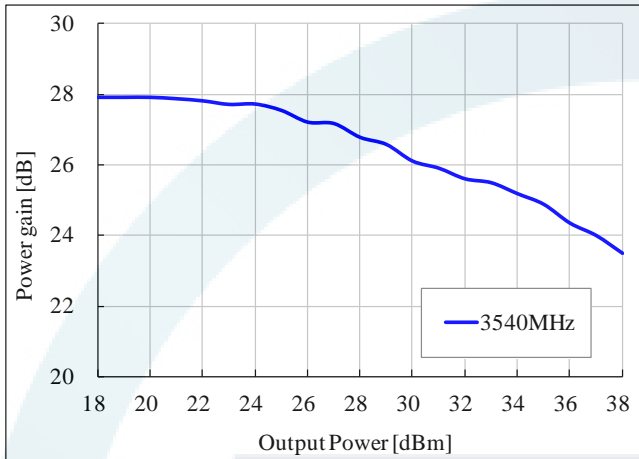
## Bill of Material (Evaluation board)

LOCATION	Part Number	Value	Manufacturer
C3, C4, C6	1812B225K101CT	2.2uF / 100V	WALSIN
C1, C2, C5	GRM1885C1H101JA01D	100pF / 50V	MURATA
PCB	RO4350B	2Layer, 20mil, 1oz	ROGERS

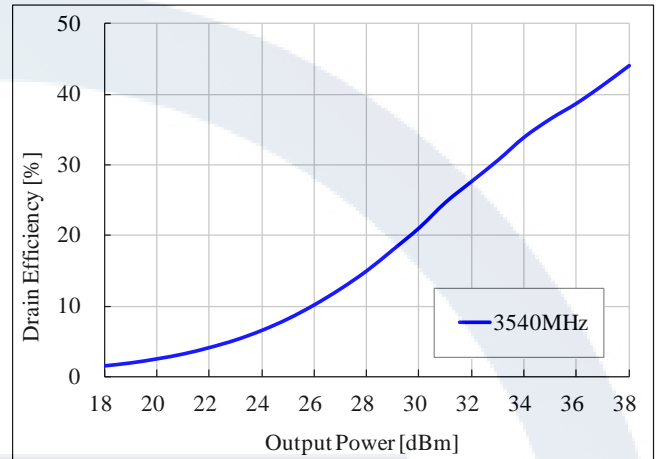
## Performance Charts

\* **Bias condition** @ Drive Idq=40mA, Carrier Idq=110mA, Peaking Idq=0mA, Ta=25°C

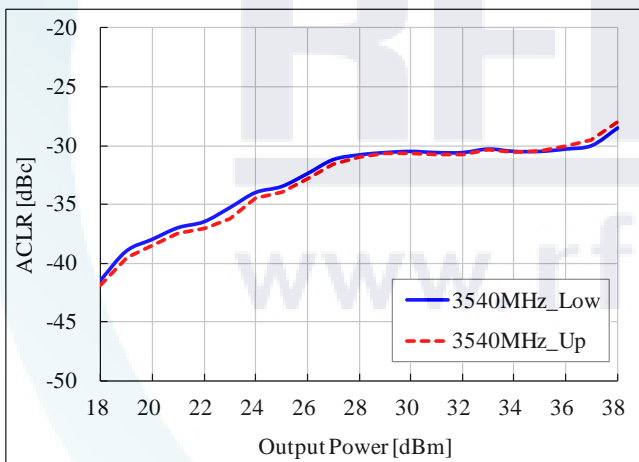
**Power Gain vs. Output Power**



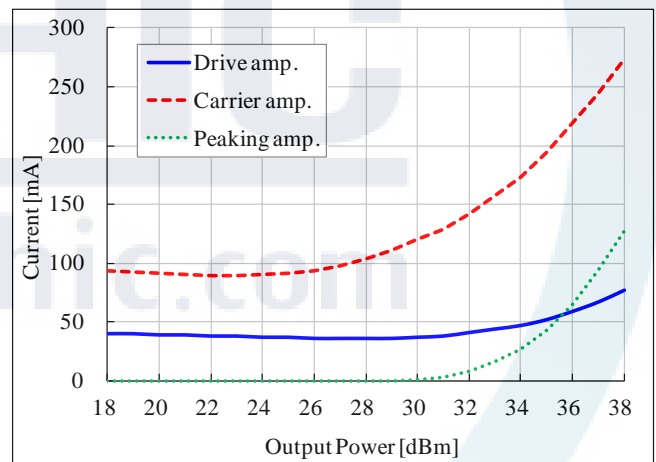
**Drain Efficiency vs. Output Power**



**ACLR vs. Output Power**

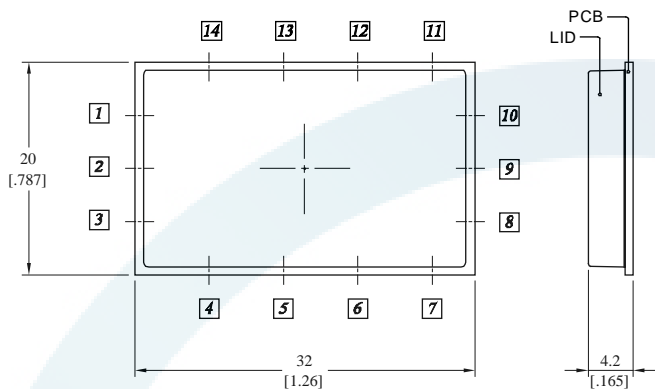


**Current vs. Output Power**



## Package Dimensions (Type: SP-1E)

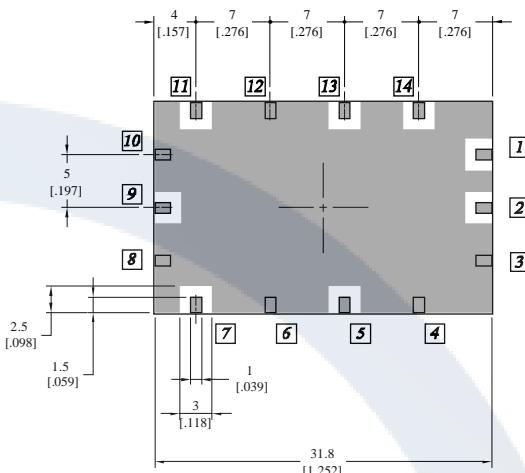
\* Unit: mm[inch] | Tolerance:  $\pm 0.15[.006]$



▲ Top View

▲ Side View

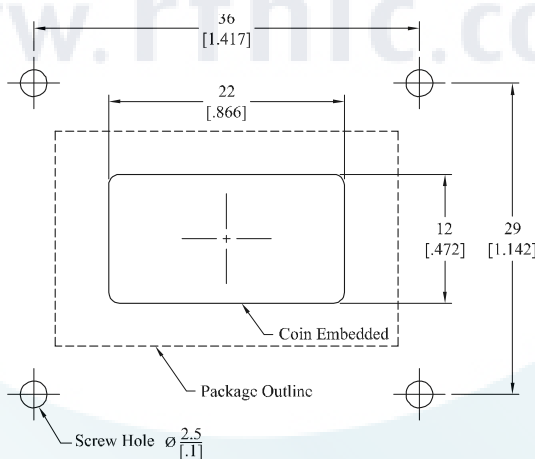
\* Unit: mm[inch] | Tolerance:  $\pm 0.15[.006]$



▲ Bottom View

Pin Description (RTH35003-20D)							
Pin No	Function	Pin No	Function	Pin No	Function	Pin No	Function
1	Vgd	4	GND	8	GND	11	Vds
2	RF In	5	Vgp	9	RF Out	12	GND
3	GND	6	GND	10	GND	13	Vgc
		7	Vds			14	Vds

## Recommended Mounting Configuration



### \* Mounting Configuration Notes

- For the proper performance of the device, Ground / Thermal via holes must be designed to remove heat.
- To properly use heatsink, ensure the ground/thermal via hole region to contact the heatsink. We recommend the mounting screws be added near the heatsink to mount the board
- In designing the necessary RF trace, width will depend upon the PCB material and construction.
- Use 1 oz. Copper minimum thickness for the heatsink.
- Do not put solder mask on the backside of the PCB in the region where the board contacts the heatsink
- We recommend adding as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
- We recommend that the PCB with the RF device in a hybrid package(RTH Series) is not washed to remove the flux.

**Ordering Information**

Part Number	Package Design
RTH35003-20D	-R (Reel)
	-B (Bulk)
	-EVB (Evaluation Board)

**Revision History**

Part Number	Release Date	Version	Modification	Data Sheet Status
RTH35003-20D	2016.04.20	3.0	Electrical Specification (1p) Performance Charts (3p)	-
RTH35003-20D	2015.10.20	1.1	Electrical Specification Absolute Maximum Ratings	-
RTH35003-20D	2015.08.28	1.0	Operating voltages & Input level	-



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