RTL8188FTV-VC-CG

SINGLE-CHIP IEEE 802.11b/g/n 1T1R WLAN

DATASHEET

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2015/02/04	Preliminary release
0.2	2017/12/27	Modify Model name

Note:

Datasheet revision / feature will be adjusted and updated continuously by Realtek without further notice.

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1. General Description

The Realtek RTL8188FTV-VC-CG is a highly integrated single-chip 802.11n Wireless LAN (WLAN) network USB interface (USB 1.0/1.1/2.0 compliant) controller. It combines a WLAN MAC, a 1T1R capable WLAN baseband, and WLAN RF in a single chip. The RTL8188FTV-VC-CG provides a complete solution for a high throughput performance integrated wireless LAN device.

The RTL8188FTV-VC-CG WLAN baseband implements Orthogonal Frequency Division Multiplexing (OFDM) with 1 transmit and 1 receive path and is compatible with the IEEE 802.11n specification. Features include one spatial stream transmission, short guard interval (GI) of 400ns, spatial spreading, and transmission over 20MHz and 40MHz bandwidth.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available, and CCK provides support for legacy data rates, with long or short preamble. The high-speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, and 64QAM modulation of the individual subcarriers and rate compatible punctured convolutional coding with coding rate of 1/2, 2/3, 3/4, and 5/6, provide higher data rates of 54Mbps and 150Mbps for IEEE 802.11g and 802.11n OFDM respectively.

The RTL8188FTV-VC-CG WLAN Controller builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams.

Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end. Selectable digital transmit and receive FIR filters are provided to meet transmit spectrum mask requirements and to reject adjacent channel interference, respectively.

The RTL8188FTV-VC-CG WLAN Controller supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, and adaptive transmit power control function to obtain the better performance in the analog portions of the transceiver.

The RTL8188FTV-VC-CG WLAN MAC supports 802.11e for multimedia applications, 802.11i for security, and 802.11n for enhanced MAC protocol efficiency. Using packet aggregation techniques such as

A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, and U-APSD, reduce the power wasted during idle time, and compensates for the extra power required to transmit OFDM. The RTL8188FTV-VC-CG provides simple legacy and 20MHz/40MHz co-existence mechanisms to ensure backward and network compatibility.

2. Features

General

- 24-pin QFN
- CMOS MAC, Baseband PHY, and RF in a single chip for IEEE 802.11b/g/n compatible WLAN
- Complete 802.11n solution for 2.4GHz band
- 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth
- 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating in 802.11n mode

Interface

- Complies with USB 1.0/1.1/2.0 for WLAN

Standards Supported

- IEEE 802.11b/g/n compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services

WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism
- Channel management and co-existence
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth

WLAN PHY Features

- IEEE 802.11n OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz and 40MHz bandwidth transmission
- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 64QAM modulation.
  Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n
- Selectable receiver FIR filters
- Programmable scaling in transmitter and receiver to trade quantization noise against increased probability of clipping
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC

Peripheral Interfaces

- General Purpose Input/Output (5 pins)

- One configurable LED pins

3. Application Diagram

3.1. Single-Band 11n (1x1) Solution with Single Antenna

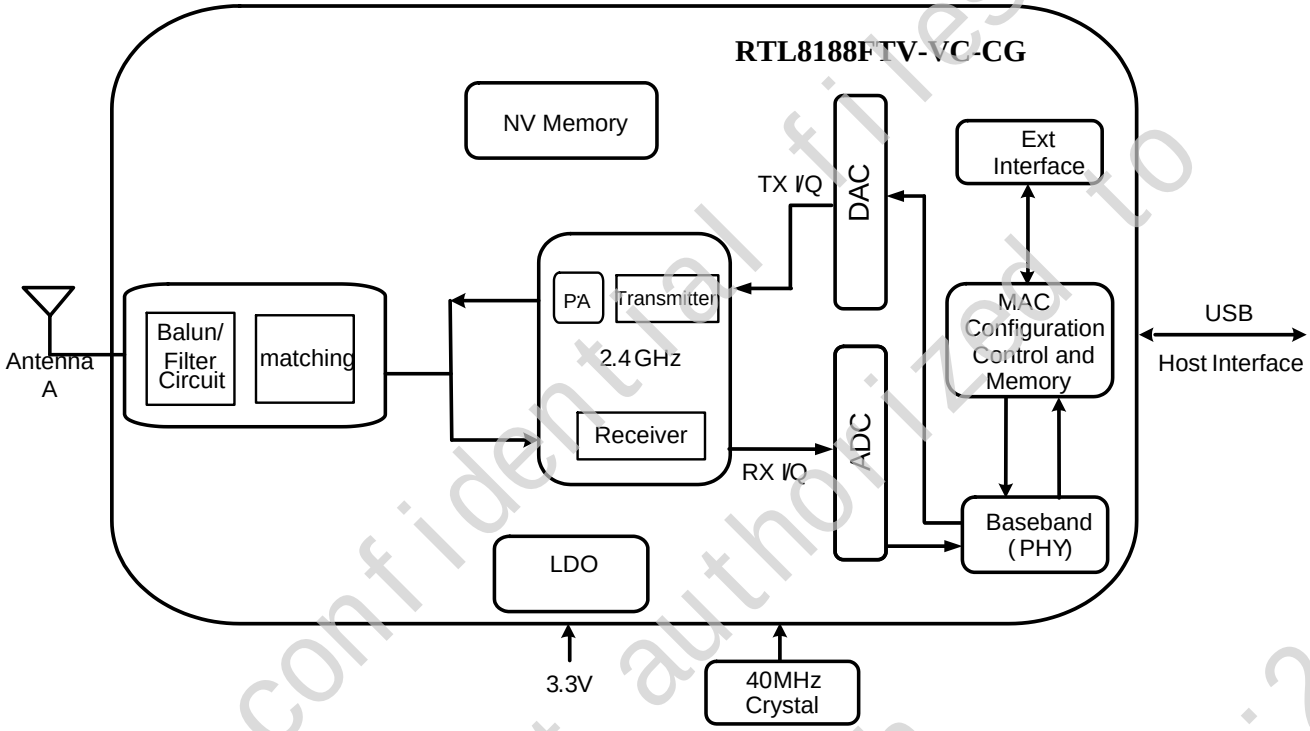


Figure 1. Single-Band 11n (1x1) Solution

4. Pin Assignments

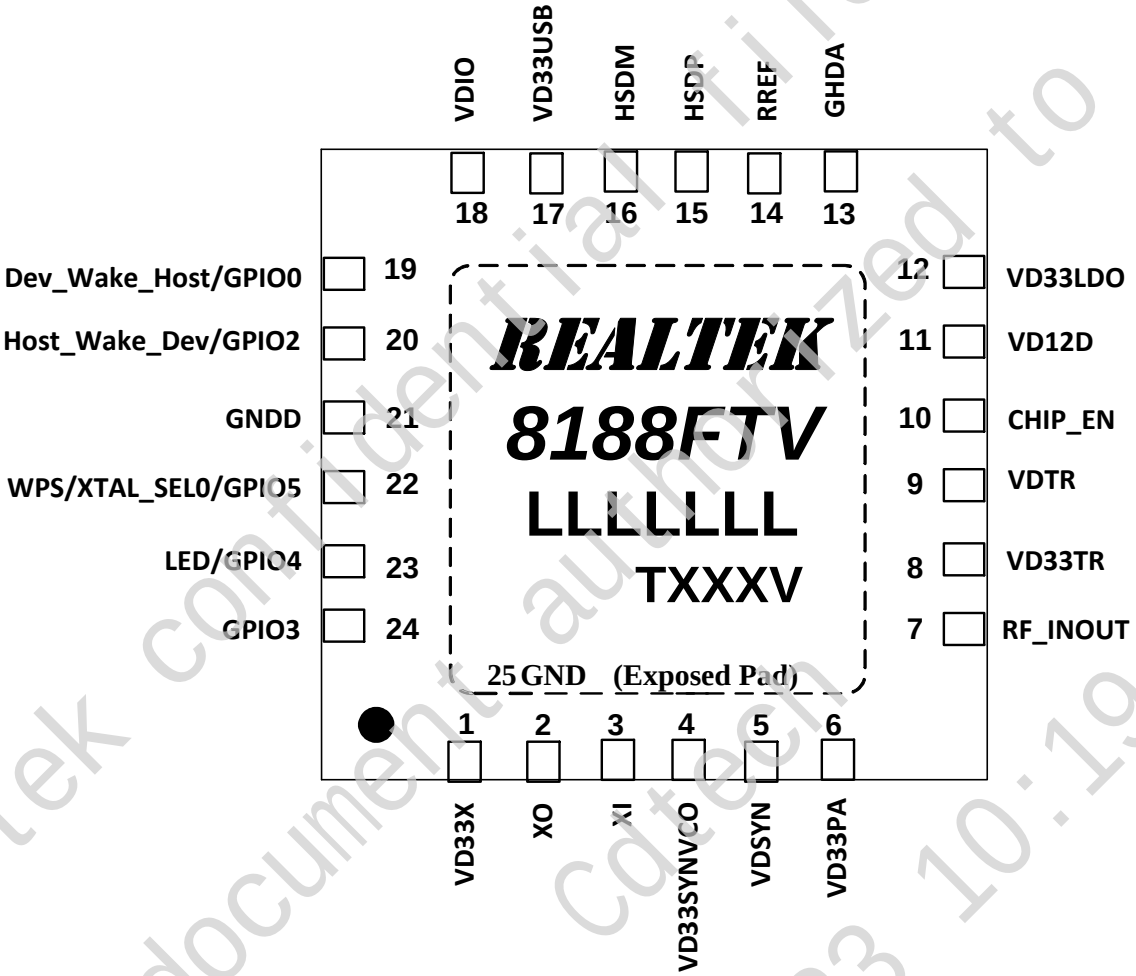


Figure 2 Pin Assignments

4.1. Package Identification

'Green' package is indicated by a 'G' in the location marked 'T' in 錯誤! 找不到參照來源。. The version is shown in the location marked 'V', e.g.,.C=Version C

5. Pin Descriptions

The following signal type codes are used in the tables:

I: Input; O:Output

I/O: bi-directional input/output pin; P:Power pin

5.1. USB Bus Transceiver Interface

Table 1. USB bus Transceiver Interface

Symbol	Type	Pin No	Description
HSDM/HSDP	I/O	16/15	USB Receive Differential Pair

5.2. Power Pins

Table 2. Power Pins

Symbol	Type	Pin No	Description
VD33X	P	1	VDD 3.3V for XTAL
VD33SYNVCO	P	4	VDD 3.3V for Analog
VDSYN	P	5	VDD 3.3V or VDD 1.2v for Analog
VD33PA	P	6	VDD 3.3V for PA
VD33TR	P	8	VDD 3.3V for RF
VDTR	P	9	VDD 3.3V or VDD 1.2v for RF
VD33LDO	P	12	VDD 3.3V for internal LDO
VD33USB	P	17	VDD 3.3V for USB
VDIO	P	18	VDD 3.3V for GPIO
VD12D	P	11	Digital 1.2V for core
GND	P	13,21	Ground

5.3. RF Interface

Table 3. RF Interface

Symbol	Type	Pin No	Description
RF_INOUT	I/O	7	RF TRX Signal

5.4. LED Interface

Table 4. LED Interface

Symbol	Type	Pin No	Description
LED/GPIO4	I/O	23	LED Pins (Active Low) Shared with GPIO4

5.5. Clock and Other Pins

Table 5. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	3	25/40MHz OSC Input Input of 25/40MHz Crystal clock reference
XO	O	2	Output of 25/40MHz Crystal Clock Reference
CHIP_EN	I	10	This Pin can Externally Shutdown RTL8188FTV-VC-CG
RREF	O	14	Band gap. It needs to link 24k resister pull down.
Dev_Wake_Host/GPIO0	I/O	19	Device wake host output pin, Shared with GPIO0
Host_Wake_Dev/GPIO2	I/O	20	Host Wake Device input pin, Shared with GPIO2
WPS/USB_XTAL_SEL0/ GPIO5	I/O	22	Trap Function: Decide to use the 27/40Mhz crystal by this pin power on latch low or high. USB_XTAL_SEL = 1, XTAL frequency is 27MHz USB_XTAL_SEL = 0, XTAL frequency is 40MHz Shared with GPIO5
GPIO3	I/O	24	General Purpose Input/Output Pin

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 6. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. DC Characteristics

6.2.1. Power Supply Characteristics

Table 7. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VD33X VD33SYNVCO VDSYN VD33PA VD33TR VDTR VD33LDO VD33USB VDIO	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
VD12D	1.2V Core Supply Voltage	1.10	1.2	1.32	V

6.2.2. Digital IO Pin DC Characteristics

Table 8. 3.3V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

7. Interface Timing Specification

7.1. USB Bus during Power On Sequence

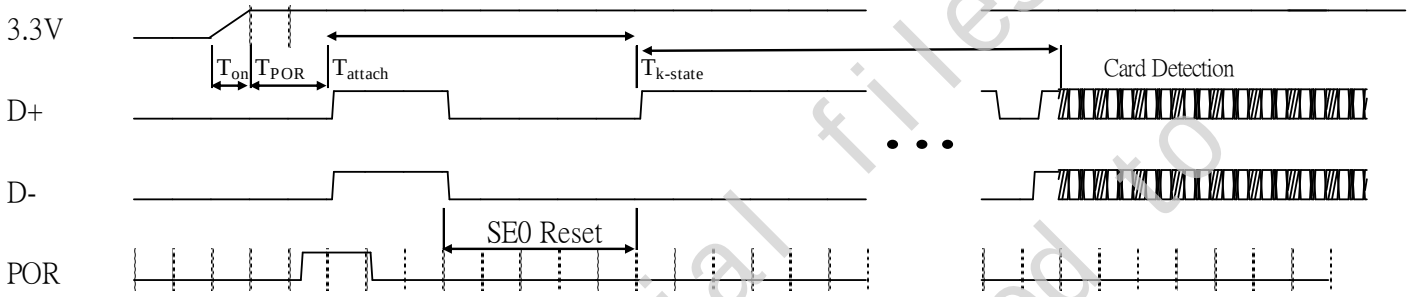


Figure 3 RTL8188FTV-VC-CG USB Bus Power On Sequence

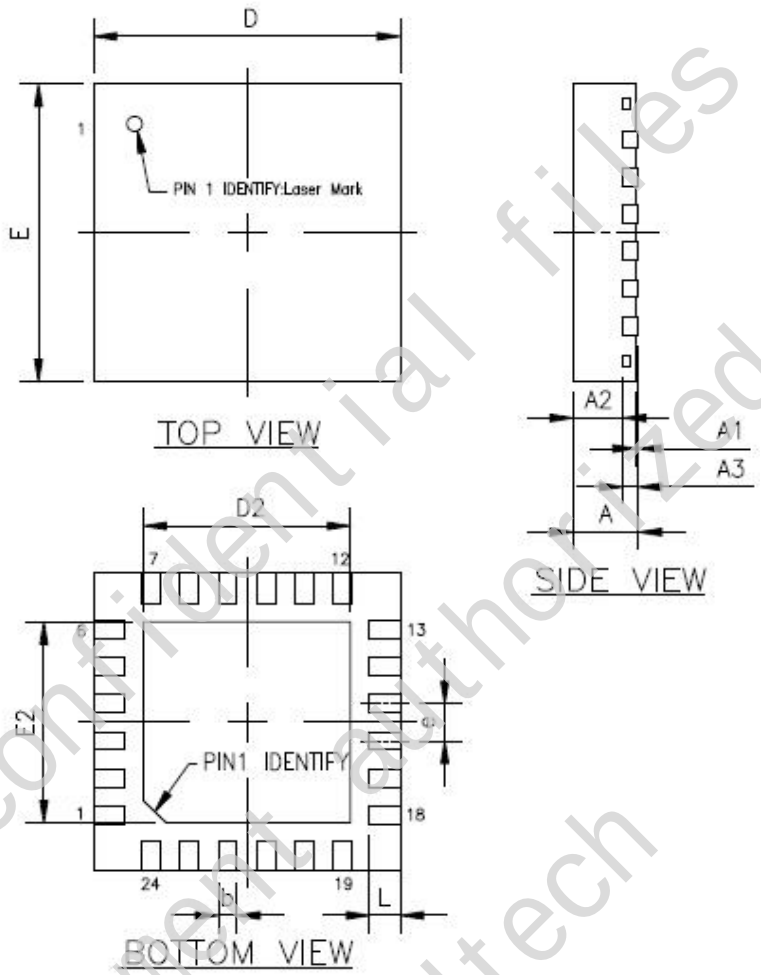
T_{on}: The main power ramp up duration
T_{por}: The power on reset releases and power management unit executes power on tasks
T_{attach}: USB attach state
$T_{k\text{-}state}$: the duration from resister attached to USB host starting card detection procedure

The power on flow description:
After main 3.3V ramp up, the internal power on reset is released by power ready detection circuit and the power management unit will be enabled. The power management unit enables the internal regulator and clock circuits.
The power management unit also enables the USB circuits.
USB analog circuits attach resisters to indicate the insertion of the USB device

Table 9. The typical timing range

	Unit	Min	Typical	Max
T_{on}	ms	0.25	1.5	5
T_{por}	ms	--	2	10
T_{attach}	ms	2	7	15
$T_{k\text{-}state}$	ms	50	250	--

8. Mechanical Dimensions



8.1 Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	—	0.65	0.70	—	0.026	0.028
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E		4.00 BSC			0.158 BSC	
D2/E2	2.00	2.20	2.45	0.078	0.087	0.096
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

9. Ordering Information

Table 10. Ordering Information

Part Number	Package	Status
RTL8188FTV-VC-CG	QFN-24, 'Green' Package	Mass Production

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