RTL8189EM-CG

SINGLE-CHIP IEEE 802.11b/g/n 1T1R WLAN With SDIO INTERFACE

DATASHEET
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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2013/12/27	Preliminary release
0.2	2014/04/02	Modify GSPI PIN define

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1. General Description

The Realtek RTL8189EM is a highly integrated single-chip 802.11n Wireless LAN (WLAN) network SDIO interface (SDIO 1.1/ 2.0 compliant) controller. It is a WLAN MAC, a 1T1R capable WLAN baseband, and WLAN RF in a single chip. The RTL8189EM provides a complete solution for a high throughput performance integrated wireless LAN device.

The RTL8189EM WLAN baseband implements Orthogonal Frequency Division Multiplexing (OFDM) with 1 transmit and 1 receive path and is compatible with the IEEE 802.11n specification. Features include one spatial stream transmission, short guard interval (GI) of 400ns, spatial spreading, and transmission over 20MHz and 40MHz bandwidth.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available, and CCK provides support for legacy data rates, with long or short preamble. The high-speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, and 64QAM modulation of the individual subcarriers and rate compatible punctured convolutional coding with coding rate of 1/2, 2/3, 3/4, and 5/6, provide higher data rates of 54Mbps and 150Mbps for IEEE 802.11g and 802.11n OFDM respectively.

The RTL8189EM WLAN Controller builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference.

Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end. Selectable digital transmit and receive FIR filters are provided to meet transmit spectrum mask requirements and to reject adjacent channel interference, respectively.

The RTL8189EM WLAN Controller supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control function to obtain the better performance in the analog portions of the transceiver.

The RTL8189EM WLAN MAC supports 802.11e for multimedia applications, 802.11i for security, and 802.11n for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, and U-APSD, reduce the power wasted during idle time, and compensates for the extra power required to transmit OFDM. The RTL8189EM provides simple legacy and 20MHz/40MHz co-existence mechanisms to ensure backward and network compatibility.

2. Features

General

- 32-pin QFN

- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN

- Complete 802.11n solution for 2.4GHz band

- 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth

- 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth

- Compatible with 802.11n specification

- Backward compatible with 802.11b/g devices while operating in 802.11n mode

Host Interface

- Complies with SDIO 1.1/ 2.0 for WLAN with clock rate up to 50MHz

- GSPI interface for configurable endian for WLAN

Standards Supported

- IEEE 802.11b/g/n compatible WLAN

- IEEE 802.11e QoS Enhancement (WMM)

- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services

WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)

- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)

- PHY-level spoofing to enhance legacy compatibility

- Power saving mechanism

- Channel management and co-existence

- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth

- Support Scan and Preferred Network Offload

WLAN PHY Features

- IEEE 802.11n OFDM

- One Transmit and one Receive path (1T1R)

- 20MHz and 40MHz bandwidth transmission

- Short Guard Interval (400ns)

- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble

- OFDM with BPSK, QPSK, 16QAM, and 64QAM modulation.
  Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6

- Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n

- Switch diversity for DSSS/CCK

- Hardware antenna diversity in per packet base

- Selectable receiver FIR filters

- Programmable scaling in transmitter and receiver to trade quantization noise against increased probability of clipping

- Fast receiver Automatic Gain Control (AGC)

- On-chip ADC and DAC

Peripheral Interfaces

- General Purpose Input/Output (5 pins)

- One configurable LED pins

3. Application Diagram

3.1. Single-Band 11n (1x1) Solution
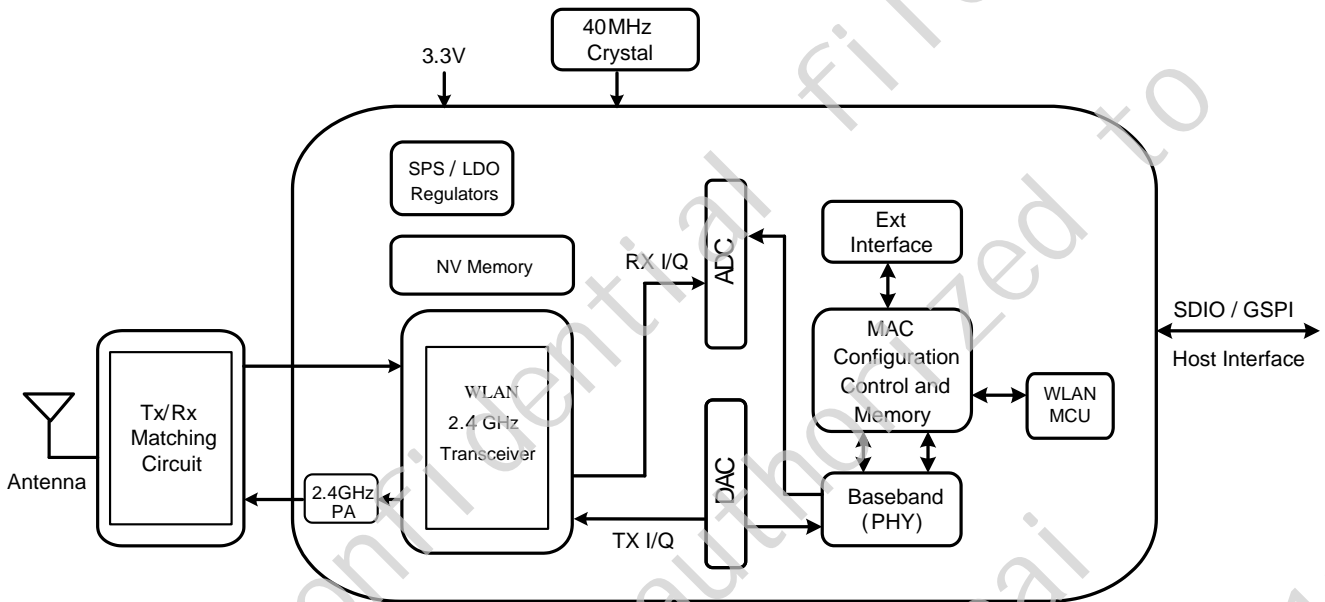
Figure 1. Single-Band 11n (1x1) Solution

4. Pin Assignments
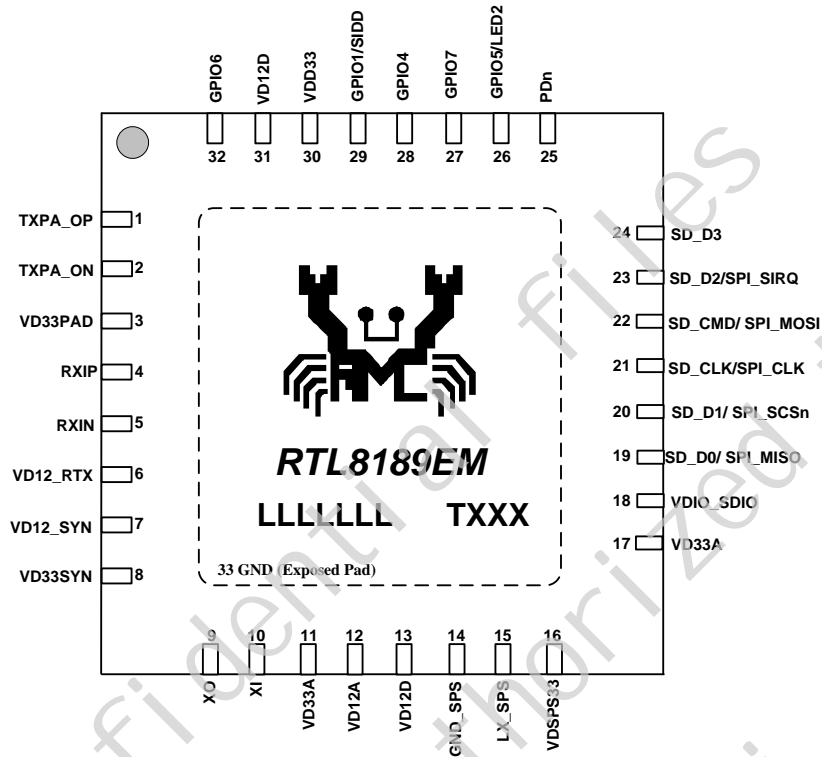
Figure 2. Pin Assignments

4.1. Package Identification

'Green' package is indicated by a 'G' in the location marked 'T' in Figure 2.

5.   Pin Descriptions

The following signal type codes are used in the tables:

I: Input	O: Output
T/S: Tri-State bi-directional input/output pin	S/T/S: Sustained Tri-State
O/D: Open Drain	P: Power pin

5.1. SDIO Interface

Table 1.   SDIO Interface

Symbol	Type	Pin No	Description
SD_CLK	I	21	SDIO Clock Input
SD_CMD	I/O	22	SDIO Command Input
SD_D0	I/O	19	SDIO Data Line 0
SD_D1	I/O	20	SDIO Data Line 1
SD_D2	I/O	23	SDIO Data Line 2
SD_D3	I/O	24	SDIO Data Line 3

The SDIO interface selection can be referred to subsection 6.5.1, "SDIO Power on Sequence".The signal level section of SDIO interface selection can be referred to subsection 6.5.1, "SDIO/GSPI Signal Level".

5.2. GSPI Interface

Table 2.   GSPI Interface

Symbol	Type	Pin No	Description
SPI_CLK	I	21	GSPI Clock Input
SPI_MOSI	I	22	GSPI Data Input
SPI_MISO	O	19	GSPI Data Out
SPI_SIRQ	O	23	GSPI Interrupt
SPI_SCSn	I	20	GSPI Chip Select Bar

The GSPI interface pins are shared with SDIO interface. The GSPI interface selection can be referred to subsection 6.5.1, "GSPI Power on Sequence". The signal level section of SDIO interface selection can be referred to subsection 6.5.1, "SDIO/GSPI Signal Level".

5.3. Power Pins

Table 3.   Power Pins

Symbol	Type	Pin No	Description
LX_SPS	P	15	Switching Regulator Output
VDSPS33	P	16	Switching Regulator Input Or Linear Regulator output from 3.3V to 1.5V
VD33A	P	11	VDD 3.3V for Analog
VDD33	P	17, 30	VDD3.3V for Digital
VD33PAD	P	3	VDD 3.3V for PAD
VD33SYN	P	8	VDD 3.3V for SYN
VDIO_SDIO	P	18	VDD for SDIO Pin, the power supply is same as the signal level of SDIO bus (3.3V - 1.8V)
VD12A	P	12	VDD 1.2V for Analog
VD12D	P	13, 31	VDD 1.2V for Digital
VD12_RTX	P	6	VDD 1.2V for RTX

Symbol	Type	Pin No	Description
VD12_SYN	P	7	VDD 1.2V for SYN
GND_SPS	P	14	Switching Regulator Ground

5.4. RF Interface

Table 4.   RF Interface

Symbol	Type	Pin No	Description
RXIN	I	5	RF RX Negative Signal
RXIP	I	4	RF RX Positive Signal
TXPA_ON	O	2	RF TX Negative Signal
TXPA_OP	O	1	RF TX Positive Signal

5.5. LED Interface

Table 5.   LED Interface

Symbol	Type	Pin No	Description
LED2	O	26	LED Pins (Active Low)
GPIO5	IO		Shared with GPIO5, can be selected by control register

5.6. Clock and Other Pins

Table 6.   Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	10	40MHz OSC Input
			Input of 40MHz Crystal Clock Reference
XO	O	9	Output of 40MHz Crystal Clock Reference
GPIO1	IO	29	Trap function: weak pull low to enable integrated switching regulator; weak pull high to enable integrated linear regulator .
			General Purpose Input/Output Pin
GPIO4	IO	28	General Purpose Input/Output Pin
GPIO5	IO	26	General Purpose Input/Output Pin
GPIO6	IO	32	TestModeSel, General Purpose Input/Output Pin,
GPIO7	IO	27	General Purpose Input/Output Pin

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 7.   Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. DC Characteristics

6.2.1.   Power Supply Characteristics

Table 8.   DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VD33A, VD33D	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
VD12A, VD12D	1.2V Core Supply Voltage	1.10	1.2	1.32	V
VD15A, VD15D	1.5V Supply Voltage	1.425	1.5	1.575	V
IDD33	3.3V Rating Current	-	-	600	mA

6.2.2.   Digital IO Pin DC Characteristics

Table 9.   3.3V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

Table 10. 2.8V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.8	2.8	3.1	V
V_{IL}	Input low voltage	--	0	0.8	V
V_{OH}	Output high voltage	2.5	--	3.1	V
V_{OL}	Output low voltage	0	--	0.28	V

<p align="center">Table 11. 1.8V GPIO DC Characteristics</p>

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.7	1.8	2.0	V
V_{IL}	Input low voltage	--	0	0.8	V
V_{OH}	Output high voltage	1.62	--	1.8	V
V_{OL}	Output low voltage	0	--	0.18	V

6.3. IO Characteristics

6.4. AC Characteristics

6.4.1. SDIO/GSPI Interface Characteristics

■ SDIO/GSPI Interface Timing
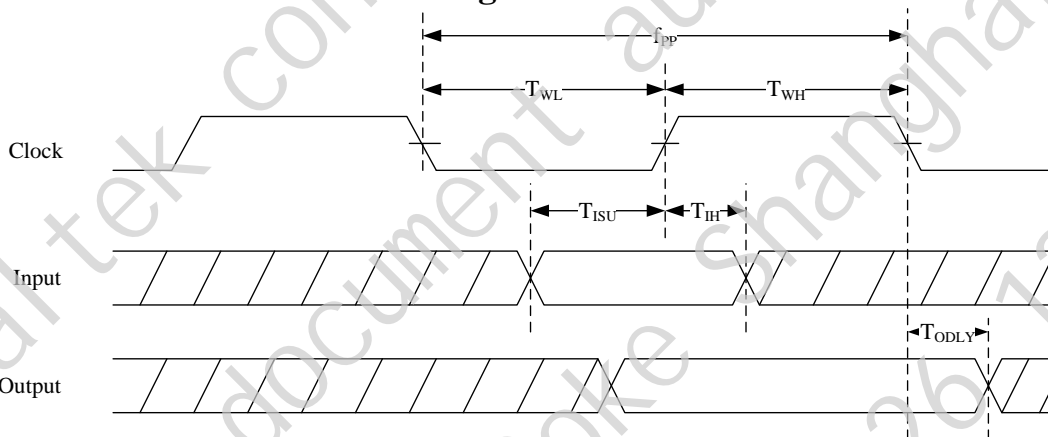
<p align="center">Figure 3. SDIO Interface Timing</p>

<p align="center">Table 12. SDIO Interface Timing Parameters</p>

NO	Parameter	Mode	MIN	MAX	Unit
f_{PP}	Clock frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock low time	DEF	10		ns
		HS	7		ns
T_{WH}	Clock high time	DEF	10		ns
		HS	7		ns
T_{ISU}	Input setup time	DEF	5		ns

|		HS	6		
T_{IH}	Input hold time	DEF	5		ns
		HS	2		
T_{ODLY}	Output delay time	DEF		14	ns
		HS		14	

■ SDIO/ GSPI Interface Signal Level

The SDIO and GSPI signal level ranges from 1.8V to 3.3V. The host shall provide the power source with targeting power level to RTL8189EM SDIO and GSPI interface via VIO_UART pin (pin # 50).

The DC characteristics of typical signal level, 3.3V/ 2.8V/ 1.8V are shown in section 6.3.2.

■ SDIO Interface Power On Sequence

After power on, the SDIO interface is selected by RTL8189EM automatically when a valid SDIO command is received. To attain better SDIO host compatibility, the following power on sequence is recommended:
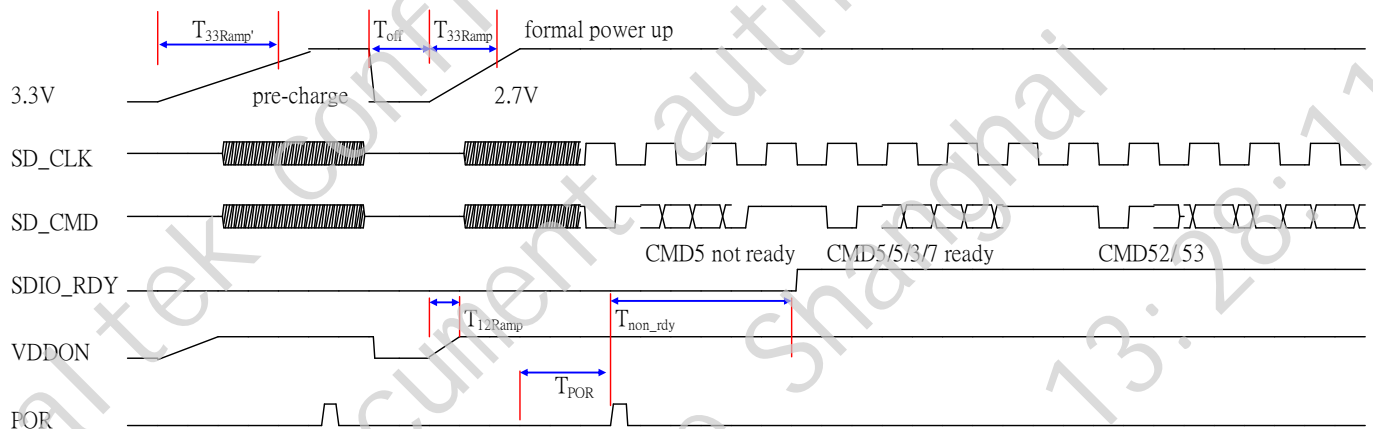
Variable definition:

T33ramp': The 3.3V power pre-charge ramp up duration before formal power up. It is recommended that a 3.3V power on and then power off sequence is executed by host controller before the formal power on sequence. This procedure can eliminate the host card detection issue when power ramp up duration is too long or the system warm reboot failure issue.

Toff : The duration the 3.3V is cut off before formal power up.

T33ramp: The 3.3V main power ramp up duration

T12ramp: The internal 1.2V ramp up duration.

T$_{POR}$: The duration the power on reset releases and power management unit executes power on tasks. The power on reset will detect both 3.3V and 1.2V power ramp up and after a predetermined duration.

T$_{non\_rdy}$: SDIO not ready duration, in this state, RTL8723AS may respond command without ready bit set. After ready bit set, host will initiate complete card detection procedure.

The power on flow description:

It is recommended that the card detection procedures are divided into two phases: a 3.3V power pre-charge phase and a formal power up phase.

For the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V is then cut off and is turned on after T$_{off}$ period. The ramp up time is specified by T$_{33ramp}$ duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit will be enabled by power ready detection circuit, and enables SDIO block. Efuse is then autoloaded to SDIO circuits during T$_{non\_rdy}$ duration. After autoload done, the SDIO responds command with ready bit set. After CMD5/ 5/ 3/ 7 procedures, the card detection is then executed. After driver loaded, normal command 52 and 53 are then used.

The typical timing spec is shown as follows:

Table 13. SDIO Interface Power On Timing Parameters

	Min	Typical	Max	Unit
T$_{33ramp}$'	--	--	No Limit	ms
T$_{off}$	250	500	1000	ms
T$_{33ramp}$	0.1	0.5	2.5	ms
T$_{12ramp}$	0.1	0.5	1.5	ms
T$_{por}$	2	2	8	ms
T$_{non-rdy}$	1	2	10	ms

■ **GSPI Interface Power On Sequence**

The GSPI interface is enabled automatically when a valid GSPI command is first received. The recommended power on sequence is as follows:
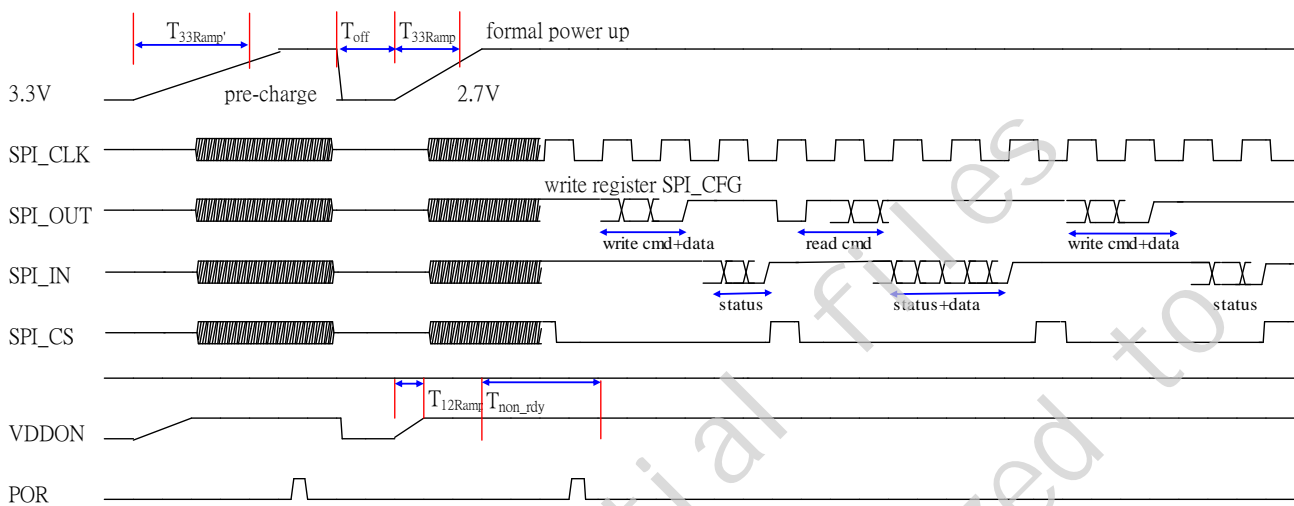
Variable definition:

T_{33ramp}`: The 3.3V power pre-charge ramp up duration before formal power up. It is recommended that a 3.3V power on and then power off sequence is executed by host controller before the formal power on sequence. This procedure can avoid the host card detection issue when power ramp up duration is too long or the system warm reboot failure.

T_{off} : The duration the 3.3V is cut off before formal power up.

T_{33ramp}: The 3.3V main power ramp up duration

T_{12ramp}: The internal 1.2V ramp up duration.

T_{non_rdy}: The duration SPI device internal initialization. After T_{non_rdy}, SPI host can then send command to write SPI_CFG register. SPI_CFG register is to control SPI endian and word length.

The power on flow description:

It is recommended that the card detection procedures are divided into two phases: a 3.3V power pre-charge phase and a formal power up phase.

For the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V is then cut off and is turned on after T_{off} period. The ramp up time is specified by T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit will be enabled by power ready detection circuit, and enables SPI block. Efuse is then autoloaded to SPI circuits, and the internal power circuits are configured during T_{non_rdy} duration.

The typical timing spec is shown as follows:

Table 14.   SPI Interface Power On Timing Parameters

	Min	Typical	Max	Unit
T_{33ramp}'	--	--	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
$T_{non-rdy}$	3	4	18	ms

7.   Mechanical Dimensions

TOP VIEW

BOTTOM VIEW
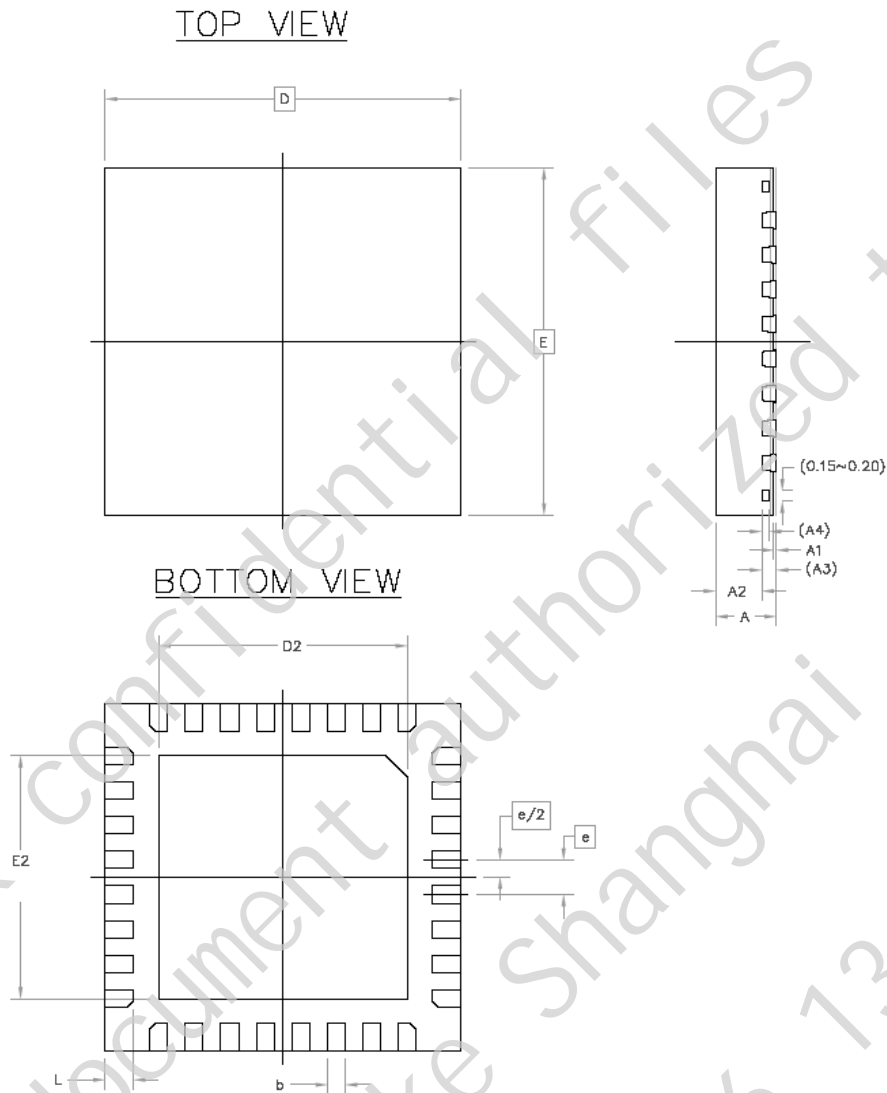
7.1.   Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
A4	0.10 REF			0.004 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	5.00 BSC			0.020 BSC		
D2/E2	3.25	3.50	3.75	0.128	0.138	0.148
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Note1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note2: REFERENCE DOCUMENT: JEDEC MO-220.

8. Ordering Information

Table 15. Ordering Information

Part Number	Package	Status
RTL8189EM-CG	QFN-32, 'Green' Package	Mass Production

Note: See page 6 for package identification.