RTL8192CE-GR

SINGLE-CHIP IEEE 802.11b/g/n 2T2R WLAN CONTROLLER w/PCI EXPRESS INTERFACE

DATASHEET

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This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2009/11/2	Preliminary release.

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1. General Description

The Realtek RTL8192CE is a highly integrated single-chip MIMO (Multiple In, Multiple Out) Wireless LAN (WLAN) solution for the wireless high throughput 802.11n specification. It combines a MAC, a 2T2R capable baseband, and RF in a single chip. The RTL8192CE provides a complete solution for a high throughput performance wireless client.

The RTL8192CE baseband implements Multiple Input, Multiple Output (MIMO) Orthogonal Frequency Division Multiplexing (OFDM) with 2 transmit and 2 receive paths (2T2R) and is compatible with the IEEE 802.11n specification. Features include two spatial streams transmission, short guard interval (GI) of 400ns, spatial spreading, and transmission over 20MHz and 40MHz bandwidth. Moreover, RTL8192CE provides one spatial stream space-time block code (STBC) to extend the range of transmission. At the receiver, extended range and good minimum sensitivity is achieved by having receiver diversity up to 2 antennas. As the recipient, the RTL8192CE also supports explicit sounding packet feedback that helps senders with beamforming capability. With 2 independent RF blocks, the RTL8192CE can perform fast roaming without link interruption.

For legacy compatibility, direct sequence spread spectrum (DSSS), complementary code keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available along with complementary code keying to provide the data rates of 1, 2, 5.5 and 11Mbps with long or short preamble. The high speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, and 64QAM modulation of the individual subcarriers and rate compatible punctured convolutional coding with coding rate of 1/2, 2/3, 3/4, and 5/6, provides the maximum data rate of 54Mbps and 300Mbps for IEEE 802.11g and 802.11n MIMO OFDM respectively.

The RTL8192CE builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate the severe multi-path effects and mutual interference in the reception of multiple streams. For better detection quality, receive diversity with maximal-ratio-combine (MRC) applying up to 2 receive paths are implemented. Robust interference detection and suppression are provided to protect against bluetooth, cordless phone, and microwave oven. Receive vector diversity for multi-stream application is implemented for efficient utilization of MIMO channel. Efficient IQ-imbalance, DC offset, phase noise, frequency offset and timing offset compensations are provided for the radio frequency front-end impairments. Selectable digital transmit and receiver FIR filters are provided to meet transmit spectrum mask requirements and to reject adjacent channel interference, respectively.

The RTL8192CE supports fast receiver automatic gain control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control function to obtain the better performance in the analog portions of the transceiver.

The RTL8192SCE MAC supports 802.11e for multimedia applications, 802.11i for security, and 802.11n for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as U-APSD, APSD, and MIMO power saving reduces the power wasted during idle time, and compensates for the extra power required to transmit MIMO OFDM. The RTL8192CE provides simple legacy and 20MHz/40MHz co-existence mechanisms to ensure backward and network compatibility.

2. Features

General

- 64-pin QFN
- CMOS MAC, Baseband MIMO PHY, and RF in a single chip for IEEE 802.11b/g/n compatible WLAN
- Complete 802.11n MIMO solution for 2.4GHz band
- 2x2 MIMO technology for extended reception robustness and exceptional throughput
- Maximum PHY data rate up to 150Mbps using 20MHz bandwidth, 300Mbps using 40MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating at 802.11n data rates

Host Interface

- Complies with PCI Express Base Specification Revision 1.1

Standards Supported

- IEEE 802.11e QoS Enhancement (WMM, WMM-SA Client mode)
- IEEE 802.11h TPC, Spectrum Measurement
- IEEE 802.11k Radio Resource Measurement
- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- Cisco Compatible Extensions (CCX) for WLAN devices

MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- MIMO power saving mechanism
- Channel management and co-existence
- Multiple BSSID feature allows the RTL8192CE to assume multiple MAC identities when used as a wireless bridge
- Supports Wake-On-WLAN via Magic Packet and Wake-up frame
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth

Peripheral Interfaces

- General Purpose Input/Output (10 pins)
- 4-wire EEPROM control interface (93C46)
- Three configurable LED pins
- Configurable Bluetooth Coexistence Interface

PHY Features

- IEEE 802.11n MIMO OFDM
- Two Transmit and Two Receive path (2T2R)

- 20MHz and 40MHz bandwidth transmission
- Short Guard Interval (400ns)
- One spatial stream STBC transmission for extended coverage
- Sounding packet
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 64QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g and 300Mbps in 802.11n
- OFDM receive diversity with MRC using up to 2 receive paths. Switch diversity used for DSSS/CCK.
- Hardware antenna diversity
- Selectable digital transmit and receiver FIR filters
- Programmable scaling in transmitter and receiver to trade quantization noise against increased probability of clipping
- Fast receiver Automatic Gain Control (AGC).
- On-chip ADC and DAC

3. Application Diagrams

3.1. 11n Compatible Single-Band 2x2 RF Application

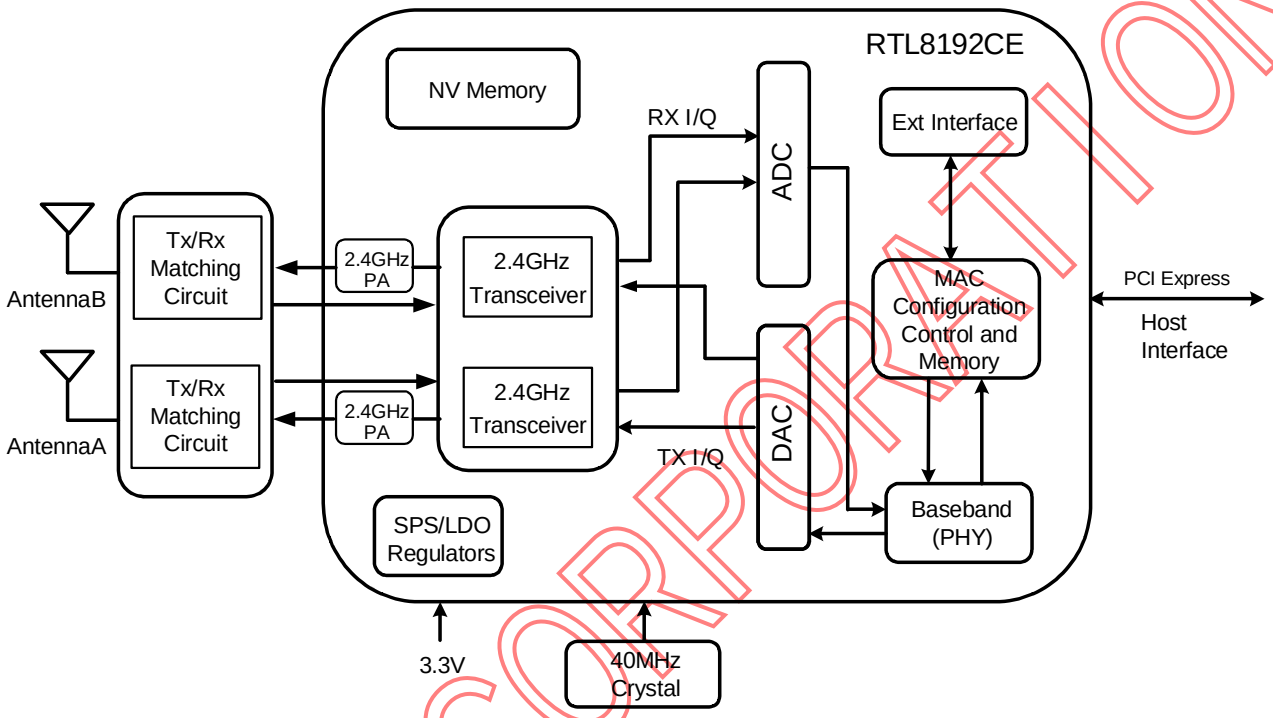


Figure 1. 11n Compatible Single-Band 2x2 Solution—RTL8192CE-GR (11n 2x2 MAC/BB/RF + 2 PAs)

4. Pin Assignments

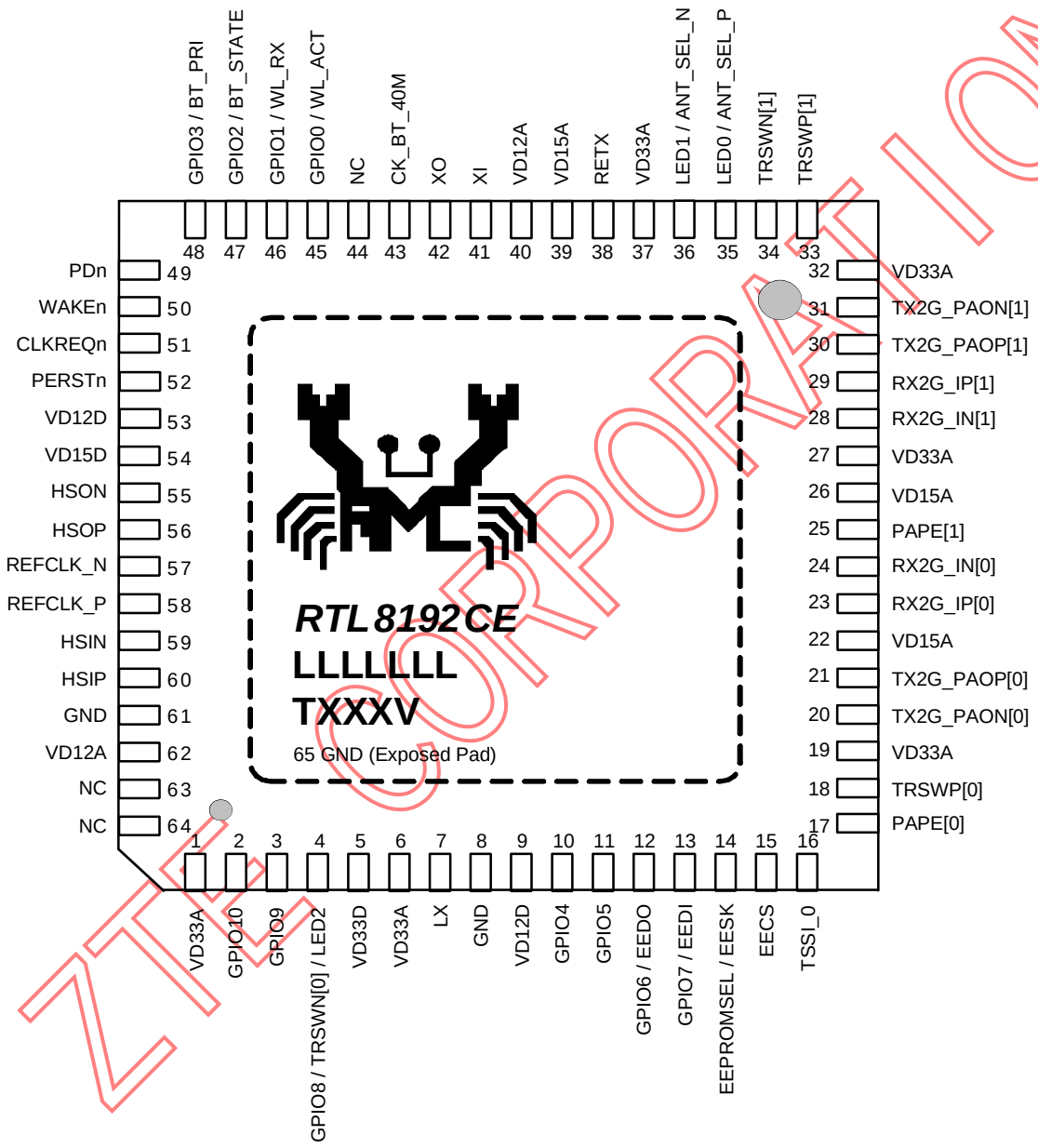


Figure 2. Pin Assignments

4.1. Package Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 2.

5. Pin Descriptions

The following signal type codes are used in the tables:

I: Input

O: Output

T/S: Tri-State bi-directional input/output pin

S/T/S: Sustained Tri-State

O/D: Open Drain

P: Power pin

5.1. PCI Express Transceiver Interface

Table 1. PCI Express Transceiver Interface

Symbol	Type	Pin No	Description
HSIN/HSIP	I	59/60	PCI Express Receive Differential Pair
HSON/HSOP	O	55/56	PCI Express Transmit Differential Pair
REFCLK_P/REFCLK_N	I	57/58	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm
CLKREQn	O	51	Reference Clock Request Signal This signal is used by the RTL8192CE-GR to request starting of the PCI Express reference clock
WAKEn	O/D	50	Power Management Event: Open drain, active low Used to reactivate the PCI Express slot's main power rails and reference clocks.
PERSTn	I	52	PCI Express Reset Signal: Active low When the PERSTB is asserted at power-on state, the RTL8192CE-GR returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.

5.2. EEPROM Interface

Table 2. EEPROM Interface

Symbol	Type	Pin No	Description
EESK	O	14	EESK in 93C46 Programming or Auto-Load Mode
EEDI	O	13	EEDI in 93C46 Programming or Auto-Load Mode
EEDO	IO	12	EEDO in 93C46 Programming or Auto-Load Mode
EECS	O	15	EEPROM Chip Select

5.3. Power Pins

Table 3. Power Pins

Symbol	Type	Pin No	Description
LX	P	7	Switching Regulator Output
VD33A	P	1, 6, 19, 27, 32, 37	VDD 3.3V for Analog
VD33D	P	5	VDD 3.3V for Digital
VD15A	P	22, 26, 39	VDD 1.5V for Analog
VD15D	P	54	VDD 1.5V for Digital
VD12A	P	40,62	Analog 1.2V Regulator Output
VD12D	P	9, 53	Digital 1.2V Regulator Output
GND	P	8, 61	Ground
REXT	P	38	24k (1%) Precision Resistor for Bandgap

5.4. RF Interface

Table 4. RF Interface

Symbol	Type	Pin No	Description
TRSWN[0]	O	4	Transmit/Receive Path Select 0 Shared with LED2, can be selected by control register
PAPE[0]	O	17	2.4GHz Transmit Power Amplifier Power Enable 0
TRSWP[0]	O	18	Transmit/Receive Path Select 0
TX2G_ON[0]	O	20	RF TX0 Negative Signal
TX2G_OP[0]	O	21	RF TX0 Positive Signal
RX2G_IP[0]	I	23	RF RX0 Positive Signal
RX2G_IN[0]	I	24	RF RX0 Negative Signal
PAPE[1]	O	25	2.4GHz Transmit Power Amplifier Power Enable 1
RX2G_IN[1]	I	28	RF RX1 Negative Signal
RX2G_IP[1]	I	29	RF RX1 Positive Signal
TX2G_OP[1]	O	30	RF TX1 Positive Signal
TX2G_ON[1]	O	31	RF TX1 Negative Signal
TRSWP[1]	O	33	Transmit/Receive Path Select 1
TRSWN[1]	O	34	Transmit/Receive Path Select 1
ANT_SEL_P	O	35	Antenna Control Positive Signal Shared with LED0, can be selected by control register
ANT_SEL_N	O	36	Antenna Control Negative Signal Shared with LED1, can be selected by control register

5.5. LED Interface

Table 5. LED Interface

Symbol	Type	Pin No	Description
LED0	O	35	LED Pins (Active Low) Shared with ANT_SEL_P, can be selected by control register
LED1	O	36	LED Pins (Active Low) Shared with ANT_SEL_N, can be selected by control register
LED2	O	4	LED Pins (Active Low) Shared with TRSWN[0] or GPIO8, can be selected by control register

5.6. Clock and Other Pins

Table 6. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	41	40MHz OSC Input Input of 40MHz Crystal clock reference
XO	O	42	Output of 40MHz Crystal Clock Reference
CK_BT_40M	O	43	Buffered 40M clock outputs for other peripheral IC
PDn	I	49	This Pin can Externally Shutdown RTL8192CE without Extra Power Switch This pin can also support WLAN Radio off function with host interface remaining connected.
EEPROMSEL/EESK	I	14	Trap function: Weakly pull high at power on to indicate the presence of external EEPROM. 1: external EEPROM, 0: internal eFuse. EEPROM Interface EESK Signal
GPIO0/WLAN_ACT	IO	45	General Purpose Input/Output Pin or Bluetooth Coexistence WLAN_ACT Pin The WLAN_ACT signal indicates when WLAN is either transmitting or receiving in the 2.4GHz ISM band.
GPIO1/WLAN_RX	IO	46	Trap Function: Weakly pull high at power on to turn on CK_BT_40M. General Purpose Input/Output Pin or Bluetooth Coexistence WLAN_RX Pin WLAN_RX is an indicator for wireless LAN RX activity.
GPIO2/BT_STATE	IO	47	General Purpose Input/Output Pin or Bluetooth Coexistence BT_STAT Pin The BTSTAT signal indicates when normal Bluetooth packets are being transmitted or received.
GPIO3/BT_PRI	IO	48	General Purpose Input/Output Pin or Bluetooth Coexistence BT_PRI Pin The BTPRI signal indicates when a high priority Bluetooth packet is being transmitted or received.
GPIO4	IO	10	General Purpose Input/Output Pin
GPIO5	IO	11	General Purpose Input/Output Pin
GPIO6/EEDO	IO	12	General Purpose Input/Output Pin or EEPROM Interface EEDO Signal
GPIO7/EEDI	IO	13	General Purpose Input/Output Pin or EEPROM Interface EEDI Signal
GPIO8/TRSWN[0]/LED2	IO	4	General Purpose Input/Output Pin or RF TX/RX path select or LED2.
GPIO9	IO	3	General Purpose Input/Output Pin
GPIO10	IO	2	General Purpose Input/Output Pin

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 7. Temperature Limit Ratings

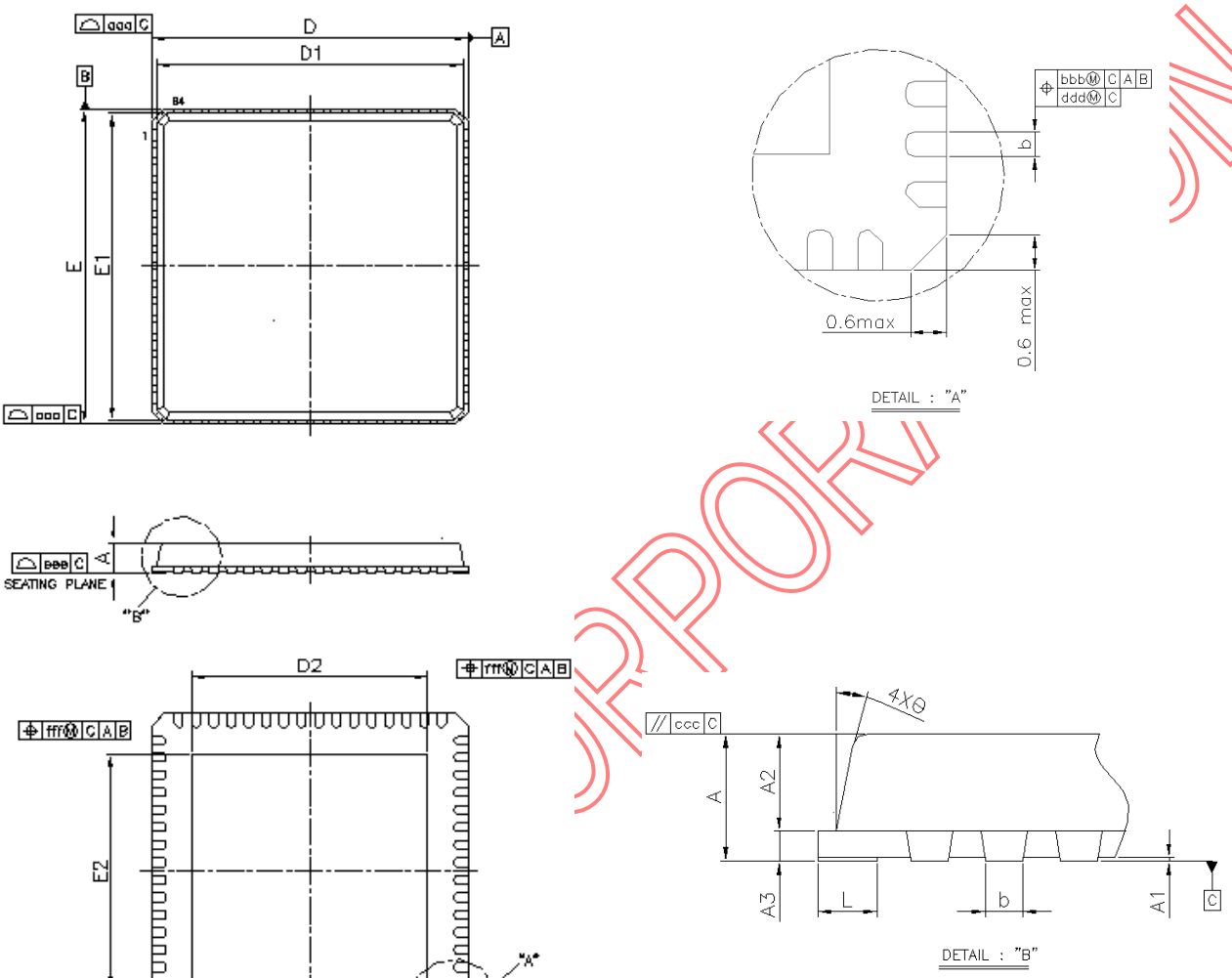
Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. DC Characteristics

Table 8. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VDD33	3.3V I/O Supply Voltage	3.135	3.3	3.465	V
VDD12	1.2V Core Supply Voltage	1.10	1.2	1.32	V
VDD15	1.5V Supply Voltage	1.425	1.5	1.575	V
IDD33	3.3V Rating Current			800	mA

7. Mechanical Dimensions



7.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.55	0.65	0.80	0.022	0.026	0.032
A_3		0.20REF			0.008REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E		9.00BSC			0.354BSC	
D_1/E_1		8.75BSC			0.344BSC	
D2/E2	5.25	5.5	5.75	0.206	0.216	0.226
e		0.50BSC			0.020BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	-	14°	0°	-	14°
aaa	-	-	0.15	-	-	0.006
bbb	-	-	0.10	-	-	0.004
ccc	-	-	0.10	-	-	0.004
ddd	-	-	0.05	-	-	0.002
eee	-	-	0.08	-	-	0.003
fff	-	-	0.10	-	-	0.004

Note1: DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
Note2: CONTROLLING DIMENSION: MILLIMETER (mm).
Note3: REFERENCE DOCUMENTL: JEDEC MO-220.

8. Ordering Information

Table 9. Ordering Information

Part Number	Package	Status
RTL8192CE-GR	QFN-64, 'Green' Package	Engineering Sample

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