RTL8192ES-CG

SINGLE-CHIP 802.11b/g/n 2T2R WLAN with SDIO INTERFACE

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2012/12/14	Preliminary release
0.2	2013/11/14	Update Power On Sequence
0.3	2015/10/13	Update SDIO clock spec
0.31	2015/12/28	SDIO clock rate to support 85MHz

Table of Contents

List of Tables

List of Figures

1. General Description

The Realtek RTL8192ES is a highly integrated single-chip 802.11n Wireless LAN (WLAN) network controller with SDIO interface (SDIO 1.1/ 2.0/ 3.0 compliant). It combines a WLAN MAC, a 2T2R capable WLAN baseband, and WLAN RF in a single chip. The RTL8192ES provides a complete solution for a high throughput performance integrated wireless LAN device.

The RTL8192ES WLAN baseband implements Orthogonal Frequency Division Multiplexing (OFDM) with 2 transmit and 2 receive paths and is compatible with the 802.11n specification. It features two spatial stream transmission, short guard interval (GI) of 400ns, spatial spreading, and transmission over 20MHz and 40MHz bandwidth.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all 802.11b and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available, and CCK provides support for legacy data rates, with long or short preamble. The high-speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, and 64QAM modulation of the individual subcarriers and rate compatible punctured convolutional coding with coding rate of 1/2, 2/3, 3/4, and 5/6, provide higher data rates of 54Mbps and 150Mbps for 802.11g and 802.11n OFDM respectively.

The RTL8192ES WLAN Controller builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference.

Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end. Selectable digital transmit and receive FIR filters are provided to meet transmit spectrum mask requirements and to reject adjacent channel interference, respectively.

The RTL8192ES WLAN Controller supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control function to obtain the better performance in the analog portions of the transceiver.

The RTL8192ES WLAN MAC supports 802.11e for multimedia applications, 802.11i for security, and 802.11n for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, and U-APSD, reduce the power wasted during idle time, and compensates for the extra power required to transmit OFDM. The RTL8192ES provides simple legacy and 20MHz/40MHz co-existence mechanisms to ensure backward and network compatibility.

2. Features

General

- 56-pin QFN
- CMOS MAC, Baseband MIMO PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Complete 802.11n MIMO solution for 2.4GHz band
- 2x2 MIMO technology for extended reception robustness and exceptional throughput
- Maximum PHY data rate up to 144.4Mbps using 20MHz bandwidth, 300Mbps using 40MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating at 802.11n data rates

Host Interface

- Complies with SDIO 1.1/ 2.0/ 3.0 for WLAN with clock rate up to 85MHz
- GSPI interface for configurable endian for WLAN

Standards Supported

- 802.11b/g/n compatible WLAN
- 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services

WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- MIMO power saving mechanism
- Channel management and co-existence
- Multiple BSSID feature allows the RTL8192ES to emulate multiple MAC identities when used as a wireless bridge
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth

Peripheral Interfaces

- General Purpose Input/Output (11 pins)
- Three configurable LED pins
- Configurable Bluetooth Coexistence Interface

PHY Features

- 802.11n MIMO OFDM
- Two Transmit and Two Receive path (2T2R)
- 20MHz and 40MHz bandwidth transmission

- Short Guard Interval (400ns)
- Sounding packet
- Low Density Parity Check (LDPC) to enhance link robustness over range
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 64QAM modulation.
  Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g and 300Mbps in 802.11n
- OFDM receive diversity with MRC using up to 2 receive paths. Switch diversity used for DSSS/CCK.
- Hardware antenna diversity
- Selectable digital transmit and receive FIR filters
- Programmable scaling in transmitter and receiver to trade quantization noise against increased probability of clipping
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC

3. Application Diagram

3.1. Single-Band 11n 2x2 MAC/BB/RF Application

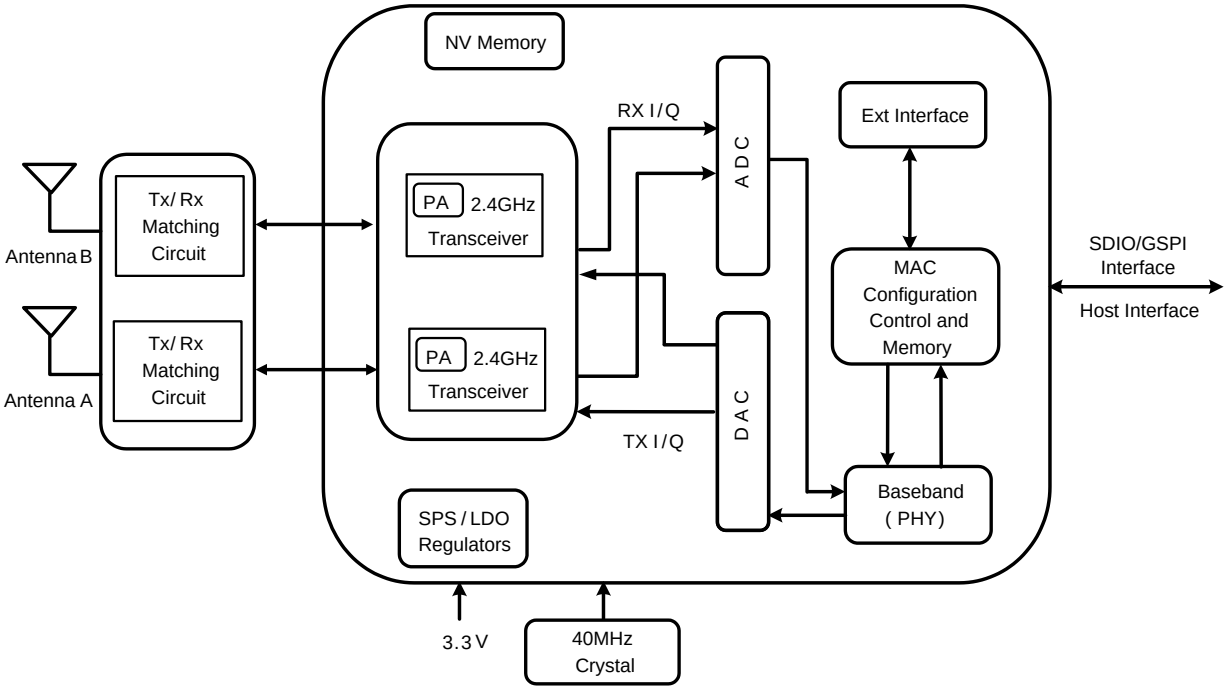


Figure 1. Single-Band 11n (2x2) Solution

4. Pin Assignments

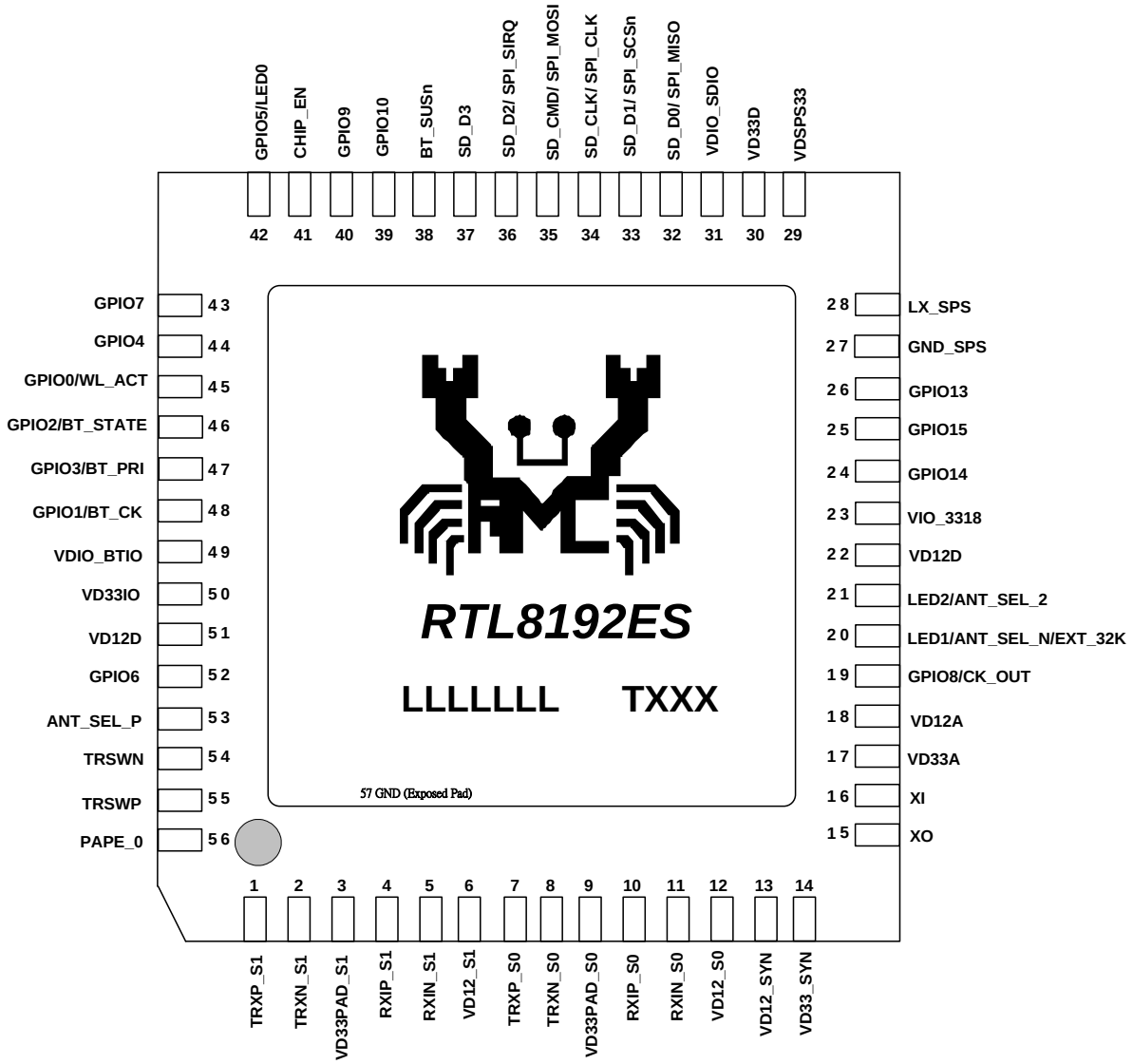


Figure 2. Pin Assignments

4.1. Package Identification

'Green' package is indicated by a 'G' in the location marked 'T' in in

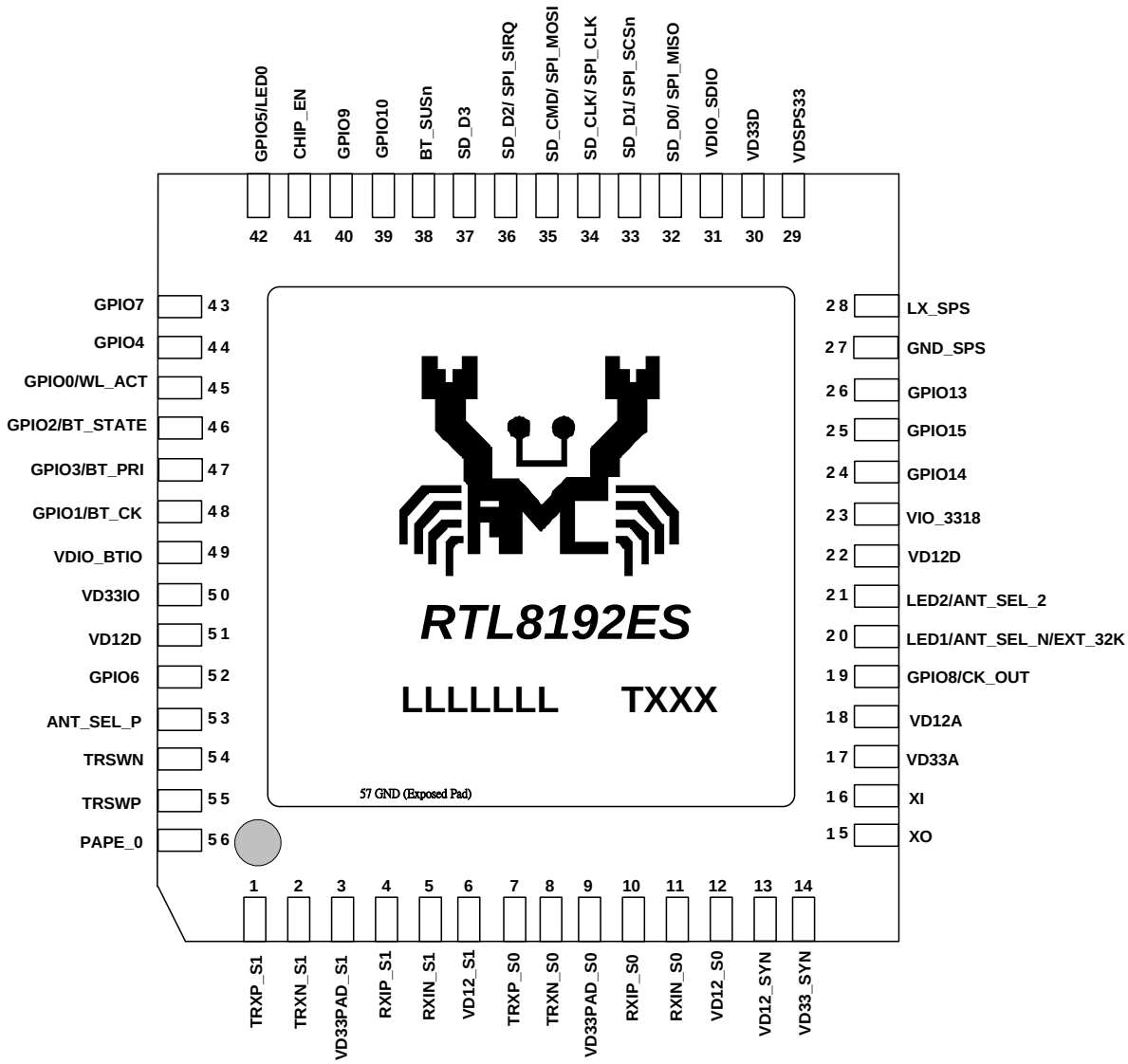


Figure 2. 2.

5. Pin Descriptions

The following signal type codes are used in the tables:

I: Input O: Output

T/S: Tri-State bi-directional input/output pin S/T/S: Sustained Tri-State

O/D: Open Drain P: Power pin

5.1. SDIO Interface

Table 1. SDIO Interface

Symbol	Type	Pin No	Description
SD_CLK	I	34	SDIO Clock Input
SD_CMD	I/O	35	SDIO Command Input
SD_D0	I/O	32	SDIO Data Line 0
SD_D1	I/O	33	SDIO Data Line 1
SD_D2	I/O	36	SDIO Data Line 2
SD_D3	I/O	37	SDIO Data Line 3

The SDIO interface selection can be referred to subsection 6.5.1, “SDIO Power on Sequence”. The signal level section of SDIO interface selection can be referred to subsection 6.5.1, “SDIO/GSPI Signal Level”.

5.2. GSPI Interface

Table 2. GSPI Interface

Symbol	Type	Pin No	Description
SPI_CLK	I	34	GSPI Clock Input
SPI_MOSI	I	35	GSPI Data Input
SPI_MISO	O	32	GSPI Data Out
SPI_SIRQ	O	36	GSPI Interrupt
SPI_SCSn	I	33	GSPI Chip Select Bar

The GSPI interface pins are shared with SDIO interface. The GSPI interface selection can be referred to subsection 6.5.1, “GSPI Power on Sequence”. The signal level section of SDIO interface selection can be referred to subsection 6.5.1, “SDIO/GSPI Signal Level”.

5.3. Power Pins

Table 3. Power Pins

Symbol	Type	Pin No	Description
LX_SPS	P	28	Switching Regulator Output
VDSPS33	P	29	Switching Regulator Input Or Linear Regulator output from 3.3V to 1.2V input
VD33A	P	17	VDD 3.3V for Analog
VD33PAD_S1, VD33PAD_S0	P	3, 9	3.3V for WLAN PA driver
VD33_SYN	P	14	3.3V for WLAN synthesizer

Symbol	Type	Pin No	Description
VD33IO	P	50	other pins power
VIO_3318	P	23	pin 38~41, pin24~26 power
VDIO_SDIO	P	31	SDIO IO Power
VD33D	P	30	Always on power souce pin
VDIO_BTIO	P	49	pin 42~48 power
VD12A	P	18	AFE power pin
VD12D	P	22,51	WLMAC digital power pin
VD12_S0, VD12_S1		12, 6	RF power pin
GND	P	57	
GND_SPS	P	57	Switching Regulator Ground

5.4. RF Interface

Table 4. RF Interface

Symbol	Type	Pin No	Description
TRSWN	O	54	Transmit/Receive Signal
TRSWP	O	55	Transmit/Receive Signal
PAPE_0	O	56	2.4GHz Transmit Power Amplifier Power Enable 0
TRXP_S0	O	7	RF TX_S0 Negative Signal
TRXN_S0	O	8	RF TX_S0 Positive Signal
RXIP_S0	I	10	RF RX_S0 Positive Signal
RXIN_S0	I	11	RF RX_S0 Negative Signal
TRXP_S1	O	1	RF TX_S1 Negative Signal
TRXN_S1	O	2	RF TX_S1 Positive Signal
RXIP_S1	I	4	RF RX_S1 Positive Signal
RXIN_S1	I	5	RF RX_S1 Negative Signal
ANT_SEL_P	O	53	Antenna Control Positive Signal
ANT_SEL_N	O	20	Antenna Control Negative Signal Shared with LED1, can be selected by control register
ANT_SEL_2	O	21	Antenna Control Extend Signal Shared with LED2, can be selected by control register

5.5. PTA Interface

Table 5. PTA Interface

Symbol	Type	Pin No	Description
WL_ACT	IO	45	Bluetooth Coexistence WL_ACT Pin The WL_ACT signal indicates when the WLAN is either transmitting or receiving in the 2.4GHz ISM band. Shared with GPIO0 , can be selected by control register

Symbol	Type	Pin No	Description
BT_STATE	IO	46	Bluetooth Coexistence BT_STAT Pin. The BTSTAT signal indicates when normal Bluetooth packets are being transmitted or received. Shared with GPIO2, can be selected by control register
BT_PRI	IO	47	Bluetooth Coexistence BT_PRI Pin. The BT_PRI signal indicates when a high priority Bluetooth packet is being transmitted or received. Shared with GPIO3, can be selected by control register

5.6. LED Interface

Table 6. LED Interface

Symbol	Type	Pin No	Description
LED0	O	42	LED Pins (Active Low) Shared with GPIO5, can be selected by control register
LED1	O	20	LED Pins (Active Low) Shared with ANT_SEL_N, can be selected by control register
LED2	O	21	LED Pins (Active Low) Shared with ANT_SEL_2, can be selected by control register

5.7. Clock and Other Pins

Table 7. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	16	Oscillator Input (default:40Mhz) Input of Crystal clock reference
XO	O	15	Output of Crystal Clock Reference
CHIP_EN	I	41	This Pin can Externally Shutdown RTL8192ES without Extra Power Switch
GPIO0 /WL_ACT	IO	45	General Purpose Input/Output Pin Shared with ANT_SEL_4 and WL_ACT, can be selected by control register
GPIO1/BT_CK	IO	48	Trap Function: Decide to use the SWR or LDO for 3.3V -> 1.2V by this pin power on latch low or high. LDO_SPS_SEL = 0, use SWR LDO_SPS_SEL = 1, use LDO General Purpose Input/Output Pin.
GPIO2/ BT_STATE	IO	46	General Purpose Input/Output Pin Shared with ANT_SEL_5 and BT_STA, can be selected by control register
GPIO3/ BT_PRI	IO	47	General Purpose Input/Output Pin Shared with ANT_SEL_6 and BT_PRI, can be selected by control register
GPIO4	IO	44	General Purpose Input/Output Pin
GPIO5/LED0	IO	42	General Purpose Input/Output Pin Shared with LED0, can be selected by control register
GPIO6	IO	52	Trap Function: Decide to enter chip normal mode, if the GPIO is not used, please leave it open.(default: internal pull down) General Purpose Input/Output Pin.
GPIO7	IO	43	This pin can also support WLAN Radio off function with host interface remaining connected.
GPIO8/CK_OUT	IO	19	General Purpose Input/Output Pin Shared with ANT_SEL_3, can be selected by control register
GPIO9	IO	40	Trap Function: With GPIO12 to decide clock source for chip to option 40Mhz,25MhzGeneral Purpose Input/Output Pin
GPIO10	IO	39	General Purpose Input/Output Pin

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 8. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. DC Characteristics

6.2.1. Power Supply Characteristics

Table 9. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VD33A, VD33PAD_S0, VD33PAD_S0, VD33_SYN, VD33IO	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
VD12A, VD12D, VD12_S0, VD12_S1	1.2V Core Supply Voltage	1.10	1.2	1.32	V
VIO_3318, VDIO_SDIO	IO Power SDIO IO Power	3.0 for 3.3V case 1.65 for 1.8V case	3.3 or 1.8	3.6 for 3.3V case 1.95 for 1.8V case	V
IDD33	3.3V Rating Current	-	-	600	mA

6.2.2. Digital IO Pin DC Characteristics

Table 10. 3.3V GPIO DC Characteristics

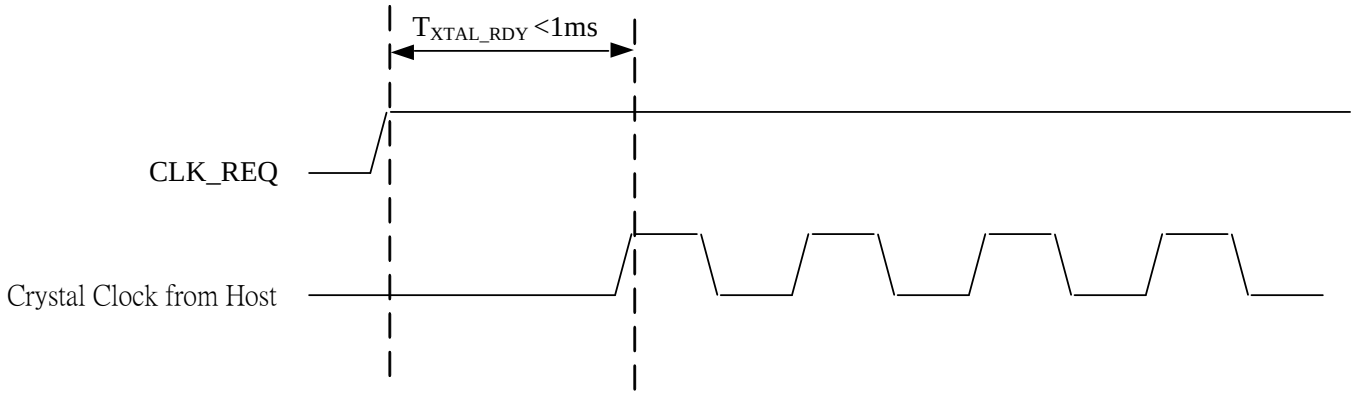
Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

Table 11. 1.8V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.7	1.8	2.0	V
V_{IL}	Input low voltage	--	0	0.8	V
V_{OH}	Output high voltage	1.62	--	1.8	V
V_{OL}	Output low voltage	0	--	0.18	V

6.3. IO Characteristics

6.4. CLK_REQ Timing



6.5. AC Characteristics

6.5.1. SDIO/GSPI Interface Characteristics

SDIO/GSPI Interface Timing

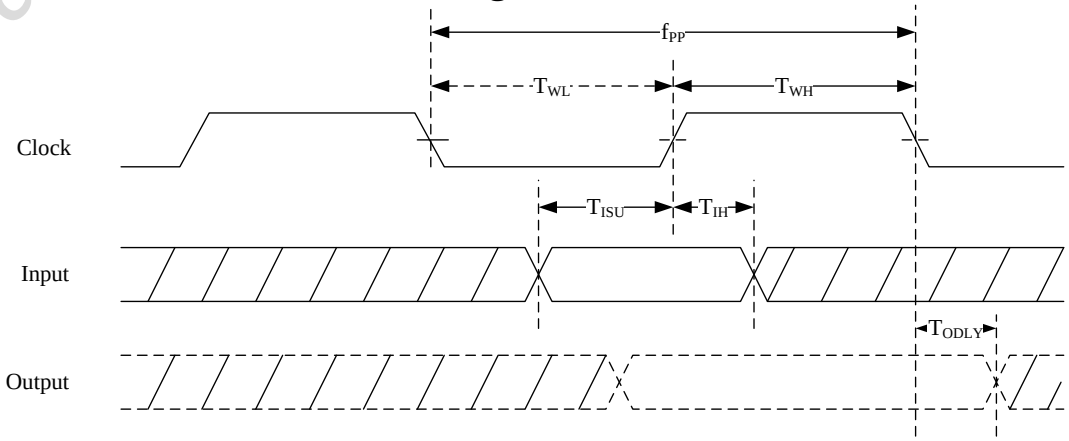


Figure 2. SDIO Interface Timing(SDIO2.0)

Table 122.SDIO 2.0 Interface Timing Parameters(Default Speed and High Speed)

NO	Parameter	Mode	MIN	MAX	Unit
f_{PP}	Clock frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock low time	DEF	10		ns
		HS	7		ns
T_{WH}	Clock high time	DEF	10		ns
		HS	7		
T_{ISU}	Input setup time	DEF	5		ns
		HS	6		
T_{IH}	Input hold time	DEF	5		ns
		HS	2		
T_{ODLY}	Output delay time	DEF		14	ns
		HS		14	

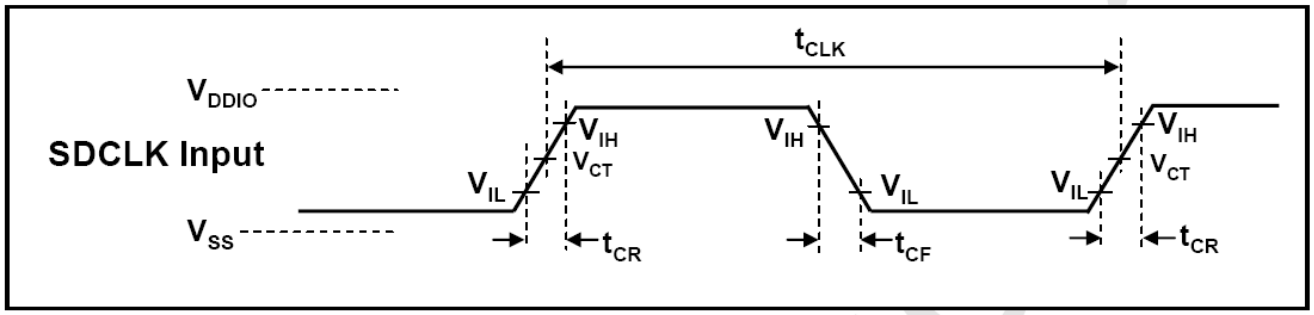


Figure 3. SDIO Interface Timing(SDIO3.0)

Table 13. SDIO 3.0 Interface Timing Parameters(SDR12, SDR25)

NO	Parameter	Mode	MIN	MAX	Unit
f_{PP}	Clock frequency = 1/Tclk	SDR12		25	MHz
		SDR25		50	MHz
Tcr/Tcf	Clock Rise time/Clock fall time	SDR12		8	ns
		SDR25		4	ns
Vct	Voltage Clock Threshold	SDR12/SDR25	0.975	0.975	V

For more detailed timing criteria, please check “SD specifications Part1 Physical Layer Specification Version 3.01”

■ SDIO/ GSPI Interface Signal Level

The SDIO and GSPI signal level ranges from 1.8V to 3.3V. The host shall provide the power source with targeting power level to RTL8192ES SDIO and GSPI interface via VDIO_SDIO pin (pin # 31).

The DC characteristics of typical signal level, 3.3V/ 2.8V/ 1.8V for SDIO2.0, 1.8V for SDIO3.0.

SDIO Interface Power On Sequence

After power on, the SDIO interface is selected by RTL8192ES automatically when a valid SDIO command is received. To attain better SDIO host compatibility, the following power on sequence is recommended:

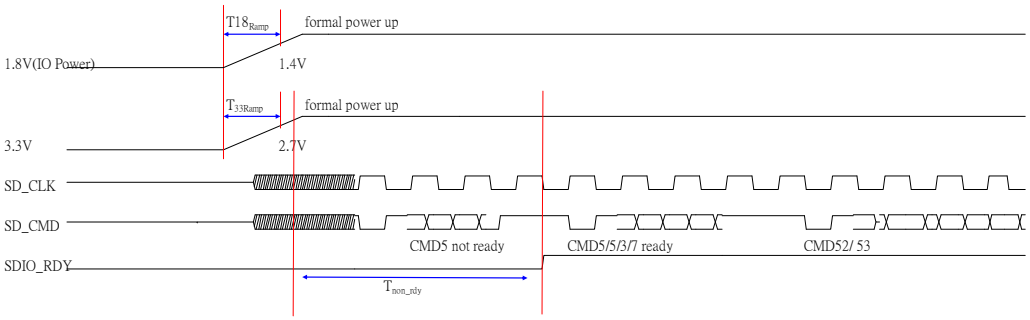


Figure 4. SDIO Interface Power On Sequence

Variable definition:

T33ramp: The 3.3V main power ramp up duration

T_{non_rdy}: SDIO not ready duration, in this state, RTL8192ES may respond command without ready bit set. After ready bit set, host will initiate complete card detection procedure.

T18ramp: The 1.8V main power ramp up duration.

The power on flow description:

The ramp up time is specified by T_{33ramp} duration.

After main 3.3V ramp up, the power management unit will be enabled by power ready detection circuit, and enables SDIO block. Efuse is then autoloaded to SDIO circuits during T_{non_rdy} duration. After autoload done, the SDIO responds command with ready bit set. After CMD5/ 5/ 3/ 7 procedures, the card detection is then executed. After driver loaded, normal command 52 and 53 are then used.

The typical timing spec is shown as follows:

Table 144.SDIO Interface Power On Timing Parameters

	Min	Typical	Max	Unit
T_{33ramp}	0.1	0.5	2.5	ms
T_{18ramp}	0.1	0.5	2.5	ms
$T_{non\text{-}rdy}$	1	2	10	ms

■ GSPI Interface Power On Sequence

The GSPI interface is enabled automatically when a valid GSPI command is first received. The recommended power on sequence is as follows:

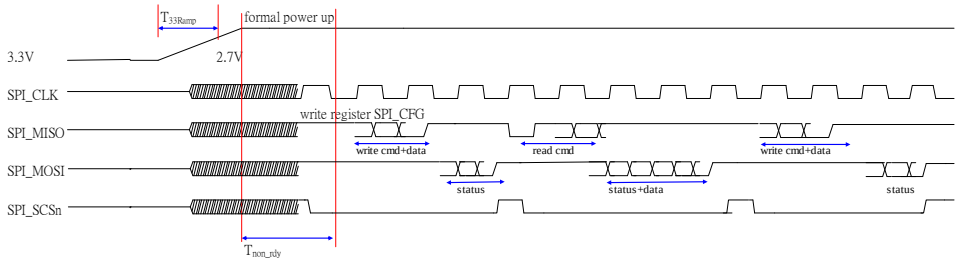


Figure 5. GPSI Interface Power On Sequence

Variable definition:

T_{33ramp}: The 3.3V main power ramp up duration

T_{non_rdy}: The duration SPI device internal initialization. After T_{non_rdy}, SPI host can then send command to write SPI_CFG register. SPI_CFG register is to control SPI endian and word length.

The power on flow description:

The ramp up time is specified by T_{33ramp} duration.

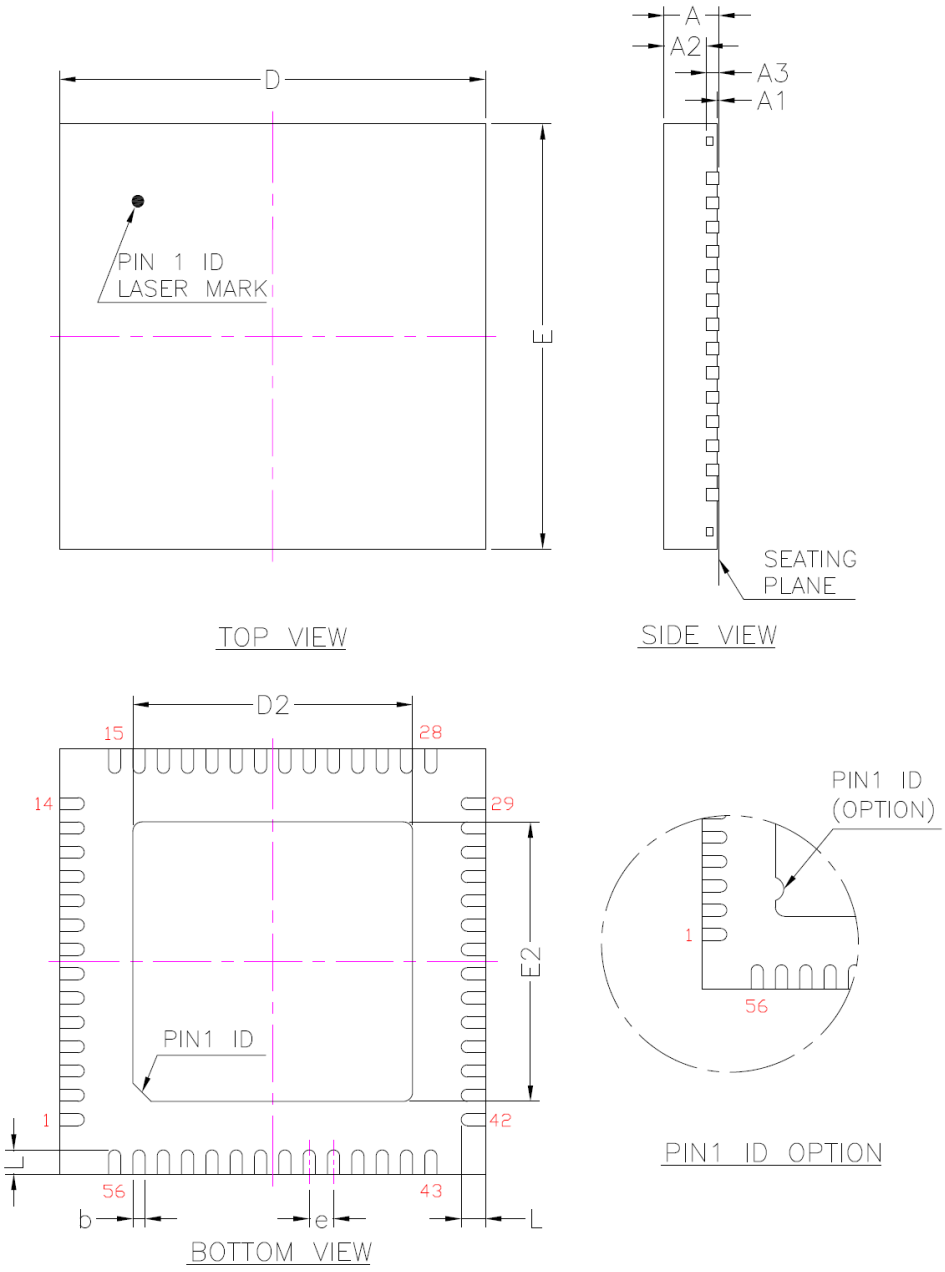
After main 3.3V ramp up, the power management unit will be enabled by power ready detection circuit, and enables SPI block. Efuse is then autoloaded to SPI circuits, and the internal power circuits are configured during T_{non_rdy} duration.

The typical timing spec is shown as follows:

Table 155.SPI Interface Power On Timing Parameters

	Min	Typical	Max	Unit
T_{33ramp}	0.1	0.5	2.5	ms
$T_{non-rdy}$	3	4	18	ms

Mechanical Dimensions



7.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	---	0.65	0.70	---	0.026	0.028
A_3	0.2 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	7.00 BSC			0.276 BSC		
D_2/E_2	4.35	4.60	4.85	0.171	0.181	0.191
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

8. Ordering Information

Table 166.Ordering Information

Part Number	Package	Status
RTL8192ES-CG	QFN56, 'Green' Package	Engineering Sample

Note: See page 7 for package identification.

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