NOT FOR PUBLIC RELEASE

RTL8198-GR

IEEE 802.11n GIGABIT ETHERNET AP/ROUTER NETWORK PROCESSOR

PRELIMINARY DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 0.91
02 August 2010
Track ID: JATR-2265-11

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

COPYRIGHT

DISCLAIMER

Realtek provides this document “as is”, without warranty of any kind. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

USING THIS DOCUMENT

This document provides detailed user guidelines to achieve the best performance when implementing the Realtek 11n AP/Routers.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.8	2010/02/26	Preliminary release.
0.9	2010/05/27	Revised section 9 Non-Flash Booting Interface (NFBI), page 38.
0.91	2010/08/02	Removed NOR Flash type support. Revised Table 52 Total Power Consumption, page 47. Revised section 11.2.3.1 Serial Flash Interface Output Timing, page 62. Added section 11.2.3.2 Serial Flash Interface Intput Timing, page 62.

Table of Contents

List of Tables

List of Figures

1. General Description

The RTL8198 is an integrated System-on-a-Chip (SoC) Application Specific Integrated Circuit (ASIC) that implements a L2 switch, L3 routing, and L4 NAT functions. An RLX5281 CPU is embedded and the clock rate can be up to 500MHz. To improve computational performance, a 16-Kbyte I-Cache, 8-Kbyte D-Cache, 40-K I-MEM, and 8-Kbyte D-MEM are provided. A standard 5-signal P1149.1 compliant EJTAG test interface is supported for CPU testing and software development.

Via table configuration and look-up, the RTL8198 can perform hard-wired network traffic forwarding. The CPU may be used to handle upper layer functions, such as DHCP, HTTP, and some other protocols, and to operate with a hard-wired forwarding engine.

The RTL8198 provides six ports (from port 0 to port 5), integrated with six Gigabit Ethernet MACs and five physical layer transceivers for 10Base-T, 100Base-TX, and 1000Base-TX. Each port of the RTL8198 may be configured as a LAN or WAN port. Port 5 supports an external MAC interface that could be an GMII/RGMII/MII interface type to work with an external MAC or PHY transceiver.

The RTL8198 supports flexible IEEE 802.3x full-duplex flow control and optional half-duplex backpressure control. For full-duplex, standard IEEE 803.3x flow control will enable pause ability only when both sides of UTP have auto-negotiation ability and have enabled pause ability. The RTL8198 also provides optional forced mode IEEE 802.3x full-duplex flow control. Based on optimized packet memory management, the RTL8198 is capable of Head-Of-Line blocking prevention.

Due to its powerful protocol parser, the RTL8198 can recognize and hard-wire-forward VLAN-tagged, SNAP/LLC, PPPoE, IP, TCP, UDP, ICMP, IGMP, and PPTP packets. Layer 2, 3, and 4 information is stored in look-up tables. For VLAN and PPPoE protocols, the RTL8198 can automatically encapsulate and decapsulate VLAN tagged frames and PPPoE headers.

L2 Switch Features: The RTL8198 contains a 1024-entry address look-up table with a 10-bit 4-way XOR hashing algorithm for address searching and learning. Auto-aging of each entry is provided and the aging time is around 200~300 seconds.

The RTL8198 supports port-based, protocol-based, and tagged VLANs. Up to four thousand VLAN groups can be assigned. VLAN tags are inserted or removed based on the VLAN table configuration. The spanning tree protocol is supported and the states are divided into four types: Disabled, Blocking/Listening, Learning, and Forwarding.

For peripheral interfaces, two 16550-compatible UARTs are supported, and a 16-byte FIFO buffer is provided. A USB 2.0 host controller is embedded in the RTL8198 to provide EHCI and OHCI 1.1 compliant host functionality. In addition, a USB PHY has been embedded in the RTL8198.

An MDI/MDIX auto crossover function is supported. For accessing high-speed devices, the RTL8198 provides a PCI Express host to access a PCI Express interface. Up to two PCI Express devices are supported via this interface on the RTL8198.

The RTL8198 requires only a single 25MHz crystal or 40MHz clock input for the system PLL. The RTL8198 also has two hardware timers and one watchdog timer to provide accurate timing and watchdog functionality. For extension and flexibility, the RTL8198 has up to 44 GPIO pins.

The RTL8198 is provided in a Thermally Enhanced Low Profile Plastic Quad Flat Package, 216-Lead (LQFP216-E-PAD) package. It requires only a 3.3V and 1.0V external power supply.

2. Features

- SOC
  - Embedded RISC CPU, RLX5281 with 16K I-Cache, 8K D-Cache, 40K I-MEM, 8K D-MEM
  - Supports MIPS-1 ISA, MIPS16 ISA
  - Clock rate up to 500MHz
  - Provides a standard 5-signal P1149.1 EJTAG test port
  - Supports RLX5281 CPU suspend mode
- L2 Capabilities
  - Six Gigabit Ethernet MACs switch with five IEEE 802.3 10/100/1000Mbps physical layer transceivers
  - Supports 1 dedicated GMII/RGMII/MII port to connect to an external MAC or PHY (supports both PHY mode and MAC mode) for HomePlug or HomePNA applications on RTL8198
  - Non-blocking wire-speed reception and transmission and non-head-of-line-blocking/forwarding
  - Internal 512Kbit SRAM for packet buffering
  - Internal 1024 entry 4-way hash L2 look-up table
  - Supports source and destination MAC address filtering
  - Three LED indicators per port for link, speed, full/half duplex
  - Bi-color LED display mode
- CPU Interface (NIC)
  - Supports BSD mbuf-like packet structure with adjustable cluster size (128-byte to 2Kbyte) to provide optimum memory utilization
  - The NIC DMA support multiple-descriptor-ring architecture for QoS applications (supports 6 RX descriptor rings and 2 TX descriptor rings)
- Peripheral Interfaces
  - Supports PCI Express Host with integrated PHY to connect up to two master devices
  - Two PCI Express PHY embedded
  - Supports one USB 2.0 host controller for access to USB-supported peripherals
  - One USB PHY is embedded
  - Supports two 16550 UARTs
  - Supports up to 44 GPIO pins
- Memory Interfaces
  - Serial Flash (SPI Type)
    - Supports two banks and dual I/O channels for SPI Flash application
    - Each Flash bank could be configured as 256K/512K/1M/2M/4M/8M/16M Bytes
    - Boot up from SPI flash is supported
  - SDR DRAM
    - Supports two SDR DRAM banks; each can be configured as 2M/4M/8M/16M/32M/64Mbyte
    - 16bit SDR DRAM data bus supported. System totally supports up to 128Mbyte SDR DRAM memory space
  - DDR1 DRAM
    - Supports one DDR1 DRAM bank that can be configured as 16M/32M/64M/128Mbytes
    - 16-bit DDR1 DRAM data bus supported. System totally supports up to 128Mbyte DDR1 DRAM memory space

- DDR2 DRAM
  - Supports one DDR2 DRAM bank that can be configured as 32M/64M/128Mbyte
  - 16-bit DDR2 DRAM data bus supported. System totally supports up to 128Mbyte DDR2 DRAM memory space

- Supports Green Ethernet
  - Cable length power saving
  - Power down power saving

- Supports pre-IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T, 100base-TX in full duplex operation and 10base-T in full/half duplex mode

- Other Add-on-Value Features
  - Supports Link Down Power Saving in Ethernet PHYceivers
  - Supports two hardware timers and one watchdog timer
  - Per-port configurable auto-crossover function
  - Built-in regulator controller
    - DDR1 DRAM to transform 3.3V to 2.5V via an external BJT transistor
    - DDR2 DRAM to transform 3.3V to 1.8V via an external BJT transistor
  - Supports Non-Flash Boot Interface (NFBI)
  - Single 25MHz crystal or 40MHz clock input
  - LQFP216-E-PAD package

3. Block Diagram

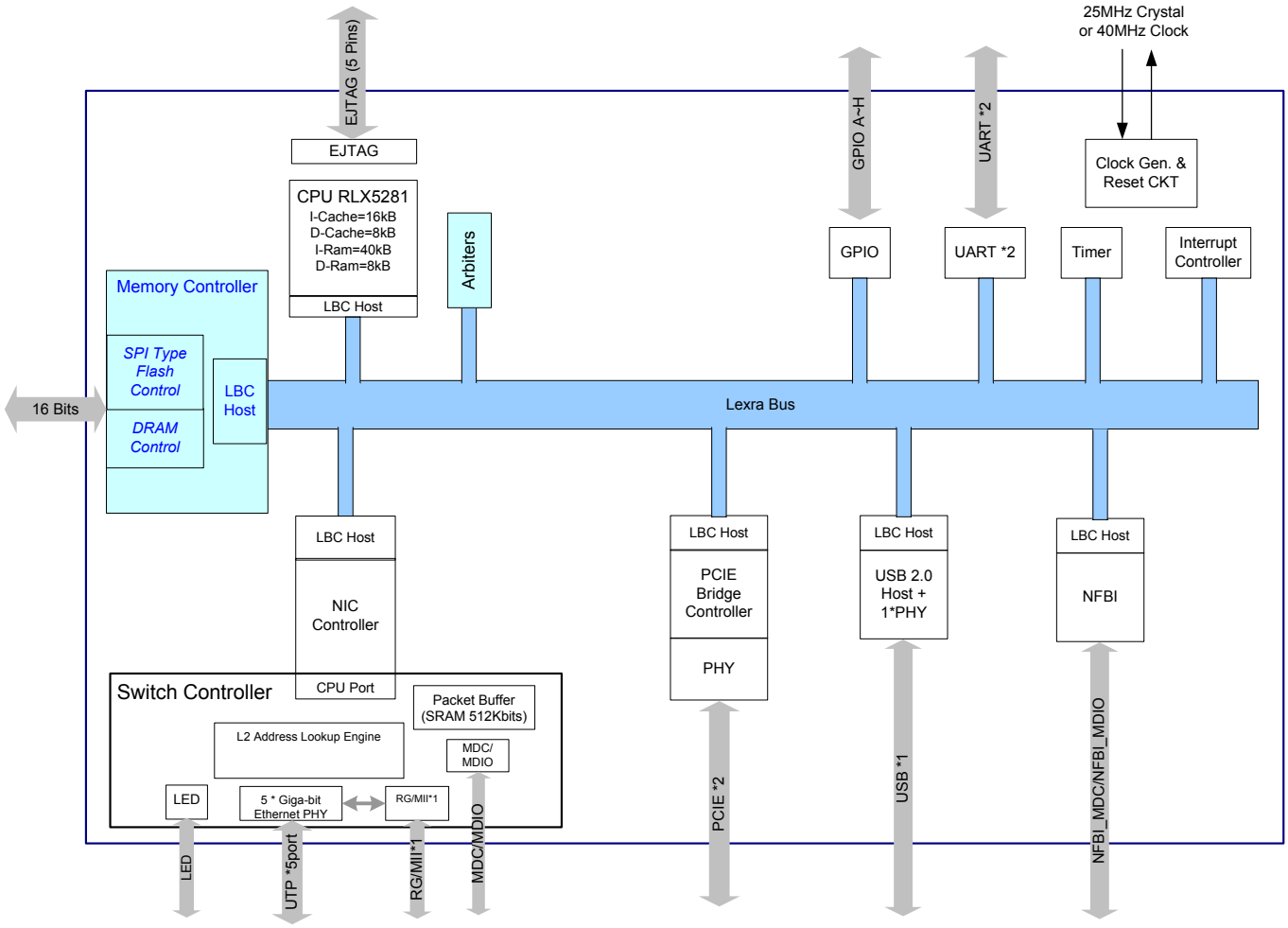


Figure 1. Block Diagram

4. Pin Assignments

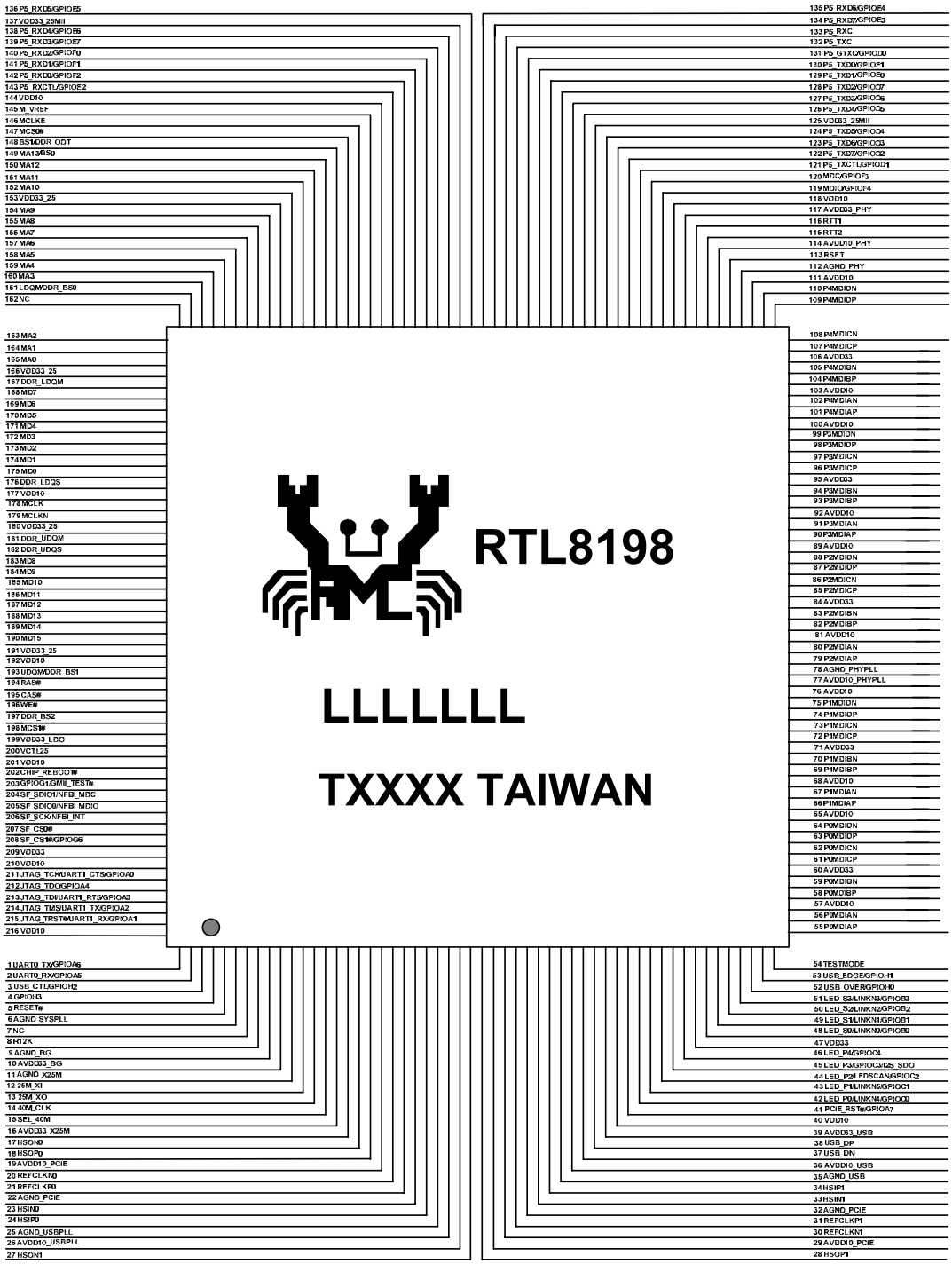


Figure 2. Pin Assignments

4.1. Package Identification

Green package is indicated by a ‘G’ in the location marked ‘T’ in Figure 2.

5. Pin Descriptions

In this section the following abbreviations are used:

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input

O: Output

I/O: Bi-Direction Input/Output

P: Digital Power

G: Digital Ground

T/S: Tri-State Bi-Directional Input/Output

IPD: Input Pin With Pull-Down Resistor

IPU: Input Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

AI: Analog Input

AO: Analog Output

AI/O: Analog Bi-Directional Input/Output

AP: Analog Power

AG: Analog Ground

S/T/S: Sustained Tri-State

OOD: Output With Open Drain

O3S: Output With Tri-State

Table 1. Pin Descriptions

Pin Name	Pin No.	Type	Description
Clock & Reset			
25M_XI	12	I	25MHz Crystal Clock Input.
25M_XO	13	O	25MHz Crystal Clock Output.
40M_CLK	14	I	40MHz Clock Input. Input voltage level 1.8V
SEL_40M	15	I	Select 40M or 25M Clock Source. 0: Use 25MHz clock 1: Use 40MHz clock
RESET#	5	I	External Reset.
Gigabit Ethernet Physical Layer			
P0MDIAP/N P0MDIBP/N P0MDICP/N P0MDIDP/N	55 56 58 59 61 62 63 64	AI/O	Port0 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.

Pin Name	Pin No.	Type	Description
P1MDIAP/N P1MDIBP/N P1MDICP/N P1MDIDP/N	66 67 69 70 72 73 74 75	AI/O	Port1 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P2MDIAP/N P2MDIBP/N P2MDICP/N P2MDIDP/N	79 80 82 83 85 86 87 88	AI/O	Port2 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P3MDIAP/N P3MDIBP/N P3MDICP/N P3MDIDP/N	90 91 93 94 96 97 98 99	AI/O	Port3 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P4MDIAP/N P4MDIBP/N P4MDICP/N P4MDIDP/N	101 102 104 105 107 108 109 110	AI/O	Port4 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
Ethernet MAC GMII/RGMII/MII Interface			
MDC	120	O	Management Data Clock.
MDIO	119	I_{PU}/O	Management Data I/O.
P5_GTXC	131	O	Shared for (1) MII Mode (2) GMII/RGMII Mode (3) MII PHY Mode. For details see section 5.2.1 MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings, page 15.
P5_TXC	132	I	Shared for (1) MII Mode (2) GMII/RGMII Mode (3) MII PHY Mode. For details see section 5.2.1 MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings, page 15.

Pin Name	Pin No.	Type	Description
P5_TXCTL	121	O	Shared for (1) MII Mode (2) GMII/RGMII Mode (3) MII PHY Mode. For details see section 5.2.1 MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings, page 15.
P5_TXD[7:0]	122, 123, 124, 126, 127, 128, 129, 130	O	Shared for (1) MII Mode (2) GMII/RGMII Mode (3) MII PHY Mode. For details see section 5.2.1 MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings, page 15.
P5_RXC	133	I	Shared for (1) MII Mode (2) GMII/RGMII Mode (3) MII PHY Mode. For details see section 5.2.1 MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings, page 15.
P5_RXCTL	143	I	Shared for (1) MII Mode (2) GMII/RGMII Mode (3) MII PHY Mode. For details see section 5.2.1 MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings, page 15.
P5_RXD[7:0]	134, 135, 136, 138, 139, 140, 141, 142	I	Shared for (1) MII Mode (2) GMII/RGMII Mode (3) MII PHY Mode. For details see section 5.2.1 MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings, page 15.
Memory Interface			
MD[15:0]	190, 189, 188, 187, 186, 185, 184, 183, 168, 169, 170, 171, 172, 173, 174, 175	I/O	Data for DDR DRAM and SDR DRAM.
MA[13:0]	149, 150, 151, 152, 154, 155, 156, 157, 158, 159, 160, 163, 164, 165	O	Address for DDR DRAM and SDR DRAM
SDR DRAM Control			
MCLK	178	O	SDR DRAM Clock.
MCLKE	146	O	SDR DRAM Clock Enable.
MCS0#	147	O	SDR DRAM Chip Select 0.
MCS1#	198	O	SDR DRAM Chip Select 1.
BS[1:0]	148, 149	O	SDR DRAM Chip Bank Select [1:0].
RAS#	194	O	Raw Address Strobe (RAS#) for SDR DRAM.
CAS#	195	O	Column Address Strobe for SDR DRAM.
WE#	196	O	Write Enable for SDR DRAM.
LDQM	161	O	Lower Data Mask Output to SDR DRAM. Corresponds to D[7:0]
UDQM	193	O	Upper Data Mask Output to SDR DRAM. Corresponds to D[15:8]
DDR DRAM Control			
MCLK	178	O	DDR DRAM Differential Clock.
MCLKN	179	O	DDR DRAM Differential Clock.
MCLKE	146	O	DDR DRAM Clock Enable.
MCS0#	147	O	DDR DRAM Chip Select 0.

Pin Name	Pin No.	Type	Description
MCS1#	198	O	DDR DRAM Chip Select 1.
DDR_BS[2:0]	197, 193, 161	O	DDR DRAM Chip Bank Select [2:0].
RAS#	194	O	Raw Address Strobe (RAS#) for DDR DRAM
CAS#	195	O	Column Address Strobe for DDR DRAM
WE#	196	O	Write Enable for DDR DRAM
DDR_LDQM	167	O	Lower Data Mask Output to DDR DRAM. Corresponds to D[7:0]
DDR_UDQM	181	O	Upper Data mask output to DDR DRAM. Corresponds to D[15:8]
DDR_LDQS	176	O	Lower Data Strobe to DDR DRAM. Corresponds to D[7:0]
DDR_UDQS	182	O	Upper Data strobe to DDR DRAM. Corresponds to D[15:8]
M_VREF	145	AI	Voltage Reference 1.25V for DDR1. Voltage Reference 0.9V for DDR2.
DDR_ODT	148	O	DDR2 On-Die Termination. ODT (registered HIGH) enables termination resistance internal to the DDR2 DRAM.
Serial SPI Flash Control			
SF_CS0#	207	O	SPI Serial Flash Chip Select 0.
SF_CS1#	208	O	SPI Serial Flash Chip Select 1.
SF_SDIO[1:0]	204, 205	I/O	SPI Serial Flash Serial Data Input/Output.
SF_SCK	206	O	SPI Serial Flash Serial Clock Output. The SF_SDI will be driven on the falling edge. The SF_SDO will be latched on the rising edge.
UART			
UART0_TX	1	O	Data Transmit Serial Output of UART0.
UART0_RX	2	I_{PU}	Data Receive Serial Input of UART0.
UART1_TX	214	O	Data Transmit Serial Output of UART1.
UART1_RX	215	I	Data Receive Serial Input of UART1.
UART1_RTS	213	O	Request to Send of UART1.
UART1_CTS	211	I	Clear to Send of UART1.
JTAG			
JTAG_TCK	211	I_{PU}	JTAG Test Clock.
JTAG_TMS	214	I_{PU}	JTAG Test Mode Select.
JTAG_TDO	212	O	JTAG Test Data Output.
JTAG_TDI	213	I_{PU}	JTAG Test Data In.
JTAG_TRST#	215	I_{PU}	JTAG Test Reset.
LED			
LED_P[4:0]	46, 45, 44, 43, 42	O	Matrix LED Mode. Phase control for 20 LED array (default active high).
LED_S[3:0]	51, 50, 49, 48	O	Matrix LED Mode. Signal control for 20 LED array (default active low).

Pin Name	Pin No.	Type	Description
LINKN[5:0]	43, 42, 51, 50, 49, 48	O	Scan LED Mode. Link or Link/Speed Status of 5 ports (Low Active). (shared with LED_P[1:0], LED_S[3:0])
LEDSCAN	44	O	Scan LED Mode. Scanning control signal for 2-pin bi-color LED in parallel LED mode topology (shared with LED_P2).
2.5V Linear Regulator			
VCTL25	200	AO	Linear Regulator Voltage Control. External 3.3V to 2.5V Transfer for DDR1 DRAM External 3.3V to 1.8V Transfer for DDR2 DRAM
GPIO			
GPIOA[3:0]	213, 214, 215, 211	I_{PU}/O	GPIO Port A.
GPIOA5	2	I_{PD}/O	GPIO Port A.
GPIOA7, GPIOA6, GPIOA4	41, 1, 212	O	GPIO Port A Output Only.
GPIOB[3:0]	51, 50, 49, 48	I/O	GPIO Port B.
GPIOC[4:0]	46, 45, 44, 43, 42	I/O	GPIO Port C.
GPIOD[7:0]	128, 127, 126, 124, 123, 122, 121, 131	I/O	GPIO Port D.
GPIOE[7:0]	139, 138, 136, 135, 134, 143, 130, 129	I/O	GPIO Port E.
GPIOF[4:0]	119, 120, 142, 141, 140	I/O	GPIO Port F.
GPIOG1	203	I/O	GPIO Port G.
GPIOG6	208	O	GPIO Port G Output Only.
GPIOH[1:0]	53, 52	I/O	GPIO Port H.
GPIOH[3:2]	4, 3	O	GPIO Port H Output Only.
USB 2.0			
USB_DP	38	AI/O	USB Device Data Plus Pin.
USB_DN	37	AI/O	USB Device Data Minus Pin.
USB_OVER	52	I	USB Power Over Current Detection.
USB_EDGE	53	I	USB Over Current Edge Signal Active Level. 0: Low active 1: High active
USB_CTL	3	O	USB Output Power Control.
PCI Express Interface			
HSON[1:0] HSOP[1:0]	27, 17 28, 18	AO	Transmitter Differential Pair.
HSIN[1:0] HSIP[1:0]	33, 23 34, 24	AI	Receiver Differential Pair.
REFCLKN[1:0] REFCLKP[1:0]	30, 20 31, 21	AO	Reference Clock Differential Pair.
PCIE_RST#	41	O	PCI Express Reset.

Pin Name	Pin No.	Type	Description
Non-Flash Booting Interface			
NFBI_MDC	204	I	Management Data Clock in NFBI Mode. This pin provides a clock synchronous to MDIO. The clock rate can be from DC to 25MHz.
NFBI_MDIO	205	I/O	Management Data I/O on NFBI Mode. NFBI access data Input/Output and it is synchronous with the rising edge of MDC clock input. The Timing specification and frame format follow IEEE 802.3 SMI (MDC/MDIO) interface specifications.
NFBI_INT	206	O	Interrupt to Host on NFBI Mode. Used by NFBI to interrupt the external host CPU. This pin is Level trigger. Level polarity can be programmed by CMD register.
CHIP_REBOOT#	202	I	Chip Reboot in NFBI Mode. When the external host needs to reboot the RTL8198 CPU, this pin must be asserted to LOW. This pin should be always pulled-up in Non-flash booting mode.
GMII_TEST#	203	I	GMII Test Mode. 0: GMII test mode 1: GMII normal mode This pin should be always pulled-up in Non-flash booting mode.
Test			
TESTMODE	54	I_{PD}	For Chip Internal Test.
RTT2, RTT1	115, 116	O	For Giga PHY Internal Test.
Reference Voltage			
RSET	113	AI	Reference Voltage for Ethernet PHY. 2.5K 1% pull down
R12K	8	AI	Reference Voltage for System. 12K 1% pull down
Power & GND			
VDD33	47, 209	P	Digital I/O Power Supply 3.3V.
VDD33/25	153, 166, 180, 191	P	Memory I/O Power Supply 3.3V, 2.5V, or 1.8V. SDR DRAM: 3.3V DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
VDD33/25_MII	125, 137	P	GMII/RGMII/MII Interface Power Supply 3.3V or 2.5V.
AVDD33	60, 71, 84, 95, 106	AP	Analog Power Supply 3.3V.
VDD33_LDO	199	AP	LDO Power Supply 3.3V.
VDD10	40, 118, 144, 177, 192, 201, 210, 216	P	Digital Core Power Supply 1.0V.
AVDD10	57, 65, 68, 76, 81, 89, 92, 100, 103, 111	AP	Analog Power Supply 1.0V.
AVDD33_X25M	16	AP	25M Crystal Power 3.3V.
AVDD33_BG	10	AP	System Band Gap Power Supply 3.3V.
AVDD10_PCIE	19, 29	AP	PCI Express Analog Power Supply 1.0V.

Pin Name	Pin No.	Type	Description
AVDD10_USBPLL	26	AP	USB PHY PLL Power 1.0V.
AVDD10_PHYPLL	77	AP	Ethernet PHY PLL Power 1.0V.
AVDD10_PHY	114	AP	Ethernet PHY Center Power 1.0V.
AVDD33_PHY	117	AP	Ethernet PHY Center Power 3.3V.
AVDD33_USB	39	AP	USB2.0 Analog Power 3.3V.
AVDD10_USB	36	AP	USB2.0 Analog Power 1.0V.
GND	E-PAD	G	System GND.
AGND_PHY	112	AG	Ethernet PHY Center GND.
AGND_SYSPLL	6	AG	System PLL GND.
AGND_PHYPLL	78	AG	Ethernet PHY PLL GND.
AGND_USBPLL	25	AG	USB PHY PLL GND.
AGND_PCIE	22, 32	AG	PCI Express GND.
AGND_USB	35	AG	USB GND.
AGND_BG	9	AG	System Bandgap GND.
AGND_X25M	11	AG	25M Crystal GND.
Not Connected Pin			
NC	162, 7	-	Not Connected.

5.1. Configuration Upon Power On Strapping

All mode configuration pins are internal pull low. The 1.0V digital core power input pin voltage is up to 0.7V on system power-on. The strap data will be latched after a delay of 300ms.

Table 2. Configuration Upon Power On Strapping

H/W Pin Name	Configuration Name	Pin No	Description
SF_CS1#, SF_CS0#, SF_SCK	ck_cpu_freq_sel[1:0]	208, 207, 206	CPU Clock Configuration. 000: 500MHz 001 to 111: Reserved
PCIE_RST#, UART_TX	ck_freq_sel[1:0]	41, 1	DRAM Clock Rate Configuration. 00: 78.125MHz 01: 125MHz 10: 168.75MHz 11: Reserved
MCS0#	bootpinsel	147	Boot Pin Selection for RTL8198 Boot Method. This is hardware strapping pin. 0: Boot from NFBI mode 1: Boot from normal flash
JTAG_TDO	MIIM_SLV	212	MDC/MDIO Mode Select. 0: Slave mode 1: Master mode
BS1	EnOLTautoTestMode	148	Enable OLT Auto Test Mode. Realtek internal use only.
DDR_BS2	DDR_TYPE	197	DDR DRAM Type. 0: DDR1 1: DDR2
MCLKE	BOOTSEL	146	Boot Device Select for Flash Booting Mode. 0: Reserved 1: Boot from Serial Flash (SPI) Test mode for NFBI mode 0: Normal mode 1: Test mode
MCS1#	DRAM_TYPE	198	DRAM Type. 0: SDR 1: DDR
USB_CTL	CLKLX_FROM_CLKM	3	Lexra Local Bus Clock Select. 0: 200MHz 1: From MCLK
GPIOH3	MIIM_SLV	4	Port 5 GMII/RGMII/MII Mode Select On Normal Booting. 0: PHY mode 1: MAC mode
JTAG_TDO	PHYIDSEL	212	Select PHY Address for NFBI Mode. Provide with 2 groups for pre-setting PHY Address 0: PHY Address is 01000b (8) 1: PHY Address is 10000b (16)

5.2. GMAC Pin Mode Description

5.2.1. MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings

The RTL8198 GMAC port supports three MAC interface modes: (1) MII mode (2) RGMII mode (3) MII PHY mode (4) GMII mode. These four modes I/O pin definition mappings are shown in Table 3.

Table 3. MAC Interface MII/RGMII Mode Pin Sharing Mappings

Pin	MII MAC Mode	RGMII Mode	MII PHY Mode	GMII Mode
GTXC (Output)	-	GTXC (Output)	-	GTXC (Output)
TXC (Input)	TXC (Input)	-	PhyRXC (Output)	-
TXCTL (Output)	TXEN (Output)	TXCTL (Output)	PhyRXDV (Output)	TXCTL (Output)
TXD[7:4] (Output)	-	-	-	TXD[7:4] (Output)
TXD[3:0] (Output)	TXD[3:0] (Output)	TXD[3:0] (Output)	PhyRXD[3:0] (Output)	TXD[3:0] (Output)
RXC (Input)	RXC (Input)	RXC (Input)	PhyTXC (Output)	RXC (Input)
RXCTL (Input)	RXDV (Input)	RXCTL (Input)	PhyTXEN (Input)	RXCTL (Input)
RXD[7:4] (Input)	-	-	-	RXD[7:4] (Input)
RXD[3:0] (Input)	RXD[3:0] (Input)	RXD[3:0] (Input)	PhyTXD[3:0] (Input)	RXD[3:0] (Input)

5.2.2. GMII/RGMII Interface Pin Descriptions

Table 4. GMII/RGMII Interface Pin Descriptions

Pin Name	Type	Description
GTXC	O	GMII/RGMII Transmit Clock. 125MHz, 25MHz, or 2.5MHz transmit clock with ±50ppm tolerance for 1000Mbps, 100Mbps, and 10Mbps respectively.
TXCTL	O	GMII/RGMII Transmit Control Signal. The GTXCTL indicates TXEN at rising of GTXC. TXER XOR TXEN is encoded on the falling edge of GTXC. @ GTXC rising edge: GTXCTL=TXEN. @ GTXC falling edge: GTXCTL=TXEN XOR TXER.
TXD[7:0]	O	GMII/RGMII Transmit Data. Transmits data synchronously to double edge of GTXC, with lower 4 bits (bit[3:0]) present on the rising edge of GTXC and the upper 4 bits (bit[7:4]) present on the falling edge of the GTXC. In GMII/RGMII 10/100Base-T mode, the transmit data nibble is present on GTXD[3:0] on the rising edge of GTXC.
RXC	I	GMII/RGMII Receive Clock. 125MHz, 25MHz, or 2.5MHz transmit clock with ±50ppm tolerance for 1000Mbps, 100Mbps, and 10Mbps respectively.
RXCTL	I	GMII/RGMII Receive Control Signal. The RXCTL indicates RXDV at rising of RXC, and RXER XOR RXDV is encoded on the falling edge of GRXC. @ RXC rising edge: RXCTL=RXEN. @ RXC falling edge: RXCTL=RXDV XOR RXER.

Pin Name	Type	Description
RXD[3:0]	I	GMII/RGMII Receive Data. Transmits data synchronously to double edge of RXC, with lower 4 bits (bit[3:0]) present on the rising edge of RXC and the upper 4 bits (bit[7:4]) present on the falling edge of the RXC. In GMII/RGMII 10/100Base-T mode, the transmit data nibble is present on RXD[3:0] on the rising edge of RXC.
VDD_RGMII	P	GMII/RGMII Interface Power Supply. VDD33/25_RGMII can be supplied with 2.5V COMS or 1.5V HSTL

5.2.3. MII MAC Mode Interface Pin Descriptions

Table 5. MII MAC Mode Interface Pin Descriptions

Pin Name	Type	Description
TXD[3:0]	O	Transmit Data Output (TXD[3:0]). Transmits data synchronously to the rising edge of GTXC.
TXEN	O	Transmit Data Enable. Transmit enable that is sent synchronously at the rising edge of GTXC.
TXC	I	Transmit Clock (25MHz/2.5MHz). 25MHz/2.5MHz clock driven by PHY when MII is operating at 100Mbps/10Mbps. TXD[3:0], TXEN are synchronized by TXC rising edge in this mode.
RXC	I	25MHz/2.5MHz. Receive Clock. RXD[3:0], RXDV, CRS, and COL are synchronized by TXC rising edge in this mode.
RXDV	I	Receive Data Valid Input.
RXD[3:0]	I	Receive Data Input (RXD[3:0]).

5.2.4. MII PHY Mode Interface Pin Descriptions

Table 6. MII PHY Mode Interface Pin Descriptions

Pin Name	Type	Description
phyRXD[3:0]	O	MII PHY Mode Receive Data (phyRXD[3:0]).
phyRXDV	O	MII PHY Mode Receive Data Valid.
phyRXC	O	MII PHY Mode Receive Clock (25MHz/2.5MHz). PhyRXD[3:0], phyRXDV, are synchronized by phyGRXC falling edge in this mode.
phyTXC	O	MII PHY Mode Transmit Clock (25MHz/2.5MHz). phyTXD[3:0], phyTXEN are synchronized by phyTXC falling edge in this mode.
phyTXEN	I	MII PHY Mode Transmit Data Enable.
phyTXD[3:0]	I	MII PHY Mode Transmit Data (phyTXD[3:0]).

5.3. Shared I/O Pin Mapping

Table 7. Shared I/O Pin Mapping

QFP216 E-PAD	GPIO	GMII	Memory	EJTAG	USB	LED	UART	Reset
211	GPIOA[0]	-	-	JTAG_TCK	-	-	UART1_CTS	-
215	GPIOA[1]	-	-	JTAG_TRST#	-	-	UART1_RX	-
214	GPIOA[2]	-	-	JTAG_TMS	-	-	UART1_TX	-
213	GPIOA[3]	-	-	JTAG_TDI	-	-	UART1_RTS	-
212	GPIOA[4]	-	-	JTAG_TDO	-	-	-	-
2	GPIOA[5]	-	-	-	-	-	UART0_RX	-
1	GPIOA[6]	-	-	-	-	-	UART0_TX	-
41	GPIOA[7]	-	-	-	-	-	-	PCIE_RST#
48	GPIOB[0]	-	-	-	-	LED_S0	-	-
49	GPIOB[1]	-	-	-	-	LED_S1	-	-
50	GPIOB[2]	-	-	-	-	LED_S2	-	-
51	GPIOB[3]	-	-	-	-	LED_S3	-	-
42	GPIOC[0]	-	-	-	-	LED_P0	-	-
43	GPIOC[1]	-	-	-	-	LED_P1	-	-
44	GPIOC[2]	-	-	-	-	LED_P2	-	-
45	GPIOC[3]	-	-	-	-	LED_P3	-	-
46	GPIOC[4]	-	-	-	-	LED_P4	-	-
131	GPIOD[0]	P5_GTXC	-	-	-	-	-	-
121	GPIOD[1]	P5_TXCTL	-	-	-	-	-	-
122	GPIOD[2]	P5_TXD7	-	-	-	-	-	-
123	GPIOD[3]	P5_TXD6	-	-	-	-	-	-
124	GPIOD[4]	P5_TXD5	-	-	-	-	-	-
126	GPIOD[5]	P5_TXD4	-	-	-	-	-	-
127	GPIOD[6]	P5_TXD3	-	-	-	-	-	-
128	GPIOD[7]	P5_TXD2	-	-	-	-	-	-
129	GPIOE[0]	P5_TXD1	-	-	-	-	-	-
130	GPIOE[1]	P5_TXD0	-	-	-	-	-	-
143	GPIOE[2]	P5_RXCTL	-	-	-	-	-	-
134	GPIOE[3]	P5_RXD7	-	-	-	-	-	-
135	GPIOE[4]	P5_RXD6	-	-	-	-	-	-
136	GPIOE[5]	P5_RXD5	-	-	-	-	-	-
138	GPIOE[6]	P5_RXD4	-	-	-	-	-	-

QFP216 E-PAD	GPIO	GMII	Memory	EJTAG	USB	LED	UART	Reset
139	GPIOE[7]	P5_RXD3	-	-	-	-	-	-
140	GPIOF[0]	P5_RXD2	-	-	-	-	-	-
141	GPIOF[1]	P5_RXD1	-	-	-	-	-	-
142	GPIOF[2]	P5_RXD0	-	-	-	-	-	-
120	GPIOF[3]	MDC	-	-	-	-	-	-
119	GPIOF[4]	MDIO	-	-	-	-	-	-
203	GPIOG[1]	-	-	-	-	-	-	-
208	GPIOG[6]	-	-	-	-	-	-	-
52	GPIOH[0]	-	-	-	USB_OVER	-	-	-
53	GPIOH[1]	-	-	-	USB_EDGE	-	-	-
3	GPIOH[2]	-	-	-	USB_CTL	-	-	-
4	GPIOH[3]	-	-	-	-	-	-	-

6. Memory Controller

The RTL8198 integrates a memory control module to access external DDR DRAM , SDR DRAM, and Flash memory.

The interface is designed for DDR-compliant DDR DRAM, and designed for PC133 or PC166-compliant SDR DRAM, and supports auto-refresh mode, which requires a 4096 refresh cycle within 64ms. The SDR DRAM interface supports two chips (MCS0#, and MCS1#). The DDR DRAM interface supports one chip (MCS0#), and the DRAM size and timing is configurable in registers.

The RTL8198 also supports two flash memory chips (SF_CS0# and SF_CS1#). The interface supports SPI flash memory. When Flash is used, the system will boot from KSEG1 at virtual address 0xBFC0_0000 (physical address: 0x1FC0_0000). Chip1 flash memory will be mapped to the address '0x1FC0_0000 + flash size'. The flash size is configurable from 1M to 32M bytes for each chip. If flash size is set to 4M, 8M, 16M, or 32M byte, 0xBFC0_0000 still maps the first 4M bytes of flash, and there will be a new memory mapping from 0xBD00_0000 (0xBD00_0000 maps to chip 0 byte 0).

6.1. SDR DRAM Control Interface

PC100~PC166-compliant SDR DRAM is supported. The SDR DRAM controller supports Auto Refresh mode, which requires a 4096-cycle refresh each 64ms. The RTL8198 provides a maximum of 512Mbit address space (8Mx16x4Banks) and the SDR DRAM size is configurable.

6.1.1. Features

- Interface (Bus Width): 16-bit
- Targeted SDR Frequency: Up to 168MHz
- Two Chip Selects (CS0# and CS1#)
- Supported SDR DRAM chip specification
  - Bank Counts: 2, 4
  - Row Counts: 2K (A0~A10), 4K (A0~A11), 8K (A0~A12)
  - Column Counts: 256 (A0~A7), 512 (A0~A8), 1K (A0~A9), 2K (A0~A9, A11)
- Programmable Timing Parameters: tRAS, tRP, tRCD, tCL, tREFI…

6.1.2. Bank2 and Bank3

Bank2 (CS0#) and Bank3 (CS1#) are designed for SDR DRAM connections. Bank2 is mapped to either kseg0 or kseg1, with a start address of 0x0000.0000 (virtual address 0x8000.0000 or 0xa000.0000). Bank3 is mapped to 0x0000.0000 + SDR DRAM size. The Bank2 and Bank3 sizes should be exactly the same. If only one SDR DRAM is on-board, the RTL8198 provides 16-bit access mode to handle this.

6.2. DDR DRAM Controller

6.2.1. Features

- Interface (Bus Width): 16-bit
- Targeted DDR Frequency: Up to 168MHz
- Supports one Chip Select (MCS0#)
- Supports both DDR1 and DDR2
- Supported DDR DRAM Chip Specification
  - Bank Counts: 8
  - Row Counts: 4K (A0~A11), 8K (A0~A12), 16K (A0~A13)
  - Column Counts: 512 (A0~A8), 1K (A0~A9), 2K (A0~A9, A11), 4K (A0~A9, A11, A12)
- Programmable Timing Parameters: tRAS, tRP, tRCD, tCL, tREFI…

6.3. SPI Flash Controller

The SPI flash controller is a new design and incorporates new features.

6.3.1. Features

- Targeted SPI flash frequency: Up to 84MHz (when DRAM clock is 168MHz)
- Supports two chips
- In addition to a programmed I/O interface, also supports a memory-mapped I/O interface for read operation
- Supports Read and Fast Read in memory-mapped I/O mode

6.3.2. Pin Mode and Definition of Serial and Dual I/O

Modes supported on the SPI flash interface:

Serial I/O Mode

- SDI: Flash chip data input pin
- SDO: Flash chip data output pin

Dual I/O Mode

- SDIO0 (SDI): Flash chip data bi-directional pin
- SDIO1 (SDO): Flash chip data bi-directional pin

6.4. Software Register Definitions

6.4.1. Memory Control Register (MCR) (0xB800_1000)

This register does not provide byte access.

Table 8. Memory Control Register (MCR) (0xB800_1000)

Bit	Name	Description	Mode	Default
31	DRAMTYPE	Report the Hardware Strapping Initial Value for DRAM Type. 0: SDR DRAM 1: DDR DRAM	R	0B
30	BOOTSEL	Report the Hardware Strapping Initial Value for Boot Flash Type. 0: Reserved 1:Serial SPI flash	R	0B
29	IPREF	Enable Instruction Prefetch Function. 0: Disable prefetch (also reset buffer status) 1: Enable prefetch (4 words)	RW	0B
28	DPREF	Enable Data Prefetch Function. 0: Disable prefetch (also reset buffer status) 1: Enable prefetch (4 words)	RW	0B
27	IPREF_MODE	Choose Instruction Prefetch Mode. 0: Old prefetch mechanism 1: New prefetch mechanism	RW	0B
26	DPREF_MODE	Choose Data Prefetch Mode. 0: Old prefetch mechanism 1: New prefetch mechanism	RW	0B
25:0	-	Reserved.	-	-

6.4.2. DRAM Configuration Register (DCR) (0xB800_1004)

This register does not provide byte access.

Table 9. DRAM Configuration Register (DCR) (0xB800_1004)

Bit	Name	Description	Mode	Default
31:30	T_CAS	CAS Latency. 00: Latency=2 01: Latency=3 10: Latency=2.5 (only used for DDR) 11: Reserved	RW	01B
29:28	DBUSWID	DRAM Bus Width. 00: Reserved 01: 16 bit (used for DDR, SDR) 10: Reserved 11: Reserved	RW	01B
27	DCHIPSEL	DRAM Chip Select. 0: CS0# 1: CS0# and CS1#	RW	1B
26:25	ROWCNT	Row Counts. 00: 2K (A0~A10) 01: 4K (A0~A11) 10: 8K (A0~A12) 11: 16K (A0~A13)	RW	00B
24:22	COLCNT	Column Counts. 000: 256 (A0~A7) 001: 512 (A0~A8) 010: 1K (A0~A9) 011: 2K (A0~A9, A11) 100: 4K (A0~A9, A11, A12) 101: Reserved 110: Reserved 111: Reserved	RW	000B
21	BSTREF	Bursted 8 Auto-Refresh Commands (Used for DDR). 0: Disable 1: Enable	RW	0B
20	ARBIT	Enforce Interface Arbitration Take Effect. 0: Reserved 1: Take effect	RW	0B
19	BANKCNT	Bank Counts. 0: 2 banks (used for SDR) 1: 4 banks (used for SDR, DDR)	RW	1B
18	FAST_RX	If RX path turnaround delay is small enough, the memory controller can return read data with reduced latency within 1DRAM clock cycle (used for DDR). 0: Normal path 1: Fast path	RW	0B
17	MR_MODE	Select the Memory Command that Memory Controller Issues (Used for DDR). 0: Mode Register 1: Extended Mode Register	RW	0B
16	DRV_STR	Drive Strength Setting of DRAM Chip (Used for DDR). For this option to be effective, MR_MODE must be first set to 1. 0: Normal 1: Reduced	RW	0B
15:0	-	Reserved.	-	-

6.4.3. DRAM Timing Register (DTR) (0xB800_1008)

This register does not provide byte access.

Table 10. DRAM Timing Register (DTR) (0xB800_1008)

Bit	Name	Description	Mode	Default
31:29	T_RP	tRP Timing Parameter of DRAM Basic unit = 1*DRAM_CLK 000: 1 unit	RW	111B
28:26	T_RCD	tRCD Timing Parameter of DRAM Basic unit = 1*DRAM_CLK 000: 1 unit	RW	111B
25:21	T_RAS	Minimum T_RAS Timing Parameter of DRAM Basic unit = 1*DRAM_CLK 00000: 1 unit	RW	11111B
20:16	T_RFC	tRFC Timing Parameter of DRAM. Refresh row cycle time Basic unit = 1*DRAM_CLK 00000: 1 unit	RW	11111B
15:12	T_REFI	tREF Timing Parameter of DRAM. Refresh row interval time Basic unit = T_REFI_UNIT 0000: 1 unit 0001: 2 units … 1111: 16 units	RW	0000B
11:9	T_REFI_UNIT	Basic Unit of T_REFI 000: 32 DRAM_CLK 001: 64 DRAM_CLK 010: 128 DRAM_CLK 011: 256 DRAM_CLK 100: 512 DRAM_CLK 101: 1024 DRAM_CLK 110: 2048 DRAM_CLK 111: 4096 DRAM_CLK	RW	111B
8:6	T_WR	tWR Timing Parameter of DRAM. Write recovery time Basic unit = 1*DRAM_CLK 000: 1 unit	RW	111B
5:0	-	Reserved.	-	-

6.4.4. DDR DRAM Calibration Register (DDCR) (0xB800_1050)

This register does not provide byte access.

Table 11. DDR DRAM Calibration Register (DDCR) (0xB800_1050)

Bit	Name	Description	Mode	Default
31	CAL_MODE	Run-Time Calibration Mode. 0: Use analog DLL calibration 1: Use digital delay line calibration	RW	0B
30	SW_CAL_RDY	Ready for Digital Delay Line Calibration. 0: Not ready 1: Ready	R	0B
29:25	DQS0_TAP[4:0]	Selects 32-Tap Delay Line for LDQS, which is Data Strobe for DQ[7:0] Reception. 00000: 1st tap 00001: 2nd tap … 11111: 32nd tap *Note: 32-tap delay is around 2.5 ns, which is chosen as it is around 1/2 the DDR cycle (1 tap is around 78.125ps).*	RW	00000B
24:20	DQS1_TAP[4:0]	Selection of 32-Tap Delay Line for UDQS, which is Data strobe for DQ[15:8] Reception. 00000: 1st tap 00001: 2nd tap … 11111: 32nd tap *Note: 32-tap delay is around 2.5 ns, which is chosen as it is around 1/2 the DDR cycle (1 tap is around 78.125ps).*	RW	00000B
19:15	DQS0_EN_TAP[4:0]	Selection of 32-Tap Delay Line for the Internal LDQS_EN Window. 00000: 1st tap 00001: 2nd tap … 11111: 32nd tap *Note: 32-tap delay is around 2.5 ns, which is chosen as it is around 1/2 the DDR cycle (1 tap is around 78.125ps).*	RW	00000B
14:10	DQS1_EN_TAP[4:0]	Selection of 32-Tap Delay Line for the Internal UDQS_EN Window. 00000: 1st tap 00001: 2nd tap … 11111: 32nd tap *Note: 32-tap delay is around 2.5 ns, which is chosen as it is around 1/2 the DDR cycle (1 tap is around 78.125ps).*	RW	00000B
9:0	-	Reserved.	-	-

6.4.5. SPI Flash Configuration Register (SFCR) (0xB800_1200)

This register does not provide byte access.

Table 12. SPI Flash Configuration Register (SFCR) (0xB800_1200)

Bit	Name	Description	Mode	Default
31:29	SPI_CLK_DIV	SPI Operating Clock Rate Selection. The value defines the divisor to generate SPI clock SPI Clock = (DRAM Clock)/(SPI_CLK_DIV) 000: DIV=2 001: DIV=4 010: DIV=6 011: DIV=8 100: DIV=10 101: DIV=12 110: DIV=14 111: DIV=16	RW	111B
28	RBO	Serial Flash Read Byte Ordering. 0: The byte order is from low to high 1: The byte order is from high to low	RW	1B
27	WBO	Serial Flash Write Byte Ordering. 0: The byte order is from low to high 1: The byte order is from high to low	RW	1B
26:23	SPI_TCS	SPI Chip Deselect Time. Basic unit = 1*DRAM clock cycle 0000: 1 unit 0001: 2 units, etc.	RW	1111B
22:0	-	Reserved.	-	-

6.4.6. SPI Flash Configuration Register 2 (SFCR2) (0xB800_1204)

This register does not provide byte access.

Table 13. SPI Flash Configuration Register 2 (SPCR2) (0xB800_1204)

Bit	Name	Description	Mode	Default
31:24	SFCMD	SPI Flash 8-Bit Command Code of a Read Transaction. Example: 'Read Data' is 0x03. 'Fast Read' is 0x0B.	RW	03H
23:21	SFSIZE	SPI Flash Size. 000: 128Kbyte 001: 256Kbyte 010: 512Kbyte 011: 1Mbyte 100: 2Mbyte 101: 4Mbyte 110: 8Mbyte 111: 16Mbyte	RW	111B
20	RD_OPT	SPI Flash Sequential Access Optimization. 0: No optimization 1: Optimization for sequential access	RW	0B
19:18	CMD_IO	SPI Flash I/O Mode Selection for the Command Phase of a Read Transaction. 00: Serial I/O (8 cycles) 01: Dual I/O (4 cycles) 10: Reserved 11: Reserved	RW	00B

Bit	Name	Description	Mode	Default
17:16	ADDR_IO	SPI Flash I/O Mode Selection for the Address Phase of a Read Transaction. 00: Serial I/O (24 cycles) 01: Dual I/O (12 cycles) 10: Reversed 11: Reserved	RW	00B
15:13	DUMMY_CYCLES	SPI Flash Inserted Dummy Cycles for the Dummy Cycle Phase of a Read Transaction. 000: 0 cycle 001: 2 cycles 010: 4 cycles 011: 6 cycles 100: 8 cycles 101: 10 cycles 110: 12 cycles 111: 14 cycles	RW	000B
12:11	DATA_IO	SPI Flash I/O Mode Selection for the Data Phase of a Read Transaction (Assume 8*N Cycles). 00: Serial I/O (8*N cycles) 01: Dual I/O (4*N cycles) 10: Reserved 11: Reserved	RW	00B
10	HOLD_TILL_SFDR2	If this bit is '1', it indicates the write operation to this register (SFCR2) will not take effect immediately but will be delayed until another write operation to SFDR2.	RW	0B
9:0	Reserved	Reserved.	-	-

6.4.7. SPI Flash Control & Status Register (SFCSR) (0xB800_1208)

This register does not provide byte access.

Table 14. SPI Flash Control & Status Register (SFCSR) (0xB800_1208)

Bit	Name	Description	Mode	Default
31	SPI_CSB0	SPI Flash Chip Select 0. 0: Active 1: Not active	RW	1B
30	SPI_CSB1	SPI Flash Chip Select 1. 0: Active 1: Not active	RW	1B
29:28	LEN	SPI Read/Write Data Length (Unit=Byte). 00: 1byte 01: 2byte 10: 3byte 11: 4byte	RW	11B
27	SPI_RDY	SPI Flash Operation Busy Indication Flag. 0: Busy (operation in progress) 1: Ready (idle or SPI access command is ready)	R	1B

Bit	Name	Description	Mode	Default
26:25	IO_WIDTH	SPI Flash I/O Mode Selection of a Transaction. 00: Serial I/O 01: Dual I/O 10: Reserved 11: Reserved	RW	00B
24	CHIP_SEL	Chip Selection. 0: CS0# 1: CS1#	RW	0B
23:16	CMD_BYTE	SPI Flash 8-Bit Command Code of a Transaction. (This field is only used in MMIO mode) Example: 'Read Data' is 0x03. 'Read ID' is 0x9F.	RW	0B
15:0	-	Reserved.	-	-

6.4.8. SPI Flash Data Register (SFDR) (0xB800_120C)

This register does not provide byte access.

This configuration register is used for the PIO (Programmed I/O) access mode.

Table 15. SPI Flash Data Register (SFDR) (0xB800_120C)

Bit	Name	Description	Mode	Default
31:24	Data3	Read/Write Data Byte 3.	RW	0B
23:16	Data2	Read/Write Data Byte 2.	RW	0B
15:8	Data1	Read/Write Data Byte 1.	RW	0B
7:0	Data0	Read/Write Data Byte 0.	RW	0B

6.4.9. SPI Flash Data Register 2 (SFDR2) (0xB800_1210)

This register does not provide byte access.

This configuration register is intended to be used under MMIO access mode.

Table 16. SPI Flash Data Register 2 (SFDR2) (0xB800_1210)

Bit	Name	Description	Mode	Default
31:24	Data3	Read/Write Data Byte 3.	RW	0B
23:16	Data2	Read/Write Data Byte 2.	RW	0B
15:8	Data1	Read/Write Data Byte 1.	RW	0B
7:0	Data0	Read/Write Data Byte 0.	RW	0B

7. Peripheral and MISC Control

7.1. GPIO Control

The RTL8198 provides 8 sets of General Purpose Input/Output (GPIO) pins (GPIO A, B, C, D, E, F, G, H). Each GPIO pin may be configured as an input or output pin. The GPIO DATA register may be used to control GPIO pin signals. The GPIO pins are shared with some peripheral pins, and the type of peripheral can affect the attributes of the shared pins. All GPIO sets can be used to generate interrupts, and an interrupt mask and status register are provided. The GPIO control registers are defined in the following table.

7.1.1. GPIO Register Set (0xB800_3500)

Table 17. GPIO Register Set (0xB800_3500)

Offset	Size (Byte)	Name	Description
0x00	4	PABCD_CNR	Port A, B, C, D Control Register.
0x08	4	PABCD_DIR	Port A, B, C, D Direction Register.
0x0C	4	PABCD_DAT	Port A, B, C, D Data Register.
0x10	4	PABCD_ISR	Port A, B, C, D Interrupt Status Register.
0x14	4	PAB_IMR	Port A, B Interrupt Mask Register.
0x18	4	PCD_IMR	Port C, D Interrupt Mask Register.
0x1C	4	PEFGH_CNR	Port E, F, G, H Control Register.
0x24	4	PEFGH_DIR	Port E, F, G, H Direction Register.
0x28	4	PEFGH_DAT	Port E, F, G, H Data Register.
0x2C	4	PEFGH_ISR	Port E, F, G, H Interrupt Status Register.
0x30	4	PEF_IMR	Port E, F Interrupt Mask Register.
0x34	4	PGH_IMR	Port G, H Interrupt Mask Register.

7.1.2. GPIO Port A, B, C, D Control Register (PABCD_CNR) (0xB800_3500)

Table 18. GPIO Port A, B, C, D Control Register (PABCD_CNR) (0xB800_3500)

Bit	Name	Description	Mode	Default
31:24	PFC_D[7:0]	Pin Function Configuration of Port D	RW	FFH
23:16	PFC_C[7:0]	Pin Function Configuration of Port C	RW	FFH
15:8	PFC_B[7:0]	Pin Function Configuration of Port B	RW	FFH
7:0	PFC_A[7:0]	Pin Function Configuration of Port A Bit Value: 0: Configured as GPIO pin 1: Configured as dedicated peripheral pin	RW	FFH

7.1.3. GPIO Port A, B, C, D Direction Register (PABCD_DIR) (0xB800-3508)

Table 19. GPIO Port A, B, C, D Direction Register (PABCD_DIR) (0xB800_3508)

Bit	Name	Description	Mode	Default
31:24	DRC_D[7:0]	Pin Direction Configuration of Port D 0: Configured as input pin 1: Configured as output pin	RW	00H
23:16	DRC_C[7:0]	Pin Direction Configuration of Port C 0: Configured as input pin 1: Configured as output pin	RW	00H
15:8	DRC_B[7:0]	Pin Direction Configuration of Port B 0: Configured as input pin 1: Configured as output pin	RW	00H
7:0	DRC_A[7:0]	Pin Direction Configuration of Port A 0: Configured as input pin 1: Configured as output pin	RW	00H

7.1.4. Port A, B, C, D Data Register (PABCD_DAT) (0xB800_350C)

Table 20. Port A, B, C, D Data Register (PABCD_DAT) (0xB800_350C)

Bit	Name	Description	Mode	Default
31:24	PD_D[7:0]	Pin Data of Port D 0: Data=0 1: Data=1	RW	00H
23:16	PD_C[7:0]	Pin Data of Port C 0: Data=0 1: Data=1	RW	00H
15:8	PD_B[7:0]	Pin Data of Port B 0: Data=0 1: Data=1	RW	00H
7:0	PD_A[7:0]	Pin Data of Port A 0: Data=0 1: Data=1	RW	00H

7.1.5. Port A, B, C, D Interrupt Status Register (PABCD_ISR) (0xB800_3510)

Table 21. Port A, B, C, D Interrupt Status Register (PABCD_ISR) (0xB800_3510)

Bit	Name	Description	Mode	Default
31:24	IPS_D[7:0]	Interrupt Pending Status of Port D Write '1' to clear the interrupt	RW	00H
23:16	IPS_C[7:0]	Interrupt Pending Status of Port C Write '1' to clear the interrupt	RW	00H
15:8	IPS_B[7:0]	Interrupt Pending Status of Port B Write '1' to clear the interrupt	RW	00H
7:0	IPS_A[7:0]	Interrupt Pending Status of Port A Write '1' to clear the interrupt	RW	00H

7.1.6. Port A, B Interrupt Mask Register (PAB_IMR) (0xB800_3514)

Table 22. Port A, B Interrupt Mask Register (PAB_IMR) (0xB800_3514)

Bit	Name	Description	Mode	Default
31:30	PB7_IM[1:0]	PortB.7 Interrupt Mode	RW	00B
29:28	PB6_IM[1:0]	PortB.6 Interrupt Mode	RW	00B
27:26	PB5_IM[1:0]	PortB.5 Interrupt Mode	RW	00B
25:24	PB4_IM[1:0]	PortB.4 Interrupt Mode	RW	00B
23:22	PB3_IM[1:0]	PortB.3 Interrupt Mode	RW	00B
21:20	PB2_IM[1:0]	PortB.2 Interrupt Mode	RW	00B
19:18	PB1_IM[1:0]	PortB.1 Interrupt Mode	RW	00B
17:16	PB0_IM[1:0]	PortB.0 Interrupt Mode	RW	00B
15:14	PA7_IM[1:0]	PortA.7 Interrupt Mode	RW	00B
13:12	PA6_IM[1:0]	PortA.6 Interrupt Mode	RW	00B
11:10	PA5_IM[1:0]	PortA.5 Interrupt Mode	RW	00B
9:8	PA4_IM[1:0]	PortA.4 Interrupt Mode	RW	00B
7:6	PA3_IM[1:0]	PortA.3 Interrupt Mode	RW	00B
5:4	PA2_IM[1:0]	PortA.2 Interrupt Mode	RW	00B
3:2	PA1_IM[1:0]	PortA.1 Interrupt Mode	RW	00B
1:0	PA0_IM[1:0]	PortA.0 Interrupt Mode 00: Disable interrupt 01: Enable falling edge interrupt 10: Enable rising edge interrupt 11: Enable both falling or rising edge interrupt	RW	00B

7.1.7. Port C, D Interrupt Mask Register (PCD_IMR) (0xB800_3518)

Table 23. Port C, D Interrupt Mask Register (PCD_IMR) (0xB800_3518)

Bit	Name	Description	Mode	Default
31:30	PD7_IM[1:0]	PortD.7 Interrupt Mode	RW	00B
29:28	PD6_IM[1:0]	PortD.6 Interrupt Mode	RW	00B
27:26	PD5_IM[1:0]	PortD.5 Interrupt Mode	RW	00B
25:24	PD4_IM[1:0]	PortD.4 Interrupt Mode	RW	00B
23:22	PD3_IM[1:0]	PortD.3 Interrupt Mode	RW	00B
21:20	PD2_IM[1:0]	PortD.2 Interrupt Mode	RW	00B
19:18	PD1_IM[1:0]	PortD.1 Interrupt Mode	RW	00B
17:16	PD0_IM[1:0]	PortC.0 Interrupt Mode	RW	00B
15:14	PC7_IM[1:0]	PortC.7 Interrupt Mode	RW	00B
13:12	PC6_IM[1:0]	PortC.6 Interrupt Mode	RW	00B
11:10	PC5_IM[1:0]	PortC.5 Interrupt Mode	RW	00B
9:8	PC4_IM[1:0]	PortC.4 Interrupt Mode	RW	00B
7:6	PC3_IM[1:0]	PortC.3 Interrupt Mode	RW	00B
5:4	PC2_IM[1:0]	PortC.2 Interrupt Mode	RW	00B
3:2	PC1_IM[1:0]	PortC.1 Interrupt Mode	RW	00B

Bit	Name	Description	Mode	Default
1:0	PC0_IM[1:0]	PortC.0 Interrupt Mode 00: Disable interrupt 01: Enable falling edge interrupt 10: Enable rising edge interrupt 11: Enable both falling or rising edge interrupt	RW	00B

7.1.8. GPIO Port E, F, G, H Control Register (PEFGH_CNR) (0xB800_351C)

Table 24. GPIO Port E, F, G, H Control Register (PEFGH_CNR) (0xB800_351C)

Bit	Name	Description	Mode	Default
31:24	PFC_H[7:0]	Pin Function Configuration of Port H	RW	FFH
23:16	PFC_G[7:0]	Pin Function Configuration of Port G	RW	FFH
15:8	PFC_F[7:0]	Pin Function Configuration of Port F	RW	FFH
7:0	PFC_E[7:0]	Pin Function Configuration of Port E Bit Value: 0: Configured as GPIO pin 1: Configured as dedicated peripheral pin	RW	FFH

7.1.9. GPIO Port E, F, G, H Direction Register (PEFGH_DIR) (0xB800_3524)

Table 25. GPIO Port E, F, G, H Direction Register (PEFGH_DIR) (0xB800_3524)

Bit	Name	Description	Mode	Default
31:24	DRC_H[7:0]	Pin Direction Configuration of Port H 0: Configured as input pin 1: Configured as output pin	RW	00H
23:16	DRC_G[7:0]	Pin Direction Configuration of Port G 0: Configured as input pin 1: Configured as output pin	RW	00H
15:8	DRC_F[7:0]	Pin Direction Configuration of Port F 0: Configured as input pin 1: Configured as output pin	RW	00H
7:0	DRC_E[7:0]	Pin Direction Configuration of Port E 0: Configured as input pin 1: Configured as output pin	RW	00H

7.1.10. Port E, F, G, H Data Register (PEFGH_DAT) (0xB800_3528)

Table 26. Port E, F, G, H Data Register (PEFGH_DAT) (0xB800_3528)

Bit	Name	Description	Mode	Default
31:24	PD_H[7:0]	Pin Data of Port H 0: Data=0 1: Data=1	RW	00H
23:16	PD_G[7:0]	Pin Data of Port G 0: Data=0 1: Data=1	RW	00H
15:8	PD_F[7:0]	Pin Data of Port F 0: Data=0 1: Data=1	RW	00H
7:0	PD_E[7:0]	Pin Data of Port E 0: Data=0 1: Data=1	RW	00H

7.1.11. Port E, F, G, H Interrupt Status Register (PEFGH_ISR) (0xB800-352C)

Table 27. Port E, F, G, H Interrupt Status Register (PEFGH_ISR) (0xB800_352C)

Bit	Name	Description	Mode	Default
31:24	IPS_H[7:0]	Interrupt Pending Status of Port H Write '1' to clear the interrupt	RW	00H
23:16	IPS_G[7:0]	Interrupt Pending Status of Port G Write '1' to clear the interrupt	RW	00H
15:8	IPS_F[7:0]	Interrupt Pending Status of Port F Write '1' to clear the interrupt	RW	00H
7:0	IPS_E[7:0]	Interrupt Pending Status of Port E Write '1' to clear the interrupt	RW	00H

7.1.12. Port E, F Interrupt Mask Register (PEF_IMR) (0xB800_3530)

Table 28. Port E, F Interrupt Mask Register (PEF_IMR) (0xB800_3530)

Bit	Name	Description	Mode	Default
31:30	PF7_IM[1:0]	PortF.7 Interrupt Mode	RW	00B
29:28	PF6_IM[1:0]	PortF.6 Interrupt Mode	RW	00B
27:26	PF5_IM[1:0]	PortF.5 Interrupt Mode	RW	00B
25:24	PF4_IM[1:0]	PortF.4 Interrupt Mode	RW	00B
23:22	PF3_IM[1:0]	PortF.3 Interrupt Mode	RW	00B
21:20	PF2_IM[1:0]	PortF.2 Interrupt Mode	RW	00B
19:18	PF1_IM[1:0]	PortF.1 Interrupt Mode	RW	00B
17:16	PF0_IM[1:0]	PortF.0 Interrupt Mode	RW	00B
15:14	PE7_IM[1:0]	PortE.7 Interrupt Mode	RW	00B
13:12	PE6_IM[1:0]	PortE.6 Interrupt Mode	RW	00B
11:10	PE5_IM[1:0]	PortE.5 Interrupt Mode	RW	00B
9:8	PE4_IM[1:0]	PortE.4 Interrupt Mode	RW	00B
7:6	PE3_IM[1:0]	PortE.3 Interrupt Mode	RW	00B

Bit	Name	Description	Mode	Default
5:4	PE2_IM[1:0]	PortE.2 Interrupt Mode	RW	00B
3:2	PE1_IM[1:0]	PortE.1 Interrupt Mode	RW	00B
1:0	PE0_IM[1:0]	PortE.0 Interrupt Mode 00: Disable interrupt 01: Enable falling edge interrupt 10: Enable rising edge interrupt 11: Enable both falling or rising edge interrupt	RW	00B

7.1.13. Port G, H Interrupt Mask Register (PGH_IMR) (0xB800_3534)

Table 29. Port G, H Interrupt Mask Register (PGH_IMR) (0xB800_3534)

Bit	Name	Description	Mode	Default
31:30	PH7_IM[1:0]	PortH.7 Interrupt Mode	RW	00B
29:28	PH6_IM[1:0]	PortH.6 Interrupt Mode	RW	00B
27:26	PH5_IM[1:0]	PortH.5 Interrupt Mode	RW	00B
25:24	PH4_IM[1:0]	PortH.4 Interrupt Mode	RW	00B
23:22	PH3_IM[1:0]	PortH.3 Interrupt Mode	RW	00B
21:20	PH2_IM[1:0]	PortH.2 Interrupt Mode	RW	00B
19:18	PH1_IM[1:0]	PortH.1 Interrupt Mode	RW	00B
17:16	PH0_IM[1:0]	PortH.0 Interrupt Mode	RW	00B
15:14	PG7_IM[1:0]	PortG.7 Interrupt Mode	RW	00B
13:12	PG6_IM[1:0]	PortG.6 Interrupt Mode	RW	00B
11:10	PG5_IM[1:0]	PortG.5 Interrupt Mode	RW	00B
9:8	PG4_IM[1:0]	PortG.4 Interrupt Mode	RW	00B
7:6	PG3_IM[1:0]	PortG.3 Interrupt Mode	RW	00B
5:4	PG2_IM[1:0]	PortG.2 Interrupt Mode	RW	00B
3:2	PG1_IM[1:0]	PortG.1 Interrupt Mode	RW	00B
1:0	PG0_IM[1:0]	PortG.0 Interrupt Mode 00: Disable interrupt 01: Enable falling edge interrupt 10: Enable rising edge interrupt 11: Enable both falling or rising edge interrupt	RW	00B

7.2. GPIO Shared Pin Configured Mapping List

The RTL8198 GPIO pins are shared with the other functions.

7.2.1. Shared Pin Register (PIN_MUX_SEL,0xB800_0040~0xB800_0043h)

Table 30. Shared Pin Register (PIN_MUX_SEL,0xB800_0040~0xB800_0043h)

Bit	Bit Name	Description	Mode	Default
31:15	Reserved	Reserved	-	-
14	reg_iocfg_spi	Configure GPIOG1 Pin as GPIO Mode 0: Reserved 1: GPIO	RW	0B
13:12	reg_iocfg_fcs1n	Configure SF_CS1# Pin as flash or GPIO Mode 0x: Reserved 10: SF_CS1# 11: GPIO	RW	00B
11:10	reg_iocfg_p5mii_2	Configure P5_TXD[7:4], P5_RXD[7:4] Pins as GMII, DBG, or GPIO Mode 0x: P5_TXD[7:4], P5_RXD[7:4] 10: DBG 11: GPIO	RW	00B
9:8	reg_iocfg_p5mii	Configure GMII except P5_TXD[7:4], P5_RXD[7:4] Pins as GMII/RGMII/MII, DBG, or GPIO Mode 00: GMII/RGMII/MII 10: DBG 11: GPIO	RW	00B
7:6	reg_iocfg_pcie	Configure PCIE_RST# Pin as PCIE, DBG, or GPIO Mode 0x: PCIE_RST# 10: DBG 11: GPIO	RW	00B
5	reg_iocfg_uart	Configure UART0_TX, UART0_RX Pins as UART or GPIO Mode 0: UART 11: GPIO	RW	0B
4:3	reg_iocfg_jtag	Configure JTAG Pins as JTAG, DBG, or GPIO Mode 00: JTAG 01: UART1 10: DBG 11: GPIO	RW	00B
2:1	reg_iocfg_gpioh	Configure GPIOH Pins as USB, DBG, or GPIO Mode 00: Reserved 01: USB 10: DBG 11: GPIO	RW	00B
0	Reserved	Reserved	-	-

7.2.2. Shared Pin Register (PIN_MUX_SEL_2,0xB800_0044~0xB800_0047h)

Table 31. Shared Pin Register (PIN_MUX_SEL_2,0xB800_0044~0xB800_0047h)

Bit	Bit Name	Description	Mode	Default
31:25	Reserved	Reserved	-	-
24	reg_iocfg_led_p4	Configure LED_P4 Pin as LED-SW, or GPIO Mode 0: LED-SW 1: GPIO	RW	0B
23:22	reg_iocfg_led_p3	Configure LED_P3 Pin as LED-SW, DBG, or GPIO Mode 00: LED-SW 01: Reserved 10: DBG 11: GPIO	RW	00B
21	Reserved	Reserved	-	-
20:19	reg_iocfg_led_p2	Configure LED_P2 Pin as LED-SW, DBG, or GPIO Mode 00: LED-SW 01: Reserved 10: DBG 11: GPIO	RW	00B
18	Reserved	Reserved	-	-
17:16	reg_iocfg_led_p1	Configure LED_P1 Pin as LED-SW, DBG, or GPIO Mode 00: LED-SW 01: Reserved 10: DBG 11: GPIO	RW	00B
15	Reserved	Reserved	-	-
14:13	reg_iocfg_led_p0	Configure LED_P0 Pin as LED-SW, DBG, or GPIO Mode 00: LED-SW 01: Reserved 10: DBG 11: GPIO	RW	00B
12	Reserved	Reserved	-	-
11:10	reg_iocfg_led_s3	Configure LED_S3 Pin as LED-SW, DBG, or GPIO Mode 00: LED-SW 01: Reserved 10: DBG 11: GPIO	RW	00B
9	Reserved	Reserved	-	-
8:7	reg_iocfg_led_s2	Configure LED_S2 Pin as LED-SW, DBG, or GPIO Mode 00: LED-SW 01: Reserved 10: DBG 11: GPIO	RW	00B
6	Reserved	Reserved	-	-
5:4	reg_iocfg_led_s1	Configure LED_S1 Pin as LED-SW, DBG, or GPIO Mode 00: LED-SW 01: Reserved 10: DBG 11: GPIO	RW	00B
3	Reserved	Reserved	-	-
2:1	reg_iocfg_led_s0	Configure LED_S0 Pin as LED-SW, DBG, or GPIO Mode 00: LED-SW 01: Reserved 10: DBG 11: GPIO	RW	00B
0	Reserved	Reserved	-	-

8. Green Ethernet

8.1. Cable Length Power Saving

The RTL8198 provides link-on and dynamic detection of cable length, and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

8.2. Link Down Power Saving

The RTL8198 implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. A port automatically enters link down power saving mode ten seconds after the cable is disconnected from it. Once a port enters link down power saving mode, it transmits normal link pulses on its TXOP/TXON pins and continues to monitor the RXIP/RXIN pins to detect incoming signals, which might be 100Base-TX MLT-3 idle pattern, 10Base-T link pulses, or Auto-Negotiation's FLP (Fast Link Pulse). After it detects an incoming signal, it wakes up from link down power saving mode and operates in normal mode according to the result of the connection.

8.3. Energy Efficient Ethernet (EEE)

The RTL8198 supports IEEE 802.3az Draft 3.0, also known as Energy Efficient Ethernet (EEE) in 100/1000base-TX in full duplex operation, and 10base-T in full/half duplex mode. This standard is being developed by the IEEE 802.3az Task Force, and should be finalized by September 2010. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled, however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported and to select the best set of parameters common to both devices.

- For 1000Base-T PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle.
- For 100Base-TX PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle.

- For 10Base-T, EEE defines a 10Mbps PHY (10Base-Te) with reduced transmit amplitude requirements. 10Base-Te is fully interoperable with 10Base-T PHYs over 100m of class-D (Cat-5) cable.

The RTL8198 MAC uses Low Power Idle signaling to indicate to the PHY and to the link partner that a break in the data stream is expected. Components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it informs the LPI Client that the link partner has sent such an indication.

9. Non-Flash Booting Interface (NFBI)

The RTL8198 total system acts in a PHY chip slave role for external host CPU master use.

- Designed with standard MDC/MDIO frame format
- PHY ID parser provided
- Supports forced RTL8198 CPU reset and enter into holding mode
- For burst read/write data, automatic increment of adjacent RAM address register

9.1. Block Diagram

The RTL8198 total system simulates a pure PHY function, and uses a standard MDC/MDIO interface to communicate with an external host CPU. The transfer data protocol is standard MDC/MDIO frame format.

On power up, the external host CPU needs to reset the RTL8198, and then read the PHYID register to check that the MDC/MDIO bus is operating correctly. Next it checks that the 'NeedBootCode' bit=1, which means the NFBI (Non-Flash Booting Interface) module is ready.

If transferring the kernel into DRAM, first the DRAM configuration and timing register must be set to suitable values. After transferring all software code, the external host CPU uses the 'StartRunBootcode' bit to allow the RTL8198 to begin booting. After the 'kernel code' boot is completed, software will respond with the 'All Software Ready' bit to notify the external host CPU that the software is ready.

The following block shows the hardware pins between the external host CPU and RTL8198 system.

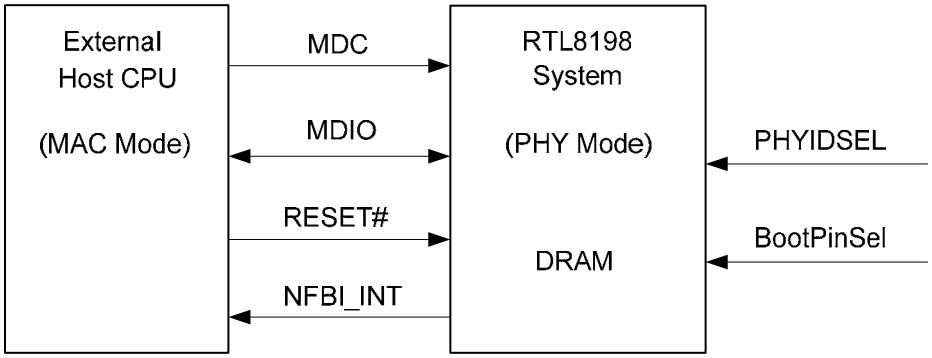


Figure 3. NFBI (Non-Flash Booting Interface)

9.2. NFBI Frame Format

The RTL8198 NFBI unit follows the same serial frame format as the IEEE 802.3 MDC/MDIO Interface. It acts in a slave role and will only respond to a command with a valid PHYID. The frame format is show in Table 32.

Table 32. NFBI Frame Format

	Preamble (8~32 bits)	Start (2 bits)	OP Code (2 bits)	PHYID (5 bits)	REGAD (5 bits)	Turn Around (2 bits)	Data (16 bits)	Idle
Read	1……..1	01	10	$A_4A_3A_2A_1A_0$	$R_4R_3R_2R_1R_0$	Z0	D_{15}…….D_0	Z*
Write	1……..1	01	01	$A_4A_3A_2A_1A_0$	$R_4R_3R_2R_1R_0$	10	D_{15}…….D_0	Z*

Note: PHYID[4:0]: Each PHY will be configured with a unique PHYID (default value is by hardware strapping pin).

9.3. NFBI Register Address Mapping

The RTL8198 supports the following register set for NFBI control functions.

Table 33. NFBI Register Address Mapping

REGAD[4:0]	Name	Size (Byte)	Register Name
0x02	PHYID1	2	PHY Identifier Register 1.
0x03	PHYID2	2	PHY Identifier Register 2.
0x10	CMD	2	Command Register.
0x11	ADDH	2	Address High Register.
0x12	ADDL	2	Address Low Register.
0x13	DH	2	Data High Register.
0x14	DL	2	Data Low Register.
0x15	SCR	2	Send Command Register.
0x16	RSR	2	Receive Status Register
0x17	SYSSR	2	System Status Register.
0x19	IMR	2	Interrupt Mask Register
0x1A	ISR	2	Interrupt Status Register

9.4. PHY Identifier Registers

The PHY Identifier Registers #1 and #2 together form a unique identifier for the PHY section of this device. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number.

Table 34. PHY Identifier Register 1 (REGAD 0x02)

Bit	Name	Description	Mode	Default
15:0	OUI_MSB	Composed of the 3rd to 18th Bits of the Organizationally Unique Identifier (OUI), Respectively.	RO	001CH

Table 35. PHY Identifier Register 2 (REGAD 0x03)

Bit	Name	Description	Mode	Default
15:10	OUI_LSB	Assigned to the 19th through 24th Bits of the OUI.	RO	110010B
9:4	Model Number	Manufacturer's Model Number.	RO	111000B
3:0	Revision Number	Manufacturer's Revision Number.	RO	0001B

9.5. Command Register

Table 36. Command Register (REGAD 0x10)

Bit	Name	Description	Mode	Default
15	CMDType	Command Type. 0: Bus Write Access command. The external host CPU writes data to the RTL8198 CPU 1: Bus Read Access command. The external host CPU reads data from the RTL8198 *Note: Writing 1 causes hardware to pre-fetch a memory word. If CMDType changes from Write to Read mode, be sure that ADDR is set correctly before changing the set CMDType to read mode.*	RW	0B
14	Busy	1: Busy. When the busy bit is high, the external CPU cannot read/write any Address or Data. 0: Done. When busy is low, NFBI can read/write address and data. Hardware will automatically clear this bit. Software can query this bit to check NFBI hardware status.	RO	0B
13:3	-	Reserved	-	-
2	IntLevel	Select interrupt level. 1: In normal operation with no interrupt having occurred, the signal NFBI_INT bit is low. When an interrupt occurs, NFBI_INT is high. 0: In normal operation with no interrupt having occurred, the signal NFBI_INT bit is high. When an interrupt occurs, NFBI_INT is low.	RW	0
1	SystemRst	The External Host CPU can write 1 to force a RTL8198 whole system reset at any time. After the hardware reset is completed, this bit automatically returns to zero.	RW	0B

Bit	Name	Description	Mode	Default
0	StartRunBootCode	After all transfer code is ready in RAM, the external host CPU will write 1 to let the RTL8198 CPU release pending mode and start to run the boot code. 1: Leave holding mode and start to run boot code 0: Ignore Read back is CPU status. 0: Pending mode 1: Running mode	RW	0

9.6. Address Registers

The External host CPU can read/write any address of the RTL8198 SDRAM and built-in SRAM. The RTL8198 CPU address and data bus width are all 32 bits, but the MDC/MDIO bus width is 16 bits. The read/write Address and Data register width is divided into the higher and lower register, and the minimal transfer data length is 4 bytes (one word, 32 bits).
When transferring boot code, the access address register is sequential by order. To save bandwidth, only a contiguous read/write data request is required, and the contiguous read/write address value is ignored. This is because the NFBI unit automatically increases the address value when accessing RAM.

Table 37. Address Register (High) (REGAD 0x11)

Bit	Name	Description	Mode	Default
15:0	ADDH[31:16]	Address Bus Higher 16 Bits.	RW	1FC0H

Table 38. Address Register (Low) (REGAD 0x12)

Reg.bit	Name	Description	Mode	Default
15:0	ADDL[15:0]	Address Bus Lower 16 Bits.	RW	0000H

9.7. Data Register

When writing the 'Data Register', be sure the write sequence is 'write high data (MSB) first' and then low data (LSB) later. This is because writing the low data register will trigger a hardware latch circuit and start a read/write procedure.

Table 39. Data Register (High) (REGAD 0x13)

Bit	Name	Description	Mode	Default
15:0	DATAH[31:16]	Read/Write Access Physical Data Bus.	RW	0000H

Table 40. Data Register (Low) (REGAD 0x14)

Bit	Name	Description	Mode	Default
15:0	DATAL[15:0]	Read/Write Access Physical Data Bus Lower 16 Bits. When this register is written, it will trigger a write procedure. It will write DATA[31:0] values to SRAM at ADD[31:0]. The built-in Address Counter will automatically increase.	RW	0000H

9.7.1. Command and Status Register

There are two communication channels between the external host CPU and the RTL8198 CPU. From the external host CPU view, one line sends commands to the RTL8198 CPU; another line is read-only and receives the status from RTL8198 CPU writes. The transfer command and status message communication is defined in Table 41 and Table 42.

Table 41. Send Command Register (REGAD 0x15)

Bit	Name	Description	Mode	Default
15:0	MsgID	External host CPU send Message ID to RTL8198 CPU	RW	0

Table 42. Receive Status Register (REGAD 0x16)

Bit	Name	Description	Mode	Default
15:0	MsgID	External host CPU receive Message ID from RTL8198 CPU write in. This register value is the same as the 'RTL8198 CPU Send Booting Status Register'.	R	0

9.8. System Status Register

The RTL8198 CPU reports the whole system status to an external host CPU to monitor device status.

Table 43. System Status Register (REGAD 0x17)

Bit	Name	Description	Mode	Default
15	CheckSumDone	1: Boot code kernel checksum done 0: Boot code has not done a checksum, or a checksum is in progress	R	0B
14	CheckSumOK	1: Checksum OK 0: Checksum fail This bit value is valid when the 'CheckSumDone' bit=1.	R	0B
13:11	-	Reserved	-	-
10	AllSoftwareReady	0: All software is not ready (possibly still booting) 1: All software has booted OK and is ready	R	0B
9:6	-	Reserved	-	-
5	Bootcode Ready	Bootcode Ready Status. Each time the boot loader boots up successfully, this bit will be modified from 1 to 0 or from 0 to 1 to indicate the boot loader is ready for service	R	0
4:0	-	Reserved	-	-

9.8.1. Interrupt Mask Register

Table 44. Interrupt Mask Register (REGAD 0x19)

Bit	Name	Description	Mode	Default
15	CheckSumDoneMask	CheckSumDone Mask. 0: Disable 1: Enable	RW	0
14	CheckSumOKMask	CheckSumOK Mask. 0: Disable 1: Enable	RW	0
13:11	-	Reserved	RW	0
10	AllSoftwareReadyMask	All Software Ready Mask. 0: Disable 1: Enable	RW	0
9:6	-	Reserved.	RW	0
5	BootcodeReadyMask	Bootcode Ready Mask. 0: Disable 1: Enable	RW	0
4:3	-	Reserved	RW	0
2	PrevMsgFetchMask	Previous Message has been Fetch Mask. 0: Disable 1: Enable	RW	0
1	NewMsgComingMask	New Message has Coming Mask. 0: Disable 1: Enable	RW	0
0	NeedBootCodeMask	Need Boot Code Mask. 0: Disable 1: Enable	RW	1

9.8.2. Interrupt Status Register

Table 45. Interrupt Status Register (REGAD 0x1A)

Bit	Name	Description	Mode	Default
15	CheckSumDoneIP	CheckSumDone Interrupt Pending. Write 1 to clear.	RW	0
14	CheckSumOKIP	CheckSumOK Interrupt Pending. Write 1 to clear.	RW	0
13:11	-	Reserved	RW	0
10	AllSoftwareReadyIP	All Software Ready Interrupt Pending. Write 1 to clear.	RW	0
9:6	-	Reserved	RW	0
5	BootcodeReadyIP	Bootcode Ready Interrupt Pending. Write 1 to clear.	RW	0
4:3	-	Reserved.	RW	0
2	PrevMsgFetchIP	Previous Message Fetch Interrupt Pending. When a message has been sent from the external host CPU to the RTL8198 CPU, and the RTL8198 has fetched the message and performed the interrupt service, this bit=1. This function is used to inform the external host CPU that Send Command Register (SCR) data was already fetched by the RTL8198 CPU. Write 1 to clear.	RW	0
1	NewMsgComingIP	New Message Coming Interrupt Pending. When a New Message is ready to be sent from the RTL8198 CPU to the external host CPU, this bit=1. The external host CPU then reads the Receive Status Register (RSR) for more information. Write 1 to clear.	RW	0
0	NeedBootCodeIP	Need Boot Code Interrupt Pending. After power on and the RTL8198 CPU is ready and waiting for boot code, this bit=1. When the external host CPU has finished transfering boot code, write 1 to clear.	RW	0

9.9. RTL8198 Internal CPU NFBI Control Register

The RTL8198 internal CPU uses these registers to control the NFBI (Non-Flash Booting Interface) block.

Table 46. CPU Internal Register Table (0xB801_9000)

Offset	Name	Size (byte)	Register Name
0x00	RCR	4	Receive Command Register
0x04	SSR	4	Send Status Register
0x10	IMR	4	Interrupt Mask Register
0x14	ISR	4	Interrupt Status Register

9.9.1. Receive Command and Send Status Register

There are two communication channels between the external host CPU and the RTL8198 CPU.

From the RTL8198 CPU's view, one line is read-only and receives commands from the external host CPU; another line sends the status to the external host CPU.

From the external host CPU view, one line sends commands to the RTL8198 CPU; another line is read-only and receives the status from RTL8198 CPU writes. The receive command and status message communication is defined in Table 47 and Table 48.

Table 47. RTL8198 CPU Receive Command Register (0xB801_9000)

Bit	Name	Description	Mode	Default
31:16	-	Reserved	-	-
15:0	MsgID	The RTL8198 CPU received a Message ID after an external host CPU write. This register value is the same as the 'External Host CPU Send Booting Status Register'.	R	0

Table 48. RTL8198 CPU Send Status Register (0xb801_9004)

Bit	Name	Description	Mode	Default
31:16	-	Reserved	-	-
15:0	MsgID	The RTL8198 CPU sent a Message ID to the external host CPU.	RW	0

9.9.2. Interrupt Mask and Interrupt Status Register On NFBI

Table 49. RTL8198 NFBI Interrupt Mask Register (0xB801_9010)

Bit	Name	Description	Mode	Default
31:3	-	Reserved	RW	0
2	PrevMsgFetchMask	Previous Message Fetch Interrupt Enable. 0: Disable 1: Enable	RW	0
1	NewMsgComingMask	New Message Coming Interrupt Enable. 0: Disable 1: Enable	RW	0
0	-	Reserved	RW	0

Table 50. RTL8198 NFBI Interrupt Status Register (0xB801_9014)

Bit	Name	Description	Mode	Default
31:3	-	Reserved	RW	0
2	PrevMsgFetchByHostIP	Previous Message Fetch By Host Pending. When a message has been sent from the RTL8198 CPU to the external host CPU, and the external host CPU has fetched the message and performed the interrupt service, this bit=1. This function is used to inform the RTL8198 CPU that Send Status Register (SSR) data was already fetched by the external host CPU. Write 1 to clear.	RW	0
1	NewMsgFromHosIP	New Message From Host Interrupt Pending. When a New Message is ready to be sent from the external host CPU to the RTL8198 CPU, this bit=1. The RTL8198 CPU then reads the Receive Command Register (RCR) for more information. Write 1 to clear.	RW	0
0	-	Reserved	RW	0

10. DC Specifications

10.1. Operating Conditions

Table 51. Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD33	Digital I/O Power Supply 3.3V	3.135	3.3	3.465	V
AVDD33	Analog Power Supply 3.3V	3.135	3.3	3.465	V
VDD10	Core Power Supply 1.0V	0.95	1.0	1.05	V
AVDD10	Analog Power Supply 1.0V	0.95	1.0	1.05	V
AVDD33_X25M	25M Crystal Power 3.3V	3.135	3.3	3.465	V
VDD33_BG	System Bandgap Power Supply 3.3V	3.135	3.3	3.465	V
AVDD10_PCIE	PCI Express Analog Power 1.0V	0.95	1.0	1.05	V
AVDD10_SYSPLL	System PLL Power 1.0V	0.95	1.0	1.05	V
VDD10_PHYPLL	Ethernet PHY PLL Power 1.0V	0.95	1.0	1.05	V
AVDD10_USBPLL	USB2.0 PLL Power 1.0V	0.95	1.0	1.05	V
AVDD33_USB	USB2.0 Analog Power 3.3V	3.135	3.3	3.465	V
AVDD10_USB	USB2.0 Analog Power 1.0V	0.95	1.0	1.05	V
VDD33/25	SDR DRAM I/O Power Supply 3.3V	3.135	3.3	3.465	V
	DDR1 DRAM I/O Power Supply 2.5V	2.4	2.5	2.7	
	DDR2 DRAM I/O Power Supply 1.8V	1.7	1.8	1.9	
VREF	DDR1/DDR2 Reference Voltage	0.49*VDD25	0.5*VDD25	0.51*VDD25	V

10.2. Total Power Consumption

Table 52. Total Power Consumption

SYM	Conditions	Min	Typ.	Max	Units
PS	All LAN Ports Idle and CPU Suspended	-	0.96	-	Watt
	All LAN Ports Idle	-	1.32	-	
	LAN Full Load Active for Link at 10Base-T	-	1.56	-	
	LAN Full Load Active for Link at 100Base-TX	-	1.47	-	
	LAN Full Load Active for Link at 1000Base-TX	-	2.47	-	

Note: Power consumption is measured at full load of the chip system.

10.3. SDR DRAM Bus DC Parameters

Table 53. SDR DRAM Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	1
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	2
V_{OH}	Output-High Voltage	-	2.4	-	-	V	3
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	3
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	µA	-
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	µA	-
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	4
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	4

Note 1: V_{IH} overshot: $V_{IH\ (MAX)}$=V_{DDH} + 2V for a pulse width ≤ 3ns, and the pulse width not greater than one third of the cycle rate.

Note 2: V_{IL} undershot: $V_{IL\ (MIN)}$=-2V for a pulse width ≤ 3ns cannot be exceeded.

Note 3: The output current buffer is 16mA for SDR DRAM clock, address, and data bus.

Note 4: These values are typical values checked in the manufacturing process and are not tested.

10.4. DDR DRAM Bus DC Parameters

Table 54. DDR DRAM Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	SSTL_2	VREF+0.15	-	VREF+0.3	V
V_{IL}	Input-Low Voltage	SSTL_2	-0.3	-	VREF-0.15	V
V_{TT}	I/O Termination Voltage	-	VREF-0.04	-	VREF+0.04	V
I_{IL}	Input-Leakage Current	V_{IN}=VREF or 0	-10	±1	10	µA
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	µA

10.5. Flash Bus DC Parameters

Table 55. Flash Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	1
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	2
V_{OH}	Output-High Voltage	-	2.4	-	-	V	3
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	3
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	µA	-
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	µA	-
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	4
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	4

Note 1: V_{IH} overshot: VIH (MAX)=VDDH + 2V for a pulse width ≤ 3ns.

Note 2: V_{IL} undershot: $V_{IL\ (MIN)}$=-2V for a pulse width ≤ 3ns.

Note 3: The output current buffer is 8mA for the flash address and data bus; and is 8mA for Flash control signals.

Note 4: These values are typical values checked in the manufacturing process and are not tested.

10.6. USB v1.1 DC Parameters

Table 56. USB v1.1 DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	-	2.0	-	-	V	2
V_{IL}	Input-Low Voltage	-	-	-	0.8	V	2
V_{OH}	Output-High Voltage	-	2.4	-	-	V	2
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	2
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-	-	-	µA	1

Note 1: These values are typical values checked in the manufacturing process and are not tested.
Note 2: For additional information, see the USB v1.1 Specification.

10.7. USB v2.0 DC Parameters

Table 57. USB v2.0 DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	-	200	-	-	mV	2
V_{IL}	Input-Low Voltage	-	-	-	10	mV	2
V_{OH}	Output-High Voltage	-	300	-	500	mV	2
V_{OL}	Output-Low Voltage	-	-10	-	10	mV	2
I_{IL}	Input-Leakage Current	-	-	-	-	µA	1

Note 1: These values are typical values checked in the manufacturing process and are not tested.
Note 2: For additional information, see the USB v2.0 Specification.

10.8. UART DC Parameters

Table 58. UART DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	-	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	µA	2
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for UART related signals.
Note 2: These values are typical values checked in the manufacturing process and are not tested.

10.9. GPIO DC Parameters

Table 59. GPIO DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	-	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	-	-10	±1	10	μA	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for GPIO related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

10.10. JTAG DC Parameters

Table 60. JTAG DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	$\lvert I_{OH} \rvert$ =2~16mA	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	$\lvert I_{OL} \rvert$ =2~16mA	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	-	-10	±1	10	μA	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 4mA for JTAG related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

10.11. MII DC Parameters

Table 61. MII DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	-	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	μA	2
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	μA	2
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for MII related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

10.12. GMII DC Parameters

Table 62. GMII DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	-	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	-	-	-	0.8	V	-
V_{OH}	Output-High Voltage	-	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	-	-10	±1	10	µA	2
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	µA	2
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for GMII related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

10.13. RGMII DC Parameters

Table 63. RGMII DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	3.3V/2.5V	2.0/1.7	-	-	V	-
V_{IL}	Input-Low Voltage	3.3V/2.5V	-	-	0.8/0.7	V	-
V_{OH}	Output-High Voltage	3.3V/2.5V	2.4/2.0	-	-	V	1
V_{OL}	Output-Low Voltage	3.3V/2.5V	-	-	0.4/0.4	V	1
I_{IL}	Input-Leakage Current	-	-10	±1	10	µA	2
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	µA	2
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for RGMII related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

10.14. Reset DC Parameters

Table 64. Reset DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V

10.15. LED DC Parameters

Table 65. LED DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OHED}	Output-High Voltage	-	2.4	-	-	V
V_{OLLED}	Output-Low Voltage	-	-	-	0.4	V

Note: The output current buffer for LED signals is 8mA.

11. AC Specifications

11.1. Clock Signal Timing

Table 66. Clock Signal Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	-	-	0.8	V	-
$T_{FREQUENCY}$	Clock Frequency for RTL8198 Crystal or Oscillator	-	25	-	MHz	1
$\Delta_{FREQUENCY}$	Clock Tolerance Over 0ºC to 50ºC	-50	-	50	ppm	-
C_{SHUNT}	Crystal Parameter (Sometimes Referred to as the Holder Capacitance)	-	-	7	pF	2
C_1	Load Capacitance	-	-	30	pF	3
C_2	Load Capacitance	-	-	30	pF	3
T_{DC}	Duty Cycle	-	50	-	%	-

Note 1: This value could be an oscillator input or a series resonant frequency from a crystal. If used as an oscillator input, tie to the crystal input pin and leave the crystal output pin disconnected.

Note 2: The 25MHz Crystal CL=16pF is used on the RTL8198.

Note 3: The RTL8198 PLL circuit requires an external 25MHz crystal with shunt capacitors. These shunt capacitors cannot be over 30pF due to chip design requirements.

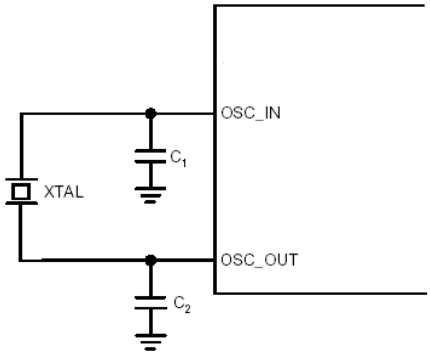


Figure 4. Typical Connection to a Crystal

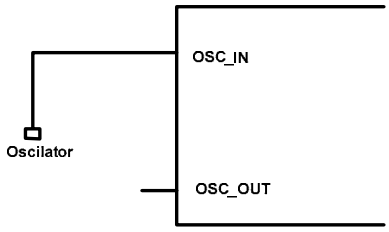


Figure 5. Typical Connection to an Oscillator

11.1.1. SDR DRAM Clock Timing

Table 67. SDR DRAM Clock Timing

Symbol	Parameter	130~180MHz			Units	Notes
		Min. (130MHz)	Typ. (160MHz)	Max. (180MHz)		
$T_{PERIOD\_SDRAMCLK}$	Clock Period for SDR DRAM Clock	7.7	6.25	5.5	ns	-
$T_{CLKHIGH}$	SDR DRAM Clock High Time	3.57	3.57	3.57	ns	-
T_{CLKLOW}	SDR DRAM Clock Low Time	3.57	3.57	3.57	ns	-
$T_{RISE/FALL}$	Rise and Fall Time Requirements for SDR DRAM Clock	-	-	2	ns	-
$T_{RISE/FALL\_OUTPUT}$	Propagation Delay for Output Rising and Falling	-	NA	-	ns	1

Note 1: For detailed information, contact Realtek for the IBIS model.

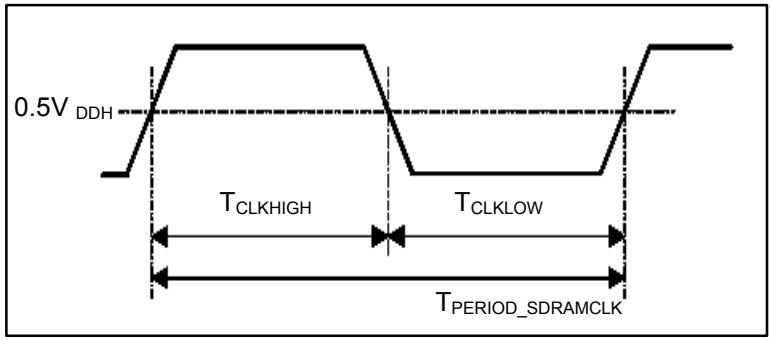


Figure 6. SDR DRAM Clock Specifications-1

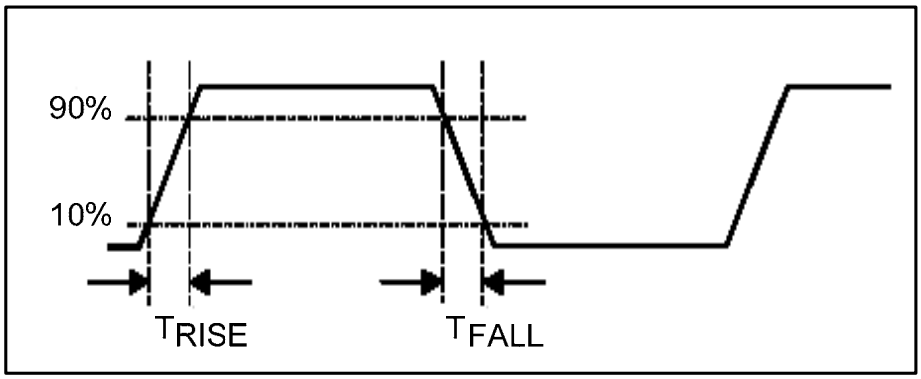


Figure 7. SDR DRAM Clock Specifications-2

11.1.2. MII Clock Timing

Table 68. MII Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$T_{PERIOD100Mbit}$	Clock Period for Tx and Rx Ethernet Clocks	-	25	25	-	-
$T_{PERIOD10Mbit}$	Clock Period for Tx and Rx Ethernet Clocks	-	2.5	2.5	MHz	-
T_{DUTY}	Duty Cycle for Tx and Rx Ethernet Clocks	35	50	65	%	-
$T_{RISE/FALL}$	Rise And Fall Time Requirement for Tx and Rx Ethernet Clocks	-	-	2	ns	-
$T_{RISE/FALL\_OUTPUT}$	Propagation Delay for Output Rising and Falling	-	NA	-	ns	1

Note 1: For detailed contact Realtek for the IBIS model.

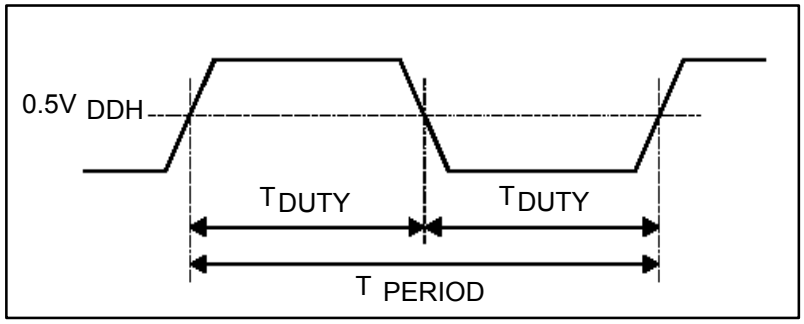


Figure 8. MII Clock Specifications-1

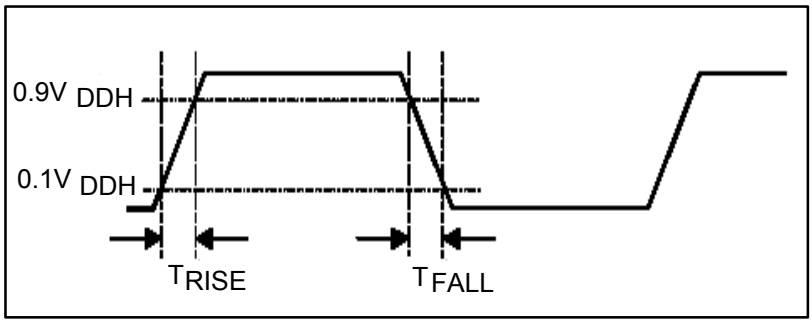


Figure 9. MII Clock Specifications-2

11.1.3. GMII Clock Timing

Table 69. GMII Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$T_{PERIOD1000Mbit}$	Clock Period for Tx and Rx Ethernet Clocks	-	8	-	-	-
T_{DUTY}	Duty Cycle for Tx and Rx Ethernet Clocks	35	50	65	%	-
$T_{RISE/FALL}$	Rise and Fall Time Requirement for Tx and Rx Ethernet Clocks	-	-	1	ns	-
$T_{RISE/FALL\_OUTPUT}$	Propagation Delay for Output Rising and Falling	-	N.A.	-	ns	1

Note 1: For detailed information contact Realtek for the IBIS model.

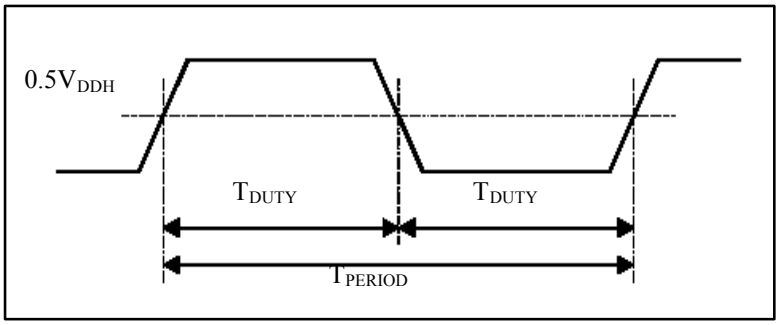


Figure 10. GMII Clock Specifications-1

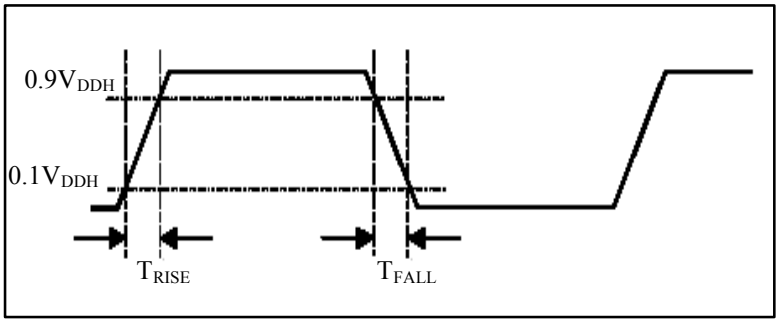


Figure 11. GMII Clock Specifications-2

11.1.4. RGMII Clock Timing

Table 70. RGMII Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$T_{PERIOD1000Mbit}$	Clock Period for Tx and Rx Ethernet Clocks	7.2	8	8.8	-	-
T_{DUTY}	Duty Cycle for Tx and Rx Ethernet Clocks	45	50	55	%	-
$T_{RISE/FALL}$	Rise And Fall Time Requirement for Tx and Rx Ethernet Clocks (20~80%)	-	-	0.75	ns	-
$T_{RISE/FALL\_OUTPUT}$	Propagation Delay for Output Rising and Falling	-	-	-	ns	1

Note 1: For detailed information contact Realtek for the IBIS model.

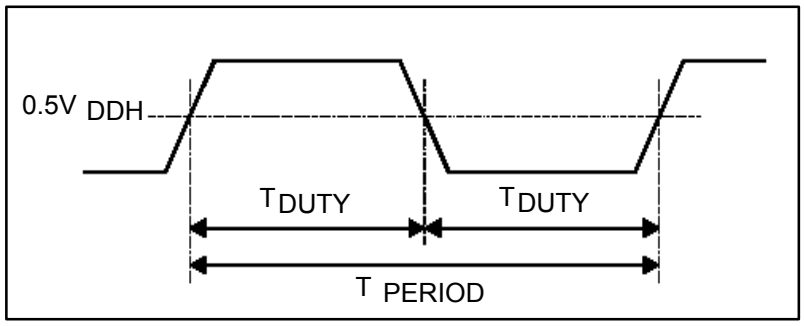


Figure 12. RGMII Clock Specifications-1

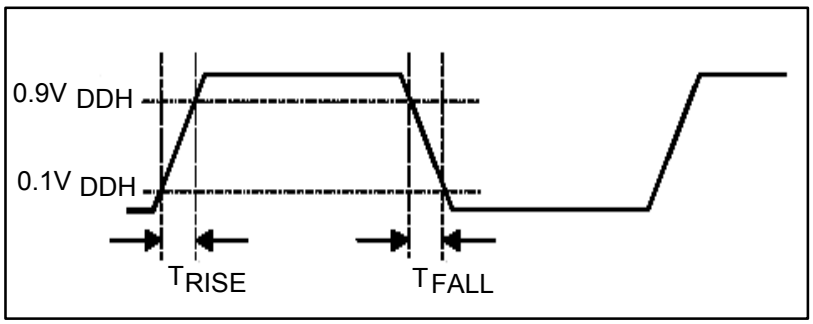


Figure 13. RGMII Clock Specifications-2

11.2. Bus Signal Timing

11.2.1. SDR DRAM Bus

11.2.1.1 SDR DRAM Input Timing

Table 71. SDR DRAM Input Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_{SETUP}	Input Setup Prior to Rising Edge of Clock Inputs included in this timing are D[31: 0] (during a read operation)	-	1.13	-	ns
T_{HOLD}	Input Hold Time after the Rising Edge of Clock Inputs included in this timing are D[31:0] (during a read operation)	-	0	-	ns

Note: The RTL8198 integrates some timing controls on the interface. Here the timing parameters listed in the table are extracted in the default situation (without specific controls).

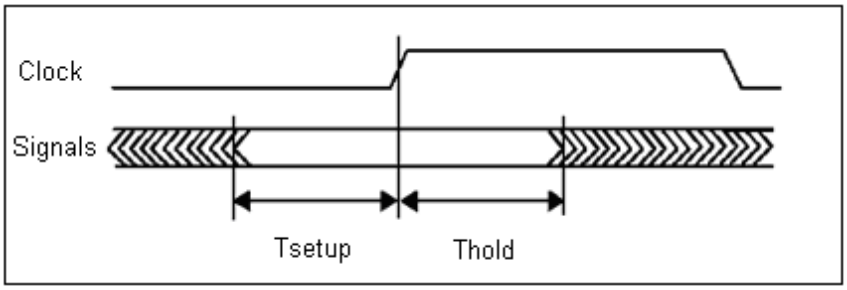


Figure 14. SDR DRAM Input Timing

11.2.1.2 SDR DRAM Output Timing

Table 72. SDR DRAM Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
$T_{CLK2OUT}$	Rising Edge of Clock-to-Signal Output. Outputs include this timing are D[31: 0], CS0#, CS1#, RAS#, CAS#, LDQM, UDQM, WE# (during a write operation)	-	-	2.3	ns
$T_{HOLDOUT}$	Signal Output Hold Time after the Rising Edge of the Clock. Outputs included in this timing are D[31: 0] (during a write operation)	0.8	-	-	ns

Note: Timing was tested with 75-pF capacitor to ground.

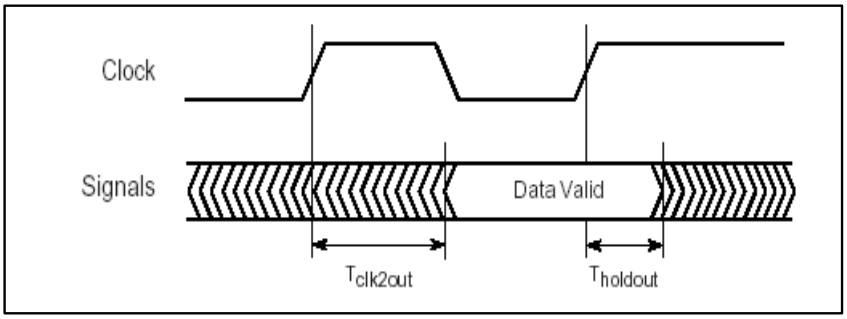


Figure 15. SDR DRAM Output Timing

11.2.1.3 SDR DRAM Access Control Timing

Table 73. SDR DRAM Access Control Timing

Symbol	Parameter	Units	Notes
$T_{REFRESH}$	Auto-Refresh Timing Controlled by Reg. 0xB8001008 (DTR)	µs	-
T_{RCD}	The Time Interval between RAS# Active and CAS# Active Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RP}	The Time Interval between Pre-Charge and the Next Active Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RAS}	The Time Interval between Active and Pre-Charge Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RC}	The Time Interval between Active and the Next Active Controlled by Reg. 0xB8001008 (DTR)	ns	1
T_{RFC}	The Time Interval between Auto-Refresh and Active Controlled by Reg. 0xB8001008 (DTR)	ns	-
$T_{CAS\_LATENCY}$	The Data Output Delay after CAS# Active Controlled by Reg. 0xB8001004 (DCR)	ns	-

Note 1: TRC=TRAS+TRP.

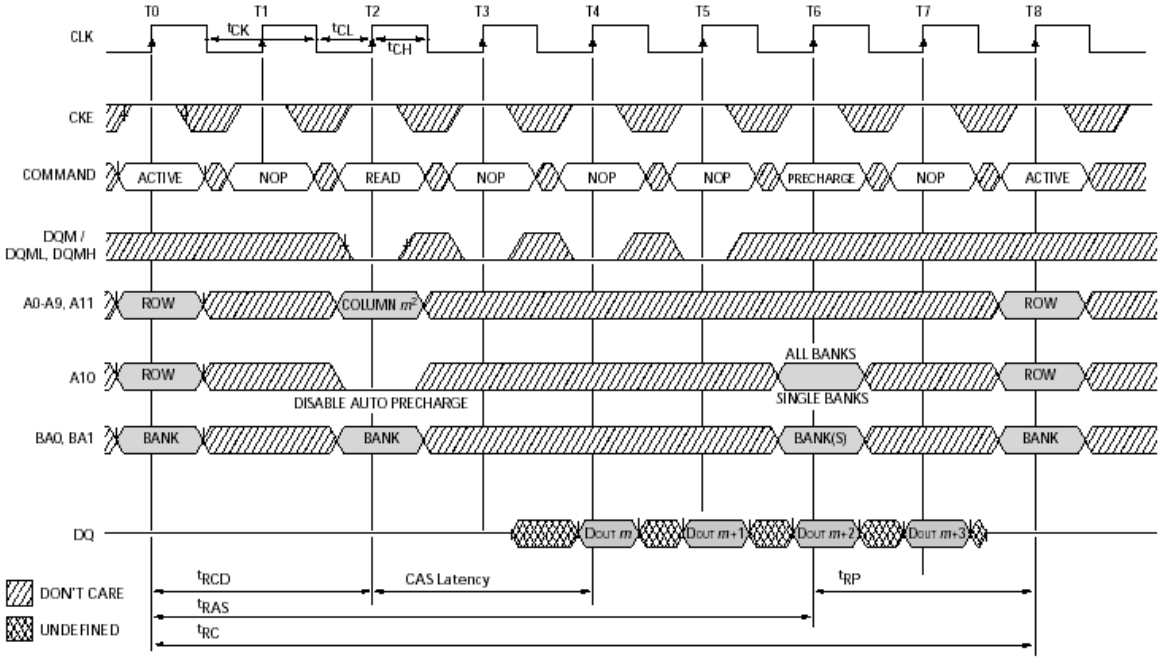


Figure 16. SDR DRAM Access Control Timing

11.2.2. DDR DRAM Bus

11.2.2.1 DDR DRAM Input Timing

Table 74. DDR DRAM Input Timing

Symbol	Parameter	Units	Notes
T_{SETUP}	Input Setup Prior to Rising Edge of Clock. Inputs included in this timing are D[31: 0] (during a read operation)	ns	1
T_{HOLD}	Input Hold Time after the Rising Edge of Clock. Inputs included in this timing are D[31:0] (during a read operation)	ns	1

Note1: The RTL8198 integrates some timing control registers on the interface.

11.2.2.2 DDR DRAM Output Timing

Table 75. DDR DRAM Output Timing

Symbol	Parameter	Units	Notes
$T_{CLK2OUT}$	Rising Edge of Clock-to-Signal Output. Outputs include this timing are D[31: 0], CS0#, CS1#, RAS#, CAS#, LDQM, UDQM, WE#, LDQS, UDQS (during a write operation)	ns	1
$T_{HOLDOUT}$	Signal Output Hold Time after the Rising Edge of the Clock. Outputs included in this timing are D[31: 0] (during a write operation)	ns	1

Note1: The RTL8198 integrates some timing control registers on the interface.

11.2.2.3 DDR DRAM Access Control Timing

Table 76. DDR DRAM Access Control Timing

Symbol	Parameter	Units	Notes
$T_{REFRESH}$	Auto-Refresh Timing. Controlled by Reg. 0xB8001008 (DTR)	µs	-
T_{RCD}	The Time Interval between RAS# Active and CAS# Active. Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RP}	The Time Interval between Pre-Charge and the Next Active. Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RAS}	The Time Interval between Active and Pre-Charge. Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RC}	The Time Interval between Active and the Next Active. Controlled by Reg. 0xB8001008 (DTR)	ns	1
T_{RFC}	The Time Interval between Auto-Refresh and Active. Controlled by Reg. 0xB8001008 (DTR)	ns	-
$T_{CAS\_LATENCY}$	The Data Output Delay after CAS# Active. Controlled by Reg. 0xB8001004 (DCR)	ns	-

Note 1: TRC=TRAS+TRP.

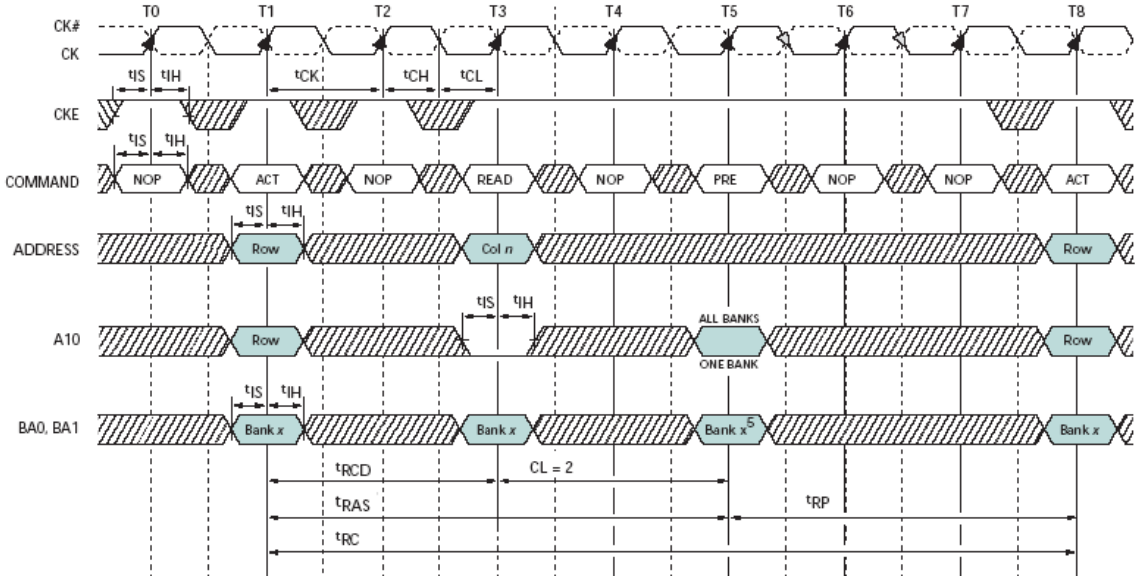


Figure 17. DDR DRAM Access Control Timing

11.2.3. Serial Flash Interface

11.2.3.1 Serial Flash Interface Output Timing

Table 77. Serial Flash Interface Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_{SLCH}	The Timing Interval from Chip-Select Activated to the First Clock Rising Edge	$0.5*T_{SFCK}$ - 1	-	$0.5*T_{SFCK}$	ns
T_{CHSH}	The Timing Interval from the Last Clock Rising Edge to Chip-Select De-Activated	T_{SFCK} + 7	-	T_{SFCK} + 9	ns
T_{CLQV}	The Timing Interval from the Last Clock Falling Edge to Data-Out Validated	-	-	1	ns
T_{CLQX}	The Timing Interval from the Next Clock Falling Edge to Data-Out Invalidated	-1	-	-	ns

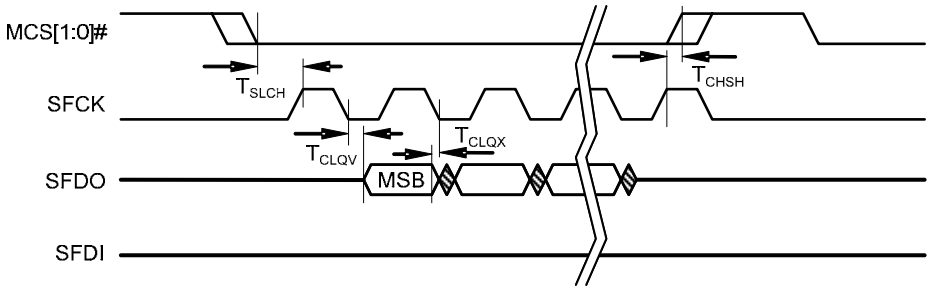


Figure 18. Serial Flash Interface Output Timing

11.2.3.2 Serial Flash Interface Intput Timing

Table 78. Serial Flash Interface Intput Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_{DVCH}	The Timing Interval from Data-Input Ready to the Clock Rising Edge	0	-	-	ns
T_{CHDX}	The Timing Interval from the Clock Rising Edge to Data-Input Invalidated	$0.5*T_{SFCK}$	-	-	ns

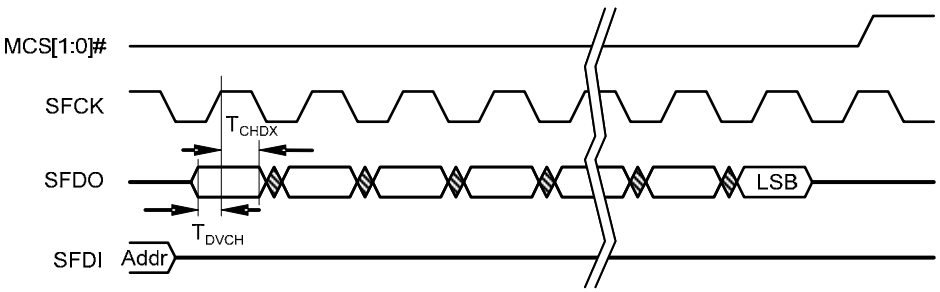


Figure 19. Serial Flash Interface Intput Timing

11.2.4. MII Interface

11.2.4.1 MII MAC Mode Output Timing

Table 79. MII MAC Mode Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_1	Clock Rising Edge to Output Delay for TXD[3:0] and TXEN	-	-	6	ns
T_2	Signal Output Hold Time after the Rising Edge of the TXCLK. Outputs included in this timing are TXD[3:0] and TXEN	3	-	-	ns

11.2.4.2 MII PHY Mode Output Timing

Table 80. MII PHY Mode Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_1	Clock Rising Edge to Output Delay for TXD[3:0] and TXEN	-	-	19	ns
T_2	Signal Output Hold Time after the Rising Edge of the TXCLK. Outputs included in this timing are TXD[3:0] and TXEN	21	-	-	ns

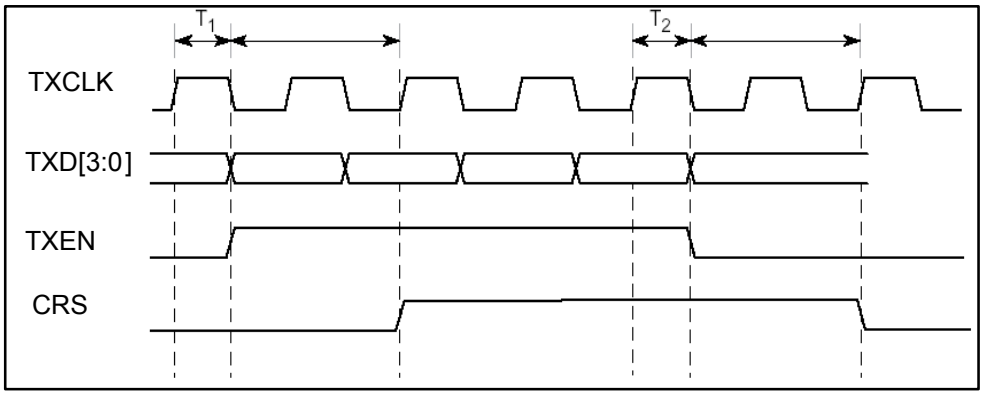


Figure 20. MII Output Timing

11.2.4.3 MII MAC Mode Input Timing Values

Table 81. MII MAC Mode Input Timing Values

Symbol	Parameter	Min.	Typ.	Max.	Units
T_3	RXD[3:0] and RXDV Setup Time Prior to Rising Edge of RXCLK	1	-	-	ns
T_4	RXD[3:0] and RXDV Hold Time after the Rising Edge of RXCLK	1	-	-	ns

11.2.4.4 MII PHY Mode Input Timing Values

Table 82. MII PHY Mode Input Timing Values

Symbol	Parameter	Min.	Typ.	Max.	Units
T_3	RXD[3:0] and RXDV Setup Time Prior to Rising Edge of RXCLK	7	-	-	ns
T_4	RXD[3:0] and RXDV Hold Time after the Rising Edge of RXCLK	0	-	-	ns

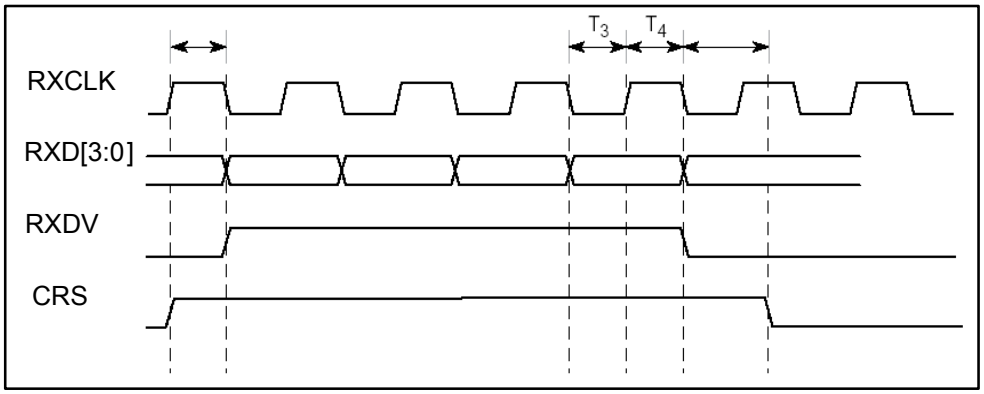


Figure 21. MII Input Timing

11.2.5. GMII Timing Characteristics

Table 83. GMII Timing Characteristics

Symbol	Description	Min	Typ.	Max	Units
T_{TX_SU}	Data to Clock Output Setup Time. Enable TXC delay	3	4	-	ns
T_{TX_HO}	Data to Clock Output Hold Time. Enable TXC delay	1	4	-	ns
T_{RX_SU}	Data to Clock Input Setup Time.	1.3	-	-	ns
T_{RX_HO}	Data to Clock Input Hold Time.	1	-	-	ns

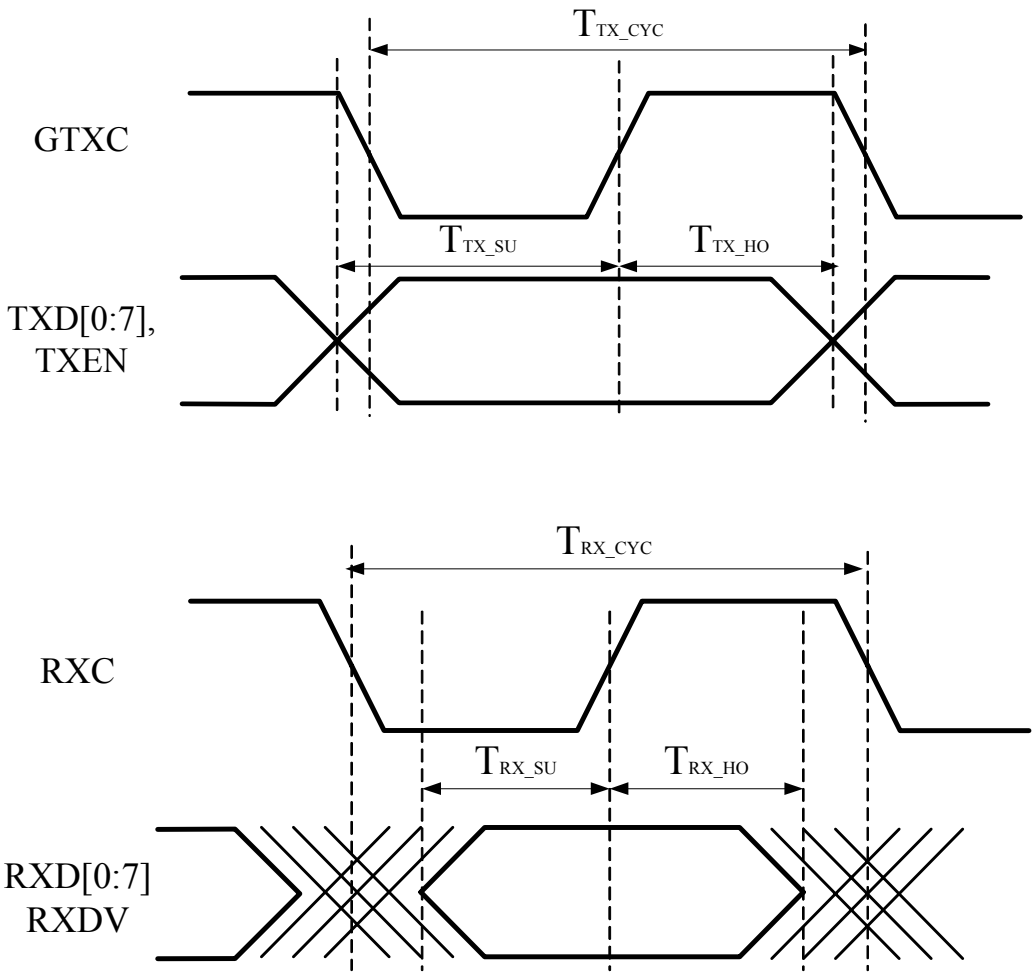


Figure 22. GMII Timing Characteristics

11.2.6. RGMII Timing Characteristics

Table 84. RGMII Timing Characteristics

SYM	Description/Condition	Min	Typ.	Max.	Units
T_{skewT}	Disable TXC Delay	-500	0	500	ps
T_{TX_SU}	Data to Clock Output Setup Time. Disable TXC Delay	-	400	-	ps
T_{TX_HO}	Data to Clock Output Hold Time. Disable TXC Delay	-	3.6	-	ns
T_{TX_SU}	Data to Clock Output Setup Time. Enable TXC Delay	-	1.6	-	ns
T_{TX_HO}	Data to Clock Output Hold Time. Enable TXC Delay	-	2.2	-	ns
T_{RX_SU}	Data to Clock Input Setup Time. Disable RXC Delay	1.0	-	-	ns
T_{RX_HO}	Data to Clock Input Hold Time. Disable RXC Delay	1.0	-	-	ns

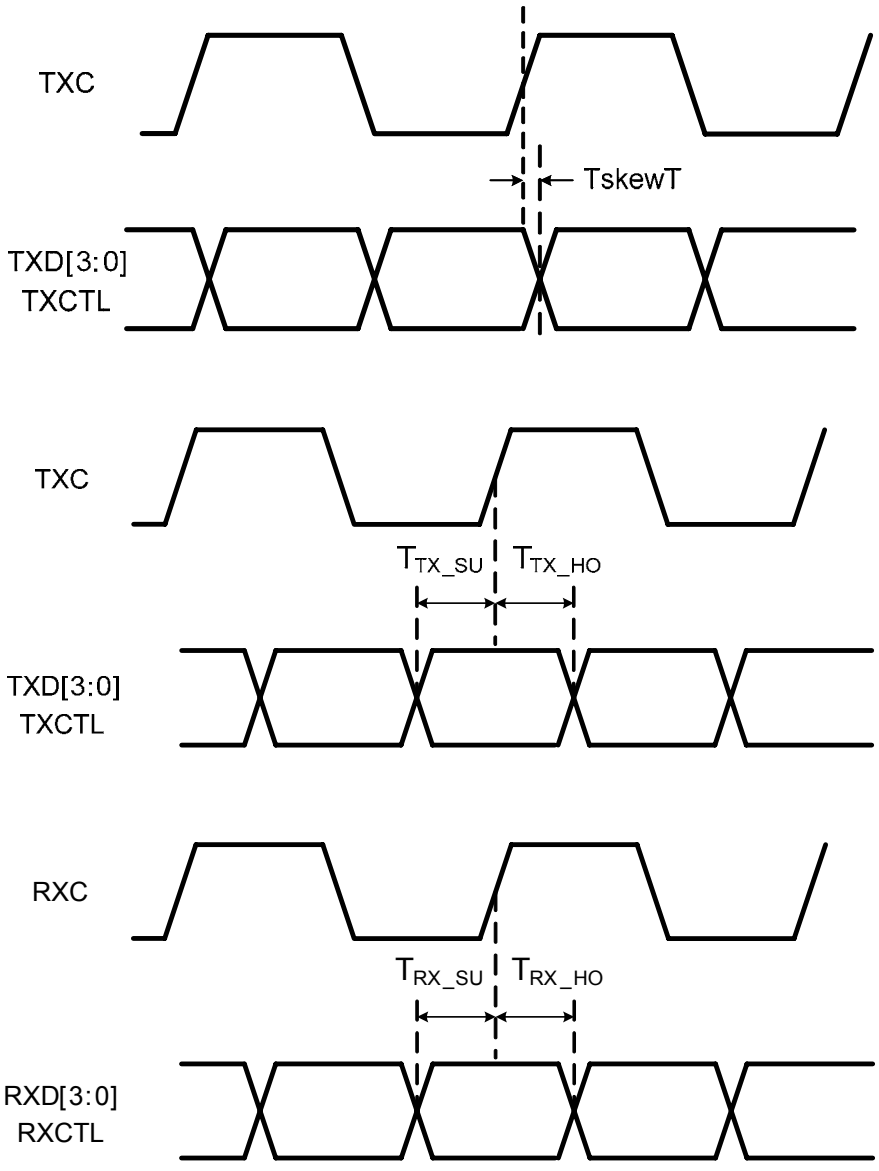


Figure 23. RGMII Timing Characteristics

11.2.7. JTAG Boundary Scan

Table 85. JTAG Boundary Scan Interface Timing Values

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_{bscl}	JTAG Clock Low Time	50	-	-	ns	1
T_{bsch}	JTAG Clock High Time	50	-	-	ns	1
T_{bsis}	TDI, TMS Setup Time to Rising Edge of TCK	10	-	-	ns	-
T_{bsih}	TDI, TMS Hold Time from Rising Edge of TCK	10	-	-	ns	-
T_{bsoh}	TDO Hold Time after Falling Edge of TCK	1.5	-	-	ns	-
T_{bsod}	TDO Output from Falling Edge of TCK	-	-	40	ns	-
T_{bsr}	JTAG Reset Period	30	-	-	ns	-
T_{bsrs}	TMS Setup Time to Rising Edge of JTAG Reset	10	-	-	ns	-
T_{bsrh}	TMS Hold Time from Rising Edge of JTAG Reset	10	-	-	ns	-

Note 1: JTAG clock TCK may be stopped indefinitely in either the low or high phase.

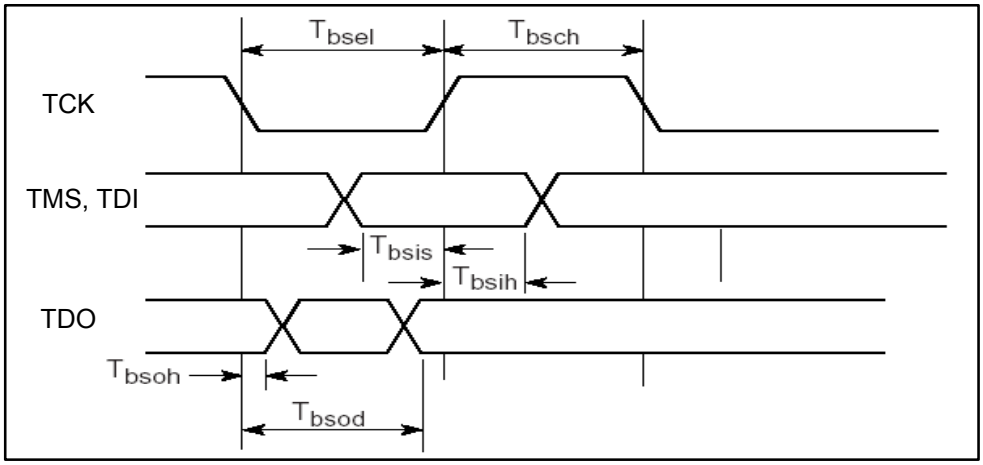


Figure 24. Boundary-Scan General Timing

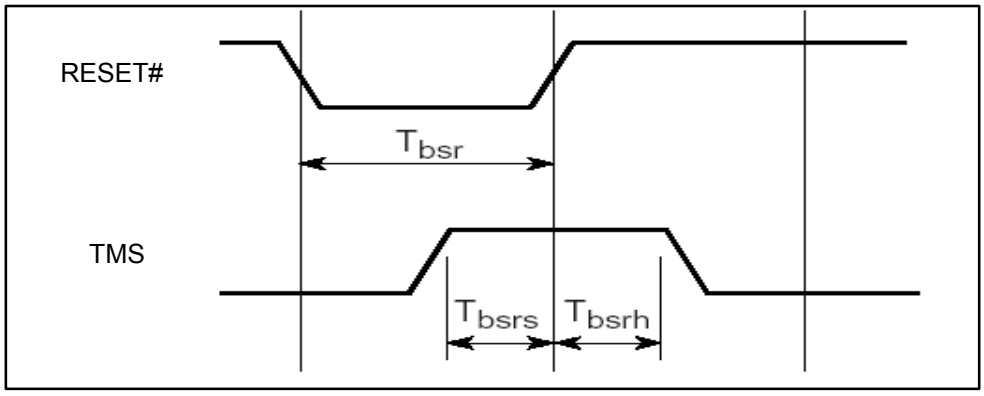


Figure 25. Boundary-Scan Reset Timing

11.2.8. Power Sequence

Table 86. Power-Up Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
t1	3.3V Stable to 1.0V	1	-	-	ms

Note 1: The 3.3V(I/O) must be powered up before 1.0V (core) and 1.0V (analog) voltage.

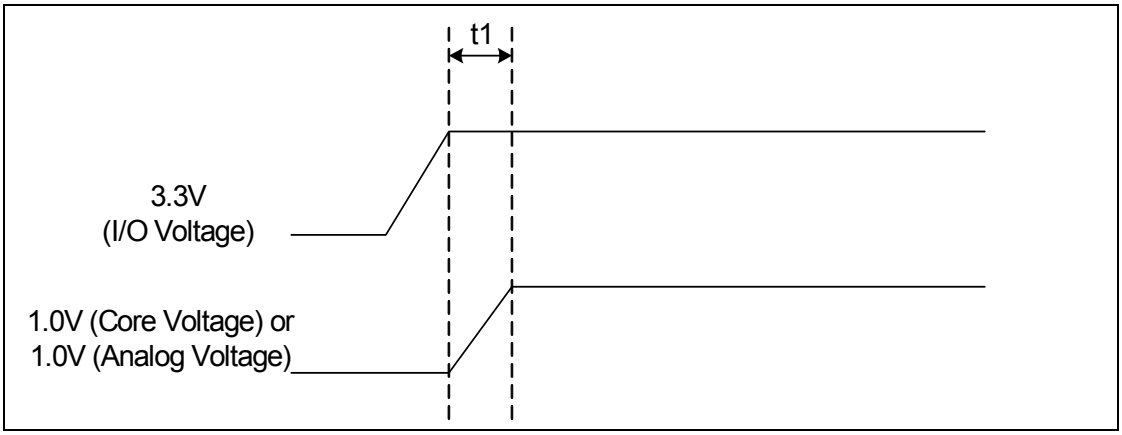


Figure 26. Power Up Sequence Timing Diagram

11.2.9. Power Configuration Timing

Power up configuration only relates to internal timing. The external hardware pin reset is unconcerned with power up configuration. The Hardware reset pin is valid when an internal reset ends the active state.

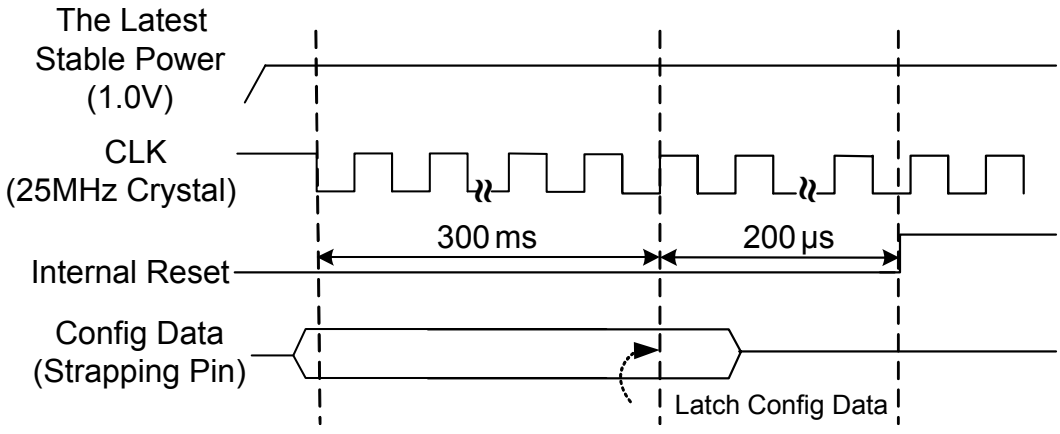


Figure 27. Power Up Configuration Timing Diagram

11.3. PCI Express Bus Parameters

11.3.1. Differential Transmitter Parameters

Table 87. Differential Transmitter Parameters

Symbol	Parameter	Min	Typical	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{TX-DIFFp-p}$	Differential Peak to Peak Output Voltage	0.800	-	1.2	V
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
T_{TX-EYE}	Minimum Tx Eye Width	0.75	-	-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between the Jitter Median and Maximum Deviation from the Median	-	-	0.125	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- Tx Output Rise/Fall Time	0.125	-	-	UI
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
$V_{TX-CM-DCACTIVE-IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
$V_{TX-CM-DCLINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
$V_{TX-RCV-DETECT}$	The Amount of Voltage Change Allowed During Receiver Detection	-	-	600	mV
$V_{TX-DC-CM}$	Tx DC Common Mode Voltage	0	-	3.6	V
$I_{TX-SHORT}$	Tx Short Circuit Current Limit	-	-	90	mA
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	50	-	-	UI
$T_{TX-IDLE-SETTO-IDLE}$	Maximum Time to Transition to A Valid Electrical Idle After Sending An Electrical Idle Ordered Set	-	-	20	UI
$T_{TX-IDLE-TOTO-DIFF-DATA}$	Maximum Time to Transition to Valid Tx Specifications After Leaving An Electrical Idle Condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{TX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80	100	120	Ω
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	-	-	500+2*UI	ps
C_{TX}	AC Coupling Capacitor	75	-	200	nF
$T_{crosslink}$	Crosslink Random Timeout	0	-	1	ms

Note1: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

Note2: The data rate can be modulated with an SSC (Spread Spectrum Clock) from +0 to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30kHz – 33kHz. The ±300ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600ppm difference.

11.3.2. Differential Receiver Parameters

Table 88. Differential Receiver Parameters

Symbol	Parameter	Min.	Typical	Max.	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential Input Peak to Peak Voltage	0.175	-	1.200	V
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time Between the Jitter Median and Maximum Deviation from the Median	-	-	0.3	UI
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{RX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω
Z_{RX--DC}	DC Input Impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	-	175	mV
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms
$L_{RX-SKEW}$	Total Skew	-	-	20	ns

Note: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

11.3.3. REFCLK Parameters

Table 89. REFCLK Parameters

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150	-	mV	2
V_{IL}	Differential Input Low Voltage	-	-150	mV	2
V_{CROSS}	Absolute Crossing Point Voltage	+250	+550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} Over All Rising Clock Edges	-	+140	mV	1, 4, 9
V_{RB}	Ring-Back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time before V_{RB} is Allowed	500	-	ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle Jitter	-	150	ps	2
V_{MAX}	Absolute Maximum Input Voltage	-	+1.15	V	1, 7
V_{MIN}	Absolute Minimum Input Voltage	-	-0.3	V	1, 8
Duty Cycle	Duty Cycle	40	60	%	2

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise-Fall Matching	Rising Edge Rate (REFCLK+) to Falling Edge Rate (REFCLK-) Matching	-	20	%	1, 14
Z_{C-DC}	Clock Source DC Impedance	40	60	Ω	1, 11

Note1: Measurement taken from single-ended waveform.

Note2: Measurement taken from differential waveform.

Note3: Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Figure 31, page 73.

Note4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 28, page 72.

Note5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 28, page 72.

Note6: Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation. See Figure 30, page 72.

Note7: Defined as the maximum instantaneous voltage including overshoot. See Figure 28, page 72.

Note8: Defined as the minimum instantaneous voltage including undershoot. See Figure 28, page 72.

Note9: Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 28, page 72.

Note10: Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding ppm considerations.

Note11: System board compliance measurements must use the test load card described in Figure 34, page 74. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL=2pF.

Note12: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to droop back into the V_{RB} ±100mV differential range. See Figure 33, page 73.

*Note13: PPM refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly, or 100Hz. For 300ppm then we have an error budget of 100Hz/ppm*300ppm=30kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±300ppm applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800ppm.*

Note14: Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 29, page 72.

Note15: Refer to PCI Express Card Electromechanical Specification, rev.1.1, for correct measurement environment setting of each parameter.

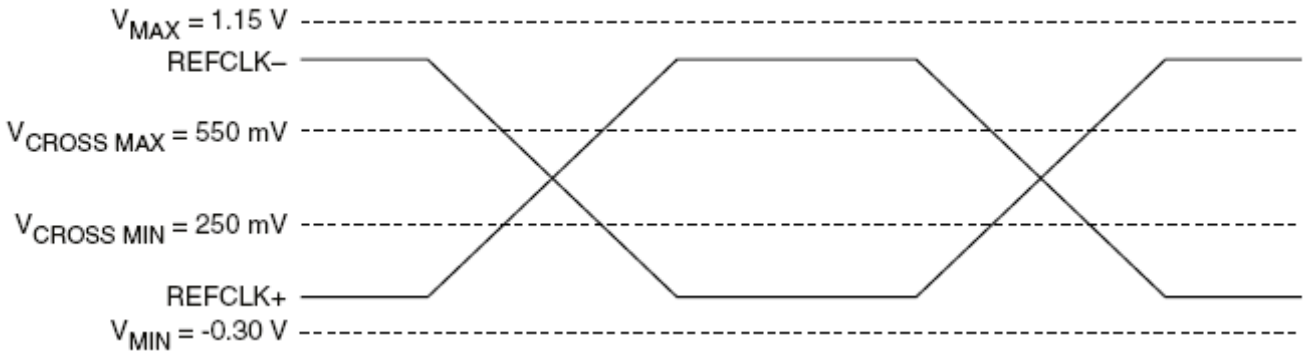


Figure 28. Single-Ended Measurement Points for Absolute Cross Point and Swing

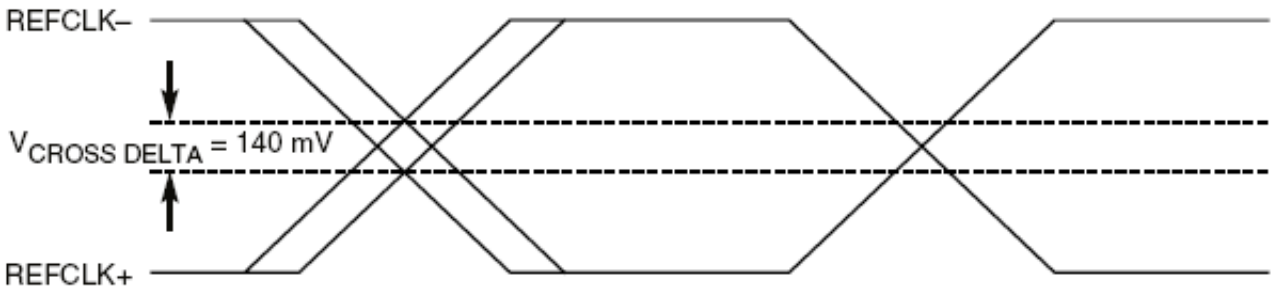


Figure 29. Single-Ended Measurement Points for Delta Cross Point

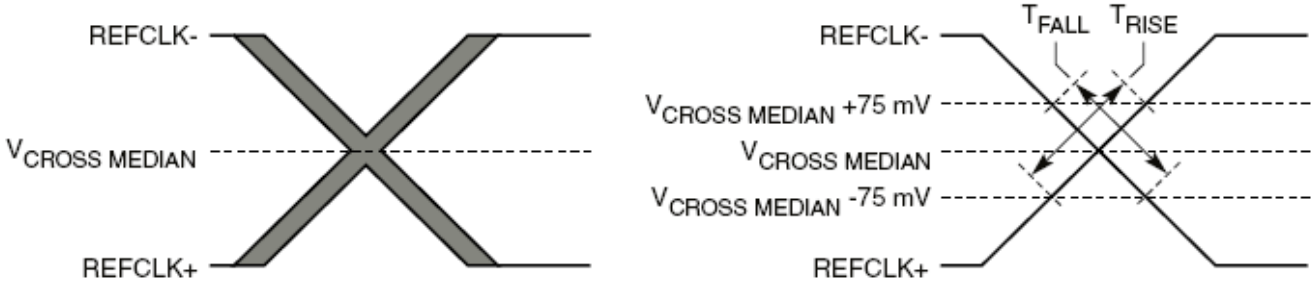


Figure 30. Single-Ended Measurement Points for Rise and Fall Time Matching

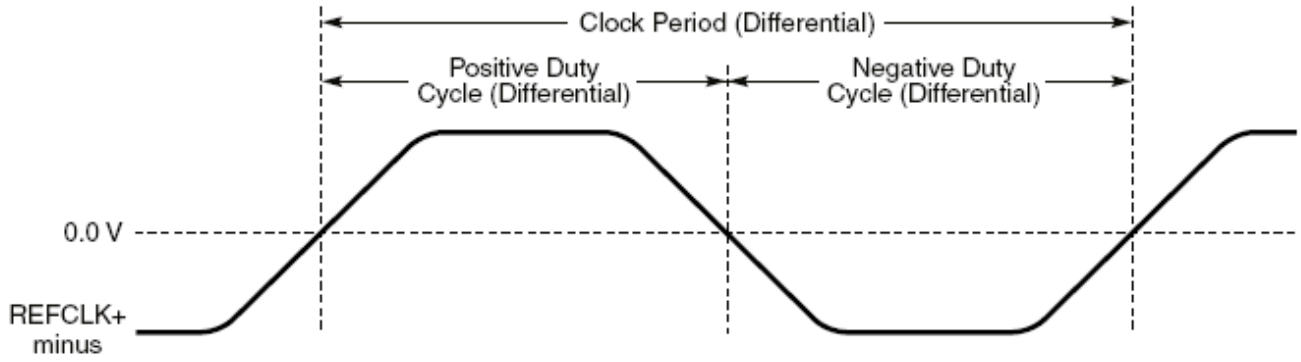


Figure 31. Differential Measurement Points for Duty Cycle and Period

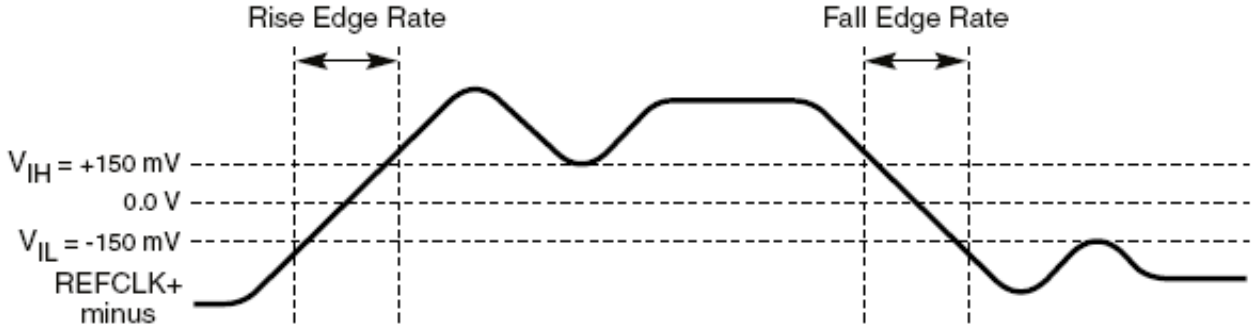


Figure 32. Differential Measurement Points for Rise and Fall Time

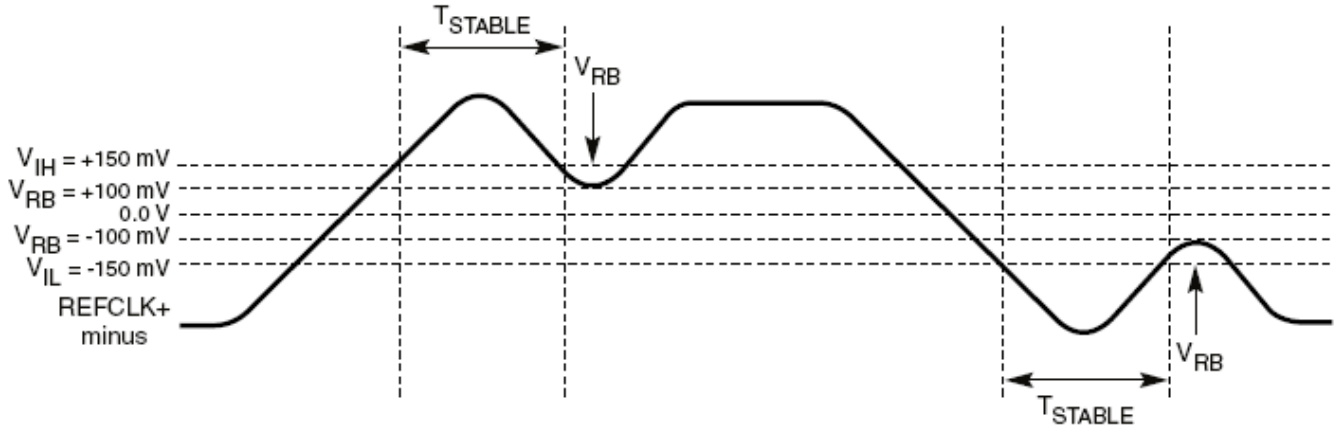


Figure 33. Differential Measurement Points for Ringback

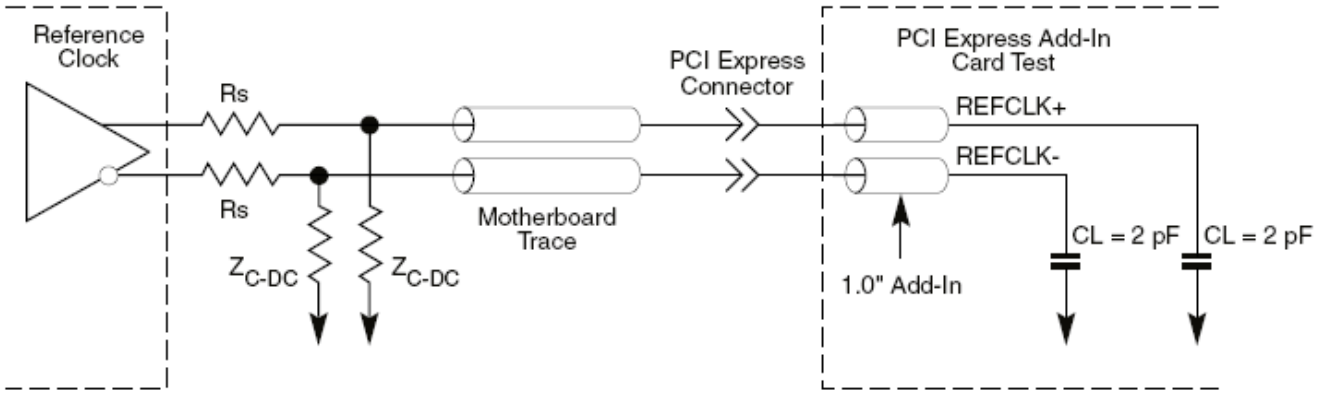


Figure 34. Reference Clock System Measurement Point and Loading

12. Thermal Characteristics

Heat generated by the chip causes a temperature rise of the package. If the temperature of the chip (Tj, junction temperature) is beyond the design limits, there will be negative effects on operation and the life of the IC package. Heat dissipation, either through a heat sink or electrical fan, is necessary to provide a reasonable environment (Ta, ambient temperature) in a closed case. As power density increases, thermal management becomes more critical. A method to estimate the possible Ta is outlined below.

Thermal parameters are defined as below according to JEDEC standard JESD 51-2, 51-6:

(1) θja (Thermal resistance from junction to ambient), represents resistance to heat flow from the chip to ambient air. This is an index of heat dissipation capability. A lower θja means better thermal performance.

θja=(Tj-Ta)/P

Where Tj is the die junction temperature, Ta is the ambient air temperature,

P is the power dissipation by device (Watts)

(2) θjc (Thermal Resistance Junction-to-Case, °C/W), measures the heat flow resistance between the die surface and the surface of the package (case). This data is relevant for packages used with external heatsinks.

θjc=(Tj-Tc)/P

Where Tj is the die junction temperature, Tc is the package case temperature.

P is the power dissipation by device (Watts)

(3) Ψjt (Thermal Characterization Parameter: Junction to package top), represents the correlation between the temperature of the chip and the package top.

Ψjt=(Tj-Tt)/P

Where Tj is the die junction temperature, Tt is the top of package temperature.

P is the power dissipation by the device (Watts)

Thermal Terminology

The major thermal dissipation paths can be illustrated as following:

Tj: The maximum junction temperature

Ta: The ambient or environment temperature

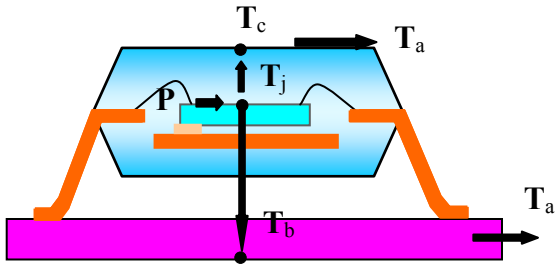
Tc: The maximum compound surface temperature

Tb: The maximum surface temperature of PCB bottom

P: Total input power

PQFP Junction to ambient thermal resistance, θja, defined as:

$$\theta JA = \frac{TJ - TA}{P}$$



Thermal Dissipation of PQFP Package

12.1. Thermal Operating Range

Table 90. Thermal Operating Range

Parameter	SYM	Condition	Min	Typ.	Max	Units
Junction Operating Temperature	Tj	-	0	-	125	°C
Ambient Operating Temperature	Ta	4-layer FR4 PCB (without heat sink)	0	25	65	°C

Note: PCB conditions (JEDEC JESD51-7). Dimensions: 120mm x 90mm. Thickness: 1.6 mm.

12.2. Thermal Parameters

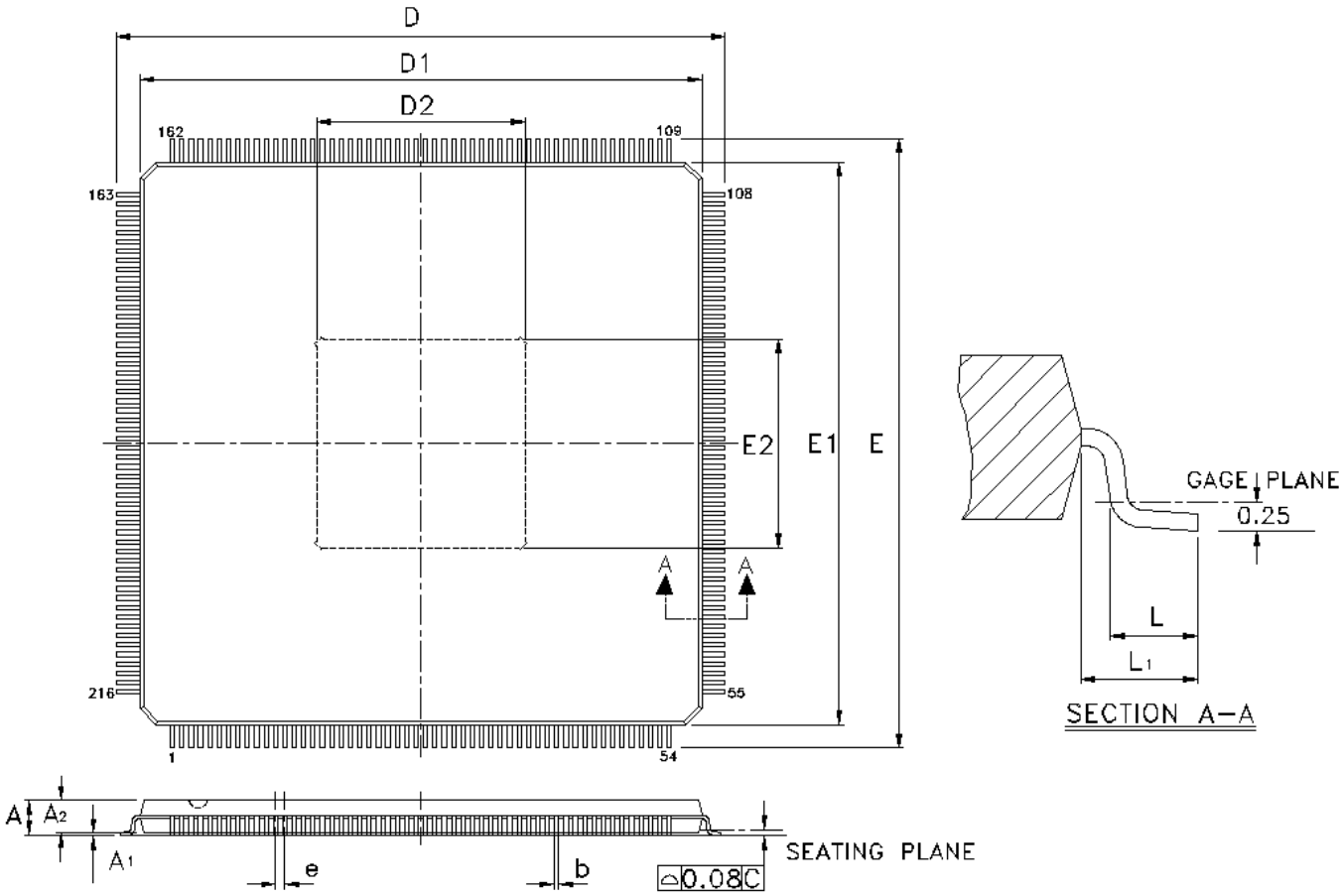
Table 91. Thermal Parameters

Parameter	SYM	Condition	Air Flow 0 m/s	Air Flow 1 m/s	Air Flow 2 m/s	Air Flow 3 m/s	Units
Thermal Resistance: Junction to Ambient	θja	2-layer FR4 PCB	18.5	14.9	13.9	13.2	°C/W
Thermal Resistance: Junction to Ambient	θja	4-layer FR4 PCB	13.8	10.7	9.7	9.3	°C/W
Thermal Characterization: Junction to Package Top	Ψjt	2-layer FR4 PCB	2.1	2.4	2.7	3.4	°C/W
Thermal Characterization: Junction to Package Top	Ψjt	4-layer FR4 PCB	1.7	1.9	2.3	2.8	°C/W

Note: PCB conditions (JEDEC JESD51-7). Dimensions: 120mm x 90mm. Thickness: 1.6mm.

13. Mechanical Dimensions

Thermally Enhanced Low Profile Plastic Quad Flat Package 216-Lead E-PAD (24x24mm)



13.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A_1	0.05	-	-	0.002	-	-
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
D/E	26.00BSC			1.024BSC		
D_1/E_1	24.00BSC			0.945BSC		
D_2/E_2	6.0	-	8.89	0.236	-	0.350
e	0.40BSC			0.016BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00REF			0.039REF		

Note 1: CONTROLLING DIMENSION: MILLIMETER(mm).
Note 2: REFERENCE DOCUMENT: JEDEC MS-26.

14. Ordering Information

Table 92. Ordering Information

Part Number	Package	Status
RTL8198-GR	Thermally Enhanced Low Profile Plastic Quad Flat Package 216-Lead E-PAD 'Green' Package	Mass Production

Note: See page 6 for 'Green' package identification information.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu, 300, Taiwan, R.O.C.
Tel: +886-3-5780211 Fax: +886-3-5776047
www.realtek.com