RTL8201CL
RTL8201CL-LF
RTL8201CL-VD
RTL8201CL-VD-LF

SINGLE-CHIP/SINGLE-PORT 10/100M FAST ETHERNET PHYCEIVER

DATASHEET

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2003/06/09	First release.
1.1	2003/09/26	Minor cosmetic changes. Modify LED Pin behavior.
1.2	2004/01/20	Add LED multi-mode definition (7.5 LED and PHY Address Configuration, page 19). Add Power dissipation info (Table 31). Bit <0:8> default setting changed to 0 (Table 9). Bit <0:13> default setting changed to 0 (Table 9). Bit <5:7> default setting changed to 0 (Table 14). Bit <17:5> default setting changed to 1 (Table 17). Bit <25:0> default setting changed to 0 (Table 20). Bit <25:1> default setting changed to 0 (Table 20). Bit <25:11~7> default setting changed to 00001 (Table 20).
1.21	2004/10/12	Package additions. See section 10, Ordering Information, page 33.
1.22	2005/04/11	Correction to Table 18, Register 18 RX_ER Counter (REC), page 13. Correction to Table 39, Transformer Characteristics, page 30. Added lead (Pb)-free package identification information on page 3 and on page 33.
1.23	2005/07/29	Corrected error in 7.8.3 10Base-T TX/RX, page 21 (10Base-T Transmit Function _ clock at 25MHz => clock at 2.5MHz). Corrections to Table 32, Input Voltage: Vcc, page 23. Vcc _ TTL Voh _ Minimum 0.9*Vcc => Minimum 0.65*Vcc Vcc _ TTL Vol _ Maximum 0.1*Vcc => Maximum 0.3*Vcc Vcc _ TTL Ioz _ Minimum -10uA => Minimum -110uA Vcc _ Iin _ Minimum -1.0uA => Minimum -110uA Vcc _ Iin _ Maximum 1.0uA => Maximum 100uA
1.24	2005/11/04	Revised Table 1, page 4 (pins 2, 3, 4, 5, 6, and 25). Corrected Table 17, page 12 (bits 17:6 and 17:5). Corrected Table 18, page 13 (mode). Revised Table 32, page 23 ($I_{IN,}$ $I_{PL,}$ I_{PH}). Revised Table 33, page 24 (t_8). Revised Table 34, page 25 ($t_{6,}$ $t_{7,}$ t_9).

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1. General Description

The RTL8201CL is a single-chip/single-port PHYceiver with an MII (Media Independent Interface)/SNI (Serial Network Interface). It implements all 10/100M Ethernet Physical-layer functions including the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Twisted Pair Physical Medium Dependent Sublayer (TP-PMD), 10Base-Tx Encoder/Decoder, and Twisted-Pair Media Access Unit (TPMAU).

A PECL (Pseudo Emitter Coupled Logic) interface is supported to connect with an external 100Base-FX fiber optical transceiver. The chip utilizes an advanced CMOS process to meet low voltage and low power requirements. With on-chip DSP (Digital Signal Processing) technology, the chip provides excellent performance under all operating conditions.

The RTL8201CL can be used for applications such as those for a Network Interface Adapter, MAU (Media Access Unit), CNR (Communication and Network Riser), ACR (Advanced Communication Riser), an Ethernet hub, and an Ethernet switch. In addition, it can be used in any embedded system with an Ethernet MAC that needs a UTP physical connection or Fiber PECL interface to an external 100Base-FX optical transceiver module.

2. Features

The Realtek RTL8201CL is a Fast Ethernet PHYceiver with selectable MII or SNI interface to the MAC chip. It provides the following features:

- Pin-to-pin compatible with the RTL8201BL
- Supports MII and 7-wire SNI (Serial Network Interface)
- 10/100Mbps operation
- Full/half duplex operation
- Twisted pair or fiber mode output
- Auto-Negotiation
- Supports power down mode
- Supports operation under Link Down Power Saving mode
- Supports Base Line Wander (BLW) compensation
- Supports repeater mode
- Adaptive Equalization
- Network status LEDs
- Flow control support
- 25MHz crystal/oscillator as clock source
- IEEE 802.3/802.3u compliant
- Supports IEEE 802.3u clause 28; 1.8V operation with 3.3V IO signal tolerance
- Low dual power supply, 1.8V and 3.3V; 1.8V is generated by an internal regulator
- 0.18µm CMOS process
- 48-pin LQFP package

3. Block Diagram

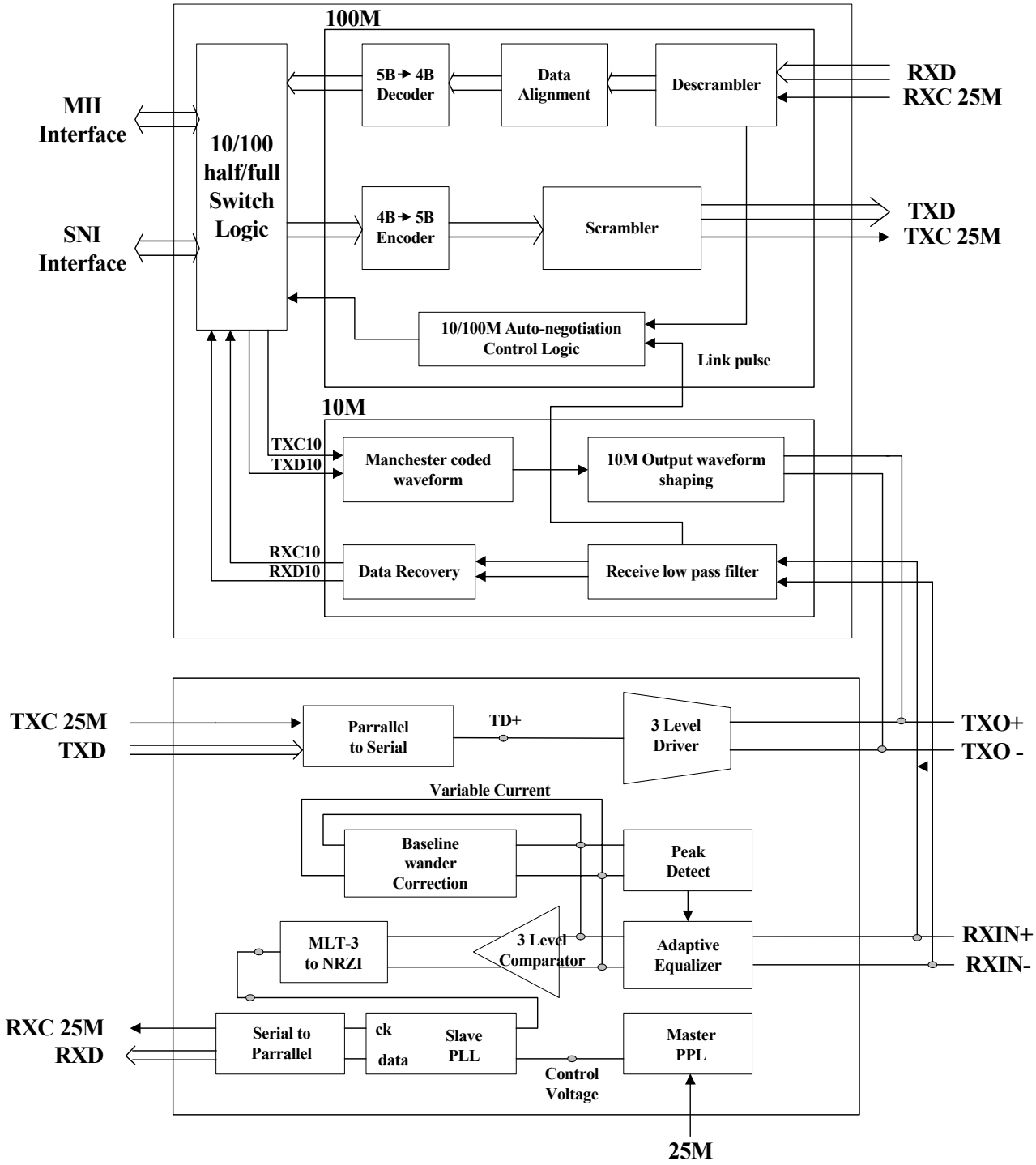


Figure 1. Block Diagram

4. Pin Assignments

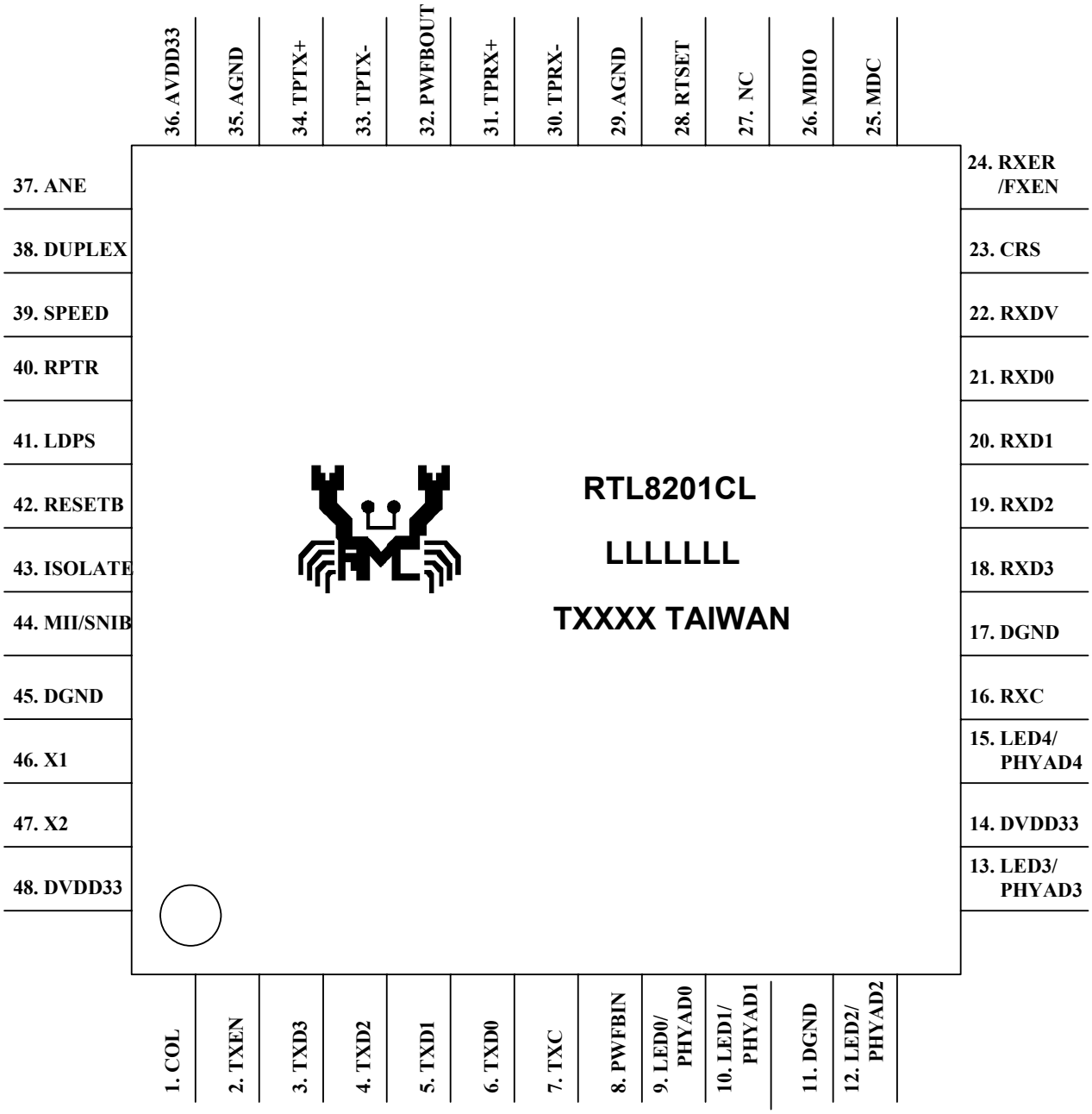


Figure 2. Pin Assignments

4.1. Lead (Pb)-Free Package Identification

Lead (Pb)-free package is indicated by an 'L' in the location marked 'T' in Figure 2.

5. Pin Descriptions

LI: Latched Input during Power up or Reset O: Output I: Input

IO: Bi-directional input and output P: Power

5.1. MII Interface

Table 1. MII Interface

Name	Type	Pin No.	Description
TXC	O	7	Transmit Clock. This pin provides a continuous clock as a timing reference for TXD[3:0] and TXEN.
TXEN	I	2	Transmit Enable. The input signal indicates the presence of valid nibble data on TXD[3:0]. An internal weak pull low resistor prevents the bus floating.
TXD[3:0]	I	3, 4, 5, 6	Transmit Data. The MAC will source TXD[0..3] synchronous with TXC when TXEN is asserted. An internal weak pull high resistor prevents the bus floating.
RXC	O	16	Receive Clock. This pin provides a continuous clock reference for RXDV and RXD[0..3] signals. RXC is 25MHz in 100Mbps mode and 2.5Mhz in 10Mbps mode.
COL	LI/O	1	Collision Detect. COL is asserted high when a collision is detected on the media. During power on reset, this pin status is latched to determine at which LED mode to operate: 0: CL LED mode 1: BL LED mode An internal weak pull low resistor sets this to the default CL LED mode. It is possible to use an external 5.1KΩ pull high resistor to enable BL LED mode.
CRS	LI/O	23	Carrier Sense. This pin's signal is asserted high if the media is not in Idle state. An internal weak pull low resistor sets this to normal operation mode. An external 5.1KΩ pull low resistor could be reserved to ensure operating at normal mode.
RXDV	O	22	Receive Data Valid. This pin's signal is asserted high when received data is present on the RXD[3:0] lines. The signal is de-asserted at the end of the packet. The signal is valid on the rising edge of the RXC.
RXD[3:0]	O	18, 19, 20, 21	Receive Data. These are the four parallel receive data lines aligned on the nibble boundaries driven synchronously to the RXC for reception by the external physical unit (PHY).

Name	Type	Pin No.	Description
RXER/ FXEN	O/LI	24	Receive Error. If a 5B decode error occurs, such as invalid /J/K/, invalid /T/R/, or invalid symbol, this pin will go high. Fiber/UTP Enable. During power on reset, this pin status is latched to determine the media mode to operate in. 1: Fiber mode 0: UTP mode An internal weak pull low resistor sets this to the default of UTP mode. It is possible to use an external 5.1KΩ pull high resistor to enable fiber mode. After power on, the pin operates as the Receive Error pin.
MDC	I	25	Management Data Clock. This pin provides a clock synchronous to MDIO, which may be asynchronous to the transmit TXC and receive RXC clocks. The clock rate can be up to 2.5MHz. An internal weak pull high resistor prevents the bus floating.
MDIO	IO	26	Management Data Input/Output. This pin provides the bi-directional signal used to transfer management information.

5.2. SNI (Serial Network Interface) 10Mbps Only

Table 2. SNI (Serial Network Interface) 10Mbps Only

Name	Type	Pin No.	Description
COL	O	1	Collision Detect.
RXD0	O	21	Received Serial Data.
CRS	O	23	Carrier Sense.
RXC	O	16	Receive Clock. Resolved from received data.
TXD0	I	6	Transmit Serial Data.
TXC	O	7	Transmit Clock. Generated by PHY.
TXEN	I	2	Transmit Enable. For MAC to indicate transmit operation.

5.3. Clock Interface

Table 3. Clock Interface

Name	Type	Pin No.	Description
X2	O	47	25MHz Crystal Output. This pin provides the 25MHz crystal output. It must be left open when an external 25MHz oscillator drives X1.
X1	I	46	25MHz Crystal Input. This pin provides the 25MHz crystal input. If a 25MHz oscillator is used, connect X1 to the oscillator's output (see 8.3 Crystal Characteristics, page 30, for clock source specifications.

5.4. 10Mbps/100Mbps Network Interface

Table 4. 10Mbps/100Mbps Network Interface

Name	Type	Pin No.	Description
TPTX+ TPTX-	O O	34 33	Transmit Output. Differential transmit output pair shared by 100Base-TX, 100Base-FX and 10Base-T modes. When configured as 100Base-TX, output is an MLT-3 encoded waveform. When configured as 100Base-FX, the output is pseudo-ECL level.
RTSET	I	28	Transmit Bias Resistor Connection. This pin should be pulled to GND by a 2KΩ (1%) resistor to define driving current for the transmit DAC. The resistance value may be changed, depending on experimental results of the RTL8201CL.
TPRX+ TPRX-	I I	31 30	Receive Input. Differential receive input pair shared by 100Base-TX, 100Base-FX, and 10Base-T modes.

5.5. Device Configuration Interface

Table 5. Device Configuration Interface

Name	Type	Pin No.	Description
ISOLATE	I	43	Set high to isolate the RTL8201CL from the MAC. This will also isolate the MDC/MDIO management interface. In this mode, the power consumption is minimum. This pin can be directly connected to GND or VCC.
RPTR	I	40	Set high to put the RTL8201CL into repeater mode. This pin can be directly connected to GND or VCC.
SPEED	LI	39	This pin is latched to input during a power on or reset condition. Set high to put the RTL8201CL into 100Mbps operation. This pin can be directly connected to GND or VCC.
DUPLEX	LI	38	This pin is latched to input during a power on or reset condition. Set high to enable full duplex. This pin can be directly connected to GND or VCC.
ANE	LI	37	This pin is latched to input during a power on or reset condition. Set high to enable Auto-negotiation mode, set low to force mode. This pin can be directly connected to GND or VCC.
LDPS	I	41	Set high to put the RTL8201CL into LDPS mode. This pin can be directly connected to GND or VCC. See 7.7 Power Down, Link Down, Power Saving, and Isolation Modes, page 20, for more information.
MII/SNIB	LI/O	44	This pin is latched to input during a power on or reset condition. Pull high to set the RTL8201CL into MII mode operation. Set low for SNI mode. This pin can be directly connected to GND or VCC.

5.6. LED Interface/PHY Address Configuration

These five pins are latched into the RTL8201CL during power up reset to configure the PHY address [0:4] used for the MII management register interface. In normal operation, after initial reset, they are used as driving pins for status indicator LEDs. The driving polarity, active low or active high, is determined by each latched status of the PHY address [4:0] during power-up reset. If the latched status is High, then it will be active low. If the latched status is Low, then it will be active high. See section 7.5 LED and PHY Address Configuration, page 19, for more information.

Table 6. LED Interface/PHY Address Configuration

Name	Type	Pin No.	Description
PHYAD0/ LED0	LI/O	9	PHY Address [0]. Link LED. Lit when linked.
PHYAD1/ LED1	LI/O	10	PHY Address [1]. Full Duplex LED. Lit when in Full Duplex operation.
PHYAD2/ LED2	LI/O	12	PHY Address [2]. CL LED Mode: 10 ACT LED Blinking when transmitting or receiving data. BL LED Mode: Link 10 / ACT LED Active when linked in 10Base-T mode, and blinking when transmitting or receiving data.
PHYAD3/ LED3	LI/O	13	PHY Address [3]. CL LED Mode: 100 ACT LED Blinking when transmitting or receiving data. BL LED Mode: Link 100 / ACT LED Active when linked in 100Base-T mode, and blinking when transmitting or receiving data.
PHYAD4/ LED4	LI/O	15	PHY Address [4]. Collision LED. Blinks when collisions occur.

5.7. Power and Ground Pins

Table 7. Power and Ground Pins

Name	Type	Pin No.	Description
AVDD33	P	36	3.3V Analog Power Input. 3.3V power supply for analog circuit; should be well decoupled.
AGND	P	29, 35	Analog Ground. Should be connected to a larger GND plane.
DVDD33	P	14, 48	3.3V Digital Power Input. 3.3V power supply for digital circuit.
DGND	P	11, 17, 45	Digital Ground. Should be connected to a larger GND plane.

5.8. Reset and Other Pins

Table 8. Reset and Other Pins

Name	Type	Pin No.	Description
RESETB	I	42	RESETB. Set low to reset the chip. For a complete reset, this pin must be asserted low for at least 10ms.
PWFBOUT	O	32	Power Feedback Output. Be sure to connect a 22uF tantalum capacitor for frequency compensation and a 0.1uF capacitor for noise de-coupling. Then connect this pin through a ferrite bead to PWFBIN (pin8). The connection method is outlined in section 7.11 3.3V Power Supply and Voltage Conversion Circuit, page 22.
PWFBIN	I	8	Power Feedback Input. See the PWFBOUT description above.
NC		27	Not Connected.

6. Register Descriptions

This section describes the functions and usage of the registers available in the RTL8201CL.

In this section the following abbreviations are used:

RO: Read Only

RW: Read/Write

6.1. Register 0 Basic Mode Control Register

Table 9. Register 0 Basic Mode Control Register

Address	Name	Description	Mode	Default
0:15	Reset	This bit sets the status and control registers of the PHY in a default state. This bit is self-clearing. 1: Software reset 0: Normal operation	RW	0
0:14	Loopback	This bit enables loopback of transmit data nibbles TXD3:0 to the receive data path. 1: Enable loopback 0: Normal operation	RW	0
0:13	Spd_Set	This bit sets the network speed. 1: 100Mbps 0: 10Mbps After completing auto negotiation, this bit will reflect the Speed status. 1: 100Base-T 0: 10Base-T) When 100Base-FX mode is enabled, this bit=1 and is read only.	RW	0
0:12	Auto Negotiation Enable	This bit enables/disables the NWay auto-negotiation function. 1: Enable auto-negotiation; bits 0:13 and 0:8 will be ignored. 0: Disable auto-negotiation; bits 0:13 and 0:8 will determine the link speed and the data transfer mode, respectively. When 100Base-FX mode is enabled, this bit=0 and is read only.	RW	1
0:11	Power Down	This bit turns down the power of the PHY chip, including the internal crystal oscillator circuit. The MDC, MDIO is still alive for accessing the MAC. 1: Power down 0: Normal operation	RW	0
0:10	Reserved			
0:9	Restart Auto Negotiation	This bits allows the NWay auto-negotiation function to be reset. 1: Re-start auto-negotiation 0: Normal operation	RW	0
0:8	Duplex Mode	This bit sets the duplex mode if auto-negotiation is disabled (bit 0:12=0). 1: Full duplex 0: Half duplex After completing auto-negotiation, this bit will reflect the duplex status. 1: Full duplex 0: Half duplex	RW	0
0:7:0	Reserved			

6.2. Register 1 Basic Mode Status Register

Table 10. Register 1 Basic Mode Status Register

Address	Name	Description	Mode	Default
1:15	100Base-T4	1: Enable 100Base-T4 support 0: Suppress 100Base-T4 support	RO	0
1:14	100Base_TX_ FD	1: Enable 100Base-TX full duplex support 0: Suppress 100Base-TX full duplex support	RO	1
1:13	100BASE_TX_HD	1: Enable 100Base-TX half duplex support 0: Suppress 100Base-TX half duplex support	RO	1
1:12	10Base_T_FD	1: Enable 10Base-T full duplex support 0: Suppress 10Base-T full duplex support	RO	1
1:11	10_Base_T_HD	1: Enable 10Base-T half duplex support 0: Suppress 10Base-T half duplex support	RO	1
1:10~7	Reserved			
1:6	MF Preamble Suppression	The RTL8201CL will accept management frames with preamble suppressed. A minimum of 32 preamble bits are required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions as per IEEE 802.3u specifications.	RO	1
1:5	Auto Negotiation Complete	1: Auto-negotiation process completed 0: Auto-negotiation process not completed	RO	0
1:4	Remote Fault	1: Remote fault condition detected (cleared on read) 0: No remote fault condition detected When in 100Base-FX mode, this bit means an in-band signal Far-End-Fault has been detected. See 0 Far End Fault Indication, page 22.	RO	0
1:3	Auto Negotiation	1: Link has not experienced fail state 0: Link experienced fail state	RO	1
1:2	Link Status	1: Valid link established 0: No valid link established	RO	0
1:1	Jabber Detect	1: Jabber condition detected 0: No jabber condition detected	RO	0
1:0	Extended Capability	1: Extended register capability 0: Basic register capability only	RO	1

6.3. Register 2 PHY Identifier Register 1

Table 11. Register 2 PHY Identifier Register 1

Address	Name	Description	Mode	Default
2:15~0	PHYID1	PHY identifier ID for software recognition of the RTL8201CL	RO	0000

6.4. Register 3 PHY Identifier Register 2

Table 12. Register 3 PHY Identifier Register 2

Address	Name	Description	Mode	Default
3:15~0	PHYID2	PHY identifier ID for software recognition of the RTL8201CL	RO	8201

6.5. Register 4 Auto-Negotiation Advertisement Register (ANAR)

This register contains the advertised abilities of this device as they will be transmitted to its link partner during auto-negotiation.

Table 13. Register 4 Auto-Negotiation Advertisement Register (ANAR)

Address	Name	Description	Mode	Default
4:15	NP	Next Page bit. 0: Transmitting the primary capability data page 1: Transmitting the protocol specific data page	RO	0
4:14	ACK	1: Acknowledge reception of link partner capability data word 0: Do not acknowledge reception	RO	0
4:13	RF	1: Advertise remote fault detection capability 0: Do not advertise remote fault detection capability	RW	0
4:12	Reserved			
4:11	TXFC	1: TX flow control is supported by local node 0: TX flow control not supported by local node	RW	0
4:10	RXFC	1: RX flow control is supported by local node 0: RX flow control not supported by local node	RW	0
4:9	T4	1: 100Base-T4 is supported by local node 0: 100Base-T4 not supported by local node	RO	0
4:8	TXFD	1: 100Base-TX full duplex is supported by local node 0: 100Base-TX full duplex not supported by local node	RW	1
4:7	TX	1: 100Base-TX is supported by local node 0: 100Base-TX not supported by local node	RW	1
4:6	10FD	1: 10Base-T full duplex supported by local node 0: 10Base-T full duplex not supported by local node	RW	1
4:5	10	1: 10Base-T is supported by local node 0: 10Base-T not supported by local node	RW	1
4:4~0	Selector	Binary encoded selector supported by this node. Currently only CSMA/CD 00001 is specified. No other protocols are supported.	RW	00001

6.6. Register 5 Auto-Negotiation Link Partner Ability Register (ANLPAR)

This register contains the advertised abilities of the Link Partner as received during auto-negotiation. The content changes after a successful auto-negotiation if Next-pages are supported.

Table 14. Register 5 Auto-Negotiation Link Partner Ability Register (ANLPAR)

Address	Name	Description	Mode	Default
5:15	NP	Next Page bit. 0: Transmitting the primary capability data page 1: Transmitting the protocol specific data page	RO	0
5:14	ACK	1: Link partner acknowledges reception of local node's capability data word 0: No acknowledgement	RO	0
5:13	RF	1: Link partner is indicating a remote fault 0: Link partner does not indicate a remote fault	RO	0
5:12	Reserved			
5:11	TXFC	1: TX flow control is supported by Link partner 0: TX flow control not supported by Link partner	RO	0

Address	Name	Description	Mode	Default
5:10	RXFC	1: RX flow control is supported by Link partner 0: RX flow control not supported by Link partner	RO	0
5:9	T4	1: 100Base-T4 is supported by link partner 0: 100Base-T4 not supported by link partner	RO	0
5:8	TXFD	1: 100Base-TX full duplex is supported by link partner 0: 100Base-TX full duplex not supported by link partner	RO	0
5:7	100BASE-TX	1: 100Base-TX is supported by link partner 0: 100Base-TX not supported by link partner This bit will also be set if the link in 100Base is established by parallel detection.	RO	0
5:6	10FD	1: 10Base-T full duplex is supported by link partner 0: 10Base-T full duplex not supported by link partner	RO	0
5:5	10Base-T	1: 10Base-T is supported by link partner 0: 10Base-T not supported by link partner This bit will also be set if the link in 10Base-T is established by parallel detection.	RO	0
5:4~0	Selector	Link Partner's binary encoded node selector Currently only CSMA/CD 00001 is specified	RO	00000

6.7. Register 6 Auto-Negotiation Expansion Register (ANER)

This register contains additional status for NWay auto-negotiation.

Table 15. Register 6 Auto-Negotiation Expansion Register (ANER)

Address	Name	Description	Mode	Default
6:15~5	Reserved	This bit is permanently set to 0.		
6:4	MLF	Indicates whether a multiple link fault has occurred. 1: Fault occurred 0: No fault occurred	RO	0
6:3	LP_NP_ABLE	Indicates whether the link partner supports Next Page negotiation. 1: Supported 0: Not supported	RO	0
6:2	NP_ABLE	This bit indicates whether the local node is able to send additional Next Pages. Internal use only.	RO	0
6:1	PAGE_RX	This bit is set when a new Link Code Word Page has been received. It is automatically cleared when the auto-negotiation link partner's ability register (register 5) is read by management.	RO	0
6:0	LP_NW_ABLE	1: Link partner supports NWay auto-negotiation.	RO	0

6.8. Register 16 NWay Setup Register (NSR)

Table 16. Register 16 NWay Setup Register (NSR)

Address	Name	Description	Mode	Default
16:15~12	Reserved			
16:11	ENNWLE	1: LED4 Pin indicates linkpulse	RW	0
16:10	Testfun	1: Auto-negotiation speeds up internal timer	RW	0
16:9	NWLPBK	1: Set NWay to loopback mode	RW	0
16:8~3	Reserved			
16:2	FLAGABD	1: Auto-negotiation experienced ability detect state	RO	0
16:1	FLAGPDF	1: Auto-negotiation experienced parallel detection fault state	RO	0
16:0	FLAGLSC	1: Auto-negotiation experienced link status check state	RO	0

6.9. Register 17 Loopback, Bypass, Receiver Error Mask Register (LBREMR)

Table 17. Register 17 Loopback, Bypass, Receiver Error Mask Register (LBREMR)

Address	Name	Description	Mode	Default
17:15	RPTR	Set to 1 to put the RTL8201CL into repeater mode.	RW	0
17:14	BP_4B5B	Assertion of this bit allows bypassing of the 4B/5B & 5B/4B encoder.	RW	0
17:13	BP_SCR	Assertion of this bit allows bypassing of the scrambler/descrambler.	RW	0
17:12	LDPS	Set to 1 to enable Link Down Power Saving mode.	RW	0
17:11	AnalogOFF	Set to 1 to power down analog function of transmitter and receiver.	RW	0
17:10	Reserve	Reserved.		
17:9	LB	Set to 1 to enable DSP Loopback.	RW	0
17:8	F_Link_10	Used to logic force good link in 10Mbps for diagnostic purposes.	RW	1
17:7	F_Link_100	Used to logic force good link in 100Mbps for diagnostic purposes.	RW	1
17:6	JBEN	Set to 1 to enable Jabber Function in 10Base-T.	RW	1
17:5	CODE_err	Assertion of this bit causes a code error detection to be reported.	RW	0
17:4	PME_err	Assertion of this bit causes a pre-mature end error detection to be reported.	RW	0
17:3	LINK_err	Assertion of this bit causes a link error detection to be reported.	RW	0
17:2	PKT_err	Assertion of this bit causes a ‘detection of packet errors due to 722 ms time-out’ to be reported.	RW	0
17:1	FXMODE	This bit indicates whether Fiber Mode is Enabled.	RO	0
17:0	RMIIMODE	This bit indicates whether RMII mode is Enabled.	RO	0

6.10. Register 18 RX_ER Counter (REC)

Table 18. Register 18 RX_ER Counter (REC)

Address	Name	Description	Mode	Default
18:15~0	RXERCNT	This 16-bit counter increments by 1 for each invalid packet received. The value is valid while a link is established.	RO	H'[0000]

6.11. Register 19 SNR Display Register

Table 19. Register 19 SNR Display Register

Address	Name	Description	Mode	Default
19:15~4	Reserved	Realtek Test Mode Internal use. Do not change this field without Realtek's approval.		
19:3~0	SNR	These 4-bits show the Signal to Noise Ratio value.	RW	0000

6.12. Register 25 Test Register

Table 20. Register 25 Test Register

Address	Name	Description	Mode	Default
25:15~12	Test	Reserved for internal testing.	RW	
25:11~7	PHYAD[4:0]	Reflects the PHY address defined by external PHY address configuration pins.	RO	00001
25:6~2	Test	Reserved for internal testing.	RO	
25:1	LINK10	1: 10Base-T link established 0: No 10Base-T link established	RO	0
25:0	LINK100	1: 100Base-FX or 100Base-TX link established 0: No 100Base link established	RO	0

7. Functional Description

The RTL8201CL PHYceiver is a physical layer device that integrates 10Base-T and 100Base-TX/100Base-FX functions, and some extra power management features into a 48-pin single chip that is used in 10/100 Fast Ethernet applications. This device supports the following functions:

- MII interface with MDC/MDIO SMI management interface to communicate with MAC
- IEEE 802.3u clause 28 Auto-Negotiation ability
- Flow control ability support to cooperate with MAC
- Speed, duplex, auto-negotiation ability configurable by hard wire or MDC/MDIO
- Flexible LED configuration
- 7-wire SNI (Serial Network Interface) support (only in 10Mbps mode)
- Power Down mode support
- 4B/5B transform
- Scrambling/De-scrambling
- NRZ to NRZI, NRZI to MLT-3
- Manchester Encode and Decode for 10Base-T operation
- Clock and Data recovery
- Adaptive Equalization
- Far End Fault Indication (FEFI) in fiber mode

7.1. MII and Management Interface

7.1.1. Data Transition

To set the RTL8201CL for MII mode operation, pull the MII/SNIB pin high and set the ANE, SPEED, and DUPLEX pins.

The MII (Media Independent Interface) is an 18-signal interface (as described in IEEE 802.3u) supplying a standard interface between the PHY and MAC layer. This interface operates at two frequencies – 25Mhz and 2.5Mhz to support 100Mbps/10Mbps bandwidth for both transmit and receive functions.

Transmission

The MAC asserts the TXEN signal. It then changes byte data into 4-bit nibbles and passes them to the PHY via TXD[0..3]. The PHY will sample TXD[0..3] synchronously with TXC — the transmit clock signal supplied by PHY – during the interval TXEN is asserted.

Reception

The PHY asserts the RXEN signal. It passes the received nibble data RXD[0..3] clocked by RXC. CRS and COL signals are used for collision detection and handling.

In 100Base-TX mode, when the decoded signal in 5B is not IDLE, the CRS signal will assert. When 5B is recognized as IDLE it will be de-asserted. In 10Base-T mode, CRS will assert when the 10M preamble has been confirmed and will be de-asserted when the IDLE pattern has been confirmed.

The RXDV signal will be asserted when decoded 5B are /J/K/ and will be de-asserted if the 5B are /T/R/ or IDLE in 100Mbps mode. In 10Mbps mode, the RXDV signal is the same as the CRS signal.

The RXER (Receive Error) signal will be asserted if any 5B decode errors occur such as invalid J/K, invalid T/R, or invalid symbol. This pin will go high for one or more clock periods to indicate to the reconciliation sublayer that an error was detected somewhere in the frame.

Note: The RTL8201CL does not use a TXER signal. This does not affect the transmit function.

7.1.2. Serial Management

The MAC layer device can use the MDC/MDIO management interface to control a maximum of 31 RTL8201CL devices, configured with different PHY addresses (00001b to 11111b). During a hardware reset, the logic levels of pins 9, 10, 12, 13, 15 are latched into the RTL8201CL to be set as the PHY address for management communication via the serial interface. Setting the PHY address to 00000b will put the RTL8201CL into power down mode. The read and write frame structure for the management interface is illustrated in Figure 3 and Figure 4.

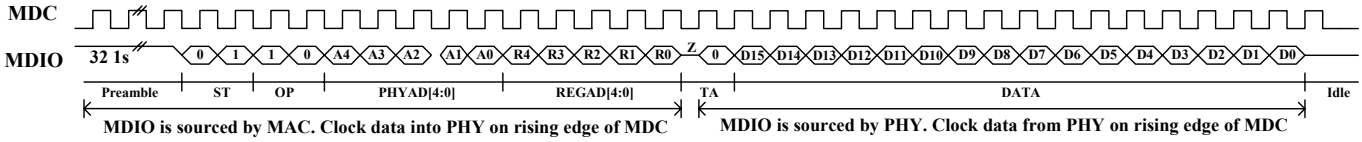


Figure 3. Read Cycle

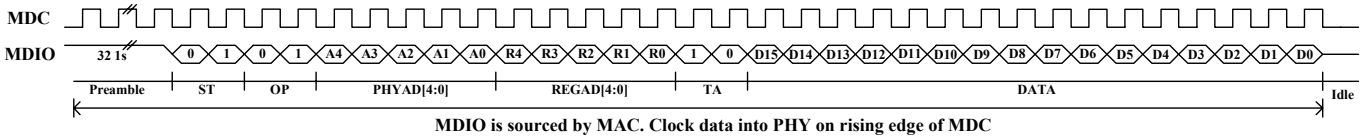


Figure 4. Write Cycle

Table 21. Serial Management

Name	Description
Preamble	32 contiguous logical ‘1’s sent by the MAC on MDIO along with 32 corresponding cycles on MDC. This provides synchronization for the PHY.
ST	Start of Frame. Indicated by a 01 pattern.
OP	Operation Code. Read: 10 Write: 01
PHYAD	PHY Address. Up to 31 PHYs can be connected to one MAC. This 5-bit field selects which PHY the frame is directed to.
REGAD	Register Address. This is a 5-bit field that sets which of the 32 registers of the PHY this operation refers to.
TA	Turnaround. This is a 2-bit time-spacing between the register address and the data field of a frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY shall remain in a high-impedance state for the first bit time of the turnaround. The PHY shall drive a zero bit during the second bit time of the turnaround of a read transaction.
DATA	Data. These are the 16 bits of data.
IDLE	Idle Condition. Not truly part of the management frame. This is a high impedance state. Electrically, the PHY’s pull-up resistor will pull the MDIO line to a logical ‘1’.

7.2. Auto-Negotiation and Parallel Detection

The RTL8201CL supports IEEE 802.3u clause 28 Auto-negotiation for operation with other transceivers supporting auto-negotiation. The RTL8201CL can auto detect the link partner's abilities and determine the highest speed/duplex configuration possible between the two devices. If the link partner does not support auto-negotiation, then the RTL8201CL will enable half duplex mode and enter parallel detection mode. The RTL8201CL will default to transmit FLP (Fast Link Pulse) and wait for the link partner to respond. If the RTL8201CL receives FLP, then the auto-negotiation process will go on. If it receives NLP (Normal Link Pulse), then the RTL8201CL will change to 10Mbps and half duplex mode. If it receives a 100Mbps IDLE pattern, it will change to 100Mbps and half duplex mode.

To enable auto-negotiation mode operation on the RTL8201CL, pull the ANE (Auto-Negotiation Enable) pin high. The SPEED and DUPLEX pins will set the ability content of the auto-negotiation register. Auto-negotiation mode can be externally disabled by pulling the ANE pin low. In this case, the SPEED pin and DUPLEX pin will change the media configuration of the RTL8201CL.

Below is a list of all configurations of the ANE/SPEED/DUPLEX pins and their operation in Fiber or UTP mode.

7.2.1. Setting the Medium Type and Interface Mode to MAC

Table 22. Setting the Medium Type and Interface Mode to MAC

FX (Pin 24)	MII/SNIB (Pin 44)	Operation Mode
L	H	UTP mode and MII interface.
L	L	UTP mode and SNI interface.
H	X	Fiber mode and MII interface.

7.2.2. UTP Mode and MII Interface

Table 23. UTP Mode and MII Interface

ANE (Pin 37)	SPEED (Pin 39)	DUPLEX (Pin 38)	Operation
H	L	L	Auto-negotiation enabled. The ability field does not support 100Mbps or full duplex mode operation.
H	L	H	Auto-negotiation enabled. The ability field does not support 100Mbps operation.
H	H	L	Auto-negotiation enabled. The ability field does not support full duplex mode operation.
H	H	H	Default setup, auto-negotiation enabled. The RTL8201CL supports 10Base-T /100Base-TX, half/full duplex mode operation.
L	L	L	Auto-negotiation disabled. Forces the RTL8201CL into 10Base-T and half duplex mode.
L	L	H	Auto-negotiation disabled. Forces the RTL8201CL into 10Base-T and full duplex mode.
L	H	L	Auto-negotiation disabled. Forces the RTL8201CL into 100Base-TX and half duplex mode.
L	H	H	Auto-negotiation disabled. Forces the RTL8201CL into 100Base-TX and full duplex mode.

7.2.3. UTP Mode and SNI Interface

SNI interface to MAC (only operates in 10Base-T when the SNI interface is enabled)

Table 24. UTP Mode and SNI Interface

ANE (Pin 37)	SPEED (Pin 39)	DUPLEX (Pin 38)	Operation
X	X	L	The duplex pin is pulled low to support the 10Base-T half duplex function. 10Base-T half duplex is the specified default mode in the SNI interface.
X	X	H	The RTL8201CL also supports full duplex in SNI mode. The duplex pin is pulled high to support 10Base-T full duplex function.

7.2.4. Fiber Mode and MII Interface

The RTL8201CL only supports 100Base-FX when Fiber mode is enabled. ANE (Auto-Negotiation Enable) and SPEED configuration is ignored when Fiber mode is enabled.

Table 25. Fiber Mode and MII Interface

ANE (Pin 37)	SPEED (Pin 39)	DUPLEX (Pin 38)	Operation
X	X	H	The duplex pin is pulled high to support 100Base-FX full duplex function.
X	X	L	The duplex pin is pulled low to support 100Base-FX half duplex function.

7.3. Flow Control Support

The RTL8201CL supports flow control indications. The MAC can program the MII register to indicate to the PHY that flow control is supported. When the MAC supports the Flow Control mechanism, setting bit 10 of the ANAR register using the MDC/MDIO SMI interface, then the RTL8201CL will add the ability to its NWay ability. If the Link partner also supports Flow Control, then the RTL8201CL can recognize the Link partner's NWay ability by examining bit 10 of ANLPAR (register 5).

7.4. Hardware Configuration and Auto-Negotiation

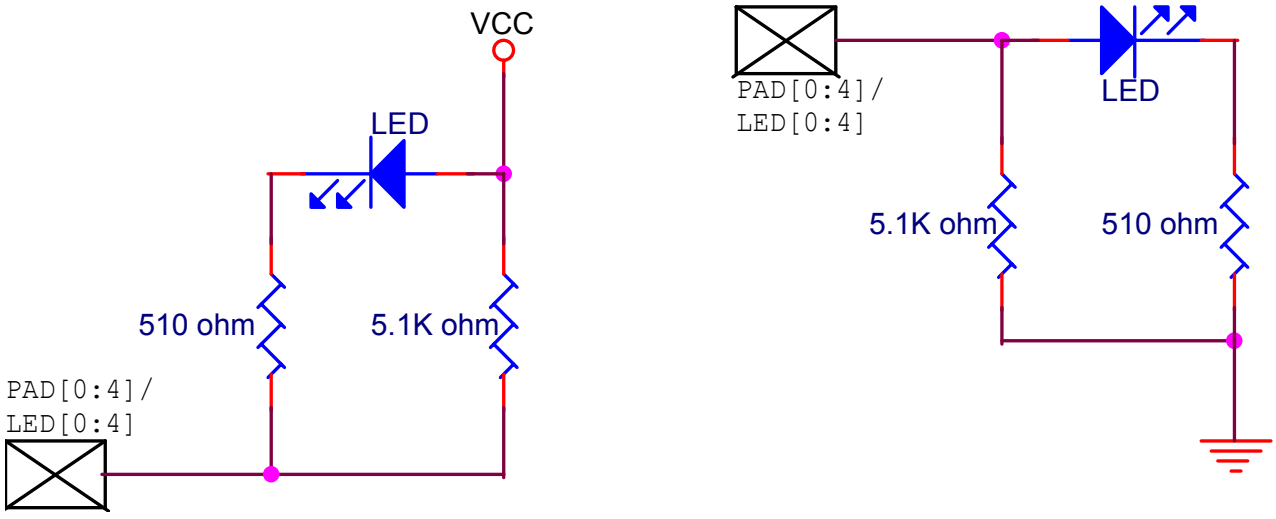
This section describes methods to configure the RTL8201CL and set the auto-negotiation mode. Table 26 shows the various pins and their settings.

Table 26. Auto-Negotiation Mode Pin Settings

Pin Name	Description
Isolate	Set high to isolate the RTL8201CL from the MAC. This will also isolate the MDC/MDIO management interface. In this mode, power consumption is minimum (see 7.7 Power Down, Link Down, Power Saving, and Isolation Modes, page 20).
RPTR	Pull high to set the RTL8201CL into repeater mode. This pin is pulled low by default (see 7.9 Repeater Mode Operation, page 22.
LDPS	Pull high to set the RTL8201CL into LDPS mode. This pin is pulled low by default (see 7.7 Power Down, Link Down, Power Saving, and Isolation Modes, page 20).
MII/SNIB	Pull high to set RTL8201CL into MII mode operation, which is the default mode for the RTL8201. This pin pulled low will set the RTL8201CL into SNI mode operation. When set to SNI mode, the RTL8201CL will operate at 10Mbps (see 7.6 Serial Network Interface, page 20).
ANE	Auto-Negotiation Enable. Pull high to enable auto-negotiation (default). Pull low to disable auto-negotiation and activate the parallel detection mechanism (see 7.2 Auto-Negotiation and Parallel Detection, page 16).
SPEED	When ANE is pulled high, the ability to adjust speed is setup. When ANE is pulled low, pull this pin low to force 10Mbps operation and high to force 100Mbps operation (see 7.2 Auto-Negotiation and Parallel Detection, page 16).
DUPLEX	When ANE is pulled high, the ability to adjust the DUPLEX pin will be setup. When ANE is pulled low, pull this pin low to force half duplex and high to force full duplex operation (see 7.2 Auto-Negotiation and Parallel Detection, page 16).

7.5. LED and PHY Address Configuration

In order to reduce the pin count on the RTL8201CL, the LED pins are duplexed with the PHY address pins. Because the PHYAD strap options share the LED output pins, the external combinations required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD input upon power-up/reset. For example, as Figure 5 (left-side) shows, if a given PHYAD input is resistively pulled high then the corresponding output will be configured as an active low driver. On the right side, we can see that if a given PHYAD input is resistively pulled low then the corresponding output will be configured as an active high driver. The PHY address configuration pins should not be connected to GND or VCC directly, but must be pulled high or low through a resistor (ex 5.1KΩ). If no LED indications are needed, the components of the LED path (LED+510Ω) can be removed.



PHY Address[:] = Logical 1
LED Indication = Active low

PHY Address[:] = Logical 0
LED Indication = Active High

Figure 5. LED and PHY Address Configuration

Table 27. LED Definitions

LED	LED Definitions
LED0	Link
LED1	Full Duplex
LED2	[CL LED Mode]10-Activity
LED3	[CL LED Mode]Fiber/100-Activity
LED4	Collision

7.6. Serial Network Interface

The RTL8201CL also supports the traditional 7-wire serial interface to operate with legacy MACs or embedded systems. To setup for this mode of operation, pull the MII/SNIB pin low. By doing so, the RTL8201CL will ignore the setup of the ANE and SPEED pins. In this mode, the RTL8201CL will set the default operation to 10Mbps and half-duplex mode.

Note: The RTL8201CL also supports full-duplex mode operation if the DUPLEX pin has been pulled high.

This interface consists of a 10Mbps transmit and receive clock generated by PHY, 10Mbps transmit and receive serial data, transmit enable, collision detect, and carry sense signals.

7.7. Power Down, Link Down, Power Saving, and Isolation Modes

The RTL8201CL offers four types of Power Saving mode operation. This section describes how to implement each mode. The first three modes are configured through software, and the fourth through hardware.

Table 28. Power Saving Mode Pin Settings

Mode	Description
Analog Off	Setting bit 11 of register 17 to 1 will put the RTL8201CL into analog off state. In analog off state, the RTL8201CL will power down all analog functions such as transmit, receive, PLL, etc. However, the internal 25MHz crystal oscillator will not be powered down. Digital functions in this mode are still available, which allows reacquisition of analog functions
LDPS	Setting bit 12 of register 17 to 1, or pulling the LDPS pin high will put the RTL8201CL into LDPS (Link Down Power Saving) mode. In LDPS mode, the RTL8201CL will detect the link status to decide whether or not to turn off the transmit function. If the link is off, FLP or 100Mbps IDLE/10Mbps NLP will not be transmitted. However, some signals similar to NLP will be transmitted. Once the receiver detects leveled signals, it will stop the signal and transmit FLP or 100Mbps IDLE/10Mbps NLP again. This can cut power used by 60%~80% when the link is down.
PWD	Setting bit 11 of register 0 to 1 puts the RTL8201CL into power down mode. This is the maximum power saving mode while the RTL8201CL is still alive. In PWD mode, the RTL8201CL will turn off all analog/digital functions except the MDC/MDIO management interface. Therefore, if the RTL8201CL is put into PWD mode and the MAC wants to recall the PHY, it must create the MDC/MDIO timing by itself (this is done by software).
Isolation	This mode is different from the three previous software configured power saving modes. This mode is configured by hardware pin 43. Setting pin 43 high will isolate the RTL8201CL from the Media Access Controller (MAC) and the MDC/MDIO management interface. In this mode, power consumption is minimal.

7.8. Media Interface

7.8.1. 100Base-TX

100Base-TX Transmit Function

Transmit data in 4-bit nibbles (TXD[3:0]) clocked at 25MHz (TXC) is transformed into 5B symbol code (4B/5B encoding). Scrambling, serializing, and conversion to 125MHz, and NRZ to NRZI then takes place. After this process, the NRZI signal is passed to the MLT-3 encoder, then to the transmit line driver.

The transmitter will first assert TXEN. Before transmitting the data pattern, it will send a /J/K/ symbol (Start-of-frame delimiter), the data symbol, and finally a /T/R/ symbol known as the End-Of-Frame delimiter. The 4B/5B and the scramble process can be bypassed via a PHY register setting (see Table 1, page 4, Pin number 24). For better EMI performance, the seed of the scrambler is based on the PHY address. In a hub/switch environment, each RTL8201CL will have different scrambler seeds and so spread the output of the MLT-3 signals.

100Base-TX Receive Function

The received signal is compensated by the adaptive equalizer to make up for signal loss due to cable attenuation and Inter Symbol Interference (ISI). Baseline Wander Correction monitors the process and dynamically applies corrections to the process of signal equalization. The PLL then recovers the timing information from the signals and from the receive clock. With this, the received signal is sampled to form NRZI data. The next steps are the NRZI to NRZ process, unscrambling of the data, serial to parallel and 5B to 4B conversion, and passing of the 4B nibble to the MII interface.

7.8.2. 100Base-FX Fiber Mode Operation

The RTL8201CL can be configured as 100Base-FX via hardware configuration. The hardware 100Base-FX setting takes priority over NWay settings. A scrambler is not required in 100Base-FX.

100Base-FX Transmit Function

Di-bits of TXD are processed as 100Base-TX except without a scrambler before the NRZI stage. Instead of converting to MLT-3 signals, as in 100Base-TX, the serial data stream is driven out as NRZI PECL signals, which enter the fiber transceiver in differential-pairs form.

100Base-FX Receive Function

The signal is received through PECL receiver inputs from the fiber transceiver and directly passed to the clock recovery circuit for data/clock recovery. The scrambler/de-scrambler is bypassed in 100Base-FX.

7.8.3. 10Base-T TX/RX

10Base-T Transmit Function

Transmit data in 4-bit nibbles (TXD[3:0]) clocked at 2.5MHz (TXC) is first fed to a parallel-to-serial converter, then the 10Mbps NRZ signal is sent to a Manchester encoder. The Manchester encoder converts the 10Mbps NRZ data into a Manchester Encoded data stream for the TP transmitter and adds a Start of Idle pulse (SOI) at the end of the packet as specified in IEEE 802.3. Finally, the encoded data stream is shaped by a bandlimited filter embedded in the RTL8201CL and then transmitted.

10Base-T Receive Function

In 10Base-T receive mode, the Manchester decoder in the RTL8201CL converts the Manchester encoded data stream into NRZ data by decoding the data and stripping off the SOI pulse. Then the serial NRZ data stream is converted to a parallel 4-bit nibble signal (RXD[0:3]).

7.9. Repeater Mode Operation

Setting bit 15 of register 17 to 1, or pulling the RPTR pin high, sets the RTL8201CL into repeater mode. In repeater mode, the RTL8201CL will assert CRS high only when receiving a packet. In NIC mode, the RTL8201CL will assert CRS high both when transmitting and receiving packets. If using the RTL8201CL in a NIC or switch application, set to the default mode. NIC/Switch mode is the default setting and has the RPTR pin pulled low, or bit 15 of register 17 is set to 0.

7.10. Reset, and Transmit Bias

The RTL8201CL can be reset by pulling the RESETB pin low for about 10ms, then pulling the pin high. It can also be reset by setting bit 15 of register 0 to 1, and then setting it back to 0. Reset will clear the registers and re-initialize them. The media interface will disconnect and restart the auto-negotiation/parallel detection process.

The RTSET pin must be pulled low by a 2KΩ resister with 1% accuracy to establish an accurate transmit bias. This will affect the signal quality of the transmit waveform. Keep its circuitry away from other clock traces and transmit/receive paths to avoid signal interference.

7.11. 3.3V Power Supply and Voltage Conversion Circuit

The RTL8201CL is fabricated in a 0.18μm process. The core circuit needs to be powered by 1.8V, however, the digital IO and DAC circuits need a 3.3V power supply. A regulator is embedded in the RTL8201CL to convert 3.3V to 1.8V. As with many commercial voltage conversion devices, the 1.8V output pin (PWFBOUT) of this circuit requires the use of an output capacitor (22uF tantalum capacitor) as part of the device frequency compensation, and another small capacitor (0.1uF) for high frequency noise de-coupling.

PWFBIN is fed with the 1.8V power from PWFBOUT through a ferrite bead as shown in the reference design schematic document (available for download from www.realtek.com.tw).

Note: Do not supply 1.8V produced by any power device other than PWFBOUT and PWFBIN.

The analog and digital ground planes should be as large and intact as possible. If the ground plane is large enough, the analog and digital grounds can be separated, which is the ideal configuration. However, if the total ground plane is not sufficiently large, partition of the ground plane is not a good idea. In this case, all the ground pins can be connected together to a larger single and intact ground plane.

7.12. Far End Fault Indication

The MII Reg.1.4 (Remote Fault) is the Far End Fault Indication (FEFI) bit when 100FX mode is enabled and indicates when a FEFI has been detected. FEFI is an alternative in-band signaling method which is composed of 84 consecutive ‘1’s followed by one ‘0’. When the RTL8201CL detects this pattern three times, Reg.1.4 is set, which means the transmit path (the Remote side’s receive path) has a problem. On the other hand, if an incoming signal fails to cause a ‘Link OK’, the RTL8201CL will start sending this pattern, which in turn causes the remote side to detect a Far End Fault. This means that the receive path has a problem from the point of view of the RTL8201CL. The FEFI mechanism is used only in 100Base-FX mode.

8. Characteristics

8.1. DC Characteristics

8.1.1. Absolute Maximum Ratings

Table 29. Absolute Maximum Ratings

Item	Minimum	Typical	Maximum
Supply Voltage	3.0V	3.3V	3.6V
Storage Temperature	-55°C		125°C

8.1.2. Operating Conditions

Table 30. Operating Conditions

Item	Conditions	Minimum	Typical	Maximum
Vcc 3.3V	3.3V Supply voltage	3.0V	3.3V	3.6V
TA	Operating Temperature	0°C		70°C

8.1.3. Power Dissipation

Test condition: VCC=3.3V

Table 31. Power Dissipation

Symbol	Condition	Total Current Consumption
P_{LDPS}	Link down power saving mode	19mA
P_{AnaOff}	Analog off mode	19mA
P_{PWD}	Power down mode	14mA
$P_{Isolate}$	Isolate mode	14mA
P_{100F}	100Base full duplex	116mA
P_{10F}	10Base-T full duplex	120mA
P_{10TX}	10Base-T transmit	120mA
P_{10RX}	10Base-T receive	19mA
P_{10IDLE}	10Base-T idle	18mA

8.1.4. Input Voltage: Vcc

Table 32. Input Voltage: Vcc

Symbol	Condition		Minimum	Maximum
TTL V_{IH}	Input High Vol.		0.5*Vcc	Vcc +0.5V
TTL V_{IL}	Input Low Vol.		-0.5V	0.3*Vcc
TTL V_{OH}	Output High Vol.	IOH=-8mA	0.65*Vcc	Vcc
TTL V_{OL}	Output Low Vol.	IOL=8mA		0.3*Vcc
TTL I_{OZ}	Tri-state Leakage	Vout=Vcc or GND	-110uA	10uA
I_{IN}	Input Current	Vin=Vcc or GND	-1uA	10uA
I_{PL}	Input Current with internal weak pull low resistor	Vin=Vcc or GND	-1uA	100uA
I_{PH}	Input Current with internal weak pull high resistor	Vin=Vcc or GND	-110uA	10uA

Symbol	Condition		Minimum	Maximum
PECL V_{IH}	PECL Input High Vol.		Vdd -1.16V	Vdd -0.88V
PECL V_{IL}	PECL Input Low Vol.		Vdd -1.81V	Vdd -1.47V
PECL V_{OH}	PECL Output High Vol.		Vdd -1.02V	
PECL V_{OL}	PECL Output Low Vol.			Vdd -1.62V

8.2. AC Characteristics

8.2.1. MII Transmission Cycle Timing

Table 33. MII Transmission Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t_1	TXCLK high pulse width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_2	TXCLK low pulse width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_3	TXCLK period	100Mbps		40		ns
		10Mbps		400		ns
t_4	TXEN, TXD[0:3] setup to TXCLK rising edge	100Mbps	10	24		ns
		10Mbps	5			ns
t_5	TXEN, TXD[0:3] hold after TXCLK rising edge	100Mbps		10	25	ns
		10Mbps	5			ns
t_6	TXEN sampled to CRS high	100Mbps			40	ns
		10Mbps			400	ns
t_7	TXEN sampled to CRS low	100Mbps			160	ns
		10Mbps			2000	ns
t_8	Transmit latency	100Mbps	60	70	140	ns
		10Mbps			2000	ns
t_9	Sampled TXEN inactive to end of frame	100Mbps		100	170	ns
		10Mbps				ns

Figure 6 shows an example of a packet transfer from MAC to PHY on the MII interface.

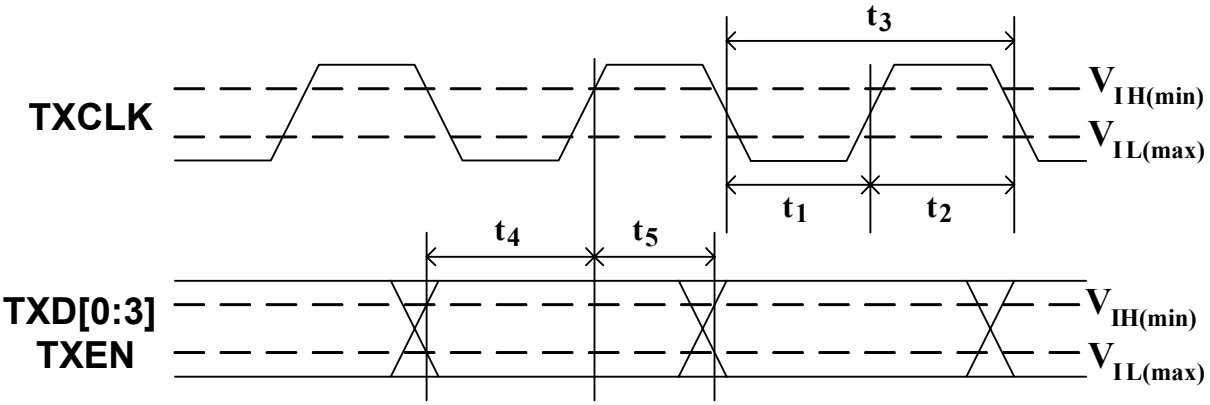


Figure 6. MII Transmission Cycle Timing-1

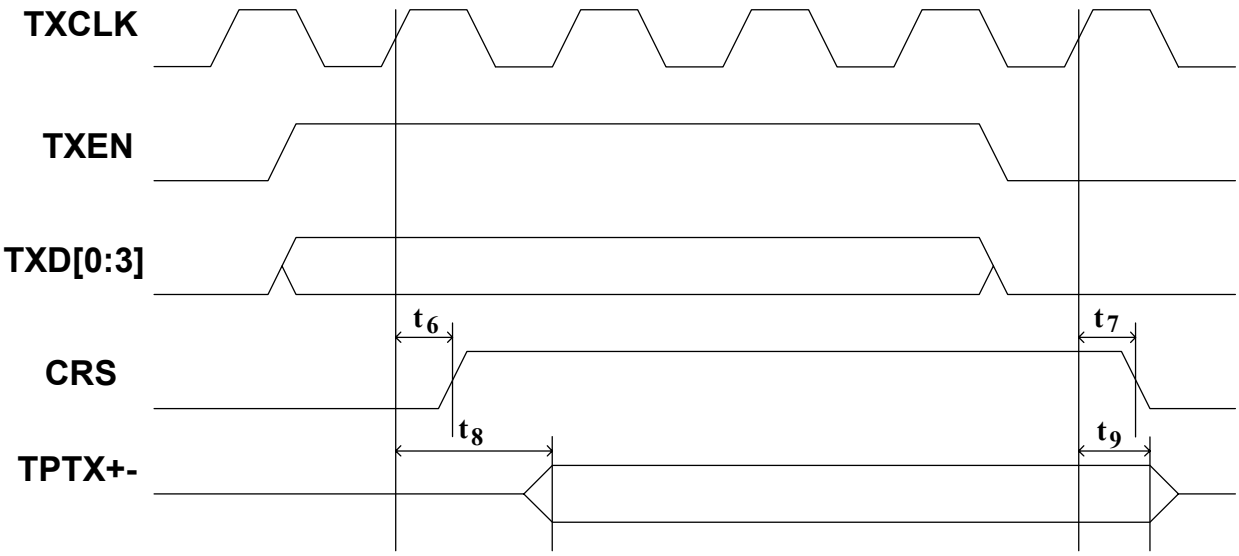


Figure 7. MII Transmission Cycle Timing-2

8.2.2. MII Reception Cycle Timing

Table 34. MII Reception Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t_1	RXCLK high pulse width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_2	RXCLK low pulse width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_3	RXCLK period	100Mbps		40		ns
		10Mbps		400		ns
t_4	RXER, RXDV, RXD[0:3] setup to RXCLK rising edge	100Mbps	10			ns
		10Mbps	6			ns
t_5	RXER, RXDV, RXD[0:3] hold after RXCLK rising edge	100Mbps	10			ns
		10Mbps	6			ns
t_6	Receive frame to CRS high	100Mbps			130	ns
		10Mbps			2000	ns
t_7	End of receive frame to CRS low	100Mbps			240	ns
		10Mbps			1000	ns
t_8	Receive frame to sampled edge of RXDV	100Mbps			150	ns
		10Mbps			3200	ns
t_9	End of receive frame to sampled edge of RXDV	100Mbps			120	ns
		10Mbps			1000	ns

Figure 8 shows an example of a packet transfer from PHY to MAC on the MII interface.

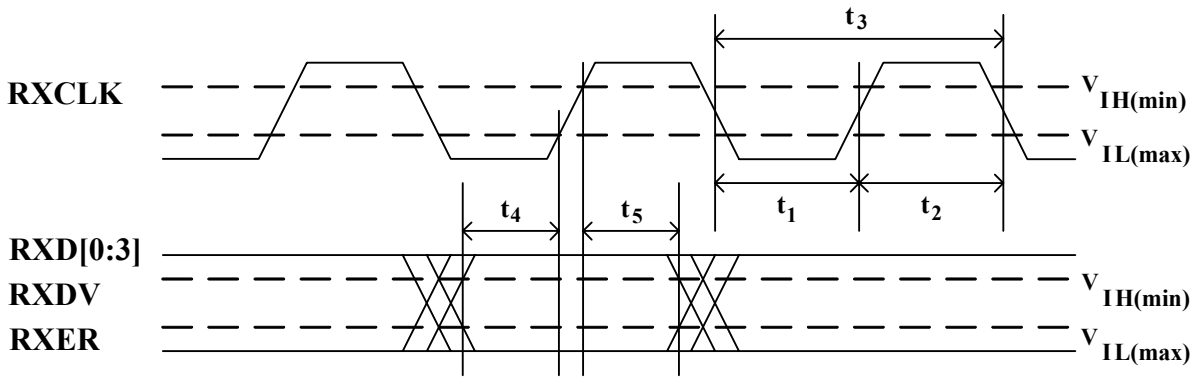


Figure 8. MII Reception Cycle Timing-1

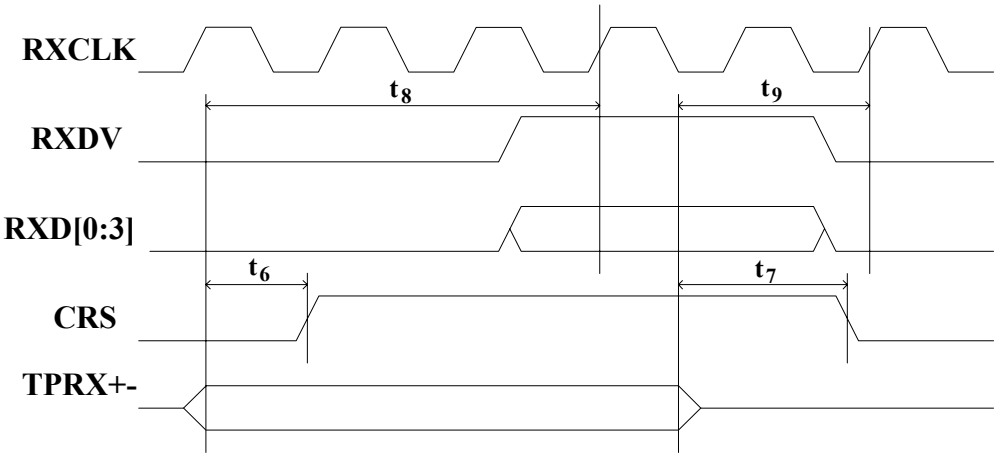


Figure 9. MII Reception Cycle Timing-2

8.2.3. SNI Transmission Cycle Timing

Table 35. SNI Transmission Cycle Timing

Symbol	Description	Minimum	Maximum	Unit
t_1	TXCLK high pulse width	36		ns
t_2	TXCLK low pulse width	36		ns
t_3	TXCLK period	80	120	ns
t_4	TXEN, TXD0 setup to TXCLK rising edge	20		ns
t_5	TXEN, TXD0 hold after TXCLK rising edge	10		ns
t_8	Transmit latency		50	ns

Figure 10 shows an example of a packet transfer from MAC to PHY on the SNI interface.
Note: SNI mode only runs at 10Mbps.

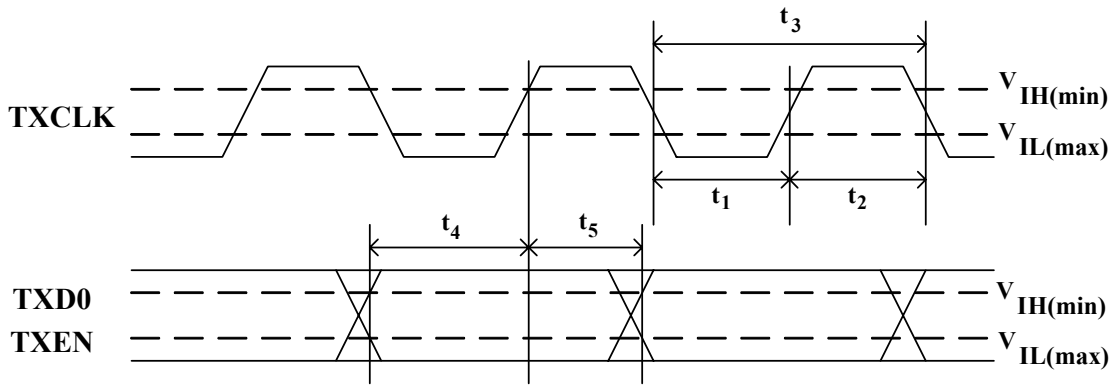


Figure 10. SNI Transmission Cycle Timing-1

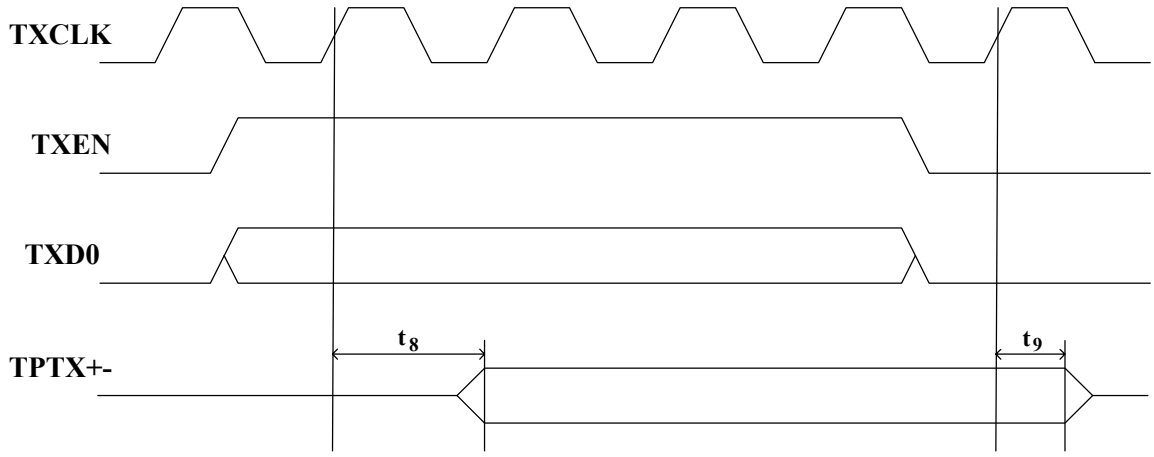


Figure 11. SNI Transmission Cycle Timing-2

8.2.4. SNI Reception Cycle Timing

Table 36. SNI Reception Cycle Timing

Symbol	Description	Minimum	Typical	Maximum	Unit
t_1	RXCLK high pulse width	36			ns
t_2	RXCLK low pulse width	36			ns
t_3	RXCLK period	80		120	ns
t_4	RXD0 setup to RXCLK rising edge	40			ns
t_5	RXD0 hold after RXCLK rising edge	40			ns
t_6	Receive frame to CRS high			50	ns
t_7	End of receive frame to CRS low			160	ns
t_8	Decoder acquisition time		600	1800	ns

Figure 12 shows an example of a packet transfer from PHY to MAC on the SNI interface.
Note: SNI mode only runs at 10Mbps.

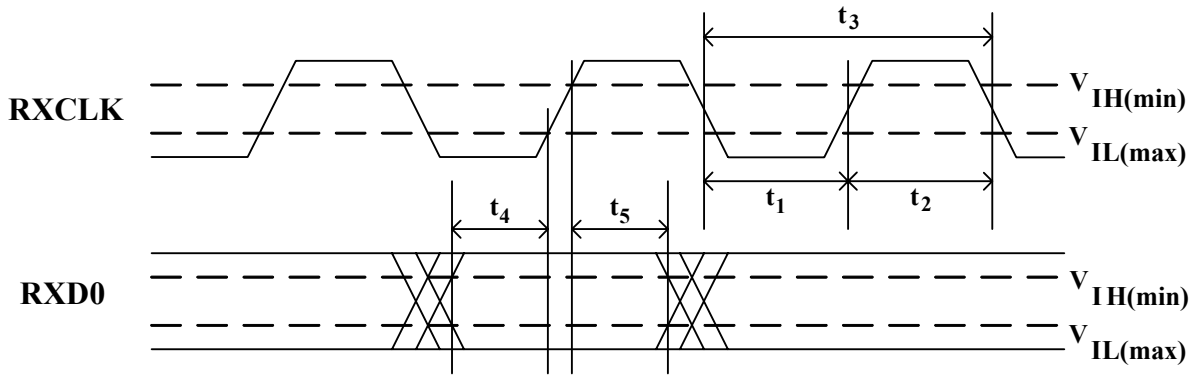


Figure 12. SNI Reception Cycle Timing-1

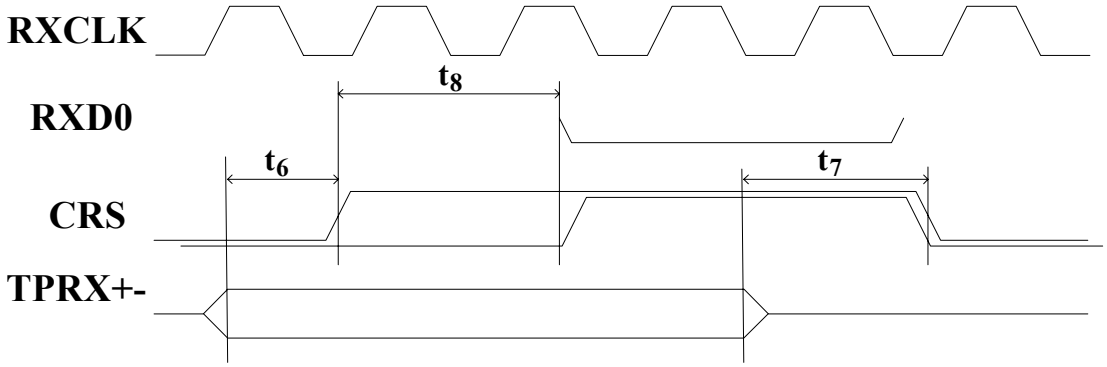


Figure 13. SNI Reception Cycle Timing-2

8.2.5. MDC/MDIO Timing

Table 37. MDC/MDIO Timing

Symbol	Description	Minimum	Maximum	Unit
t_1	MDC high pulse width	160		ns
t_2	MDC low pulse width	160		ns
t_3	MDC period	400		ns
t_4	MDIO setup to MDC rising edge	10		ns
t_5	MDIO hold time from MDC rising edge	10		ns
t_6	MDIO valid from MDC rising edge	0	300	ns

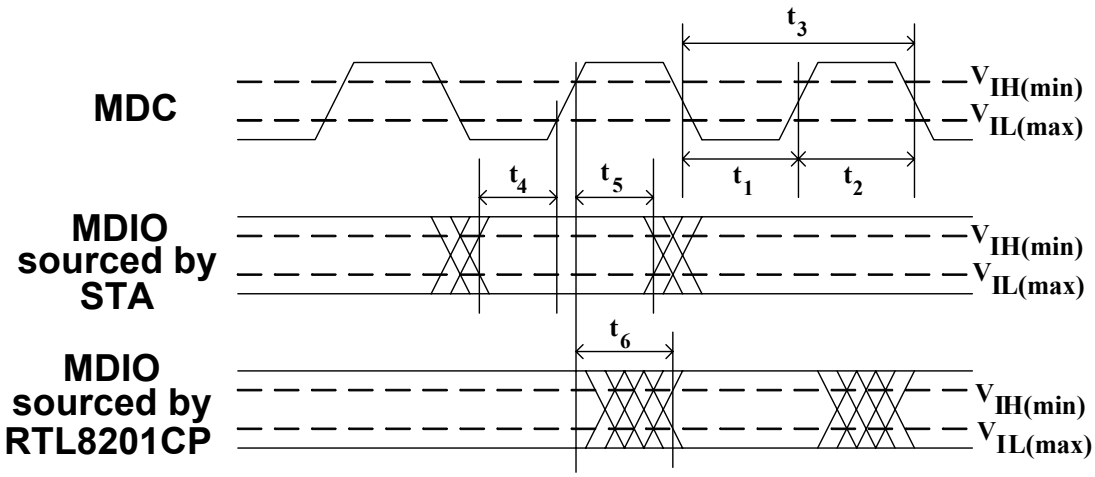


Figure 14. MDC/MDIO Timing

Transmission Without Collision

Figure 15 shows an example of a packet transfer from MAC to PHY.

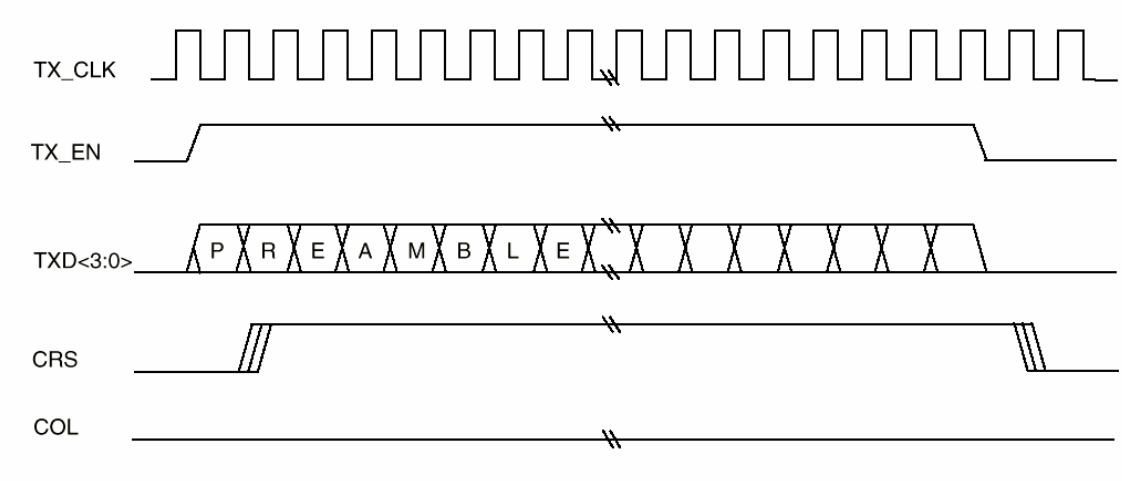


Figure 15. MDC/MDIO MAC to PHY Transmission Without Collision

Reception Without Error

Figure 16 shows an example of a packet transfer from PHY to MAC.

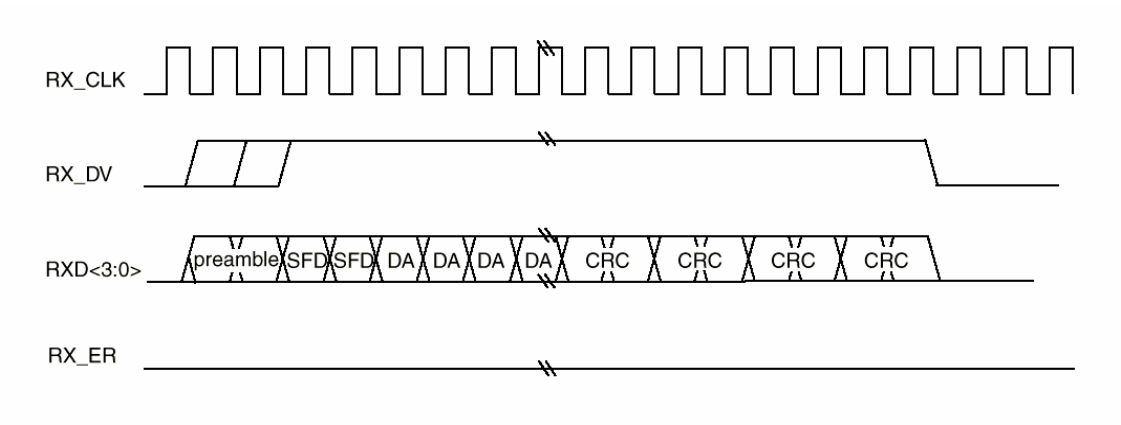


Figure 16. MDC/MDIO PHY to MAC Reception Without Error

8.3. Crystal Characteristics

Table 38. Crystal Characteristics

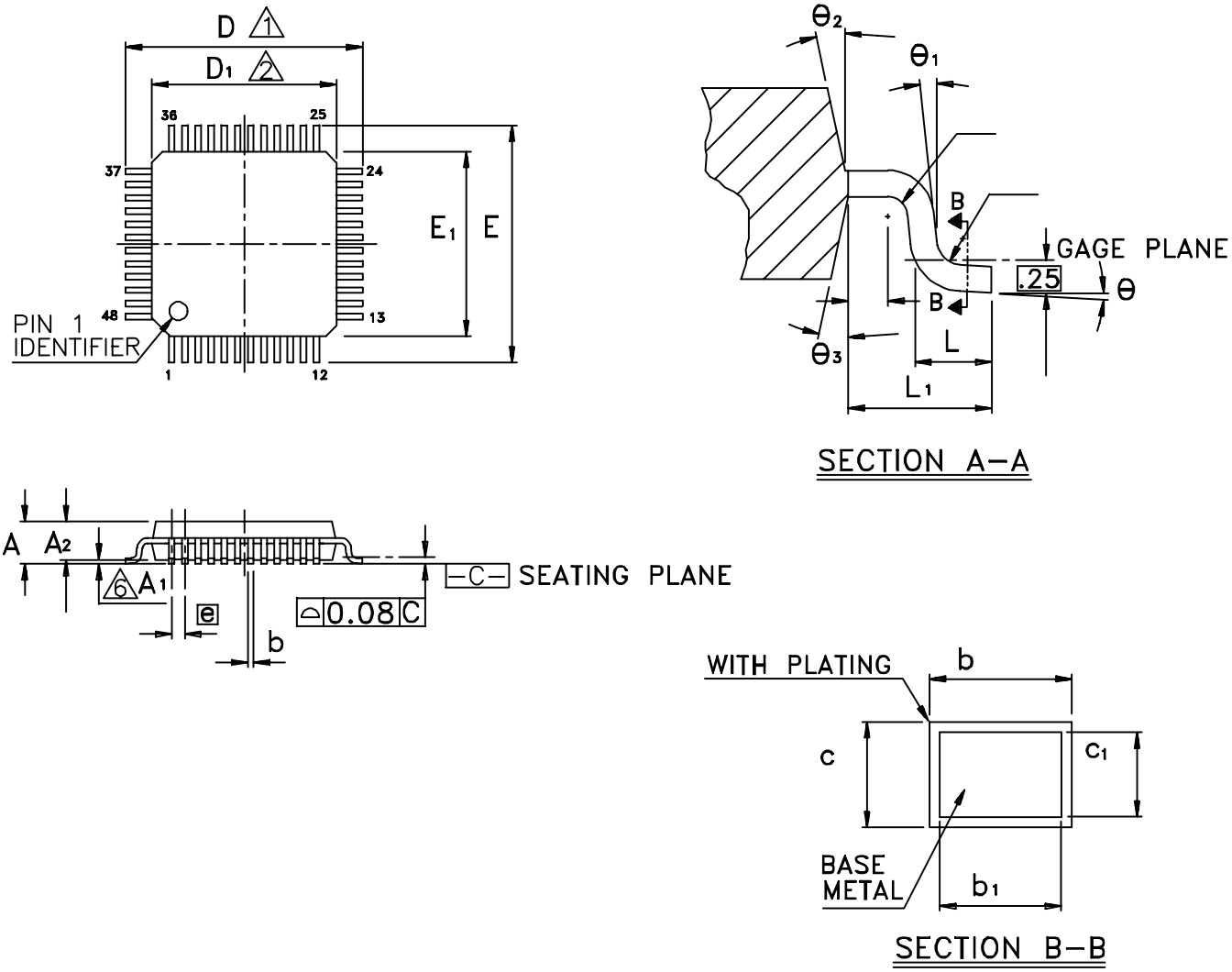
Parameter	Range
Nominal Frequency	25.000MHz
Oscillation Mode	Base wave
Frequency Tolerance at 25°C	±50 ppm
Operating Temperature Range	-10°C ~ +70°C
Equivalent Series Resistance	30 ohm Max.
Drive Level	0.1 mV
Load Capacitance	20 pF
Shunt Capacitance	7 pF Max.
Insulation Resistance	Mega ohm Min./DC 100V
Test Impedance Meter	Saunders 250A
Aging Rate Per Year	±0.0003%

8.4. Transformer Characteristics

Table 39. Transformer Characteristics

Parameter	Transmit End	Receive End
Turn Ratio	1:1 CT	1:1
Inductance (min.)	350 uH @ 8mA	350 uH @ 8mA

9. Mechanical Dimensions



See the following page for drawing related notes.

9.1. Mechanical Dimensions Notes

Symbol	Dimension in inchs			Dimension in millimeters		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.067	-	-	1.70
A1	0.000	0.004	0.008	0.00	0.1	0.20
A2	0.051	0.055	0.059	1.30	1.40	1.50
b	0.006	0.009	0.011	15	0.22	0.29
b1	0.006	0.008	0.010	0.15	0.20	0.25
c1	0.004	-	0.006	0.09	-	0.16
D	0.354 BSC			9.00 BSC		
D1	0.276 BSC			7.00 BSC		
E	0.354 BSC			9.00 BSC		
E1	0.276 BSC			7.00 BSC		
e	0.020 BSC			0.50 BSC		
L	0.016	0.024	0.031	0.40	0.60	0.80
L1	0.039 REF			1.00 REF		
θ	0°	3.5°	9°	0°	3.5°	9°
θ1	0°	-	-	0°	-	-
θ2	12° TYP			12° TYP		
θ3	12° TYP			12° TYP		

Notes:
1.To be determined at seating plane -c-
2.Dimensions D1 and E1 do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3.Dimension b does not include dambar protrusion. Dambar can not be located on the lower radius of the foot.
4.Exact shape of each corner is optional.
5.These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7.Controlling dimension: millimeter.
8. Reference document: JEDEC MS-026, BBC

TITLE: 48LD LQFP (7x7x1.4mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL:		
APPROVE	DOC. NO.	
	VERSION	1
	PAGE	OF
CHECK	DWG NO.	SS048 - P1
	DATE	
REALTEK SEMICONDUCTOR CORP.		

10. Ordering Information

Table 40. Ordering Information

Part Number	Package	Status
RTL8201CL	Rev. C. 48-pin LQFP	
RTL8201CL-LF	Rev. C. 48-pin LQFP Lead (Pb)-Free package	
RTL8201CL-VD	Rev. D. 48-pin LQFP	
RTL8201CL-VD-LF	Rev. D. 48-pin LQFP Lead (Pb)-Free package	

Note: See page 3 for lead (Pb)-free package identification.

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