RTL8211BG-GR

INTEGRATED 10/100/1000 GIGABIT ETHERNET TRANSCEIVER

DATASHEET

Rev. 1.2
18 July 2007
Track ID: JATR-1076-21

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com.tw

COPYRIGHT

DISCLAIMER

Realtek provides this document "as is", without warranty of any kind, neither expressed nor implied, including, but not limited to, the particular purpose. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2007/06/05	First release.
1.1	2007/07/05	Added Figure 3, page 11. Corrected section 11 Ordering Information, page 43.
1.2	2007/07/18	Modify pin 34, and 51~56 descriptions, Table 3, page 4.

Table of Contents

List of Tables

List of Figures

1. General Description

The Realtek RTL8211BG is a highly integrated Ethernet transceiver that complies with 10Base-T, 100Base-TX, and 1000Base-T IEEE 802.3 standards. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable.

The RTL8211BG uses state-of-the-art DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented in the RTL8211BG to provide robust transmission and reception capabilities at 10Mbps, 100Mbps, or 1000Mbps.

Data transfer between MAC and PHY is via the Reduced Gigabit Media Independent Interface (RGMII) and Gigabit Media Independent Interface (GMII), for 1000Base-T, and Media Independent Interface (MII) for 10Base-T/100Base-TX.

2. Features

- 1000Base-T IEEE 802.3ab Compliant
- 100Base-TX IEEE 802.3u Compliant
- 10Base-T IEEE 802.3 Compliant
- IEEE 802.3 Compliant RGMII/GMII/MII
- Supports Auto-Negotiation
- Supports Parallel Detection
- Crossover Detection & Auto-Correction
- Automatic polarity correction
- Transmit wave-shaping
- DSP processing
- Internal hybrids for 1000Base-T
- Baseline Wander Correction
- Supports half/full duplex operation
- Transmission rate up to 1Gbps over industry standard CAT.5 UTP cable with BER less than 10-10 in 1000Base-T
- The design transceiver capability target is up to 140m for CAT.5 cable in 1000Base-T
- Supports 3.3V or 2.5V signaling for GMII /RGMII
- Supports power down mode
- Supports Link Down Power Saving
- Supports 25MHz external crystal or OSC
- Provides 125MHz clock source for MAC
- Provides 6 network status LEDs
- 100-pin LQFP
- 0.15µm process with very low power consumption

3. System Applications

Network Interface Adapter, MAU (Media Access Unit), CNR (Communication and Network Riser), ACR (Advanced Communication Riser), Ethernet hub, Ethernet switch.

In addition, it can be used in any embedded system with an Ethernet MAC that needs a UTP physical connection.

4. Pin Assignments

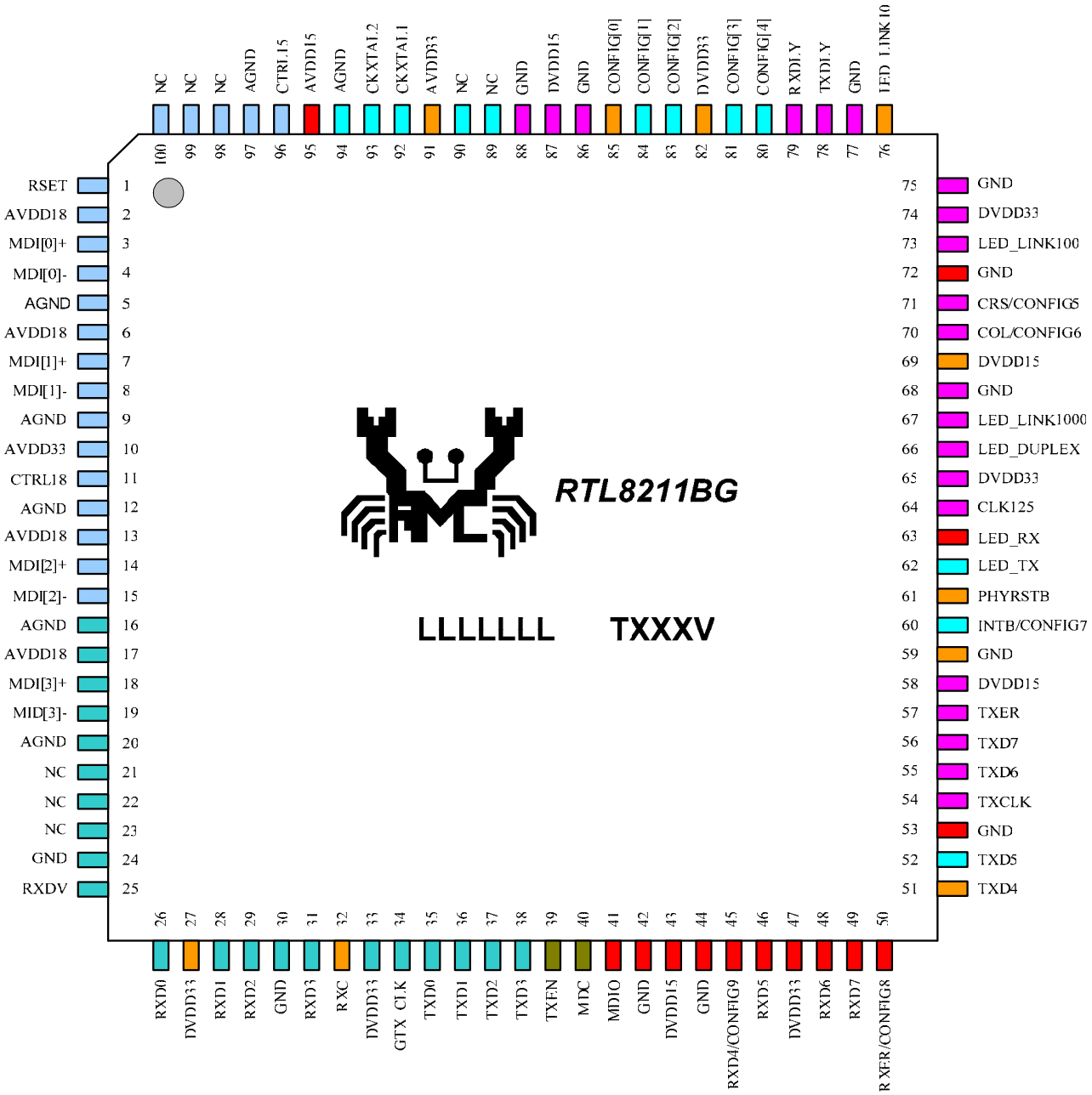


Figure 1. Pin Assignments (100-Pin LQFP)

4.1. Package Identification

'Green' package is indicated by a 'G' in the location marked 'T' in Figure 1.

5. Pin Descriptions

5.1. Transceiver Interface

Table 1. Transceiver Interface

Pin No.	Pin Name	Type	Description
3	MDI+[0]	I/O	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
4	MDI–[0]	I/O	
7	MDI+[1]	I/O	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
8	MDI–[1]	I/O	
14	MDI+[2]	I/O	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
15	MDI–[2]	I/O	
18	MDI+[3]	I/O	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
19	MDI–[3]	I/O	

5.2. Clock

Table 2. Clock

Pin No.	Pin Name	Type	Description
92	CKXTAL1	I	Input/Output of 25MHz Clock Reference.
93	CKXTAL2	O	
64	CLK125	O	125MHz Reference Clock Generated from Internal PLL.

5.3. RGMII/GMII/MII

Table 3. RGMII/GMII/MII

Pin No.	Pin Name	Type	Description
54	TXCLK	O	Transmit Clock in MII Mode.
34	GTXCLK	I	In RGMII mode the transmit reference clock will be 125MHz, 25MHz, or 2.5MHz ±50ppm depending on speed.
35	TXD[0]	I	Transmit Data. Data is transmitted from MAC to PHY via TXD[7:0] in GMII 1000Base-T. In RGMII and 10/100Base-TX, only TXD[3:0] are active and valid.
36	TXD[1]	I	
37	TXD[2]	I	
38	TXD[3]	I	
51	TXD[4]	I	
52	TXD[5]	I	
55	TXD[6]	I	
56	TXD[7]	I	
39	TXEN	I	Transmit Enable. In RGMII the pin name is TXCTL.
57	TXER		Transmit Error. When both TXER and TXEN are asserted, the transmit error symbol is transmitted onto the cable. When TXER is asserted and TXEN is de-asserted, the carrier extension symbol is transmitted onto the cable.
32	RXC	O	The continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz ±50ppm. and shall be derived from the received data stream
26	RXD[0]	O	Receive Data. Data is transmitted from PHY to MAC via RXD[7:0] in GMII 1000Base-T. In RGMII and 10/100Base-TX only RXD[3:0] are active and valid
28	RXD[1]	O	
29	RXD[2]	O	
31	RXD[3]	O	
45	RXD[4]	O	
46	RXD[5]	O	
48	RXD[6]	O	
49	RXD[7]	O	
25	RXDV	O	Receive Data Valid. In RGMII the pin name is RXCTL.
50	RXER	O	Receive Error. When both RXER and RXDV are asserted, an error symbol is received from the cable. When RXER is asserted and RXDV is de-asserted, it means false carrier or carrier extension symbol is detected on the cable.
70	COL	O	Collision In Half Duplex Mode.
71	CRS	O	Carrier Sense in RGMII/MII Mode.
78	TXDLY	I	RGMII Transmit Clock Timing Control. 1 = Add 2ns delay to TXC for TXD latching
79	RXDLY	I	RGMII Receiver Clock Timing Control. 1 = Add 2ns delay to RXC for RXD latching

5.4. Management Interface

Table 4. Management Interface

Pin No.	Pin Name	Type	Description
40	MDC	I	Management Data Clock.
41	MDIO	I/O	Input/Output of Management Data.
60	INTB	O	Interrupt. Active low.

5.5. Reset

Table 5. Reset

Pin No.	Pin Name	Type	Description
61	PHYRSTB	I	Hardware Reset. Active low.

5.6. Mode Selection

Table 6. Mode Selection

Pin No.	Pin Name	Type	Description
85	CONFIG[0]	I	PHY Configuration.
84	CONFIG[1]	I	
83	CONFIG[2]	I	
81	CONFIG[3]	I	
80	CONFIG[4]	I	
71	CONFIG[5]	I	
70	CONFIG[6]	I	
60	CONFIG[7]	I	
50	CONFIG[8]	I	
45	CONFIG[9]	I	

Note: See section 6.3 Hardware Configuration, page 8, for details.

5.7. LED Indication

Table 7. LED Indication

Pin No.	Pin Name	Type	Description
76	LED_LINK10	O	LED 1, 10Mbps Link Indicator.
73	LED_LINK100	O	LED 2, 100Mbps Link Indicator.
67	LED_LINK1000	O	LED 3, 1000Mbps Link Indicator.
66	LED_DUPLEX	O	Duplex LED.
63	LED_RX	O	Receive LED.
62	LED_TX	O	Transmit LED.

Note: See section 7.3.9 LEDCR (LED Control Register, Address 0x18), page 32, for details.

5.8. Regulator & Reference

Table 8. Regulator & Reference

Pin No.	Pin Name	Type	Description
1	RSET	I	Reference. External resistor reference.
11	CTRL18	O	Regulator Control. Voltage control to external 1.8V regulator.
96	CTRL15	O	Regulator Control. Voltage control to external 1.5V regulator.

5.9. Power & Ground

Table 9. Power & Ground

Pin No.	Pin Name	Type	Description
27, 33, 47, 65, 74, 82	DVDD33	Power	RGMII/GMII interface I/O voltage =3.3V (2.5V tolerance).
43, 58, 69, 87,	DVDD15	Power	Digital Power. 1.5V.
10, 91	AVDD33	Power	Analog Power. 3.3V.
2, 6, 13, 17	AVDD18	Power	Analog Power. 1.8V.
95	AVDD15	Power	Analog Power. 1.5V.
5, 9, 12, 16, 20, 94, 97	AGND	Ground	Analog Ground.
24, 30, 42, 44, 53, 59, 68, 72, 75, 77, 86, 88	DGND	Ground	Digital Ground.

5.10. Not Connected

Table 10. Not Connected

Pin No. (100-pin)	Pin Name	Type	Description
21, 22, 23, 89, 90, 98, 99, 100	NC	NC	0: Not Connected.

6. Function Description

6.1. Transmitter

Based on state-of-the-art DSP technology and mixed-mode signal processing technology, the RTL8211BG is capable of operating at 10/100/1000Mbps link speed over standard CAT.5 UTP cable and CAT.3 UTP cable (10Mbps).

6.1.1. GMII/RGMII (1000Mbps) Mode

The RTL8211BG's PCS layer receives data bytes from the MAC through the GMII/RGMII interface and performs the generation of continuous code-groups through 4D-PAM5 coding technology. Then, those code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

6.1.2. MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. After that, the NRZI signal are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

6.1.3. MII (10Mbps) Mode

The transmit 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. Then, the 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

6.2. Receiver

6.2.1. GMII/RGMII (1000Mbps) Mode

Input signals from the media first pass through the on-chip sophisticated hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. Afterwards, the received signal is processed with state-of-the-art technology, such as adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. Then, the 8-bit-wide data is recovered and is sent to the GMII/RGMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the receive MII/GMII/RGMII interface and sends it to the Rx Buffer Manager.

6.2.2. MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

6.2.3. MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder, and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

6.3. Hardware Configuration

The operation speed, interface mode, and PHY address can be set by the CONFIG[9:0] pins. The respective value mapping of CONFIG[9:0] with the configurable vector is listed in Table 11. To set the CONFIG[9:0] pins, the externally pull-high or pull-low by resister are required.

Table 11. CONFIG[9:0] Pins vs. Configuration Register

Pin	Pin Name
CONFIG[0]	PHYAD[0]
CONFIG[1]	PHYAD[1]
CONFIG[2]	PHYAD[2]
CONFIG[3]	PHYAD[3]
CONFIG[4]	PHYAD[4]
CONFIG[5]	AN[0]
CONFIG[6]	AN[1]
CONFIG[7]	AN[2]
CONFIG[8]	AN[3]
CONFIG[9]	MODE

Table 12. Configuration Register Definition

Configuration	Description
PHYAD[4:0]	PHY Address. PHYAD sets the PHY address for the device.
AN[3:0] register bit 16.6=0	Auto-Negotiation (NWay) Configuration. AN[3:0] controls the setting of Auto-Negotiation enable/disable, master/slave preference, speed and duplex setting. 0000 = 10Base-T half duplex 0001 = 10Base-T full duplex 0010 = 100Base-TX half duplex 0011 = 100Base-TX full duplex 0100 = NWay, advertise only 1000Base-T half duplex, forced Master 0101 = NWay, advertise only 1000Base-T half duplex, forced Slave 0110 = NWay, advertise only 1000Base-T half duplex, preferred Master 0111 = NWay, advertise only 1000Base-T half duplex, preferred Slave 1000 = NWay, advertise only 1000Base-T full duplex, forced Master 1001 = NWay, advertise only 1000Base-T full duplex, forced Slave 1010 = NWay, advertise only 1000Base-T full duplex, preferred Master 1011 = NWay, advertise only 1000Base-T full duplex, preferred Slave 1100 = NWay, advertise all capabilities, forced Master 1101 = NWay, advertise all capabilities, forced Slave 1110 = NWay, advertise all capabilities, prefer Master 1111 = NWay, advertise all capabilities, prefer Slave For register bit 16.6=0, the AN[3:0] bits 0100-1011 will NOT have the register bit 0.12 indicate that Auto-Negotiation is enabled. Register bit 16.6 is Enable Crossover Detection & Auto-Correction function. 1: Enable 0: Disable If Crossover Detection & Auto-Correction is enabled, then Auto-Negotiation is automatically enabled. If the Crossover Detection & Auto-Correction function is disabled then the device assumes the MDI configuration.

Configuration	Description
AN[3:0] register bit 16.6=1	Auto-Negotiation (NWay) Configuration. AN[3:0] controls the setting of Auto-Negotiation enable/disable, master/slave preference, speed and duplex setting. 0000 = NWay, 10Base-T half duplex 0001 = NWay, 10Base-T full duplex 0010 = NWay, 100Base-TX half duplex 0011 = NWay, 100Base-TX full duplex 0100 = NWay, advertise only 1000Base-T half duplex, forced Master 0101 = NWay, advertise only 1000Base-T half duplex, forced Slave 0110 = NWay, advertise only 1000Base-T half duplex, preferred Master 0111 = NWay, advertise only 1000Base-T half duplex, preferred Slave 1000 = NWay, advertise only 1000Base-T full duplex, forced Master 1001 = NWay, advertise only 1000Base-T full duplex, forced Slave 1010 = NWay, advertise only 1000Base-T full duplex, preferred Master 1011 = NWay, advertise only 1000Base-T full duplex, preferred Slave 1100 = NWay, advertise all capabilities, forced Master 1101 = NWay, advertise all capabilities, forced Slave 1110 = NWay, advertise all capabilities, prefer Master 1111 = NWay, advertise all capabilities, prefer Slave
MODE	Interface Mode Select. MODE specifies the operating mode of the RTL8211BG. 0: GMII 1: RGMII/MII to Copper

6.4. MAC/PHY Interface

The RTL8211BG supports several industry standards and is suitable for most off-the-shelf MACs with an MII/RGMII interface. They are enabled by hardware configuration bit MODE. The MII interface supports up to 100Mbps operation, and the GMII/RGMII interface supports up to 1000Mbps operation.

6.4.1. MII

In 100Base-TX and 10Base-T modes (MII mode is selected), TXC and RXC sources are 25MHz and 2.5MHz, respectively. TXC will always be generated by the MAC and RXC will always be generated by the PHY. TXD[3:0] and RXD[3:0] signals are used for date transitions.

6.4.2. GMII

In 1000Base-T mode (GMII interface is selected), the 125MHz transmit clock is expected on GTXCLK. TXCLK sources 25MHz, 2.5MHz, or 0MHz clock depending on the register setting, and RXCLK sources the 125MHz receive clock.

6.4.3. RGMII

In 1000Base-T mode (RGMII interface is selected), TXC and RXC sources are 125MHz. TXC will always be generated by the MAC and RXC will always be generated by the PHY. TXD[3:0] and RXD[3:0] signals are used for date transitions on rising edge and on falling edge of clock.

6.4.4. Management Interface

The management interface provides access to the internal registers through the MDC and MDIO pins as described in IEEE 802.3u section 22. The MDC signal, provided by the MAC, is the management data clock reference to the MDIO signal. The MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC. The MDIO pin needs a 10k Ohm pull-up resistor to maintain the MDIO high during idle and turnaround.

Preamble suppression (register bit 1.6 = 1) is the default setting of the RTL8211BG after power-on. However, there still must be at least one idle bit between operations.

Up to 32 RTL8211BGs can share the same MDIO line. In switch/router applications, each port should be assigned a unique address during the hardware reset sequence, and it can only be addressed via that unique PHY address. For detailed information on the RTL8211BG management registers, see section 7. Register Descriptions, page 20.

Table 13. Typical MDIO Frame Format

MII Management Serial Protocol	<idle><start><op code><PHY addr.><reg. addr.><turnaround><data><idle>
Read	<idle><01><10><AAAAA><RRRRR><Z0><xxxx xxxx xxxx xxxx><idle>
Write	<idle><01><01><AAAAA><RRRRR><10><xxxx xxxx xxxx xxxx><idle>

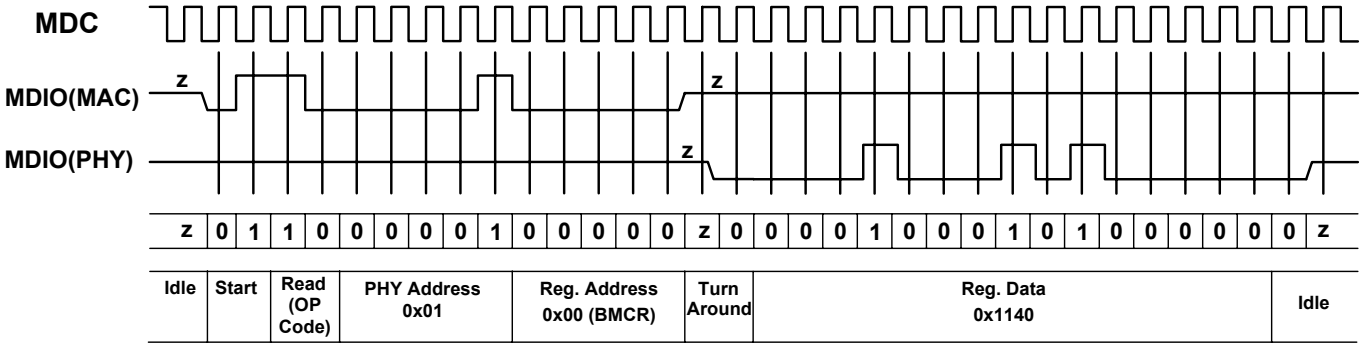


Figure 2. Typical MDC/MDIO Read Timing

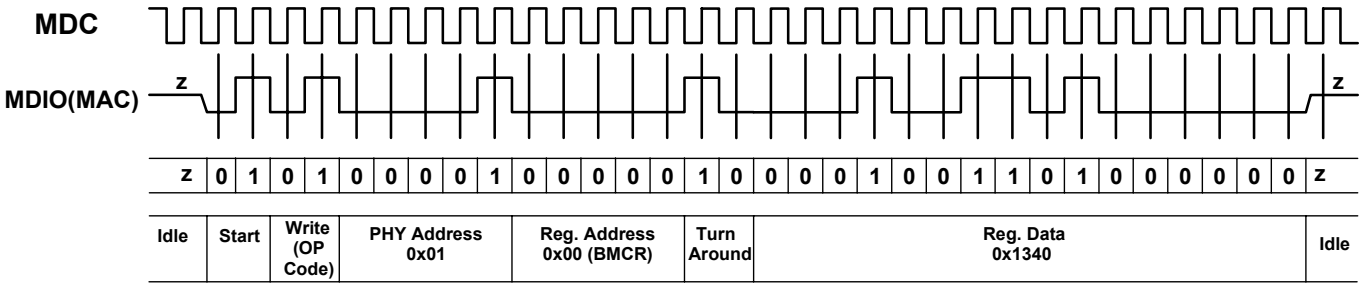


Figure 3. Typical MDC/MDIO Write Timing

6.4.5. Interrupt

Whenever the RTL8211BG detects a status change on the media, the RTL8211BG will drive the interrupt pin (INTB) low to issue an interrupt event. The MAC senses the status change and in response accesses the registers through the MDC/MDIO interface. Register 18 (Table 31, page 30) controls the mask to enable which events will assert the interrupt (INTB) signal. Register 19 (Table 32, page 31) is the interrupt status register and reflects which interrupt events have occurred, even though the corresponding bits in register 18 are not set.

The value of register 19 is cleared automatically when register 19 is read through MDC/MDIO, and the INTB is de-asserted at the same time. The RTL8211BG interrupt function removes the need for continuous polling through the MDC/MDIO management interface.

6.5. Auto-Negotiation

Auto-Negotiation is a mechanism to determine the fastest connection between two link partners. For copper media applications, it was introduced in IEEE 802.3u for Ethernet and Fast Ethernet, and then in IEEE 802.3ab to address extended functions for Gigabit Ethernet. It performs the following:

- Auto-Negotiation Priority Resolution
- Auto-Negotiation Master/Slave Resolution
- Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution
- Crossover Detection & Auto-Correction Resolution

Upon de-assertion of a hardware reset, the RTL8211BG can be configured to have auto-negotiation enabled, or be forced to operate in 10Base-T, 100Base-TX, or 1000Base-T mode via the CONFIG[4:0] pins (see section 6.3 Hardware Configuration, page 8). If the RTL8211BG is configured to operate only in 1000Base-T mode, then auto-negotiation is still enabled with only 1000Base-T mode advertised.

The auto-negotiation process is initiated automatically upon any of the following:

- Power-up
- Hardware reset
- Software reset (register 0.15)
- Restart auto-negotiation (register 0.9)
- Transition from power down to power up (register 0.11)
- Entering the link fail state

Table 14. 1000Base-T Base and Next Pages Bit Assignments

Bit	Name	Bit Description	Register Location
Base Page			
D15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	-
D14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	-
D13	RF	Remote Fault. 1: Indicates to its link partner that a device has encountered a fault condition	-
D[12:5]	A[7:0]	Technology Ability Field. Indicates to its link partner the supported technologies specific to the selector field value.	Register 4.[12:5] Table 21, page 24.
D[4:0]	S[4:0]	Selector Field. Always 00001. Indicates to its link partner that it is an IEEE Std 802.3 device.	Register 4.[4:0] Table 21, page 24.
PAGE 0 (Message Next Page)			
M15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	-
M14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	-
M13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page.	-
M12	Ack2	Acknowledge 2. 1: Indicates to its link partner that a device has the ability to comply with the message.	-
M11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	-
M[10:0]	-	1000Base-T Message Code. Always 8.	-
PAGE 1 (Unformatted Next Page)			
U15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	-
U14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	-
U13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page.	-

Bit	Name	Bit Description	Register Location
U12	Ack2	Acknowledge 2. 1: Indicates to its link partner that a device has the ability to comply with the message.	-
U11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	-
U[10:5]	-	Reserved. Transmit as 0	-
U4	-	1000Base-T Half Duplex. 1: Half duplex 0: No half duplex	RGMII register 9.8 (GBCR) Table 26, page 27.
U3	-	1000Base-T Full Duplex. 1: Full duplex 0: No full duplex	RGMII register 9.9 (GBCR) Table 26, page 27.
U2	-	1000Base-T Port Type Bit. 1: Multi-port device 0: Single-port device	RGMII register 9.10 (GBCR) Table 26, page 27.
U1	-	1000Base-T Master-Slave Manual Configuration Value. 1: Master 0: Salve This bit is ignored if bit 9.12 = 0	RGMII register 9.11 (GBCR) Table 26, page 27.
U0	-	1000Base-T Master-Slave Manual Configuration Enable. 1: Manual Configuration Enable This bit is intended to be used for manual selection in Master-Slave mode, and is to be used in conjunction with bit 9.11	RGMII register 9.12 (GBCR) Table 26, page 27.
PAGE 2 (Unformatted Next Page)			
U15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	-
U14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	-
U13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page.	-
U12	Ack2	Acknowledge 2. 1: Indicates to its link partner that a device has the ability to comply with the message.	-
U11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	-
U[10:0]	-	1000Base-T Master-Slave Seed Bit[10:0]	Master-Slave Seed Value SB[10:0]

6.5.1. Auto-Negotiation Priority Resolution

Upon the start of auto-negotiation, to advertise its capabilities, each station transmits a 16-bit packet called a Link Code Word (LCW), within a burst of 17 to 33 Fast Link Pulses (FLP). A device capable of auto-negotiation transmits and receives the FLPs. The receiver must identify three identical LCWs before the information is authenticated and used in the arbitration process. The devices decode the base LCW and select capabilities with the highest common denominator supported by both devices.

To advertise 1000Base-T capability, both link partners, sharing the same link medium, should engage in Next Page (1000Base-T Message Page, Unformatted Page 1, and Unformatted Page 2) exchange.

Auto-negotiation ensures that the highest priority protocol will be selected as the link speed based on the following priority advertised through the Link Code Word (LCW) exchange. Refer to IEEE 802.3 Clause 28 for detailed information.

1.) 1000Base-T full duplex (highest priority)

2.) 1000Base-T half duplex

3.) 100Base-TX full duplex

4.) 100Base-TX half duplex

5.) 10Base-T full duplex

6.) 10Base-T half duplex (lowest priority)

6.5.2. Auto-Negotiation Master/Slave Resolution

To establish a valid 1000Base-T link, the Master/Slave mode of both link partners should be resolved through the auto-negotiation process:

- Master Priority:
  - Multi-port > Single port
  - Manual > Non-manual
- Determination of Master/Slave configuration from LCW:
  - Manual_MASTER = U0 * U1
  - Manual_SLAVE = U0 * !U1
  - Single-port device = !U0 * !U2
  - Multi-port device = !U0 * U2

  Where:

  U0 is bit 0 of the Unformatted Page 1
  U1 is bit 1 of the Unformatted Page 1
  U2 is bit 2 of the Unformatted Page 1

Where there are two stations with the same configuration, the one with higher Master-Slave seed SB[10:0] in the unformatted page 2 shall become Master.

- Master-Slave configuration process resolution:
  - Successful: Bit 10.15 Master-Slave Configuration Fault is set to logical 0, and bit 10.14 is set to logical 1 for Master resolution, or set to logical 0 for Slave resolution.
  - Unsuccessful: Auto-Negotiation restarts.
  - Fault detect: Bit 10.15 is set to logical 1 to indicate that a configuration fault has been detected. Auto-Negotiation restarts automatically. This happens when both stations are set to manual Master mode or manual Slave mode, or after seven attempts to configure the Master-Slave relationship through the seed method has failed.

6.5.3. Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution

Auto-negotiation is also used to determine the flow control capability between link partners. Flow control is a mechanism that can force a busy transmitting link partner to stop transmitting in a full duplex environment by sending special MAC control frames. In IEEE 802.3u, a PAUSE control frame had already been defined. However, in IEEE 802.3ab, a new ASY-PAUSE control frame was defined; if the MAC can only generate PAUSE frames but is not able to respond to PAUSE frames generated by the link partner, then it is called Asymmetric PAUSE.

PAUSE/ASYMMETRIC PAUSE capability can be configured by setting the ANAR bits 10 and 11 (Table 21). Link partner PAUSE capabilities can be determined from ANLPAR bits 10 and 11 (Table 22). A PHY layer device such as the RTL8211BG is not directly involved in PAUSE resolution, but simply advertises and reports PAUSE capabilities during the Auto-Negotiation process. The MAC is responsible for final PAUSE/ASYMMETRIC PAUSE resolution after a link is established, and is responsible for correct flow control actions thereafter.

6.6. Crossover Detection & Auto-Correction

Ethernet needs a crossover mechanism between both link partners to cross the transmit signal to the receiver when the medium is twisted-pair cable (e.g. CAT.3 or CAT.5 UTP). Crossover Detection & Auto-Correction Configuration eliminates the need for crossover cables between devices, such as two PC's connected to each other with a CAT.3 or CAT.5 Ethernet cable. The basic concept is to assume the initial default setting is MDI mode, and then check the link status. If no link is established after a certain time, change to MDI Crossover mode and repeat the process until a link is established. An 11-bit pseudo-random timer is applied to decide the mode change time interval.

Crossover Detection & Auto-Correction is not a part of the Auto-Negotiation process, but it utilizes the process to exchange the MDI/MDI Crossover configuration. If the RTL8211BG is configured to only operate in 100Base-TX or only in 10Base-T mode, then Auto-Negotiation is disabled only if the Crossover Detection & Auto-Correction function is also disabled. If Crossover Detection & Auto-Correction are enabled, then Auto-Negotiation is enabled and the RTL8211BG advertises only 100Base-TX mode or 10Base-T mode. If the speed of operation is configured manually and Auto-Negotiation is still enabled because the Crossover Detection & Auto-Correction function is enabled, then the duplex advertised is as follows:

1). If CONFIG is set to half duplex, then only half duplex is advertised.

2). If CONFIG is set to full duplex, then both full and half duplex are advertised.

If the user wishes to advertise only full duplex at a particular speed with the Crossover Detection & Auto-Correction function enabled, then Auto-Negotiation should be enabled (register 0.12) with the appropriate advertising capabilities set in registers 4 or 9. The Crossover Detection & Auto-Correction function may be enabled/disabled by setting (register 16.6) manually.

After initial configuration following a hardware reset, Auto-Negotiation can be enabled and disabled via register 0.12, speed via registers 0.13, 0.6, and duplex via register 0.8. The abilities that are advertised can be changed via registers 4 and 9. Changes to registers 0.12, 0.13, 0.6, and 0.8 do not take effect unless at least one of the following events occurs:

- Software reset (register 0.15)
- Restart of Auto-Negotiation (register 0.9)
- Transition from power-down to power-up (register 0.11)

Registers 4 and 9 are internally latched once each time Auto-Negotiation enters the ABILITY DETECT state in the arbitration state machine (IEEE 802.3). Hence a write into register 4 or 9 has no effect once the RTL8211BG begins to transmit Fast Link Pulses.

Register 7 is treated in a similar manner as 4 and 9 during additional Next Page exchanges. Once the RTL8211BG completes Auto-Negotiation, it updates the various statuses in registers 1, 5, 6, and 10. The speed, duplex, page received, and Auto-Negotiation completed statuses are also available in registers 17 and 19.

6.7. LED Configuration

The RTL8211BG supports six LED pins, suitable for multiple types of applications, that can directly drive the LEDs. These pins are LED10, LED100, LED1000, LEDDUP, LEDRX, and LEDTX. The output of these pins is determined by setting the corresponding bits in register 24. The functionality of the LED pins is shown in Table 15.

Table 15. LED Configuration

Pin	Register 24 Control Bit	Register 24 Control Bit = 0 (default)	Register 24 Control Bit = 1
LED_LINK10	24.3	Low = 10 Link Up High = 10 Link Down	LED10, LED100: Low, Low = 1000Mbps Low, High = 100Mbps High, Low = 10Mbps High, High = Link Down
LED_LINK100	24.3	Low = 100 Link Up High = 100 Link Down	
LED_LINK1000	24.3	Low = 1000 Link Up High = 1000 Link Down	Low = Link Up (Any speed) High = Link Down (Any speed)
LED_DUPLEX	24.2	Low = Full Duplex High = Half Duplex Blink = Collision	Low = Full Duplex High = Half Duplex
LED_RX	24.1	Low = Receiving High = Not Receiving	Low = Link Up High = Link Down Blinking = Receiving
LED_TX	24.1	Low = Transmitting High = Not Transmitting	Low = Link Up High = Link Down Blinking = Transmitting or Receiving

Some of the statuses can be pulse-stretched. Pulse-stretching is necessary because the duration of these status events may be too short to be observable on the LEDs. The pulse-stretch duration can be programmed via register 24.14:12. The default pulse-stretch duration is 42 to 84ms. The pulse-stretch duration applies to all applicable LEDs. Some of the statuses indicate multiple events by blinking LEDs. The blink period can be programmed via register 24.10:8. The default blink setting is ‘No blinking’. The blink rate applies to all applicable LEDs.

6.8. Polarity Correction

The RTL8211BG automatically corrects polarity errors on the receive pairs in 1000Base-T and 10Base-T modes. In 100Base-TX polarity is irrelevant. In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock. In 10Base-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

6.9. Power

The RTL8211BG implements two voltage regulators to generate operating power. The system vendor needs to supply a 3.3V, 1A steady power source. The RTL8211BG converts the 3.3V steady power source to 1.8V and 1.5V with two separate transistors. The transistor should have a beta value large enough to supply sufficient current for internal logic. A transistor with beta value larger than 100 is recommended.

Another implementation is using three regulators to generate 3.3V, 1.8V, and 1.5V. Note that the regulators need to meet the required rate current.

The RTL8211BG implements an option for the DVDD33 power pins. The I/O voltage of the GMII/RGMII interface=3.3V (2.5V tolerance).

7. Register Descriptions

7.1. Register Mapping and Definitions

Table 16. Register Mapping and Definitions

Offset	Access	Name	Description
0	RW	BMCR	Basic Mode Control Register.
1	RO	BMSR	Basic Mode Status Register.
2	RO	PHYID1	PHY Identifier Register 1.
3	RO	PHYID2	PHY Identifier Register 2.
4	RW	ANAR	Auto-Negotiation Advertising Register.
5	RW	ANLPAR	Auto-Negotiation Link Partner Ability Register.
6	RW	ANER	Auto-Negotiation Expansion Register.
7	RW	ANNPTR	Auto-Negotiation Next Page Transmit Register.
8	RW	ANNPRR	Auto-Negotiation Next Page Receive Register.
9	RW	GBCR	1000Base-T Control Register.
10	RO	GBSR	1000Base-T Status Register.
11-14	RO	Reserved	Reserved.
15	RO	GBESR	1000Base-T Extended Status Register.
16	RW	PHYCR	PHY Specific Control Register.
17	RO	PHYSR	PHY Specific Status Register.
18	RW	INER	Interrupt Enable Register.
19	RO	INSR	Interrupt Status Register.
20	RW	EPHYCR	Extended PHY specific Control Register.
21	RO	RXERC	Receive Error Counter.
24	RW	LEDCR	LED Control Register.
25-31	RO	Reserved	Reserved.

7.2. Register Descriptions

7.2.1. BMCR (Basic Mode Control Register, Address 0x00)

Table 17. BMCR (Basic Mode Control Register, Address 0x00)

Bit	Name	RW	Default	Description
0.15	Reset	RW, SC	0	Reset. 1: PHY reset 0: Normal operation
0.14	Loopback	RW	0	Loopback. 1: Enable loopback mode 0: Disable loopback mode The loopback function enables MII/RGMII transmit data to be routed to the MII/RGMII receive data path.
0.13	Speed[0]	RW	0	Speed Select bit 0. In forced mode, i.e. when Auto-Negotiation is disabled, bits 6 and 13 determine device speed selection.
0.12	ANE	RW	1	Auto-Negotiation Enable. 1: Enable Auto-Negotiation 0: Disable Auto-Negotiation
0.11	PWD	RW	0	Power Down. 1: Power down (only Management Interface and logic active, link is down) 0: Normal operation
0.10	Isolate	RW	0	Isolate. 1: MII interface is isolated; the serial management interface (MDC, MDIO) is still active. When this bit is asserted, the RTL8211BG ignores TXD[3:0], and TXCLT inputs, and presents a high impedance on TXC, RXC, RXCLT, RXD[3:0], COL and CRS outputs. 0: Normal operation
0.9	Restart_AN	RW, SC	0	Restart Auto-Negotiation. 1: Restart Auto-Negotiation 0: Normal operation
0.8	Duplex	RW	-	Duplex Mode. 1: Full Duplex operation 0: Half Duplex operation This bit is valid only in force mode, i.e., NWay is disabled.

Speed[1]	Speed[0]	Speed Enabled
1	1	Reserved
1	0	1000Mbps
0	1	100Mbps
0	0	10Mbps

Bit	Name	RW	Default	Description
0.7	Collision test	RW	0	Collision Test. 1: Collision test enabled 0: Normal operation When set, this bit will cause the COL signal to be asserted in response to the assertion of TXEN within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the de-assertion of TXEN.
0.6	Speed[1]	RW	0	Speed Select bit 1. Refer to bit 0.13.
0.5:0	RSVD	RO	000000	Reserved.

Note 1: The power-on duplex, speed, and ANE values take on the values set by external pins AN[3:0] on hardware reset only. A write to these registers has no effect unless any one of the following also occurs: Software reset (0.15) is asserted, Restart_AN (0.9) is asserted, or PWD (0.11) transitions from power down to normal operation.

Note 2: When the RTL8211BG is switched from power down to normal operation, software reset and restart auto-negotiation are performed even if bits Reset (0.15) and Restart_AN (0.9) are not set by the user.

Note 3: Auto-Negotiation is enabled when speed is set to 1000Base-T. Crossover Detection & Auto-Correction takes precedence over Auto-Negotiation disable (0.12=0). If ANE is disabled, speed and duplex capabilities are advertised by 0.13, 0.6, and 0.8. Otherwise, register 4.8:5 and 9.9:8 take effect.

Note 4: Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set.

7.2.2. BMSR (Basic Mode Status Register, Address 0x01)

Table 18. BMSR (Basic Mode Status Register) Address 0x01

Bit	Name	RW	Default	Description
1.15	100Base-T4	RO	0	100Base-T4 Capability. The RTL8211BG does not support 100Base-T4 mode. This bit should always be 0.
1.14	100Base-TX (full)	RO	1	100Base-TX Full Duplex Capability. 1: Device is able to perform 100Base-TX in full duplex mode 0: Device is not able to perform 100Base-TX in full duplex mode
1.13	100Base-TX (half)	RO	1	100Base-TX Half Duplex Capability. 1: Device is able to perform 100Base-TX in half duplex mode 0: Device is not able to perform 100Base-TX in half duplex mode
1.12	10Base-T (full)	RO	1	10Base-T Full Duplex Capability. 1: Device is able to perform 10Base-T in full duplex mode. 0: Device is not able to perform 10Base-T in full duplex mode.
1.11	10Base-T (half)	RO	1	10Base-T Half Duplex Capability. 1: Device is able to perform 10Base-T in half duplex mode 0: Device is not able to perform 10Base-T in half duplex mode
1.10	100Base-T2 (full)	RO	0	100Base-T2 Full Duplex Capability. The RTL8211BG does not support 100Base-T2 mode and this bit should always be 0.
1.9	100Base-T2 (half)	RO	0	100Base-T2 Half Duplex Capability. The RTL8211BG does not support 100Base-T2 mode. This bit should always be 0.

Bit	Name	RW	Default	Description
1.8	1000Base-T Extended status	RO	1	1000Base-T Extended Status Register. 1: Device supports Extended Status Register 0x0F (15) 0: Device does not support Extended Status Register 0x0F This register is read-only and is always set to 1.
1.7	RSVD	RO	0	Reserved.
1.6	Preamble Suppression	RO	1	Preamble Suppression Capability (permanently on). The RTL8211BG always accepts transactions with preamble suppressed.
1.5	Auto-Negotiation Complete	RO	0	Auto-Negotiation Complete. 1: Auto-Negotiation process complete, and contents of registers 5, 6, 8, and 10 are valid 0: Auto-Negotiation process not complete
1.4	Remote Fault	RO	0	Remote Fault. 1: Remote fault condition detected (cleared on read or by reset). Indication or notification of remote fault from Link Partner 0: No remote fault condition detected
1.3	Auto-Negotiation Ability	RO	1	Auto Configured Link. 1: Device is able to perform Auto-Negotiation 0: Device is not able to perform Auto-Negotiation
1.2	Link Status	RO	0	Link Status. 1: Linked 0: Not Linked This register indicates whether the link was lost since the last read. For the current link status, either read this register twice or read register bit 17.10 Link Real Time.
1.1	Jabber detect	RO	0	Jabber Detect. 1: Jabber condition detected 0: No Jabber occurred
1.0	Extended Capability	RO	1	1: Extended register capabilities, always 1

7.2.3. PHYID1 (PHY Identifier Register 1, Address 0x02)

Table 19. PHYID1 (PHY Identifier Register 1, Address 0x02)

Bit	Name	RW	Default	Description
2.15:0	OUI_MSB	RO	0000000000011100	Organizationally Unique Identifier (OUI) Bit 3:18. Always 0000000000011100.

Note: Realtek OUI is 0x000732.

7.2.4. PHYID2 (PHY Identifier Register 2, Address 0x03)

Table 20. PHYID2 (PHY Identifier Register 2, Address 0x03)

Bit	Name	RW	Default	Description
3.15:10	OUI_LSB	RO	110010	Organizationally Unique Identifier Bit 19:24. Always 110010.
3.9:4	Model Number	RO	010001	Always 010001.
3.3:0	Revision Number	RO	0010	-

7.2.5. ANAR (Auto-Negotiation Advertising Register, Address 0x04)

Table 21. ANAR (Auto-Negotiation Advertising Register, Address 0x04)

Bit	Name	RW	Default	Description
4.15	NextPage	RW	0	1: Additional next pages exchange desired 0: No additional next pages exchange desired
4.14	RSVD	RO	0	Reserved.
4.13	Remote Fault	RW	0	1: Set Remote Fault bit 0: No Remote Fault detected
4.12	RSVD	RO	0	Reserved.
4.11	Asymmetric PAUSE	RW	0	1: Advertise support of asymmetric pause 0: No support of asymmetric pause
4.10	PAUSE	RW	0	1: Advertise support for pause frames 0: No support for pause frames
4.9	100Base-T4	RO	0	0: Not capable of 100Base-T4
4.8	100Base-TX(full)	RW	1	1: Advertise support for 100Base-TX full-duplex mode 0: Not advertised
4.7	100Base-TX(half)	RW	1	1: Advertise support for 100Base-TX half-duplex mode 0: Not advertised
4.6	10Base-T(full)	RW	1	1: Advertise support for 10Base-TX full-duplex mode 0: Not advertised
4.5	10Base-T(half)	RW	1	1: Advertise support for 10Base-TX full-duplex mode 0: Not advertised
4.4:0	Selector field	RO	00001	Indicates the RTL8211BG supports IEEE 802.3

Note 1: The setting of Register 4 has no effect unless NWay is restarted or the link goes down.

Note 2: If 1000Base-T is advertised, then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed.

7.2.6. ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)

Table 22. ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)

Bit	Name	RW	Default	Description
5.15	Next Page	RO	0	Next Page Indication. Received Code Word Bit 15.
5.14	ACK	RO	0	Acknowledge. Received Code Word Bit 14.
5.13	Remote Fault	RO	0	Remote Fault Indicated by Link Partner. Received Code Word Bit 13.
5.12:5	Technology Ability Field	RO	00000000	Received Code Word Bit 12:5.
5.4:0	Selector Field	RO	00000	Received Code Word Bit 4:0.

Note: Register 5 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

7.2.7. ANER (Auto-Negotiation Expansion Register, Address 0x06)

Table 23. ANER (Auto-Negotiation Expansion Register, Address 0x06)

Bit	Name	RW	Default	Description
6.15:5	RSVD	RO	0x000	Reserved.
6.4	Parallel Detection Fault	RO	0	1: A fault has been detected via the Parallel Detection function 0: A fault has not been detected via the Parallel Detection function
6.3	Link Partner Next Pageable	RO	0	1: Link Partner supports Next Page exchange 0: Link Partner does not support Next Page exchange
6.2	Local Next Pageable	RO	1	1: Local Device is able to send Next Page Always 1.
6.1	Page Received	RO	0	1: A New Page (new LCW) has been received 0: A New Page has not been received
6.0	Link Partner Auto-Negotiation capable	RO	0	1: Link Partner supports Auto-Negotiation 0: Link Partner does not support Auto-Negotiation

Note: Register 6 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

7.2.8. ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)

Table 24. ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)

Bit	Name	RW	Default	Description
7.15	Next Page	RW	0	Next Page Indication. 0: No more next pages to send 1: More next pages to send Transmit Code Word Bit 15.
7.14	RSVD	RO	0	Transmit Code Word Bit 14.
7.13	Message Page	RW	1	Message Page. 0: Unformatted Page 1: Message Page Transmit Code Word Bit 13.
7.12	Acknowledge 2	RW	0	Acknowledge2. 0: Local device has no ability to comply with the message received 1: Local device has the ability to comply with the message received Transmit Code Word Bit 12.
7.11	Toggle	RO	0	Toggle Bit. Transmit Code Word Bit 11.
7.10:0	Message/ Unformatted Field	RW	0x001	Content of Message/Unformatted Page. Transmit Code Word Bit 10:0.

7.2.9. ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08)

Table 25. ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08)

Bit	Name	RW	Default	Description
8.15	Next Page	RO	0	Received Link Code Word Bit 15.
8.14	Acknowledge	RO	0	Received Link Code Word Bit 14.
8.13	Message Page	RO	0	Received Link Code Word Bit 13.
8.12	Acknowledge 2	RO	0	Received Link Code Word Bit 12.
8.11	Toggle	RO	0	Received Link Code Word Bit 11.
8.10:0	Message/ Unformatted Field	RO	0x00	Received Link Code Word Bit 10:0.

Note: Register 8 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

7.3. GBCR (1000Base-T Control Register, Address 0x09)

Table 26. GBCR (1000Base-T Control Register, Address 0x09)

Bit	Name	RW	Default	Description
9.15:13	Test Mode	RW	0	Test Mode Select. 000 = Normal Mode 001 = Test Mode 1 - Transmit Jitter Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 101, 110, 111 = Reserved
9.12	MASTER/SLAVE Manual Configuration Enable	RW	AN[3:0]	Enable Manual Master/Slave Configuration. 1: Manual MASTER/SLAVE configuration 0: Automatic MASTER/SLAVE
9.11	MASTER/SLAVE Configuration Value	RW	AN[3:0]	Advertise Master/Slave Configuration Value. 1: Manual configure as MASTER 0: Manual configure as SLAVE
9.10	Port Type	RW	AN[3:0]	Advertise Device Type Preference. 1: Prefer multi-port device (MASTER) 0: Prefer single port device (SLAVE)
9.9	1000Base-T Full Duplex	RW	AN[3:0]	Advertise 1000Base-T Full-Duplex Capability. 1: Advertise 0: Do not advertise
9.8	1000Base-T Half Duplex	RW	AN[3:0]	Advertise 1000Base-T Half-Duplex Capability. 1: Advertise 0: Do not advertise
9.7:0	RSVD	RW	0	Reserved.

Note 1: Values set in register 9.12:8 have no effect unless Auto-Negotiation is restarted (Reg0.9) or the link goes down.
Note 2: Bits 9.11 and 9.10 are ignored when bit 9.12 = 0.

7.3.1. GBSR (1000Base-T Status Register, Address 0x0A)

Table 27. GBSR (1000Base-T Status Register, Address 0x0A)

Bit	Name	RW	Default	Description
10.15	MASTER/SLAVE Configuration Fault	RO, SC	0	Master/Slave Manual Configuration Fault Detected. 1: MASTER/SLAVE configuration fault detected 0: No MASTER/SLAVE configuration fault detected
10.14	MASTER/SLAVE Configuration Resolution	RO	0	Master/Slave Configuration Result. 1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE
10.13	Local Receiver Status	RO	0	Local Receiver Status. 1: Local Receiver OK 0: Local Receiver Not OK
10.12	Remote Receiver Status	RO	0	Remote Receiver Status. 1: Remote Receiver OK 0: Remote Receiver Not OK

Bit	Name	RW	Default	Description
10.11	Link Partner 1000Base-T Full Duplex Capability	RO	0	Link Partner 1000Base-T Full Duplex Capability. 1: Link Partner is capable of 1000Base-T full duplex 0: Link Partner is not capable of 1000Base-T full duplex
10.10	Link Partner 1000Base-T Half Duplex Capability	RO	0	Link Partner 1000Base-T Half Duplex Capability. 1: Link Partner is capable of 1000Base-T half duplex 0: Link Partner is not capable of 1000Base-T half duplex
10.9:8	RSVD	RO	00	Reserved.
10.7:0	Idle Error Count	RO, SC	0x00	MSB of Idle Error Counter. The counter stops automatically when it reaches 0xff.

Note 1: Values set in register 10.11:10 are not valid until register 6.1 is set to 1.

Note 2: SC: Self-cleared after read.

Note 3: Register 10 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

7.3.2. GBESR (1000Base-T Extended Status Register, Address 0x0F)

Table 28. GBESR (1000Base-T Extended Status Register, Address 0x0F)

Bit	Name	RW	Default	Description
15.15	1000Base-X FD	RO	0	0: Not 1000Base-X full duplex capable
15.14	1000Base-X HD	RO	0	0: Not 1000Base-X half duplex capable
15.13	1000Base-T FD	RO	1	1: 1000Base-T full duplex capable
15.12	1000Base-T HD	RO	1	1: 1000Base-T half duplex capable
15.11:0	RSVD	RO	0x000	Reserved.

7.3.3. PHYCR (PHY Specific Control Register, Address 0x10)

Table 29. PHYCR (PHY Specific Control Register, Address 0x10)

Bit	Name	RW	Default	Description
16.15:12	RSVD	RW	0000	Reserved.
16.11	Assert CRS on Transmit	RW	0	1: Assert CRS on transmit 0: Never assert CRS on transmit
16.10	Force Link Good	RW	0	1: Force link good 0: Normal operation
16.9:7	RSVD	RW	000	Reserved.
16.6:5	MDI Crossover Mode	RW	10	00 = Manual MDI configuration 01 = Manual MDI Crossover configuration 10 = Enable Crossover Detection & Auto-Correction for all modes 11 = Enable Crossover Detection & Auto-Correction for all modes *Note: After setting the register, a PHY reset is required.*
16.4	Disable CLK125	RW	0	1: CLK125 remains at logic high 0: CLK125 toggling
16.3:1	RSVD	RW	000	Reserved.
16.0	Disable Jabber	RW	0	1: Disable jabber function 0: Enable jabber function

7.3.4. PHYSR (PHY Specific Status Register, Address 0x11)

Table 30. PHYSR (PHY Specific Status Register, Address 0x11)

Bit	Name	RW	Default	Description
17.15:14	Speed	RO	00	Link Speed. 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps
17.13	Duplex	RO	0	Full/Half Duplex Mode. 1: Full duplex 0: Half duplex
17.12	Page Received	RO	0	New Page Received. 1: Page received 0: Page not received
17.11	Speed And Duplex Resolved	RO	0	Speed and Duplex Mode Resolved. 1: Resolved 0: Not resolved
17.10	Link (Real-Time)	RO	0	Real-Time Link Status. 1: Link OK 0: Link not OK
17.9:7	Reserved	RO	000	Reserved.
17.6	MDI Crossover Status	RO	0	MDI/MDI Crossover Status. 1: MDI Crossover 0: MDI
17.5:1	RSVD	RO	00000	Reserved
17.0	Jabber (Real-Time)	RO	0	Real-Time Jabber Indication. 1: Jabber Indication 0: No jabber Indication

7.3.5. INER (Interrupt Enable Register, Address 0x12)

Table 31. INER (Interrupt Enable Register, Address 0x12)

Bit	Name	RW	Default	Description
18.15	Auto-Negotiation Error Interrupt	RW	0	1: Interrupt enable 0: Interrupt disable
18.14	Speed Change Interrupt	RW	0	1: Interrupt enable 0: Interrupt disable
18.13	Duplex Mode Change Interrupt	RW	0	1: Interrupt enable 0: Interrupt disable
18.12	Page Received Interrupt	RW	0	1: Interrupt enable 0: Interrupt disable
18.11	Auto-Negotiation Completed Interrupt	RW	0	1: Interrupt enable 0: Interrupt disable
18.10	Link Status Change Interrupt	RW	0	1: Interrupt enable 0: Interrupt disable
18.9	Symbol Error Interrupt	RW	0	1: Interrupt enable 0: Interrupt disable
18.8	False Carrier Interrupt	RW	0	1: Interrupt enable 0: Interrupt disable
18.7	Reserved	RW	0	Reserved.
18.6	MDI Crossover Change Interrupt	RW	0	1: Interrupt enable 0: Interrupt disable
18.5:2	Reserved	RW	0	Reserved.
18.1	Polarity Change Interrupt	RW	0	1: Interrupt enable 0: Interrupt disable
18.0	Jabber Interrupt	RW	0	1: Interrupt enable 0: Interrupt disable

7.3.6. INSR (Interrupt Status Register, Address 0x13)

Table 32. INSR (Interrupt Status Register, Address 0x13)

Bit	Name	RW	Default	Description
19.15	Auto-Negotiation Error	RO	0	1: Auto-Negotiation Error 0: No Auto-Negotiation Error
19.14	Speed Change	RO	0	1: Link speed changed 0: Link speed not changed
19.13	Duplex Mode Change	RO	0	1: Duplex mode changed 0: Duplex mode not changed
19.12	Page Received	RO	0	1: Page (a new LCW) received 0: Page not received
19.11	Auto-Negotiation Completed	RO	0	1: Auto-Negotiation completed 0: Auto-Negotiation not completed
19.10	Link Status Change	RO	0	1: Link status changed 0: Link status not changed
19.9	Symbol Error	RO	0	1: Symbol error detected 0: No symbol error detected
19.8	False Carrier	RO	0	1: False carrier 0: No false carrier detected
19.7	RSVD	RO	0	Reserved.
19.6	MDI Crossover Change	RO	0	1: Crossover status changed 0: Crossover status not changed
19.5:2	RSVD	RO	0000	Reserved.
19.1	Polarity Change	RO	0	1: Polarity Changed 0: Polarity not changed *Note: This bit is valid only when 1000Base-T is enabled.*
19.0	Jabber	RO	0	1: Jabber detected 0: No jabber detected

7.3.7. EPHYCR (Extended PHY Specific Control Register, Address 0x14)

Table 33. EPHYCR (Extended PHY Specific Control Register, Address 0x14)

Bit	Name	RW	Default	Description
20.15:7	Reserved	RW	0 0000 0000	Reserved.
20.6:4	TXC Speed	RW	100	TXC Speed. 0xx = 0MHz 10x = 125MHz 110 = 2.5MHz 111 = 25MHz
20.3:0	Reserved	RW	000	Reserved.

Note: Bits 20.6:4 specify TXC speed.

7.3.8. RXERC (Receive Error Counter, Address 0x15)

Table 34. RXERC (Receive Error Counter, Address 0x15)

Bit	Name	RW	Default	Description
21.15:0	Receive Error Count	RO	0x0000	Receive Error Count.

Note: The RXERC register is self-cleared after a read.

7.3.9. LEDCR (LED Control Register, Address 0x18)

Table 35. LEDCR (LED Control Register, Address 0x18)

Bit	Name	RW	Default	Description
24.15	Disable LED	RW	0	0: Enable 1: Disable
24.14:12	LED Pulse Stretch Duration	RW	010	000 = No pulse stretching 001 = 21ms to 42ms 010 = 42ms to 84ms 011 = 84ms to 170ms 100 = 170ms to 340ms 101 = 340ms to 670ms 110 = 670ms to 1.3s 111 = 1.3s to 2.7s
24.11	RSVD	RW	0	Reserved.
24.10:8	LED Blink Rate	RW	111	000 = 42ms 001 = 84ms 010 = 170ms 011 = 340ms 100 = 670ms 101 = 21ms 110 = 10ms 111 = No blinking
24.7:4	RSVD	RW	0100	Reserved.
24.3	LEDLINK Control	RW	0	1: Link and Speed Indication by combination of LEDs 0: Link and Speed Indication by specific LED Refer to section 6.7 LED Configuration, page 18.
24.2	LEDDUP Control	RW	0	1: Full Duplex Indication 0: Full Duplex/Collision Indication
24.1	LEDRX Control	RW	0	1: Rx Activity/Link Indication 0: Rx Activity Indication only
24.0	LEDTX Control	RW	0	1: Tx or Rx Activity/Link Indication 0: Tx Activity Indication only

8. Application Diagram

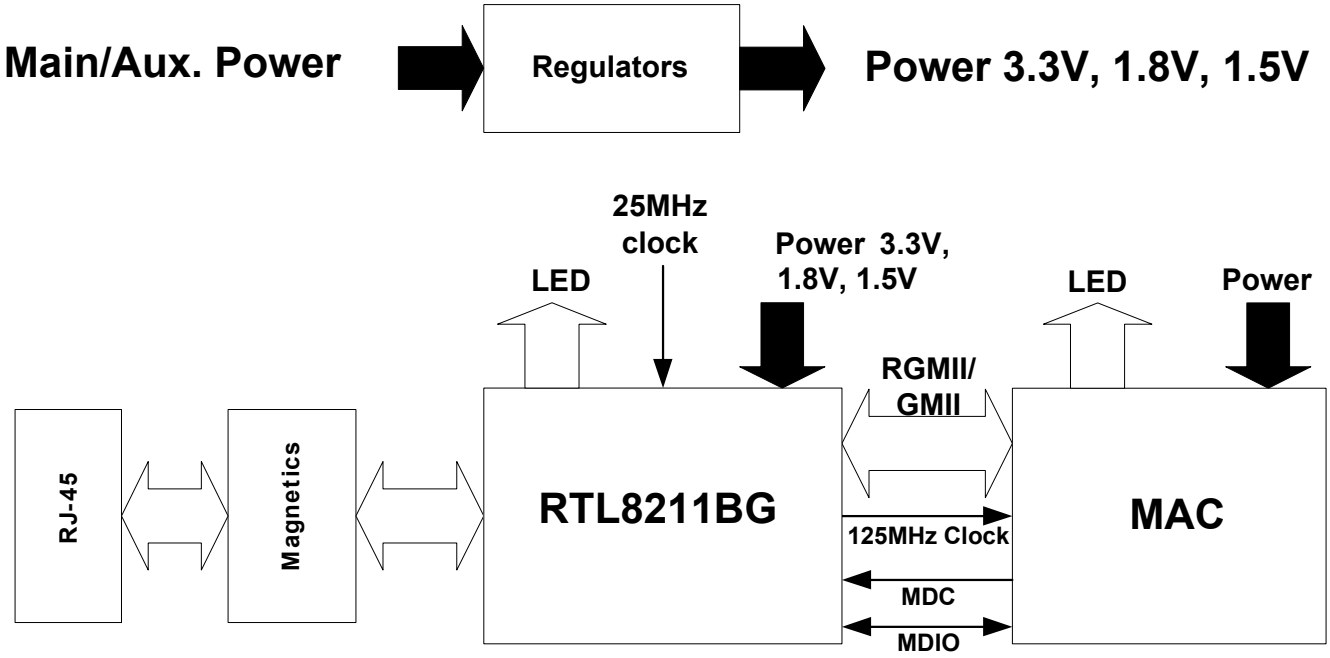


Figure 4. Application Diagram

9. Characteristics

9.1. Absolute Maximum Ratings

Table 36. Absolute Maximum Ratings

Description/Symbol	Minimum	Maximum	Unit
Supply Voltage (DVDD33, AVDD33)	-0.5	4	V
Supply Voltage (AVDD18)	-0.5	2.5	V
Supply Voltage (AVDD15, DVDD15)	-0.5	2	V
Input Voltage (DC input)	-0.5	AVDD33 + 0.5	V
Output Voltage (DC output)	-0.5	AVDD33 + 0.5	V
Storage Temperature	-55	+125	°C

9.2. Recommended Operating Conditions

Table 37. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	DVDD33, AVDD33	3.14	3.3	3.46	V
	AVDD18	1.68	1.8	2.13	V
	AVDD15, DVDD15	1.33	1.5	1.68	V
Ambient Operating Temperature T_A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

9.3. Crystal Requirements

Table 38. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F_{ref} Stability	Parallel Resonant Crystal Frequency Stability, Fundamental Mode, AT-Cut Type. T_a=25°C.	-50	-	+50	ppm
F_{ref} Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=-20°C ~+70°C.	-30	-	+30	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
DL	Drive Level.	-	-	0.5	mW

9.4. DC Characteristics

Table 39. DC Characteristics

Symbol	Description	Pins	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage	I	-	0.5 * VDD	-	-	V
V_{IL}	Input Low Voltage	I	-	-	-	0.3 * VDD	V
V_{OH}	Output High Voltage	O, I/O	VDD=Min, I_{OH} = -8mA	0.9 * VDD	-	-	V
V_{OL}	Output Low Voltage	O, I/O	VDD=Min, I_{OL} = 8mA	-	-	0.1 * VDD	V
I_{IH}	Input High Current	I, I/O	V_{IN}=VDD, VDD=VDD(max)	-	-	1	µA
I_{IL}	Input Low Current	I, I/O	V_{IN}=GND, VDD=VDD(max)	-1	-	-	µA
I_{OZ}	Tri-State Output Leakage Current	I/O	V_{OUT}=VDD	-	-	10	µA
I_{OZ}	Tri-State Output Leakage Current	I/O	V_{OUT}=GND	-10	-	-	µA

9.5. AC Characteristics

9.5.1. MII Timing

MII Timing – MII PORT – Transmit

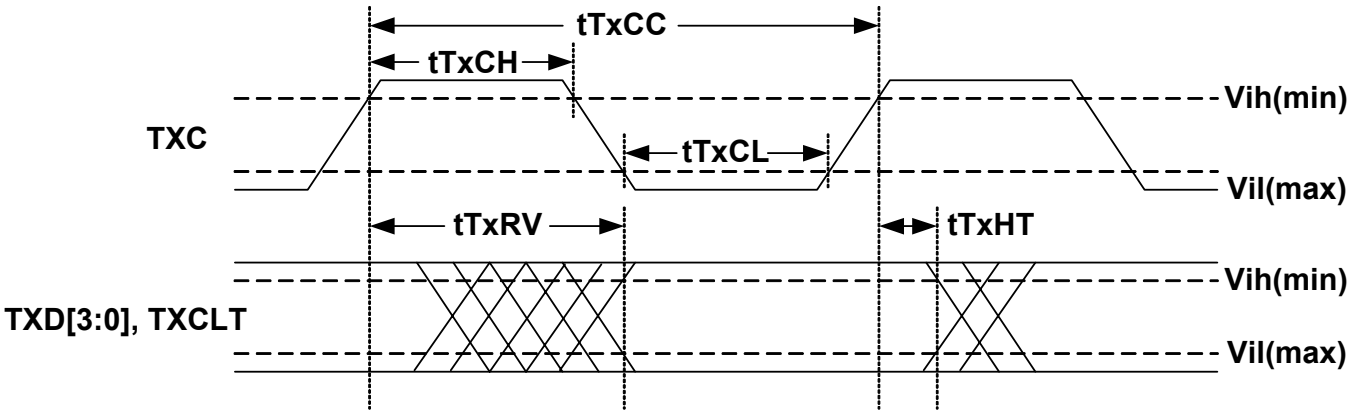


Figure 5. MII Timing – MII PORT – Transmit

Table 40. MII Transmit Timing Parameters

		10MHz			100MHz			
Symbol	**Description**	**Min**	**Typical**	**Max**	**Min**	**Typical**	**Max**	**Units**
tTxCC	Tx Clock Cycle	-	400	-	-	40	-	ns
tTxCH	Tx Clock High Time	140	-	260	14	-	26	ns
tTxCL	Tx Clock Low Time	140	-	260	14	-	26	ns
tTxRV	Tx Clock Rise to TxD, TXCLT Valid	-	-	20	-	-	20	ns
tTxHT	TxD, TXCLT Hold Time	5	-	-	5	-	-	ns

MII Timing – MII PORT – Receive

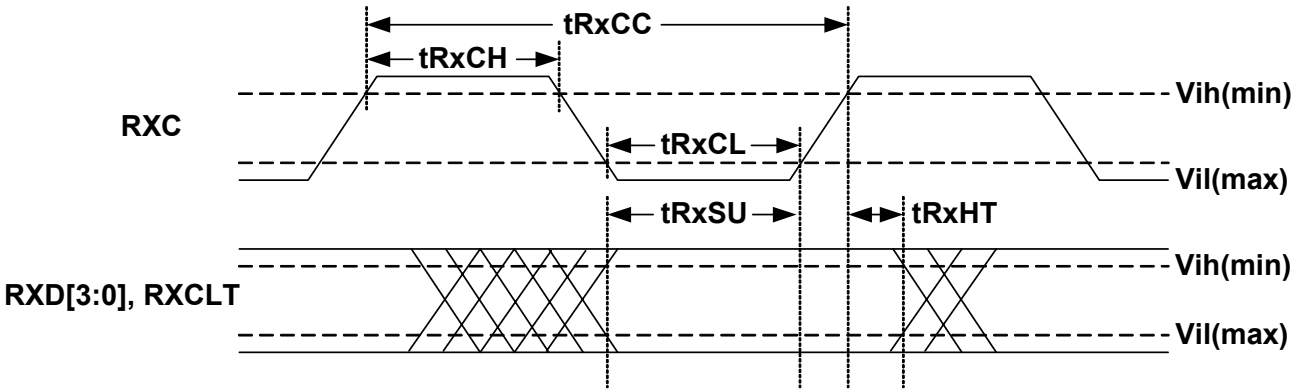


Figure 6. MII Timing – MII PORT – Receive

Table 41. MII Receive Timing Parameters

		10MHz			100MHz			
Symbol	**Description**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
tRxCC	Rx Clock Cycle.	-	400	-	-	40	-	ns
tRxCH	Rx Clock High Time.	140	-	260	14	-	26	ns
tRxCL	Rx Clock Low Time.	140	-	260	14	-	26	ns
tRxSU	RxD, RXCLT Setup Time.	10	-	20	10	-	20	ns
tRxHT	RxD, RXCLT Hold Time.	5	-	-	5	-	-	ns

MII Timing – MII Management Port

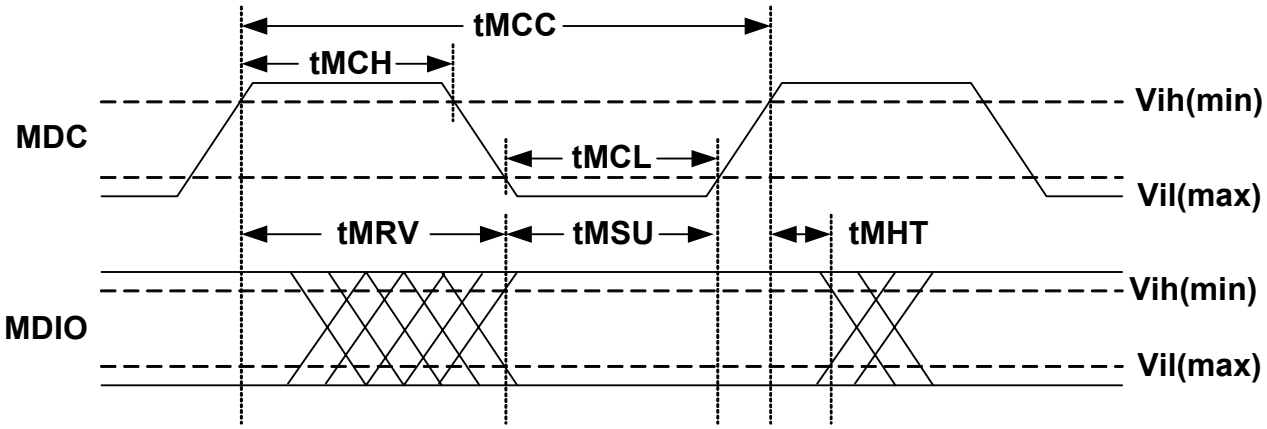


Figure 7. MII Management Timing Parameters

Table 42. MII Management Timing Parameters

Symbol	Description	Min	Max	Units
tMCC	MDC Cycle Time.	80	-	ns
tMCH	MDC High Time.	30	-	ns
tMCL	MDC Low Time.	30	-	ns
tMSU	MDIO Setup Time.	10	-	ns
tMHT	MDIO Hold Time.	10	-	ns
tMRV	MDC Clock Rise to MDIO valid.	-	40	ns

9.5.2. RGMII Timing Modes

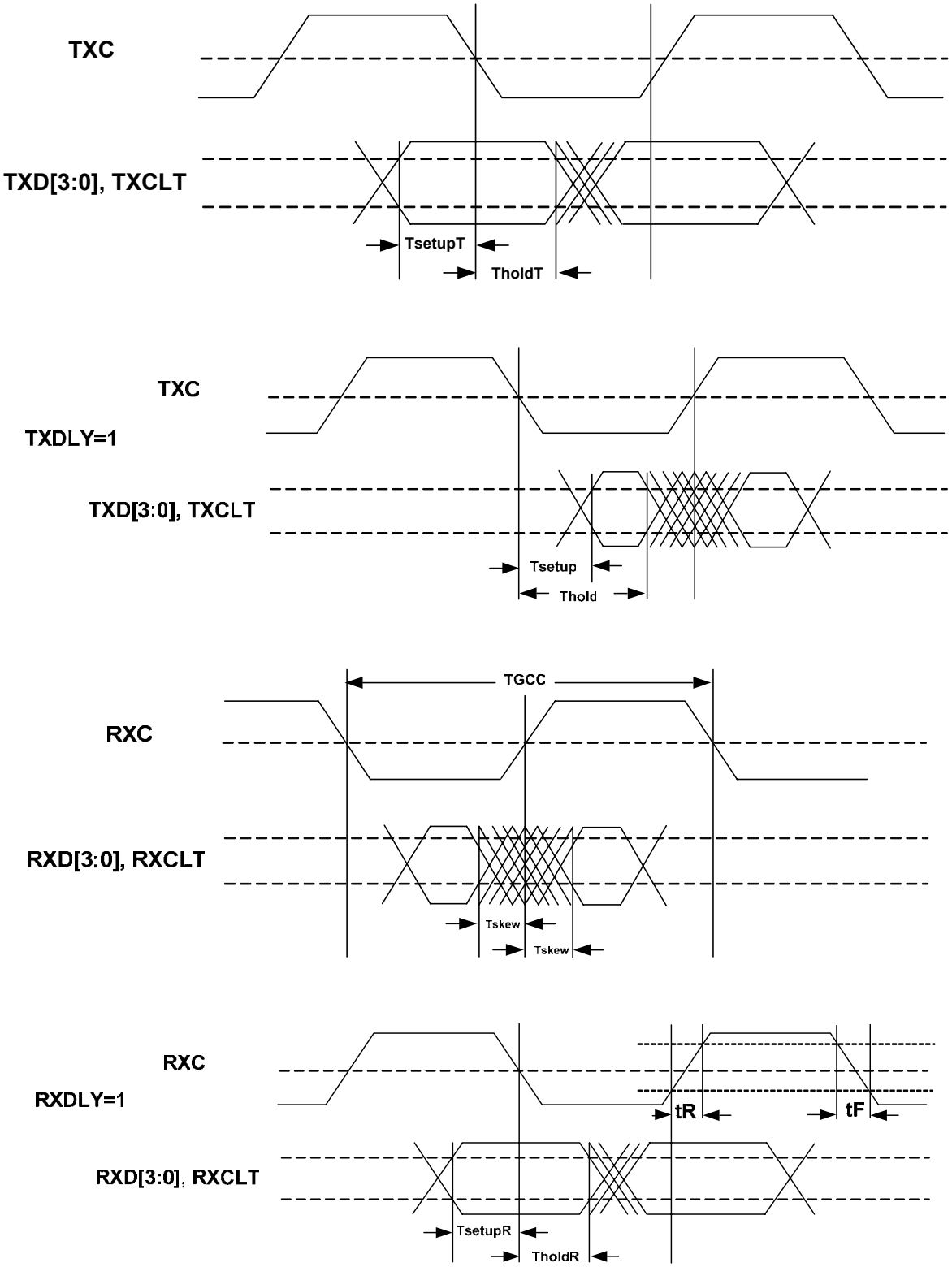


Figure 8. RGMII Timing Modes

Table 43. RGMII Timing Parameters

Symbol	Description	Min	Typical	Max	Units
TXC/RXC	TXC, RXC Frequency.	125 - 100ppm	125	125 + 100ppm	MHz
tGCC	TXC, RXC Cycle Time.	-	8	-	ns
tR	RXC Rise Time.	-	-	1	ns
tF	RXC Fall Time.	-	-	1	ns
TsetupT	TxD, TXCLT Setup to TXC.	1	2	-	ns
TholdT	TxD, TXCLT Hold from TXC.	0.8	2	-	ns
Tsetup	TXDLY=1; TxD, TXCLT Setup to TXC.	-0.9	-	-	ns
Thold	TXDLY=1; TxD, TXCLT Hold from TXC.	2.7	-	-	ns
Tskew	Data to Clock Output Skew	-0.5	0	0.5	ns
TsetupR	RXDLY=1; RxD, RXCLT Setup to RXC.	1.2	2	-	ns
TholdR	RXDLY=1; RxD, RXCLT Hold from RXC.	1	2	-	ns

9.5.3. GMII Timing

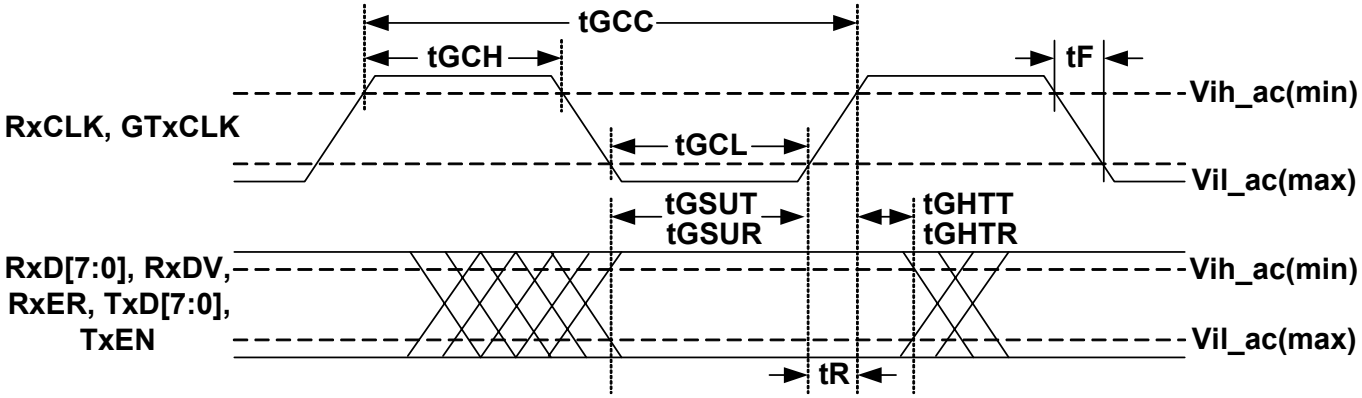


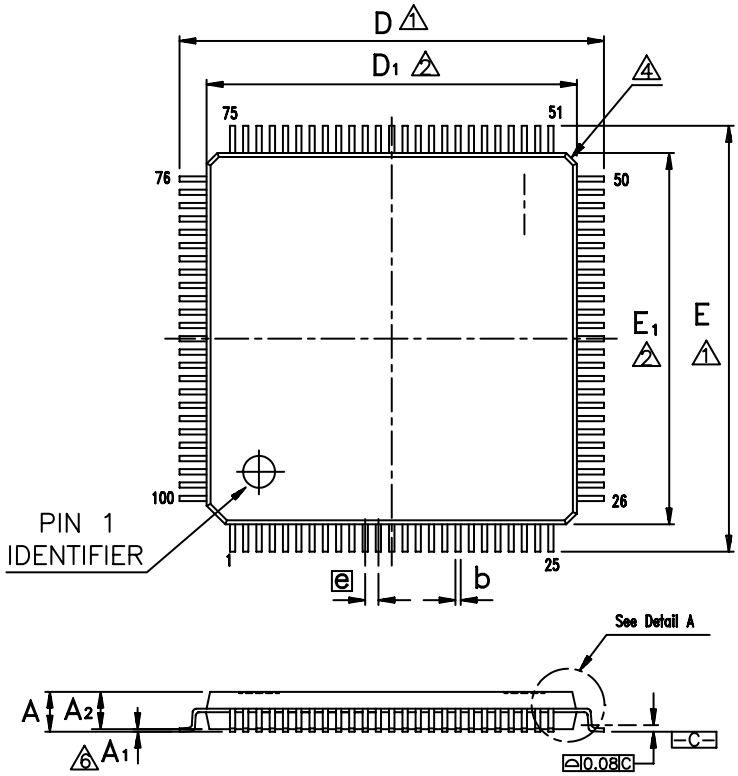
Figure 9. GMII Timing

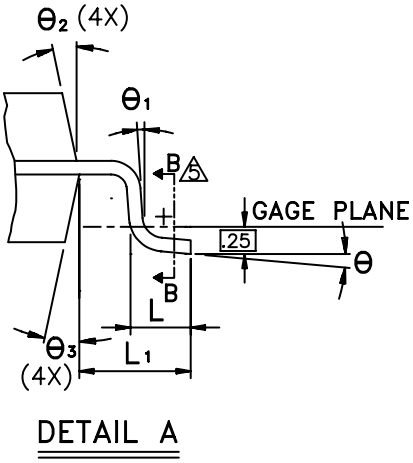
Table 44. GMII Timing Parameters

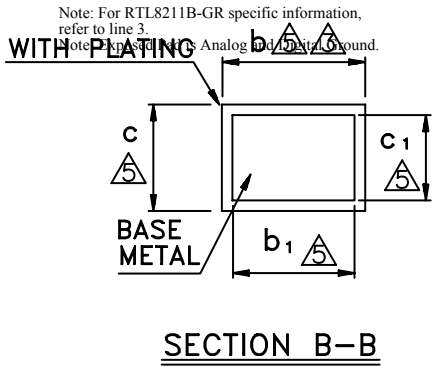
Symbol	Description	Min	Typical	Max	Units
Vil_ac	Input Low Voltage AC.	-	-	0.7	V
Vih_ac	Input High Voltage AC.	1.9	-	-	V
fGTxCLK, fRxCLK	GTxCLK, RxCLK Frequency.	125 - 100ppm	125	125 + 100ppm	MHz
tGCC	GTxCLK, RxCLK Cycle Time.	7.5	8	8.5	ns
tGCH	GTxCLK, RxCLK High Time.	2.5	-	-	ns
tGCL	GTxCLK, RxCLK Low Time.	2.5	-	-	ns
tR	GTxCLK, RxCLK Rise Time.	-	-	1	ns
tF	GTxCLK, RxCLK Fall Time.	-	-	1	ns
RSR	GTxCLK, RxCLK Rising Slew Rate.	0.6	-	-	V/ns
FSR	GTxCLK, RxCLK Falling Slew Rate.	0.6	-	-	V/ns
tGSUT	TxD, TxEN Setup to ↑ of GTxCLK.	2.5	-	-	ns
tGHTT	TxD, TxEN Hold from ↑ of GTxCLK.	0.5	-	-	ns
tGSUR	RxD, RxDV, RxER Setup to ↑ of RxCLK.	2	-	-	ns
tGHTR	RxD, RxDV, RxER Hold from ↑ of RxCLK.	0	-	-	ns

10. Mechanical Dimensions

10.1. 100-Pin LQFP Mechanical Dimensions







10.2. Mechanical Dimensions Notes

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.067	-	-	1.70
A1	0.000	0.004	0.008	0.00	**0.1**	0.20
A2	0.051	0.055	0.059	1.30	**1.40**	1.50
B	0.006	0.009	0.011	0.15	**0.22**	0.29
b1	0.006	0.008	0.010	0.15	**0.20**	0.25
C	0.004	-	0.008	0.09	-	0.20
c1	0.004	-	0.006	0.09	-	0.16
D	0.630 BSC			16.00 BSC		
D1	0.551 BSC			14.00 BSC		
E	0.630 BSC			16.00 BSC		
E1	0.551 BSC			14.00 BSC		
e	0.020 BSC			0.50 BSC		
L	0.016	0.024	0.031	0.40	0.60	0.80
L1	0.039 REF			1.00 REF		
θ	0°	3.5°	9°	0°	3.5°	9°
θ1	0°	-	-	0°	-	-
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

Notes:

1.To be determined at seating plane -c-

2.Dimensions D1 and E1 do not include mold protrusion. D1 and E1 dimensions are maximum plastic body size dimensions, including m

3.Dimension b does not include dambar protrusion.
Dambar can not be located on the lower radius of the foot.

4.Exact shape of each corner is optional.

5.These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

6. A1 is defined as the distance from the seating plane to the lowest point of the package body.

7.Controlling dimension: millimeter.

8. Reference document: JEDEC MS-026 , BED.

TITLE: 100LD LQFP (14x14x1.4mm) PACKAGE OUTLINE DRAWING , FOOTPRINT 2.0mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	LQ100 - P1
		DATE	
REALTEK SEMICONDUCTOR CORP.			

11. Ordering Information

Table 45. Ordering Information

Part Number	Package	Status
RTL8211BG-GR	100-Pin LQFP with Green Package	Production

Note: See page 2 for package identification.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com.tw