

REALTEK

NOT FOR PUBLIC RELEASE

**RTL8211D-VB-GR
RTL8211DG-VB-GR
RTL8211DN-VB-GR**

INTEGRATED 10/100/1000MBPS ETHERNET TRANSCEIVER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

**Rev. 1.2
13 August 2010
Track ID: JATR-2265-11**



Realtek Semiconductor Corp.

No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan

Tel.: +886-3-578-0211 Fax: +886-3-577-6047

www.realtek.com

COPYRIGHT

©2010 Realtek Semiconductor Corp. All rights reserved. No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language in any form or by any means without the written permission of Realtek Semiconductor Corp.

DISCLAIMER

Realtek provides this document “as is”, without warranty of any kind. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

LICENSE

This product is covered by one or more of the following patents: US5,307,459, US5,434,872, US5,732,094, US6,570,884, US6,115,776, and US6,327,625.

USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2010/04/28	First release.
1.1	2010/08/09	Revised IEEE 802.3az to Draft 3.2. Added section 3.7 UTP/Fiber Auto-Detection to GMII/RGMII Application Diagram (RTL8211DN), page 5. Revised Table 15 MII/MDI Interface Configuration, page 19. Added section 6.9 Green Ethernet (Gigabit Mode Only), page 20. Added section 6.10.6 Access to Extension Page (ExtPage), page 22. Added section 6.10.7 Access to MDIO Manageable Device (MMD), page 22. Revised Table 21 Page0 Register Mapping and Definitions, page 32. Added section 7.3 MMD Register Mapping and Definition, page 33. Added Table 35 MACR (MMD Access Control Register, Address 0x0D), page 40. Added Table 36 MAADR (MMD Access Address Data Register, Address 0x0E), page 41. Added Table 45, page 44 to Table 50, page 45. Revised section 9.6.4 RGMII Timing Modes, page 61.
1.2	2010/08/13	Revised section 9.6.2 MII Timing Modes, page 58. Revised section 9.6.5 SGMII Timing Modes, page 64.

Table of Contents

1. GENERAL DESCRIPTION	1
2. FEATURES	2
3. SYSTEM APPLICATIONS	3
3.1. APPLICATION DIAGRAM (RTL8211D).....	3
3.2. APPLICATION DIAGRAM (RTL8211DG).....	3
3.3. FIBER APPLICATION DIAGRAM (RTL8211DN).....	4
3.4. UTP APPLICATION DIAGRAM (RTL8211DN).....	4
3.5. FIBER TO UTP (BRIDGE MODE) APPLICATION DIAGRAM (RTL8211DN).....	4
3.6. SGMII TO GMII/RGMII (BRIDGE MODE) APPLICATION DIAGRAM (RTL8211DN).....	5
3.7. UTP/FIBER AUTO-DETECTION TO GMII/RGMII APPLICATION DIAGRAM (RTL8211DN).....	5
4. PIN ASSIGNMENTS	6
4.1. RTL8211D PIN ASSIGNMENTS (48-PIN QFN)	6
4.2. PACKAGE IDENTIFICATION	6
4.3. RTL8211DG PIN ASSIGNMENTS (64-PIN QFN)	7
4.4. PACKAGE IDENTIFICATION	7
4.5. RTL8211DN PIN ASSIGNMENTS (88-PIN QFN)	8
4.6. PACKAGE IDENTIFICATION	8
5. PIN DESCRIPTIONS	9
5.1. TRANSCEIVER INTERFACE.....	9
5.2. CLOCK	9
5.3. GMII/MII (RTL8211DN AND RTL8211DG ONLY).....	10
5.4. RGMII	11
5.5. SGMII (RTL8211DN ONLY)	12
5.6. MANAGEMENT INTERFACE.....	12
5.7. RESET	13
5.8. MODE SELECTION	13
5.9. LED INDICATION	13
5.10. REGULATOR AND REFERENCE.....	14
5.11. POWER AND GROUND	14
5.12. NOT CONNECTED	14
6. FUNCTION DESCRIPTION	15
6.1. 1000BASE-T TRANSMITTER.....	15
6.2. 1000BASE-T RECEIVER	15
6.3. ENERGY EFFICIENT ETHERNET (EEE).....	15
6.4. WAKE-ON-LAN (WOL).....	16
6.5. MDI INTERFACE	16
6.6. SERDES (SGMII) INTERFACE (RTL8211DN ONLY).....	17
6.7. HARDWARE CONFIGURATION	17
6.8. LED AND PHY ADDRESS CONFIGURATION	19
6.9. GREEN ETHERNET (GIGABIT MODE ONLY).....	20
6.9.1. Cable Length Power Saving.....	20
6.9.2. Register Setting.....	20
6.10. MAC/PHY INTERFACE	20
6.10.1. MII.....	20
6.10.2. GMII.....	21
6.10.3. RGMII.....	21

6.10.4.	SGMII	21
6.10.5.	Management Interface.....	21
6.10.6.	Access to Extension Page (ExtPage).....	22
6.10.7.	Access to MDIO Manageable Device (MMD).....	22
6.11.	AUTO-NEGOTIATION.....	23
6.11.1.	Auto-Negotiation Priority Resolution.....	26
6.11.2.	Auto-Negotiation Master/Slave Resolution	26
6.11.3.	Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution.....	27
6.12.	CROSSOVER DETECTION AND AUTO-CORRECTION	28
6.13.	LED CONFIGURATION.....	29
6.14.	POLARITY CORRECTION	31
6.15.	POWER.....	31
7.	REGISTER DESCRIPTIONS.....	32
7.1.	PAGE0 REGISTER MAPPING AND DEFINITIONS.....	32
7.2.	EXTENSION PAGE REGISTER MAPPING AND DEFINITION.....	32
7.3.	MMD REGISTER MAPPING AND DEFINITION.....	33
7.4.	REGISTER TABLE	33
7.4.1.	BMCR (Basic Mode Control Register, Address 0x00)	33
7.4.2.	BMSR (Basic Mode Status Register, Address 0x01).....	35
7.4.3.	PHYID1 (PHY Identifier Register 1, Address 0x02)	36
7.4.4.	PHYID2 (PHY Identifier Register 2, Address 0x03)	36
7.4.5.	ANAR (Auto-Negotiation Advertising Register, Address 0x04)	37
7.4.6.	ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)	37
7.4.7.	ANER (Auto-Negotiation Expansion Register, Address 0x06).....	38
7.4.8.	ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)	38
7.4.9.	ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08).....	39
7.4.10.	GBCR (1000Base-T Control Register, Address 0x09).....	39
7.4.11.	GBSR (1000Base-T Status Register, Address 0x0A)	40
7.4.12.	MACR (MMD Access Control Register, Address 0x0D)	40
7.4.13.	MAADR (MMD Access Address Data Register, Address 0x0E).....	41
7.4.14.	GBESR (1000Base-T Extended Status Register, Address 0x0F)	41
7.4.15.	PHYCR (PHY Specific Control Register, Address 0x10).....	41
7.4.16.	PHYSR (PHY Specific Status Register, Address 0x11).....	42
7.4.17.	INER (Interrupt Enable Register, Address 0x12)	42
7.4.18.	INSR (Interrupt Status Register, Address 0x13)	43
7.4.19.	RXERC (Receive Error Counter, Address 0x18).....	43
7.4.20.	PAGSEL (Page Select Register, Address 0x1F)	43
7.4.21.	SDSR (SerDes Register, ExtPage 140, Address 0x16)	44
7.4.22.	PC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)	44
7.4.23.	PS1R (PCS Status 1 Register, MMD Device 3, Address 0x01)	44
7.4.24.	EEECR (EEE Capability Register, MMD Device 3, Address 0x14).....	44
7.4.25.	EEEWER (EEE Wake Error Register, MMD Device 3, Address 0x16)	45
7.4.26.	EEEAR (EEE Advertisement Register, MMD Device 7, Address 0x3c)	45
7.4.27.	EEELPAR (EEE Link Partner Ability Register, MMD Device 7, Address 0x3d)	45
8.	SWITCHING REGULATOR.....	46
8.1.	PCB LAYOUT.....	46
8.2.	INDUCTOR AND CAPACITOR PARTS LIST	47
8.3.	MEASUREMENT CRITERIA	48
8.4.	EFFICIENCY MEASUREMENT	52
8.5.	POWER SEQUENCE	53

9.	CHARACTERISTICS	54
9.1.	ABSOLUTE MAXIMUM RATINGS.....	54
9.2.	RECOMMENDED OPERATING CONDITIONS	54
9.3.	CRYSTAL REQUIREMENTS.....	55
9.4.	OSCILLATOR REQUIREMENTS.....	55
9.5.	DC CHARACTERISTICS.....	56
9.5.1.	<i>SGMII DC Characteristics</i>	56
9.6.	AC CHARACTERISTICS.....	57
9.6.1.	<i>MDC/MDIO Timing</i>	57
9.6.2.	<i>MII Timing Modes</i>	58
9.6.3.	<i>GMII Timing Modes</i>	60
9.6.4.	<i>RGMII Timing Modes</i>	61
9.6.5.	<i>SGMII Timing Modes</i>	64
10.	MECHANICAL DIMENSIONS.....	66
10.1.	RTL8211D 48-PIN QFN MECHANICAL DIMENSIONS	66
10.2.	RTL8211D 48-PIN QFN MECHANICAL DIMENSIONS NOTES.....	66
10.3.	RTL8211DG 64-PIN QFN MECHANICAL DIMENSIONS	67
10.4.	RTL8211DG 64-PIN QFN MECHANICAL DIMENSIONS NOTES.....	68
10.5.	RTL8211DN 88-PIN QFN MECHANICAL DIMENSIONS	69
10.6.	RTL8211DN 88-PIN QFN MECHANICAL DIMENSIONS NOTES.....	70
11.	ORDERING INFORMATION.....	71

List of Tables

TABLE 1. TRANSCEIVER INTERFACE	9
TABLE 2. CLOCK	9
TABLE 3. GMII/MII (RTL8211DG AND RTL8211DN ONLY)	10
TABLE 4. RGMII	11
TABLE 5. SGMII (RTL8211DN ONLY)	12
TABLE 6. MANAGEMENT INTERFACE	12
TABLE 7. RESET	13
TABLE 8. MODE SELECTION	13
TABLE 9. LED INDICATION	13
TABLE 10. REGULATOR AND REFERENCE	14
TABLE 11. POWER AND GROUND	14
TABLE 12. NOT CONNECTED	14
TABLE 13. CONFIG PINS VS. CONFIGURATION REGISTER	17
TABLE 14. CONFIGURATION REGISTER DEFINITION (PHY AD AND NWay)	18
TABLE 15. MII/MDI INTERFACE CONFIGURATION	19
TABLE 16. TYPICAL MDIO FRAME FORMAT	21
TABLE 17. 1000BASE-T AND NEXT PAGES BIT ASSIGNMENTS	24
TABLE 18. LED DEFAULT DEFINITIONS	29
TABLE 19. LED REGISTER TABLE	29
TABLE 20. LED CONFIGURATION TABLE	30
TABLE 21. PAGE0 REGISTER MAPPING AND DEFINITIONS	32
TABLE 22. EXTENSION PAGE REGISTER MAPPING AND DEFINITION	32
TABLE 23. MMD REGISTER MAPPING AND DEFINITION	33
TABLE 24. BMCR (BASIC MODE CONTROL REGISTER, ADDRESS 0x00)	33
TABLE 25. BMSR (BASIC MODE STATUS REGISTER, ADDRESS 0x01)	35
TABLE 26. PHYID1 (PHY IDENTIFIER REGISTER 1, ADDRESS 0x02)	36
TABLE 27. PHYID2 (PHY IDENTIFIER REGISTER 2, ADDRESS 0x03)	36
TABLE 28. ANAR (AUTO-NEGOTIATION ADVERTISING REGISTER, ADDRESS 0x04)	37
TABLE 29. ANLPAR (AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER, ADDRESS 0x05)	37
TABLE 30. ANER (AUTO-NEGOTIATION EXPANSION REGISTER, ADDRESS 0x06)	38
TABLE 31. ANNPTR (AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER, ADDRESS 0x07)	38
TABLE 32. ANNPRR (AUTO-NEGOTIATION NEXT PAGE RECEIVE REGISTER, ADDRESS 0x08)	39
TABLE 33. GBCR (1000BASE-T CONTROL REGISTER, ADDRESS 0x09)	39
TABLE 34. GBSR (1000BASE-T STATUS REGISTER, ADDRESS 0x0A)	40
TABLE 35. MACR (MMD ACCESS CONTROL REGISTER, ADDRESS 0x0D)	40
TABLE 36. MAADR (MMD ACCESS ADDRESS DATA REGISTER, ADDRESS 0x0E)	41
TABLE 37. GBESR (1000BASE-T EXTENDED STATUS REGISTER, ADDRESS 0x0F)	41
TABLE 38. PHYCR (PHY SPECIFIC CONTROL REGISTER, ADDRESS 0x10)	41
TABLE 39. PHYSR (PHY SPECIFIC STATUS REGISTER, ADDRESS 0x11)	42
TABLE 40. INER (INTERRUPT ENABLE REGISTER, ADDRESS 0x12)	42
TABLE 41. INSR (INTERRUPT STATUS REGISTER, ADDRESS 0x13)	43
TABLE 42. RXERC (RECEIVE ERROR COUNTER, ADDRESS 0x18)	43
TABLE 43. PAGSEL (PAGE SELECT REGISTER, ADDRESS 0x1F)	43
TABLE 44. SDSR (SERDES REGISTER, EXTPAGE 140, ADDRESS 0x16)	44
TABLE 45. PC1R (PCS CONTROL 1 REGISTER, MMD DEVICE 3, ADDRESS 0x00)	44
TABLE 46. PS1R (PCS STATUS 1 REGISTER, MMD DEVICE 3, ADDRESS 0x01)	44
TABLE 47. EEECR (EEE CAPABILITY REGISTER, MMD DEVICE 3, ADDRESS 0x14)	44
TABLE 48. EEEWER (EEE WAKE ERROR REGISTER, MMD DEVICE 3, ADDRESS 0x16)	45
TABLE 49. EEEAR (EEE ADVERTISEMENT REGISTER, MMD DEVICE 7, ADDRESS 0x3C)	45
TABLE 50. EEELPAR (EEE LINK PARTNER ABILITY REGISTER, MMD DEVICE 7, ADDRESS 0x3D)	45
TABLE 51. INDUCTOR AND CAPACITOR PARTS LIST	47

TABLE 52. POWER SEQUENCE PARAMETER.....	53
TABLE 53. ABSOLUTE MAXIMUM RATINGS.....	54
TABLE 54. RECOMMENDED OPERATING CONDITIONS	54
TABLE 55. CRYSTAL REQUIREMENTS	55
TABLE 56. OSCILLATOR REQUIREMENTS.....	55
TABLE 57. DC CHARACTERISTICS.....	56
TABLE 58. DIFFERENTIAL TRANSMITTER OUTPUT DC CHARACTERISTICS.....	56
TABLE 59. DIFFERENTIAL RECEIVER INPUT DC CHARACTERISTICS.....	56
TABLE 60. MDC/MDIO MANAGEMENT TIMING PARAMETERS.....	57
TABLE 61. MII TRANSMIT TIMING PARAMETERS	58
TABLE 62. MII RECEIVE TIMING PARAMETERS.....	59
TABLE 63. GMII TIMING PARAMETERS.....	60
TABLE 64. RGMII TIMING PARAMETERS	63
TABLE 65. DIFFERENTIAL TRANSMITTER OUTPUT AC TIMING	65
TABLE 66. DIFFERENTIAL RECEIVER INPUT AC TIMING.....	65
TABLE 67. ORDERING INFORMATION	71

List of Figures

FIGURE 1. APPLICATION DIAGRAM (RTL8211D).....	3
FIGURE 2. APPLICATION DIAGRAM (RTL8211DG).....	3
FIGURE 3. FIBER APPLICATION DIAGRAM (RTL8211DN).....	4
FIGURE 4. UTP APPLICATION DIAGRAM (RTL8211DN).....	4
FIGURE 5. FIBER TO UTP (BRIDGE MODE) APPLICATION DIAGRAM (RTL8211DN).....	4
FIGURE 6. SGMII TO GMII/RGMII (BRIDGE MODE) APPLICATION DIAGRAM (RTL8211DN).....	5
FIGURE 7. UTP/FIBER AUTO-DETECTION TO GMII/RGMII APPLICATION DIAGRAM (RTL8211DN).....	5
FIGURE 8. RTL8211D PIN ASSIGNMENTS (48-PIN QFN).....	6
FIGURE 9. RTL8211DG PIN ASSIGNMENTS (64-PIN QFN).....	7
FIGURE 10. RTL8211DN PIN ASSIGNMENTS (88-PIN QFN).....	8
FIGURE 11. PHY APPLICATION (RTL8211DN).....	17
FIGURE 12. LED AND PHY ADDRESS CONFIGURATION.....	19
FIGURE 13. TYPICAL MDC/MDIO READ TIMING.....	22
FIGURE 14. TYPICAL MDC/MDIO WRITE TIMING.....	22
FIGURE 15. SWITCHING REGULATOR.....	46
FIGURE 16. INPUT VOLTAGE OVERSHOOT <4V (GOOD).....	48
FIGURE 17. INPUT VOLTAGE OVERSHOOT >4V (BAD).....	48
FIGURE 18. CERAMIC 22 μ F 1210(X5R) (GOOD).....	49
FIGURE 19. CERAMIC 22 μ F 0805(Y5V) (BAD).....	49
FIGURE 20. ELECTROLYTIC 100 μ F (RIPPLE TOO HIGH).....	50
FIGURE 21. 4R7GTS32 (GOOD).....	51
FIGURE 22. 1 μ H BEAD (BAD).....	51
FIGURE 23. SWITCHING REGULATOR EFFICIENCY MEASUREMENT CHECKPOINT.....	52
FIGURE 24. POWER SEQUENCE.....	53
FIGURE 25. MDC/MDIO MANAGEMENT TIMING PARAMETERS.....	57
FIGURE 26. MII TIMING – MII PORT – TRANSMIT.....	58
FIGURE 27. MII TIMING – MII PORT – RECEIVE.....	59
FIGURE 28. GMII TIMING.....	60
FIGURE 29. RGMII TIMING MODES.....	62
FIGURE 30. SGMII TIMING MODES.....	64

1. General Description

The Realtek RTL8211D/DG/DN-VB is a highly integrated Ethernet transceiver that complies with 10Base-T, 100Base-TX, 100Base-FX, 1000Base-T, and 1000Base-X IEEE 802.3 standards. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable.

The RTL8211D/DG/DN uses state-of-the-art DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented in the RTL8211D/DG/DN to provide robust transmission and reception capabilities at 10Mbps, 100Mbps, or 1000Mbps. The advanced DSP algorithms provide robust communication even in critical environments.

The RTL8211D/DG/DN supports various interfaces to communicate with the MAC and PHY, including:

- RGMII (Reduced Gigabit Media Independent Interface) for 1000/10Base-T and 100Base-TX (RTL8211D, RTL8211DG, and RTL8211DN)
- GMII/MII (Gigabit Media Independent Interface) for 1000/10Base-T and 100Base-TX (RTL8211DG and RTL8211DN only)
- SGMII (Serial Gigabit Media Independent Interface) for 1000Base-X and 100Base-FX (RTL8211DN only)

The RTL8211DN supports a SerDes interface that can be configured as SGMII, 1000Base-X, and 100Base-FX.

2. Features

- 1000Base-T/1000Base-X IEEE 802.3ab Compliant
- 100Base-TX/100Base-FX IEEE 802.3u Compliant
- 10Base-T IEEE 802.3 Compliant
- IEEE 802.3 Compliant RGMII (RTL8211D/DG/DN)
- IEEE 802.3 Compliant GMII/MII (RTL8211DG/DN)
- Supports IEEE 802.3az Draft 3.2 (Energy Efficient Ethernet)
- Supports SerDes (RTL8211DN)
- RTL8211DN supports UTP or fiber mode output
- Supports PHYRSTB core power Turn-Off
- Built-in Wake-On-LAN (WOL)
- Supports Interrupt function
- Supports media converter/interface converter (SGMII to GMII/RGMII or 1000Base-X to 1000Base-T)
- Supports Auto-Negotiation
- Supports Parallel Detection
- Green Ethernet (Gigabit mode only)
- Crossover Detection & Auto-Correction
- Automatic polarity correction
- Baseline Wander Correction
- Supports 120m for CAT.5 cable in 1000Base-T
- Supports 3.3V or 2.5V signaling for GMII/RGMII
- Supports 25MHz external crystal or OSC
- Provides 125MHz clock source for MAC
- LEDs
 - ◆ RTL8211DN provides 4 network status LEDs
 - ◆ RTL8211D/DG provides 3 network status LEDs
- Built-in switching regulator
- Packages
 - ◆ 48-pin QFN (RTL8211D)
 - ◆ 64-pin QFN (RTL8211DG)
 - ◆ 88-pin QFN (RTL8211DN)
- RTL8211D-VB layout-compatible with RTL8211CN/RTL8211E
- 0.11μm process with very low power consumption

3. System Applications

Network Interface Adapter, MAU (Media Access Unit), CNR (Communication and Network Riser), ACR (Advanced Communication Riser), Ethernet hub, and Ethernet switch.

In addition, it can be used in any embedded system with an Ethernet MAC that needs a UTP or Fiber physical connection (only the RTL8211DN supports fiber mode).

3.1. Application Diagram (RTL8211D)

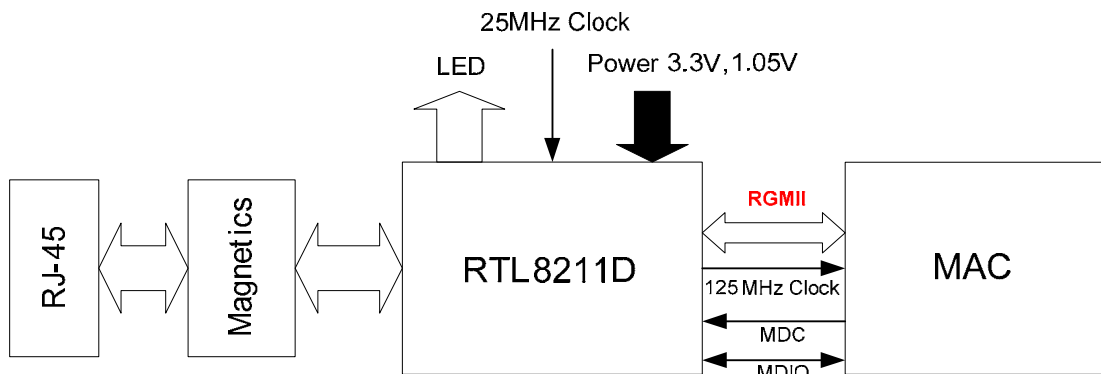


Figure 1. Application Diagram (RTL8211D)

3.2. Application Diagram (RTL8211DG)

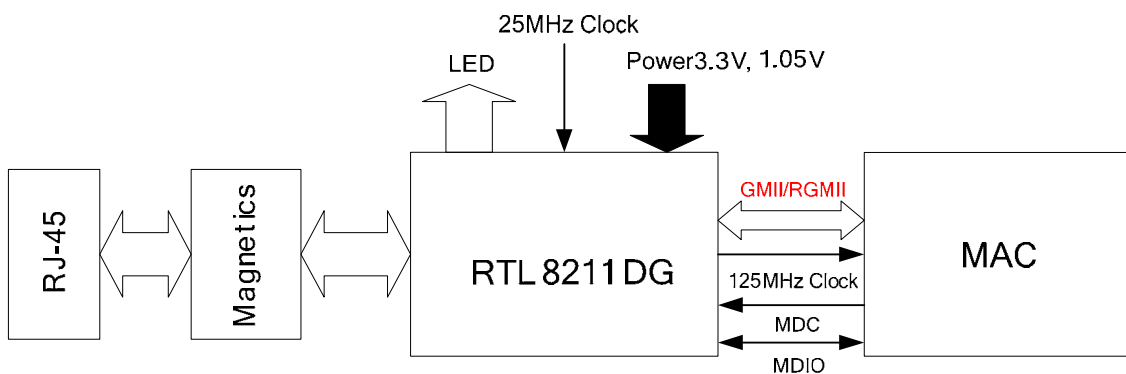


Figure 2. Application Diagram (RTL8211DG)

3.3. Fiber Application Diagram (RTL8211DN)

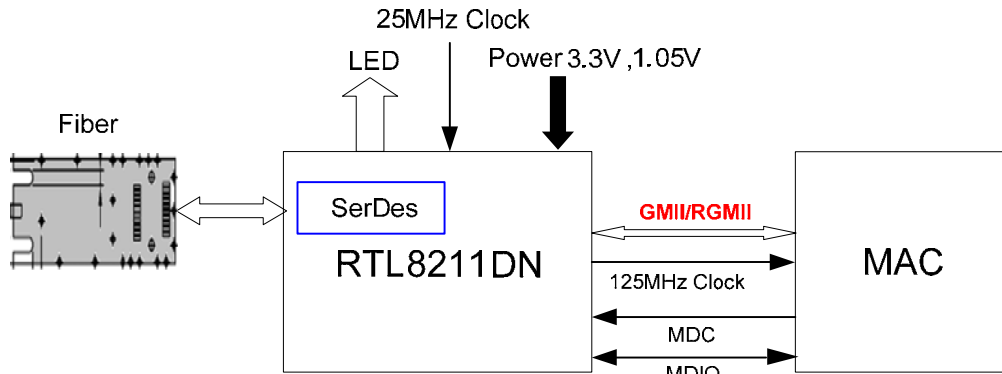


Figure 3. Fiber Application Diagram (RTL8211DN)

3.4. UTP Application Diagram (RTL8211DN)

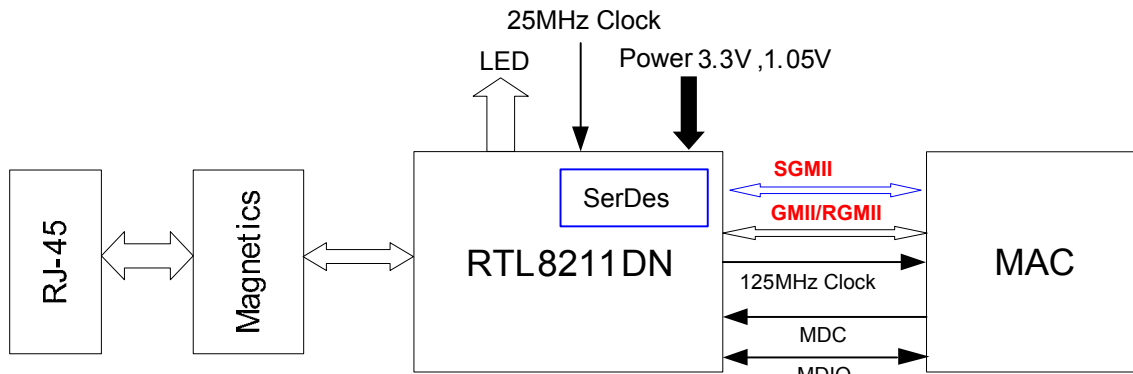


Figure 4. UTP Application Diagram (RTL8211DN)

3.5. Fiber to UTP (Bridge Mode) Application Diagram (RTL8211DN)

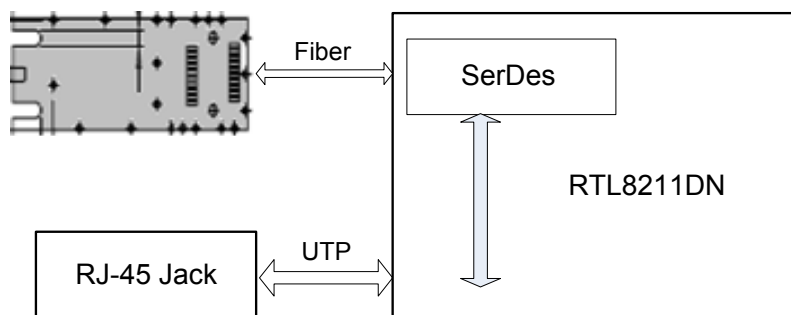


Figure 5. Fiber to UTP (Bridge Mode) Application Diagram (RTL8211DN)

3.6. SGMII to GMII/RGMII (Bridge Mode) Application Diagram (RTL8211DN)

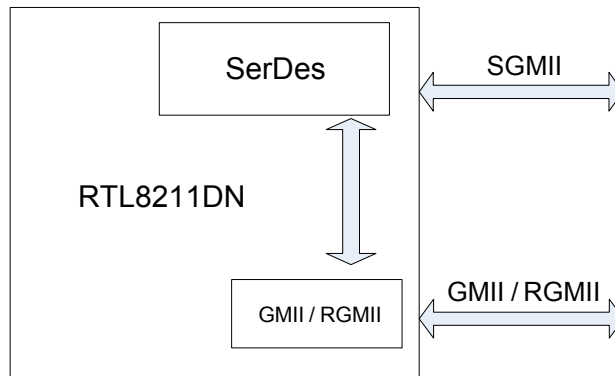


Figure 6. SGMII to GMII/RGMII (Bridge Mode) Application Diagram (RTL8211DN)

3.7. UTP/Fiber Auto-Detection to GMII/RGMII Application Diagram (RTL8211DN)

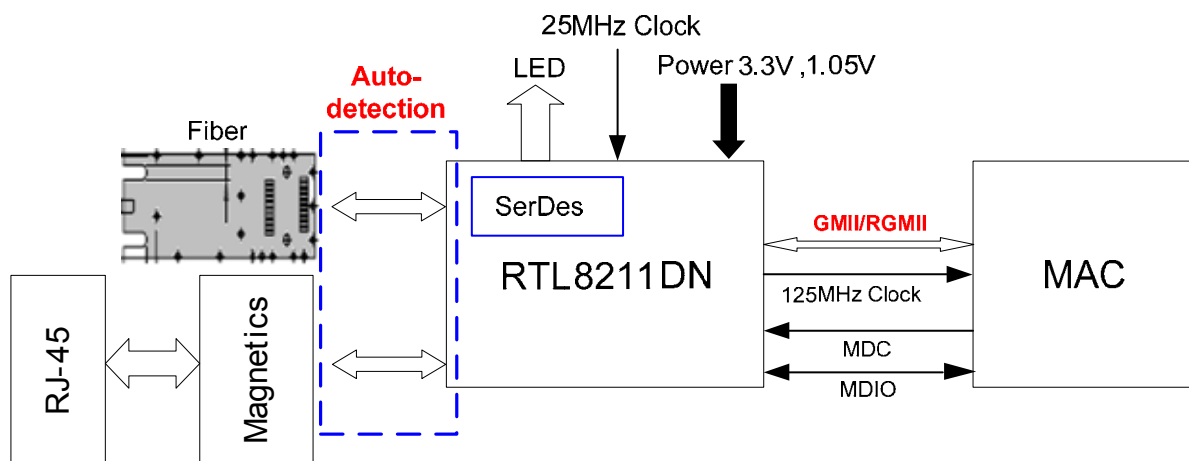


Figure 7. UTP/Fiber Auto-Detection to GMII/RGMII Application Diagram (RTL8211DN)

4. Pin Assignments

4.1. RTL8211D Pin Assignments (48-Pin QFN)

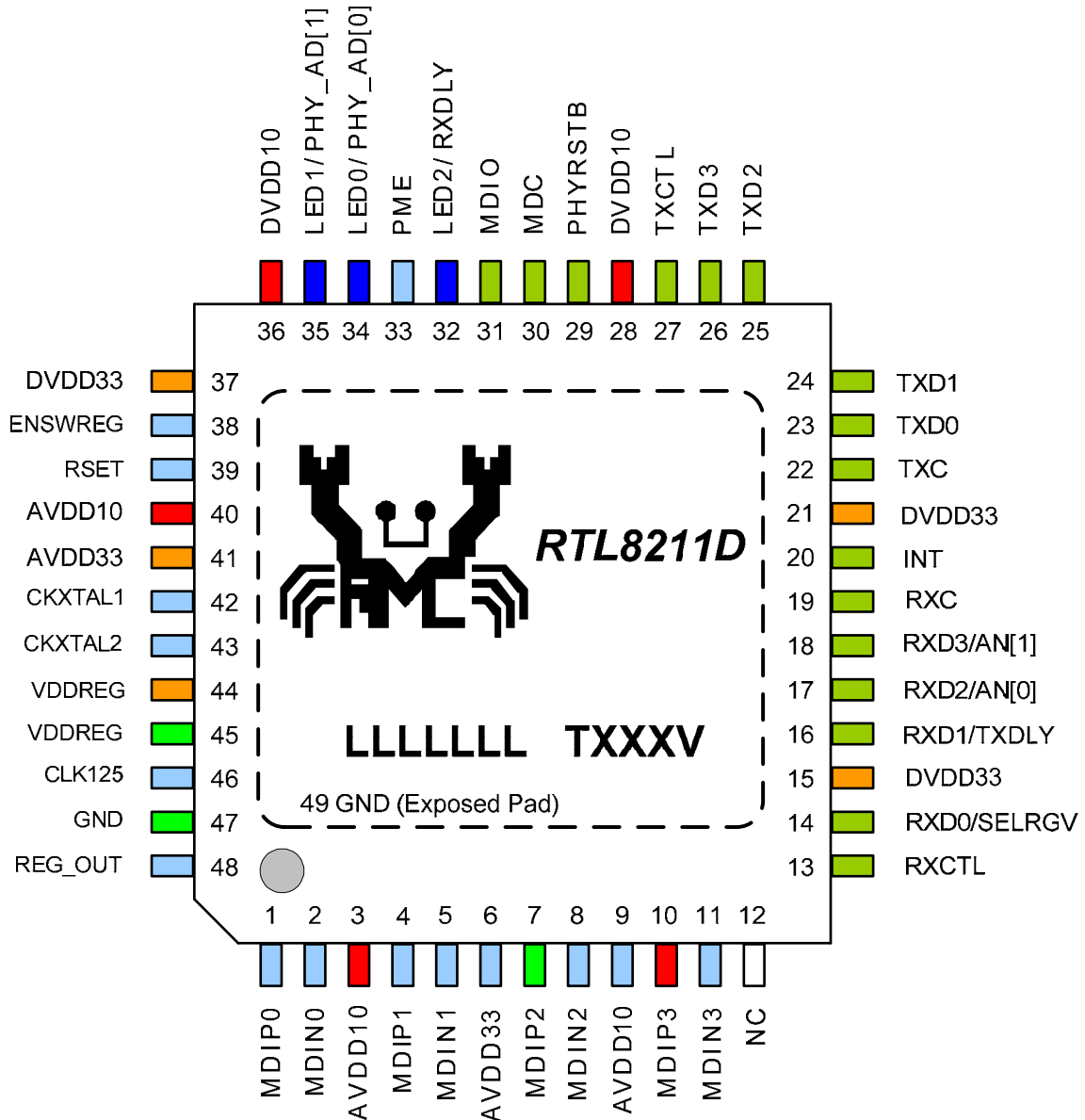


Figure 8. RTL8211D Pin Assignments (48-Pin QFN)

4.2. Package Identification

'Green' package is indicated by a 'G' in the location marked 'T' in Figure 8. The version is shown in the location marked 'V'.

4.3. RTL8211DG Pin Assignments (64-Pin QFN)

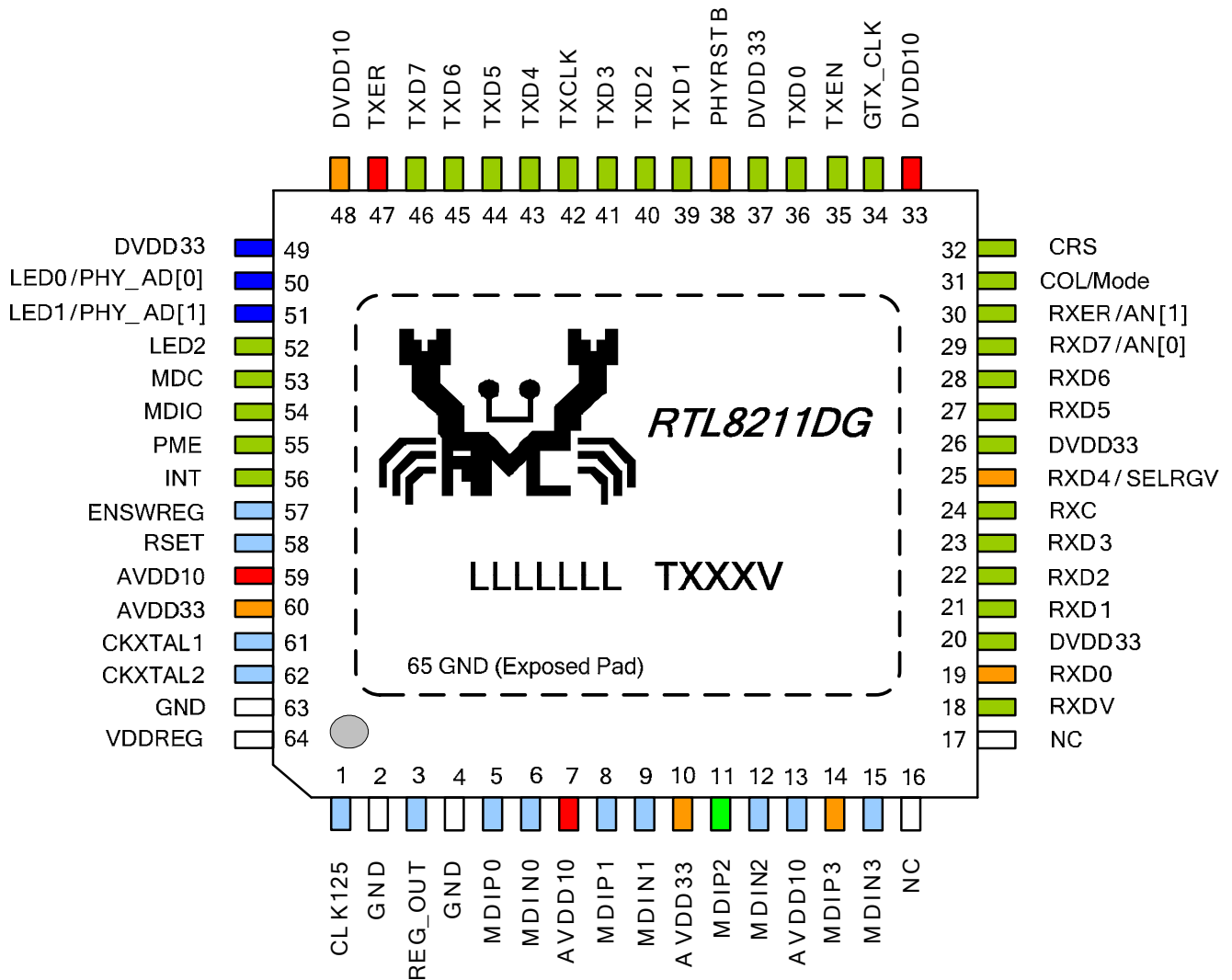


Figure 9. RTL8211DG Pin Assignments (64-Pin QFN)

4.4. Package Identification

‘Green’ package is indicated by a ‘G’ in the location marked ‘T’ in Figure 9. The version is shown in the location marked ‘V’.

4.5. RTL8211DN Pin Assignments (88-Pin QFN)

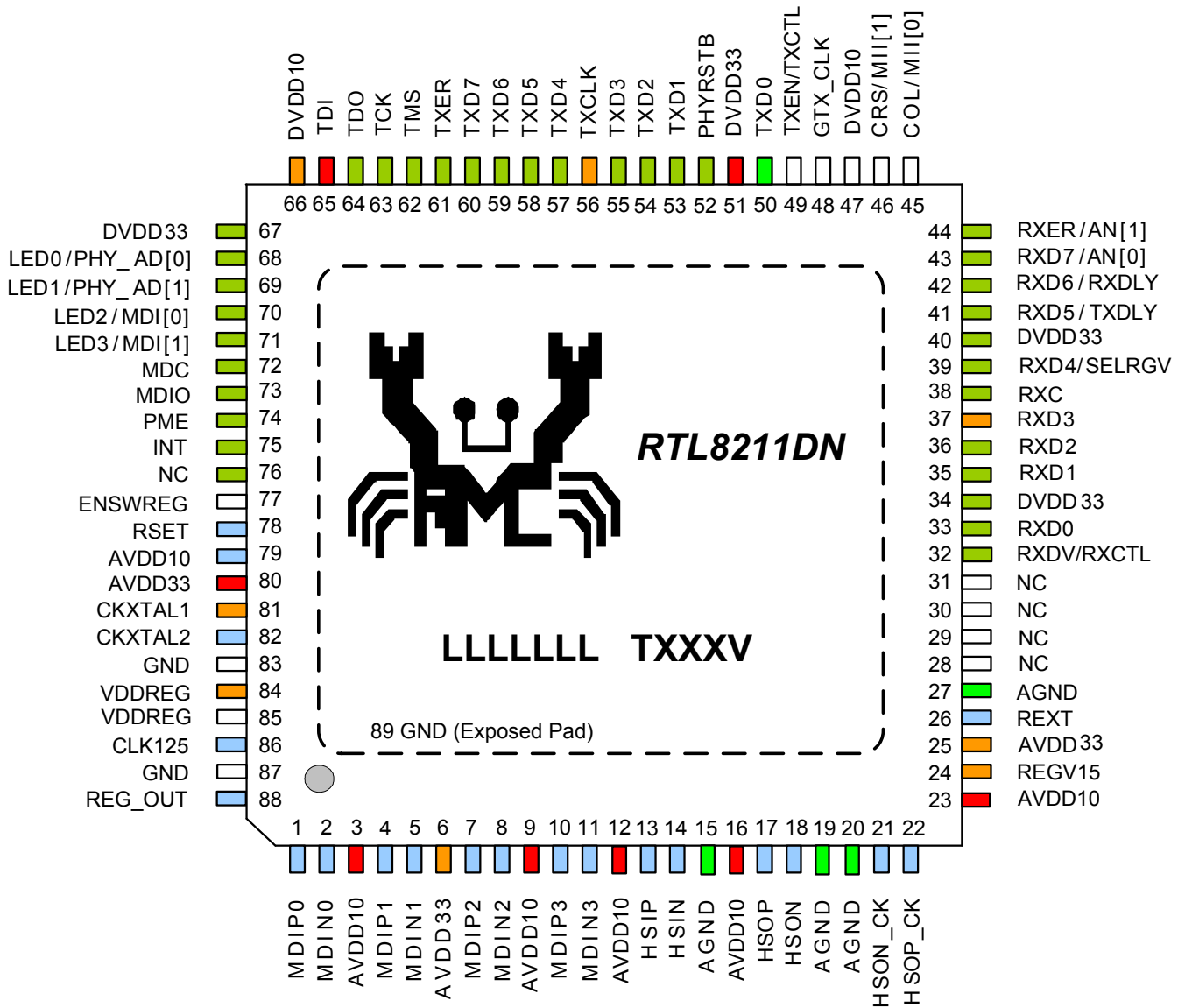


Figure 10. RTL8211DN Pin Assignments (88-Pin QFN)

4.6. Package Identification

'Green' package is indicated by a 'G' in the location marked 'T' in Figure 10. The version is shown in the location marked 'V'.

5. Pin Descriptions

Note that some pins have multiple functions. Refer to the Pin Assignments figures for a graphical representation.

I: Input	LI: Latched Input during Power up or Reset
O: Output	IO: Bi-directional input and output
P: Power	HZ: High impedance during power on reset
PU: Internal Pull up during power on reset	PD: Internal Pull down during power on reset
G: Ground	OP: Open Drain

5.1. Transceiver Interface

Table 1. Transceiver Interface

Pin No. (48-pin)	Pin No. (64-pin)	Pin No. (88-pin)	Pin Name	Type	Description
1	5	1	MDIP0	IO	In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
2	6	2	MDIN0	IO	
4	8	4	MDIP1	IO	In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
5	9	5	MDIN1	IO	
7	11	7	MDIP2	IO	In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
8	12	8	MDIN2	IO	
10	14	10	MDIP3	IO	In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
11	15	11	MDIN3	IO	

5.2. Clock

Table 2. Clock

Pin No. (48-pin)	Pin No. (64-pin)	Pin No. (88-pin)	Pin Name	Type	Description
42	61	81	CKXTAL1	I	Input/Output of 25MHz Clock Reference.
43	62	82	CKXTAL2	O	
46	1	86	CLK125	O/HZ	125MHz Reference Clock Generated from Internal PLL. This pin should be left floating if this function is not used.

5.3. GMII/MII (RTL8211DN and RTL8211DG Only)

Table 3. GMII/MII (RTL8211DG and RTL8211DN Only)

Pin No. (48-pin)	Pin No. (64-pin)	Pin No. (88-pin)	Pin Name	Type (64-pin)	Type (88-pin)	Description
-	34	48	GTX_CLK	I		The transmit reference clock is 125MHz.
-	42	56	TXCLK	O		The transmit reference clock is 25MHz or 2.5MHz depending on speed.
-	36	50	TXD0	I		Transmit Data.
-	39	53	TXD1	I		Data is transmitted from MAC to PHY via TXD[7:0].
-	40	54	TXD2	I		
-	41	55	TXD3	I		
-	43	57	TXD4	I		
-	44	58	TXD5	I		
-	45	59	TXD6	I		
-	46	60	TXD7	I		
-	35	49	TXEN	I		
-	47	61	TXER	I		Transmit Error. When both TXER and TXEN are asserted, the transmit error symbol is transmitted onto the cable. When TXER is asserted and TXEN is de-asserted, the carrier extension symbol is transmitted onto the cable.
-	24	38	RXC	O		The continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz. And is derived from the received data stream.
-	19	33	RXD0	O		Receive Data.
-	21	35	RXD1	O		Data is transmitted from PHY to MAC via RXD[7:0].
-	22	36	RXD2	O		
-	23	37	RXD3	O		
-	25	39	RXD4	LI/O/PU		
-	27	41	RXD5	LI/O/PD		
-	28	42	RXD6	LI/O/PU		
-	29	43	RXD7	LI/O/PU		
-	18	32	RXDV	O		
-	30	44	RXER	LI/O/PU		Receive Error. When both RXER and RXDV are asserted, an error symbol is received from the cable. When RXER is asserted and RXDV is de-asserted, it means false carrier or carrier extension symbol is detected on the cable.
-	31	45	COL	LI/O/PD		Collision In Half Duplex Mode
-	32	46	CRS	O/PD	LI/O/PD	Carrier Sense.

5.4. RGMII

Table 4. RGMII

Pin No. (48-pin)	Pin No. (64-pin)	Pin No. (88-pin)	Pin Name	Type (48-pin)	Type (64-pin)	Type (88-pin)	Description
22	34	48	GTX_CLK		I		The transmit reference clock will be 125MHz, 25MHz, or 2.5MHz depending on speed. The RTL8211D pin22 is named TXC.
23	36	50	TXD0		I		Transmit Data.
24	39	53	TXD1		I		Data is transmitted from MAC to PHY via TXD[3:0].
25	40	54	TXD2		I		
26	41	55	TXD3		I		
27	35	49	TXCTL		I		Receive Control Signal from the MAC. In GMII/MII mode, the RTL8211DG pin35 and RTL8211DN pin49 are named TXEN.
19	24	38	RXC		O		The continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream.
14	19	33	RXD0	LI/O/PU		O	Receive Data. Data is transmitted from PHY to MAC via RXD[3:0].
16	21	35	RXD1	LI/O/PD		O	
17	22	36	RXD2	LI/O/PU		O	
18	23	37	RXD3	LI/O/PU		O	
13	18	32	RXCTL		O		Transmit Control Signal to the MAC. In GMII/MII mode, the RTL8211DG pin18 and RTL8211DN pin32 are named RXDV.
16	27	41	TXDLY		LI/O/PD		RGMII Transmit Clock Timing Control. 1: Add 2ns delay to TXC for TXD latching The RTL8211DG pin27 is named RXD5.
32	28	42	RXDLY		LI/O/PU		RGMII Receiver Clock Timing Control. 1: Add 2ns delay to RXC for RXD latching The RTL8211DG pin28 is named RXD6.

5.5. SGMII (RTL8211DN Only)

Table 5. SGMII (RTL8211DN Only)

Pin No. (48-pin)	Pin No. (64-pin)	Pin No. (88-pin)	Pin Name	Type	Description
-	-	13	HSIP	I	SGMII Differential Input: 1.25GHz serial interfaces to receive data from an External device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
-	-	14	HSIN	I	
-	-	15, 19, 20, 27	AGND	G	Analog Ground for SGMII Circuits.
-	-	17	HSOP	O	SGMII Differential Output: 1.25GHz serial interfaces to transfer data from an External device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
-	-	18	HSOIN	O	
-	-	21	HSOIN_CLK	O	SGMII 625MHz Receive CLK Pair. 625MHz differential serial clock output.
-	-	22	HSOP_CLK	O	The differential pair has an internal 100-ohm termination resistor.
-	-	24	REGV15	P	Internal 1.5V regulator power when fiber mode enabled. AVDD10 power pin when SGMII enabled.
-	-	26	REXT	O	Reference. External Resistor Reference. Connect to 12k-ohm resistor.

5.6. Management Interface

Table 6. Management Interface

Pin No. (48-pin)	Pin No. (64-pin)	Pin No. (88-pin)	Pin Name	Type	Description
30	53	72	MDC	I	Management Data Clock.
31	54	73	MDIO	IO	Input/Output of Management Data.
33	55	74	PME	O/OD	Power Management Event (Supports 3.3V and 5V Pull Up). Set low if receives magic packet or wake up frame; active low. The pin should be left floating if does not use this function.
-	-	64	TDO	O	Test Data In for JTAG interface.
-	-	65	TDI	I/PU	Test Data Out for JTAG interface.
-	-	62	TMS	I/PU	Test Mode State for JTAG interface.
-	-	63	TCK	I/PD	Test Clock for JTAG interface.
20	56	75	INT	O/OD	Interrupt. Set low if status changes; Active Low. The pin should be left floating if this function not used.

5.7. Reset

Table 7. Reset

Pin No. (48-pin)	Pin No. (64-pin)	Pin No. (88-pin)	Pin Name	Type	Description
29	38	52	PHYRSTB	I/PU	Hardware Reset. Active low.

5.8. Mode Selection

Table 8. Mode Selection

Pin No. (48-pin)	Pin No. (64-pin)	Pin No. (88-pin)	Pin Name	Type	Description
34	50	68	PHY_AD[0]	LI/O/PU	PHY Address Configuration.
35	51	69	PHY_AD[1]	LI/O/PD	
17	29	43	AN[0]	LI/O/PU	NWay Configuration.
18	30	44	AN[1]	LI/O/PU	
-	-	45	MII[0]	LI/O/PD	MDI and Interface (SGMII/GMII/MII/RGMII) Configuration.
-	-	46	MII[1]	LI/O/PD	
-	-	70	MDI[0]	LI/O/PU	
-	-	71	MDI[1]	LI/O/PD	
-	31	-	Mode	LI/O/PD	Pull Up for RTL8211DG RGMII mode. Pull Down for RTL8211DG GMII mode.
14	25	39	SELRGV	LI/O/PU	Pull Up for 3.3V GMII/RGMII. Pull Down for 2.5V GMII/RGMII.

Note: See section 6.7 Hardware Configuration, page 17 for details.

5.9. LED Indication

Table 9. LED Indication

Pin No. (48-pin)	Pin No. (64-pin)	Pin No. (88-pin)	Pin Name	Type (48-pin)	Type (64-pin)	Type (88-pin)	Description
34	50	68	LED0	LI/O/PU			Active
35	51	69	LED1	LI/O/PD			LED 10/100/1000
32	52	70	LED2	LI/O/PU	O/PU	LI/O/PU	LED 10/100/1000+Active
-	-	71	LED3	LI/O/PD			LED100/1000 (Fiber mode only) + Activity (Fiber only)

Note: See section 6.13 LED Configuration, page 29 for details.

5.10. Regulator and Reference

Table 10. Regulator and Reference

Pin No. (48-pin)	Pin No. (64-pin)	Pin No. (88-pin)	Pin Name	Type	Description
39	58	78	RSET	O	External Resistor Reference. Connect to 2.49k-ohm resistor
44, 45	64	84, 85	VDDREG	P	3.3V Analog Power Supply for Switching Regulator.
48	3	88	REG_OUT	O	Switching Regulator 1.05V Output. Connect to a 4.7 μ H inductor.
3	7	3	AVDD10	P	Feedback Pin for Switching Regulator.
38	57	77	ENSWREG	I	3.3V: Enable switching regulator. 0V: Disable switching regulator.

5.11. Power and Ground

Table 11. Power and Ground

Pin No. (48-pin)	Pin No. (64-pin)	Pin No. (88-pin)	Pin Name	Type	Description
15, 21, 37	20, 26, 37, 49	34, 40, 51, 67	DVDD33	P	Digital Power. 3.3V.
15, 21	20, 26	34, 40	DVDD33	P	GMII/RGMII Power Pins. For 3.3 or 2.5V GMII/RGMII I/O.
28, 36	33, 48	47, 66	DVDD10	P	Digital Power. 1.05V.
6, 41	10, 60	6, 25, 80	AVDD33	P	Analog Power. 3.3V.
3, 9, 40	7, 13, 59	3, 9, 12, 16, 23, 79	AVDD10	P	Analog Power. 1.05V.
47	2, 4, 63	83, 87	GND	G	Ground. Exposed Pad (E-Pad) Digital Ground (see section 10.3, page 67).

5.12. Not Connected

Table 12. Not Connected

Pin No. (48-pin)	Pin No. (64-pin)	Pin No. (88-pin)	Pin Name	Type	Description
12	16, 17	28, 29, 30, 31, 76	NC	-	Not Connected.

6. Function Description

6.1. 1000Base-T Transmitter

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto 4-pair CAT5 cable at 125Mbps through a D/A converter.

6.2. 1000Base-T Receiver

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. Afterwards, the received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and sent to the GMII/MII/RGMII/SGMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the internal receive GMII/MII/RGMII/SGMII interface and sends it to the packet buffer manager.

6.3. Energy Efficient Ethernet (EEE)

The RTL8211D/DG/DN supports IEEE 802.3az Draft 3.2, also known as Energy Efficient Ethernet (EEE), at 10Mbps, 100Mbps, and 1000Mbps. This standard is being developed by the IEEE 802.3az Task Force, and should be finalized by September 2010. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled, however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported and to select the best set of parameters common to both devices.

Refer to <http://ieee802.org/3/interims/index.html> for more details.

6.4. Wake-On-LAN (WOL)

The RTL8211D/DG/DN can monitor the network for a Wakeup Frame or a Magic Packet, and notify the system via the PME (Power Management Event) pin when such a packet or event occurs. The system can then be restored to a normal state to process incoming jobs. The PME pin needs to be connected with a 4.7k-ohm resistor and pulled up to 3.3V or 5V. When the Wakeup Frame or a Magic Packet is sent to the PHY, the PME pin will be set low to notify the system to wake up. Refer to the WOL application note for details.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8211D/DG/DN, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8211D/DG/DN.
- The received Magic Packet does not contain a CRC error.
- The Magic Packet pattern matches; i.e., $6 * FFh + MISC$ (can be none) + $16 * DID$ (Destination ID) in any part of a valid Ethernet packet.

A Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8211D/DG/DN, e.g., a broadcast, multicast, or unicast address to the current RTL8211D/DG/DN.
- The received Wakeup Frame does not contain a CRC error.
- The 16-bit CRC* of the received Wakeup Frame matches the 16-bit CRC of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8211D/DG/DN is configured to allow direct packet wakeup, e.g., a broadcast, multicast, or unicast network packet.

Note: 16-bit CRC: The RTL8211D/DG/DN supports eight long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet).

6.5. MDI Interface

This interface consists of four signal pairs; MDI0, MDI1, MDI2, and MDI3. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

6.6. SerDes (SGMII) Interface (RTL8211DN Only)

The RTL8211DN supports one SerDes interface for 1000/100Base-X application. The SerDes interface can be enabled/disabled by pin strapping MDI[1:0] and MII[1:0]. These pins must be connected to 3.3V via a 4.7K-ohm resistor for SerDes operation.

Table 15, page 19 shows the SerDes interface configuration options. The application diagram is shown in Figure 11. When SerDes is selected in MDI mode, SGMII cannot be selected as PHY and MAC interface.

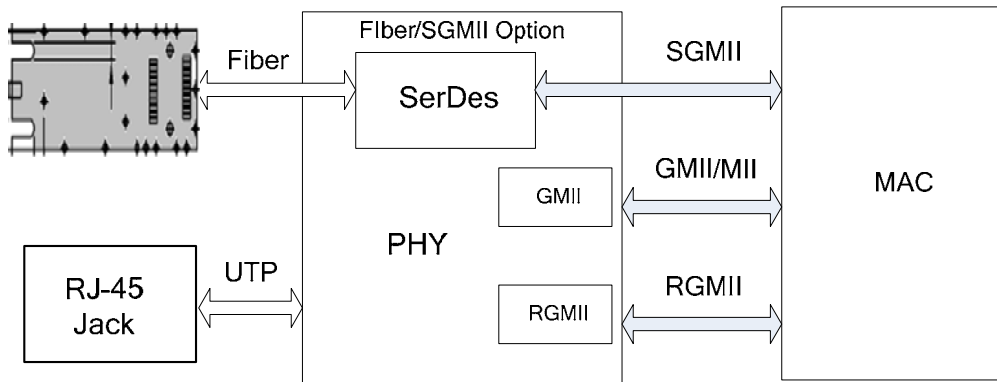


Figure 11. PHY Application (RTL8211DN)

6.7. Hardware Configuration

The operation speed, interface mode, and PHY address can be set by the CONFIG pins. The respective value mapping of CONFIG with the configurable vector is listed in Table 13. To set the CONFIG pins, an external pull-high or pull-low resistor is required.

Table 13. CONFIG Pins vs. Configuration Register

RTL8211DN Pin	RTL8211DG Pin	RTL8211D Pin	Pin Name
LED0	LED0	LED0	PHY_AD[0]
LED1	LED1	LED1	PHY_AD[1]
LED2	-	-	MDI[0]
LED3	-	-	MDI[1]
RXD7	RXD7	RXD2	AN[0]
RXER	RXER	RXD3	AN[1]
COL	-	-	MII[0]
CRS	-	-	MII[1]
RXD6	RXD6	LED2	RX Delay
RXD5	RXD5	RXD1	TX Delay

Table 14. Configuration Register Definition (PHY AD and NWay)

Configuration	Description
PHYAD[1:0]	PHY Address. PHYAD sets the PHY address for the device. <i>Note: PHYAD[:]=0 can support all PHY addresses. It can automatically remember the first PHY address sent by the MAC.</i>
AN[1:0]	Auto-Negotiation (NWay) Configuration. AN[1:0] controls the setting of Auto-Negotiation enable/disable, speed, and duplex setting. 00: 10Base-T Full Duplex 01: 100Base-Tx Half Duplex 10: 100Base-Tx Full Duplex 11: NWay. Advertises all capabilities
Mode	Interface Mode Select. MODE specifies the RTL8211DG operating mode. 0: MII/GMII (via 4.7k-ohm to GND) 1: RGMII (via 4.7k-ohm to 3.3V)

For the interface configuration, MDI CONFIG pins and MII CONFIG pins can be easily set via an external resistor (RTL8211DN Only). The various settings are shown below:

CFG_MDI[1:0]

{0, 0}: Use fiber as MDI, with GMII, RGMII, SGMII as MII options

{0, 1}: Use UTP as MDI, with GMII, RGMII as MII options

{1, 0}: Auto-sense UTP/fiber as MDI, with GMII/RGMII as MII options

{1, 1}: Operate as interface converter at MAC site

CFG_MII[1:0]

{0, 0}: Use GMII as MII, with UTP/fiber/auto-sensing as MDI options

{0, 1}: Use RGMII as MII, with UTP/fiber/auto-sensing as MDI options

{1, 0}: Use SGMII as MII, with UTP as MDI

{1, 1}: Operate as media converter. Convert packets between UTP and fiber

Table 15. MII/MDI Interface Configuration

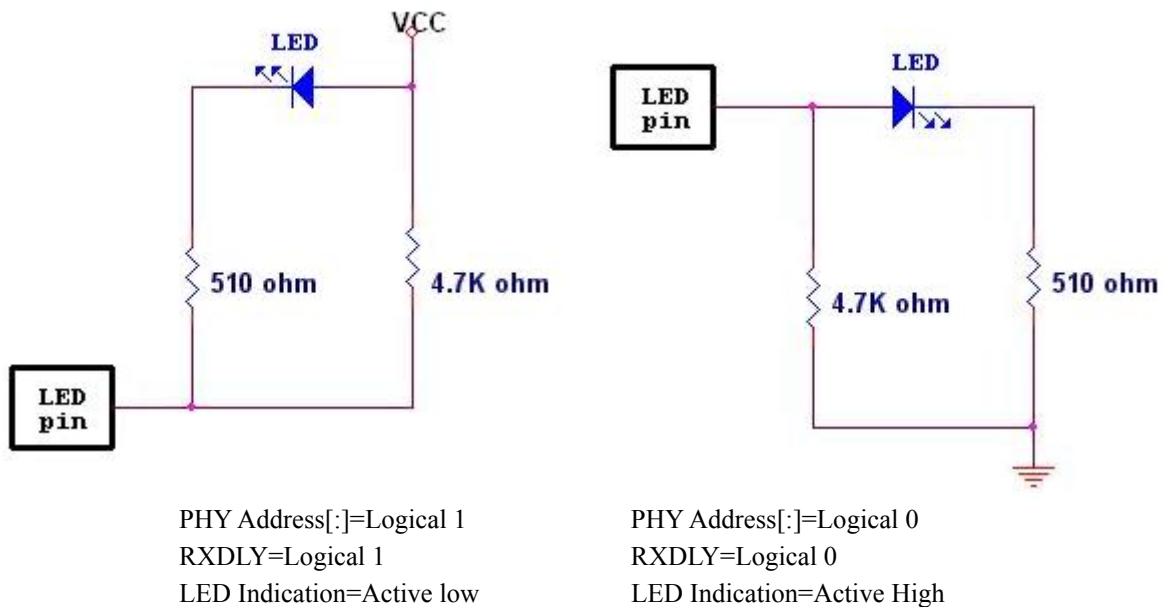
	MDI[0,0]	MDI[0,1]	MDI[1,0]	MDI[1,1]
MII[0,0]	Fiber<->GMII	UTP<->GMII	UTP/Fiber<->GMII	SGMII<->GMII
MII[0,1]	Fiber<->RGMII	UTP<->RGMII	UTP/Fiber<->RGMII	SGMII<->RGMII
MII[1,0]	Not Valid Setting	UTP<->SGMII	Not Valid Setting	
MII[1,1]		UTP<->Fiber		

Note: The RTL8211DN default setting is UTP<->GMII mode {MDI[0,1] MII[0,0]}. UTP/Fiber = media detection.

6.8. LED and PHY Address Configuration

In order to reduce the pin count on the RTL8211D/DG/DN, the LED pins are duplexed with the PHY address pins. As the PHYAD strap options share the LED output pins, the external combinations required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD input upon power-up/reset.

For example, as Figure 12 (left-side) shows, if a given PHYAD input is resistively pulled high then the corresponding output will be configured as an active low driver. On the right side, we can see that if a given PHYAD input is resistively pulled low then the corresponding output will be configured as an active high driver. The PHY address configuration pins should not be connected to GND or VCC directly, but must be pulled high or low through a resistor (e.g., 4.7KΩ). If no LED indications are needed, the components of the LED path (LED+510Ω) can be removed.


Figure 12. LED and PHY Address Configuration

6.9. Green Ethernet (Gigabit Mode Only)

6.9.1. Cable Length Power Saving

In Gigabit mode the RTL8211Dx provides dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

6.9.2. Register Setting

Follow the register settings below to enable Green Ethernet:

Reg31 write 0x0003 (page3)

Reg25 write 0x3247

Reg31 write 0x0005 (page5)

Reg1 write 0x0240

Reg31 write 0x0000 (page0)

Follow the register settings below to disable Green Ethernet:

Reg31 write 0x0003 (page3)

Reg25 write 0x3246

Reg31 write 0x0000 (page0)

6.10. MAC/PHY Interface

The RTL8211D(G) supports industry standards and is suitable for most off-the-shelf MACs with GMII/MII interfaces.

The RTL8211DN supports industry standards and is suitable for most off-the-shelf MACs with GMII/MII/RGMII/SGMII interfaces.

6.10.1. MII

In 100Base-TX and 10Base-T modes (MII mode is selected), TXC and RXC sources are 25MHz and 2.5MHz respectively. TXC and RXC will always be generated by the PHY. TXD[3:0] and RXD[3:0] signals are used for data transitions.

6.10.2. GMII

In 1000Base-T mode (GMII interface is selected), a 125MHz transmit clock is expected on GTX_CLK. TXCLK sources 25MHz or 2.5MHz clock depending on the register setting. RXCLK sources the 125MHz receive clock.

6.10.3. RGMII

In 1000Base-T mode (RGMII interface is selected), TXC and RXC sources are 125MHz. TXC will always be generated by the MAC and RXC will always be generated by the PHY. TXD[3:0] and RXD[3:0] signals are used for data transitions on rising and falling edges of the clock.

6.10.4. SGMII

The Serial Gigabit Media Independent Interface (SGMII) is a follow-on from MII, a standard interface used to connect a MAC-block to a PHY. It is used for Gigabit Ethernet (Ethernet/Fast Ethernet uses MII). It differs from GMII/MII by its low-power requirements and low-pin-count serial interface (commonly referred to as SerDes). To carry frame data and link rate information between a 10/100/1000 PHY and an Ethernet MAC, SGMII uses a differential pair for data signals and for clocking signals, with both being present in each direction (i.e., transmit and receive). The data signals operate at 1.25G/ baud and the clocks operate at 625MHz (a DDR interface). Due to the high speed of operation, the use of differential pairs provides signal integrity while minimizing system noise.

6.10.5. Management Interface

The management interface provides access to the internal registers through the MDC and MDIO pins as described in IEEE 802.3u section 22. The MDC signal, provided by the MAC, is the management data clock referenced to the MDIO signal. The MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC. The MDIO pin needs a 1.5k-ohm pull-up resistor to maintain the MDIO high during idle and turnaround.

Preamble suppression is the default setting of the RTL8211D/DG/DN after power-on. However, there still must be at least one idle bit between operations.

Up to 32 bits, the RTL8211D/DG/DNs can share the same MDIO line. In switch/router applications, each port should be assigned a unique address during the hardware reset sequence, and it can only be addressed via that unique PHY address. For detailed information on the RTL8211D/DG/DN management registers, see section 7 Register Descriptions, page 32.

Table 16. Typical MDIO Frame Format

Management Serial Protocol	<idle><start><op code><PHY addr.><reg. addr.><turnaround><data><idle>
Read	<idle><01><10><AAAAA><RRRRR><Z0><xxxx xxxx xxxx xxxx><idle>
Write	<idle><01><01><AAAAA><RRRRR><10><xxxx xxxx xxxx xxxx><idle>

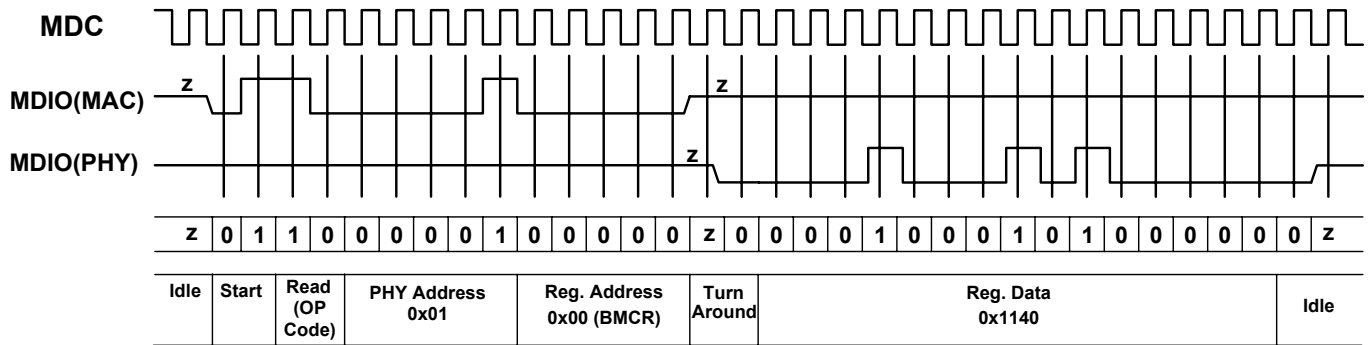


Figure 13. Typical MDC/MDIO Read Timing

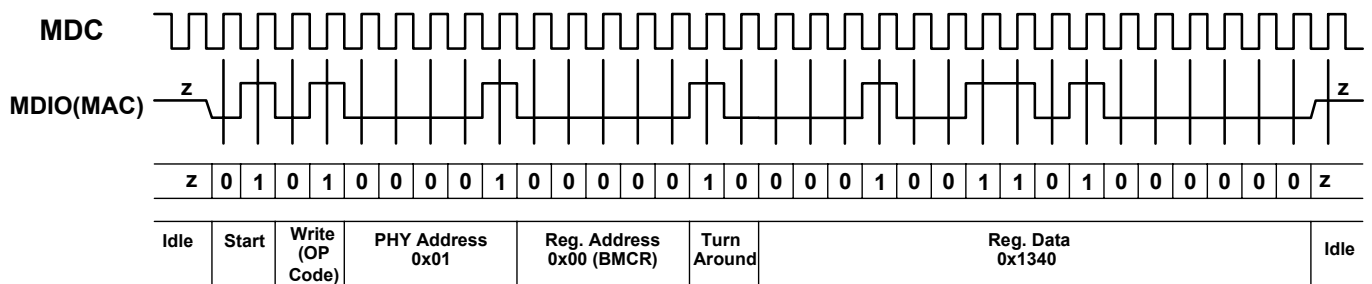


Figure 14. Typical MDC/MDIO Write Timing

6.10.6. Access to Extension Page (ExtPage)

Set MDIO commands as shown below to switch to the Extension Page (ExtPage) 0xXY (in Hex).

1. Set Register 31 Data=0x0007 (set to Extension Page)
2. Set Register 31 Data=0x00XY (Extension Page XY)
3. Set the target Register Data
4. Set Register 31 Data=0x0000 (switch to Page 0)

6.10.7. Access to MDIO Manageable Device (MMD)

The MDIO Manageable Device (MMD) is an extension to the management interface that provides the ability to access more device registers while still retaining logical compatibility with the MDIO interface, defined in section 7.1 Page0 Register Mapping and Definitions, page 32. Access to MMD configuration is provided via Registers 13 and 14.

MMD Read/Write Operation

1. Write Function field to 00 (address mode) and DEVAD field to the device address value for the desired MMD (Register 13).

2. Write the desired address value to the MMD's address register (Register 14).
3. Write Function field to 01 (data mode; no post increment) and DEVAD field to the same device address for the desired MMD (Register 13).
4. Read: Go to step 5. Write: Go to step 6.
5. Read the content of the selected register in MMD (Register 14).
6. Write the content of the selected register in MMD (Register 14).

6.11. Auto-Negotiation

Auto-Negotiation is a mechanism to determine the fastest connection between two link partners. For copper media applications, it was introduced in IEEE 802.3u for Ethernet and Fast Ethernet, and then in IEEE 802.3ab to address extended functions for Gigabit Ethernet. It performs the following:

- Auto-Negotiation Priority Resolution
- Auto-Negotiation Master/Slave Resolution
- Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution
- Crossover Detection & Auto-Correction Resolution

Upon de-assertion of a hardware reset, the RTL8211D can be configured to have auto-negotiation enabled, or be forced to operate in 10Base-T, 100Base-TX, or 1000Base-T mode via the CONFIG pins (see section 6.7 Hardware Configuration, page 17). If the RTL8211D is configured to operate only in 1000Base-T mode, then auto-negotiation is still enabled with only 1000Base-T mode advertised.

The auto-negotiation process is initiated automatically upon any of the following:

- Power-up
- Hardware reset
- Software reset (register 0.15)
- Restart auto-negotiation (register 0.9)
- Transition from power down to power up (register 0.11)
- Entering the link fail state

Table 17. 1000Base-T and Next Pages Bit Assignments

Bit	Name	Bit Description	Register Location
Base Page			
D15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	-
D14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	-
D13	RF	Remote Fault. 1: Indicates to its link partner that a device has encountered a fault condition	-
D[12:5]	A[7:0]	Technology Ability Field. Indicates to its link partner the supported technologies specific to the selector field value.	Register 4.[12:5] Table 28, page 37.
D[4:0]	S[4:0]	Selector Field. Always 00001. Indicates to its link partner that it is an IEEE Std 802.3 device.	Register 4.[4:0] Table 28, page 37.
PAGE 0 (Message Next Page)			
M15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	-
M14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	-
M13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page	-
M12	Ack2	Acknowledge 2. 1: Indicates to its link partner that a device has the ability to comply with the message	-
M11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	-
M[10:0]	-	1000Base-T Message Code. Always 8.	-
PAGE 1 (Unformatted Next Page)			
U15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	-
U14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	-
U13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page	-

Bit	Name	Bit Description	Register Location
U12	Ack2	Acknowledge 2. 1: Indicates to its link partner that a device has the ability to comply with the message	-
U11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	-
U[10:5]	-	Reserved. Transmit as 0	-
U4	-	1000Base-T Half Duplex. 1: Half duplex 0: No half duplex	Register 9.8 (GBCR) Table 33, page 39.
U3	-	1000Base-T Full Duplex. 1: Full duplex 0: No full duplex	Register 9.8 (GBCR) Table 33, page 39.
U2	-	1000Base-T Port Type Bit. 1: Multi-port device 0: Single-port device	Register 9.8 (GBCR) Table 33, page 39.
U1	-	1000Base-T Master-Slave Manual Configuration Value. 1: Master 0: Slave This bit is ignored if bit 9.12=0	Register 9.8 (GBCR) Table 33, page 39.
U0	-	1000Base-T Master-Slave Manual Configuration Enable. 1: Manual Configuration Enable This bit is intended to be used for manual selection in Master-Slave mode, and is to be used in conjunction with bit 9.11	Register 9.8 (GBCR) Table 33, page 39.
PAGE 2 (Unformatted Next Page)			
U15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	-
U14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	-
U13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page.	-
U12	Ack2	Acknowledge 2. 1: Indicates to its link partner that a device has the ability to comply with the message	-
U11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	-
U[10:0]	-	1000Base-T Master-Slave Seed Bit[10:0]	Master-Slave Seed Value SB[10:0]

6.11.1. Auto-Negotiation Priority Resolution

Upon the start of auto-negotiation, to advertise its capabilities each station transmits a 16-bit packet called a Link Code Word (LCW), within a burst of 17 to 33 Fast Link Pulses (FLP). A device capable of auto-negotiation transmits and receives the FLPs. The receiver must identify three identical LCWs before the information is authenticated and used in the arbitration process. The devices decode the base LCW and select capabilities with the highest common denominator supported by both devices.

To advertise 1000Base-T capability, both link partners, sharing the same link medium, should engage in Next Page (1000Base-T Message Page, Unformatted Page 1, and Unformatted Page 2) exchange.

Auto-negotiation ensures that the highest priority protocol will be selected as the link speed based on the following priorities advertised through the Link Code Word (LCW) exchange. Refer to IEEE 802.3 Clause 28 for detailed information.

1. 1000Base-T Full Duplex (highest priority)
2. 1000Base-T Half Duplex
3. 100Base-Tx Full Duplex
4. 100Base-Tx Half Duplex
5. 10Base-T Full Duplex
6. 10Base-T Half Duplex (lowest priority)

6.11.2. Auto-Negotiation Master/Slave Resolution

To establish a valid 1000Base-T link, the Master/Slave mode of both link partners should be resolved through the auto-negotiation process:

- Master Priority:
 - ◆ Multi-port > Single port
 - ◆ Manual > Non-manual
- Determination of Master/Slave configuration from LCW:
 - ◆ Manual_MASTER=U0*U1
 - ◆ Manual_SLAVE=U0*!U1
 - ◆ Single-port device=!U0*!U2

- ◆ Multi-port device= $!U0*U2$
Where: U0 is bit 0 of the Unformatted Page 1
U1 is bit 1 of the Unformatted Page 1
U2 is bit 2 of the Unformatted Page 1
- Where there are two stations with the same configuration, the one with higher Master-Slave seed SB[10:0] in the unformatted page 2 shall become Master.
- Master-Slave configuration process resolution:
 - ◆ Successful: Bit 10.15 Master-Slave Configuration Fault is set to logical 0, and bit 10.14 is set to logical 1 for Master resolution, or set to logical 0 for Slave resolution.
 - ◆ Unsuccessful: Auto-Negotiation restarts.
 - ◆ Fault detect: Bit 10.15 is set to logical 1 to indicate that a configuration fault has been detected. Auto-Negotiation restarts automatically. This happens when both stations are set to manual Master mode or manual Slave mode, or after seven attempts to configure the Master-Slave relationship through the seed method has failed.

6.11.3. Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution

Auto-negotiation is also used to determine the flow control capability between link partners. Flow control is a mechanism that can force a busy transmitting link partner to stop transmitting in a full duplex environment by sending special MAC control frames. In IEEE 802.3u, a PAUSE control frame had already been defined. However, in IEEE 802.3ab, a new ASY-PAUSE control frame was defined; if the MAC can only generate PAUSE frames but is not able to respond to PAUSE frames generated by the link partner, then it is called ASYMMETRIC PAUSE.

PAUSE/ASYMMETRIC PAUSE capability can be configured by setting the ANAR bits 10 and 11 (Table 28, page 37). Link partner PAUSE capabilities can be determined from ANLPAR bits 10 and 11 (Table 29, page 37). A PHY layer device such as the RTL8211D/DG/DN is not directly involved in PAUSE resolution, but simply advertises and reports PAUSE capabilities during the Auto-Negotiation process. The MAC is responsible for final PAUSE/ASYMMETRIC PAUSE resolution after a link is established, and is responsible for correct flow control actions thereafter.

6.12. Crossover Detection and Auto-Correction

Ethernet needs a crossover mechanism between both link partners to cross the transmit signal to the receiver when the medium is twisted-pair cable (e.g., CAT.3 or CAT.5 UTP). Crossover Detection & Auto-Correction Configuration eliminates the need for crossover cables between devices, such as two PC's connected to each other with a CAT.3 or CAT.5 Ethernet cable. The basic concept is to assume the initial default setting is MDI mode, and then check the link status. If no link is established after a certain time, change to MDI Crossover mode and repeat the process until a link is established. An 11-bit pseudo-random timer is applied to decide the mode change time interval.

Crossover Detection & Auto-Correction is not a part of the Auto-Negotiation process, but it utilizes the process to exchange MDI/MDI Crossover configuration. If the RTL8211D/DG/DN is configured to only operate in 100Base-TX or only in 10Base-T mode, then Auto-Negotiation is disabled only if the Crossover Detection & Auto-Correction function is also disabled. If Crossover Detection & Auto-Correction are enabled, then Auto-Negotiation is enabled and the RTL8211D/DG/DN advertises only 100Base-TX mode or 10Base-T mode. If the speed of operation is configured manually and Auto-Negotiation is still enabled because the Crossover Detection & Auto-Correction function is enabled, then the duplex advertised is as follows:

1. If CONFIG is set to half duplex, then only half duplex is advertised.
2. If CONFIG is set to full duplex, then both full and half duplex are advertised.

If the user wishes to advertise only full duplex at a particular speed with the Crossover Detection & Auto-Correction function enabled, then Auto-Negotiation should be enabled (register 0.12) with the appropriate advertising capabilities set in registers 4 or 9. The Crossover Detection & Auto-Correction function may be enabled/disabled by setting (register 16.6) manually.

After initial configuration following a hardware reset, Auto-Negotiation can be enabled and disabled via register 0.12, speed via registers 0.13, 0.6, and duplex via register 0.8. The abilities that are advertised can be changed via registers 4 and 9. Changes to registers 0.12, 0.13, 0.6, and 0.8 do not take effect unless at least one of the following events occurs:

- Software reset (register 0.15)
- Restart of Auto-Negotiation (register 0.9)
- Transition from power-down to power-up (register 0.11)

Registers 4 and 9 are internally latched once each time Auto-Negotiation enters the ABILITY DETECT state in the arbitration state machine (IEEE 802.3). Hence a write into register 4 or 9 has no effect once the RTL8211D/DG/DN begins to transmit Fast Link Pulses.

Register 7 is treated in a similar manner as 4 and 9 during additional Next Page exchanges. Once the RTL8211D/DG/DN completes Auto-Negotiation, it updates the various statuses in registers 1, 5, 6, and 10. The speed, duplex, page received, and Auto-Negotiation completed statuses are also available in registers 17 and 19.

6.13. LED Configuration

The RTL8211D and RTL8211DG support three LED pins, the RTL8211DN (with fiber mode LED3) supports four LED pins, suitable for multiple types of applications that can directly drive the LEDs. The output of these pins is determined by setting the corresponding bits in extension Page44 Register 28. The functionality of the RTL8211D/DG/DN LEDs is shown in Table 18.

Table 18. LED Default Definitions

Pin	Description
LED0	Blinking=Transmitting or Receiving
LED1	Low=Link Up (Any speed) High=Link Down (Any speed)
LED2	Low=Link Up (Any speed) High=Link Down (Any speed) Blinking=Transmitting or Receiving
LED3	Low=Link Up (Fiber mode) High=Link Down (Fiber mode) Blinking=Transmitting or Receiving (Fiber mode)

Note: When in EEE mode, blinking duration is 400ms ON and 2 seconds OFF.

The RTL8211D/DG/DN LED pins can be customized from extension Page44 Register 28 and Register 26. To change the register page, see note (below) and Table 19. There are 24 configuration types (see Table 20, page 30).

Note: To switch to extension Page44, set Register 31 Data=0x0007 (set to extension page). Set Register 30 Data=0x002c (extension Page44). After LED setting, switch to PHY's Page0 (Register 31 Data=0000).

Table 19. LED Register Table

	LINK Speed				Active (Tx/Rx)
	10Mbps	100Mbps	1000Mbps	Fiber	
LED0	Reg28 Bit0	Reg28 Bit1	Reg28 Bit2	Reg28 Bit3	Reg26 Bit4
LED1	Reg28 Bit4	Reg28 Bit5	Reg28 Bit6	Reg28 Bit7	Reg26 Bit5
LED2	Reg28 Bit8	Reg28 Bit9	Reg28 Bit10	Reg28 Bit11	Reg26 Bit6
LED3	Reg28 Bit12	Reg28 Bit13	Reg28 Bit14	Reg28 Bit15	Reg26 Bit7

Table 20. LED Configuration Table

Pin	LINK Bit				Active (Tx/Rx) Bit	Description
	10	100	1000	Fiber		
LED	0	0	0	0	0	N/A (LED Always Dark)
	0	0	0	0	1	Active
	1	0	0	0	0	Link 10
	1	0	0	0	1	Link 10+Active
	0	1	0	0	0	Link 100
	0	1	0	0	1	Link 100+Active
	1	1	0	0	0	Link 10/100
	1	1	0	0	1	Link 100/100+Active
	0	0	1	0	0	Link 1000
	0	0	1	0	1	Link 1000+Active
	1	0	1	0	0	Link 10/1000
	1	0	1	0	1	Link 10/1000+Active
	0	1	1	0	0	Link 100/1000
	0	1	1	0	1	Link 100/1000+Active
	1	1	1	0	0	Link 10/100/1000
	1	1	1	0	1	Link 10/100/1000+Active
	0	0	0	1	1	Fiber Active
	0	0	0	1	0	N/A (LED Always Dark)
	1	0	0	1	1	Fiber Link/Fiber Active
	1	0	0	1	0	Fiber Link
	0	1	0	1	0	Fiber Link
	0	1	0	1	1	Fiber Link/Fiber TX
	1	1	0	1	0	Fiber Link
	1	1	0	1	1	Fiber Link/Fiber RX

6.14. Polarity Correction

The RTL8211D/DG/DN automatically corrects polarity errors on the receive pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode polarity is irrelevant. In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock. In 10Base-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

6.15. Power

The RTL8211D/DG/DN implements a switching regulator to generate operating power. The system vendor needs to supply a 3.3V, 1A steady power source. The RTL8211D/DG/DN converts the 3.3V steady power source to 1.05V via a switching regulator.

Another possible implementation is to use an external regulator to generate 1.0V. Be sure that the regulator meets the required current rate.

The RTL8211D/DG/DN implements an option for the (R)GMII power pins. The standard I/O voltage of the (R)GMII interface is 3.3V, with support for 2.5V to lower EMI. The 2.5V power source for (R)GMII is from an external regulator.

7. Register Descriptions

7.1. Page0 Register Mapping and Definitions

Table 21. Page0 Register Mapping and Definitions

Offset	Access	Name	Description
0	RW	BMCR	Basic Mode Control Register.
1	RO	BMSR	Basic Mode Status Register.
2	RO	PHYID1	PHY Identifier Register 1.
3	RO	PHYID2	PHY Identifier Register 2.
4	RW	ANAR	Auto-Negotiation Advertising Register.
5	RW	ANLPAR	Auto-Negotiation Link Partner Ability Register.
6	RW	ANER	Auto-Negotiation Expansion Register.
7	RW	ANNPTR	Auto-Negotiation Next Page Transmit Register.
8	RW	ANNPRR	Auto-Negotiation Next Page Receive Register.
9	RW	GBCR	1000Base-T Control Register.
10	RO	GBSR	1000Base-T Status Register.
11~12	RW	RSVD	Reserved.
13	WO	MACR	MMD Access Control Register.
14	RW	MAADR	MMD Access Address Data Register.
15	RO	GBESR	1000Base-T Extended Status Register.
16	RW	PHYCR	PHY Specific Control Register.
17	RO	PHYSR	PHY Specific Status Register.
18	RW	INER	Interrupt Enable Register.
19	RO	INSR	Interrupt Status Register.
24	RO	RXERC	Receive Error Counter.
25~30	RW	RSVD	Reserved.
31	RW	PAGSEL	Page Select Register.

Note: To switch to extension Page44, set Register 31 Data=0x0007 (set to extension page). Set Register 30 Data=0x002c (extension Page44). After setting, switch to PHY's Page0 (Register 31 Data=0000).

7.2. Extension Page Register Mapping and Definition

Table 22. Extension Page Register Mapping and Definition

ExtPage	Offset	Access	Name	Description
140	22	RW	SDSR	SerDes Register.

7.3. MMD Register Mapping and Definition

Table 23. MMD Register Mapping and Definition

Device	Offset	Access	Name	Description
3	0	RW	PC1R	PCS Control 1 Register
3	1	RW	PS1R	PCS Status 1 Register
3	20	RO	EEECR	EEE Capability Register
3	22	RC	EEEWER	EEE Wake Error Register
7	60	RW	EEEAR	EEE Advertisement Register
7	61	RO	EEELPAR	EEE Link Partner Ability Register

7.4. Register Table

7.4.1. BMCR (Basic Mode Control Register, Address 0x00)

Table 24. BMCR (Basic Mode Control Register, Address 0x00)

Bit	Name	RW	Default	Description															
0.15	Reset	RW, SC ¹	0	Reset. 1: PHY reset 0: Normal operation															
0.14	Loopback	RW	0	Loopback Mode for 10M & 100M. 1: Enable loopback mode 0: Disable loopback mode The loopback function enables MII transmit data to be routed to the MII receive data path.															
0.13	Speed[0]	RW	0	Speed Select Bit 0. In forced mode, i.e., when Auto-Negotiation is disabled, bits 6 and 13 determine device speed selection. <table border="1" data-bbox="683 1290 1425 1480"> <thead> <tr> <th>Speed[1]</th> <th>Speed[0]</th> <th>Speed Enabled</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>0</td> <td>1</td> <td>100Mbps</td> </tr> <tr> <td>0</td> <td>0</td> <td>10Mbps</td> </tr> </tbody> </table>	Speed[1]	Speed[0]	Speed Enabled	1	1	Reserved	1	0	Reserved	0	1	100Mbps	0	0	10Mbps
Speed[1]	Speed[0]	Speed Enabled																	
1	1	Reserved																	
1	0	Reserved																	
0	1	100Mbps																	
0	0	10Mbps																	
0.12	ANE	RW	1	Auto-Negotiation Enable Bit. 1: Enable Auto-Negotiation 0: Disable Auto-Negotiation															
0.11	PWD	RW	0	Power Down Analog Block. 1: Power down (only Management Interface and logic active, link is down) 0: Normal operation															

Bit	Name	RW	Default	Description
0.10	Isolate	RW	0	Isolate. 1: RGMII/GMII interface is isolated; the serial management interface (MDC, MDIO) is still active. When this bit is asserted, the RTL8211D/DG/DN ignores TXD[7:0], and TXCLT inputs, and presents a high impedance on TXC, RXC, RXCLT, RXD[7:0]. 0: Normal operation
0.9	Restart_AN	RW, SC	0	Restart Auto-Negotiation. 1: Restart Auto-Negotiation 0: Normal operation
0.8	Duplex	RW	1	Duplex Mode. 1: Full Duplex operation 0: Half Duplex operation This bit is valid only in force mode, i.e., NWay is disabled.
0.7	Collision Test	RW	0	Collision Test. 1: Collision test enabled 0: Normal operation When set, this bit will cause the COL signal to be asserted in response to the assertion of TXEN within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the de-assertion of TXEN.
0.6	Speed[1]	RW	1	Speed Select bit 1. Refer to bit 0.13.
0.5:0	RSVD	RO	000000	Reserved.

Note 1: SC: Self-cleared

Note 2: The power-on duplex, speed, and ANE values take on the values set by external pins AN[3:0] on hardware reset only. A write to these registers has no effect unless any one of the following also occurs: Software reset (0.15) is asserted, Restart_AN (0.9) is asserted, or PWD (0.11) transitions from power down to normal operation.

Note 3: When the RTL8211D/DG/DN is switched from power down to normal operation, a software reset and restart auto-negotiation are performed even if bits Reset (0.15) and Restart_AN (0.9) are not set by the user.

Note 4: Auto-Negotiation is enabled when speed is set to 1000Base-T. Crossover Detection & Auto-Correction takes precedence over Auto-Negotiation disable (0.12=0). If ANE is disabled, speed and duplex capabilities are advertised by 0.13, 0.6, and 0.8. Otherwise, register 4.8:5 and 9.9:8 take effect.

Note 5: Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set.

7.4.2. BMSR (Basic Mode Status Register, Address 0x01)

Table 25. BMSR (Basic Mode Status Register, Address 0x01)

Bit	Name	RW	Default	Description
1.15	100Base-T4	RO	0	100Base-T4 Capability. The RTL8211D/DG/DN does not support 100Base-T4 mode. This bit should always be 0.
1.14	100Base-TX (Full)	RO	1	100Base-TX Full Duplex Capability. 1: Device is able to perform 100Base-TX in full duplex mode 0: Device is not able to perform 100Base-TX in full duplex mode
1.13	100Base-TX (Half)	RO	1	100Base-TX Half Duplex Capability. 1: Device is able to perform 100Base-TX in half duplex mode 0: Device is not able to perform 100Base-TX in half duplex mode
1.12	10Base-T (Full)	RO	1	10Base-T Full Duplex Capability. 1: Device is able to perform 10Base-T in full duplex mode. 0: Device is not able to perform 10Base-T in full duplex mode.
1.11	10Base-T (Half)	RO	1	10Base-T Half Duplex Capability. 1: Device is able to perform 10Base-T in half duplex mode 0: Device is not able to perform 10Base-T in half duplex mode
1.10	100Base-T2 (Full)	RO	0	100Base-T2 Full Duplex Capability. The RTL8211D/DG/DN does not support 100Base-T2 mode and this bit should always be 0.
1.9	100Base-T2 (Half)	RO	0	100Base-T2 Half Duplex Capability. The RTL8211D/DG/DN does not support 100Base-T2 mode. This bit should always be 0.
1.8	1000Base-T Extended Status	RO	1	1000Base-T Extended Status Register. 1: Device supports Extended Status Register 0x0F (15) 0: Device does not support Extended Status Register 0x0F This register is read-only and is always set to 1.
1.7	RSVD	RO	0	Reserved.
1.6	Preamble Suppression	RO	1	Preamble Suppression Capability (Permanently On). The RTL8211D/DG/DN always accepts transactions with preamble suppressed.
1.5	Auto-Negotiation Complete	RO	0	Auto-Negotiation Complete. 1: Auto-Negotiation process complete, and contents of registers 5, 6, 8, and 10 are valid 0: Auto-Negotiation process not complete
1.4	Remote Fault	RC*	0	Remote Fault. 1: Remote fault condition detected (cleared on read or by reset). Indication or notification of remote fault from Link Partner 0: No remote fault condition detected
1.3	Auto-Negotiation Ability	RO	1	Auto Configured Link. 1: Device is able to perform Auto-Negotiation 0: Device is not able to perform Auto-Negotiation

Bit	Name	RW	Default	Description
1.2	Link Status	RO	0	Link Status. 1: Linked 0: Not Linked This register indicates whether the link was lost since the last read. For the current link status, either read this register twice or read register bit 17.10 Link Real Time.
1.1	Jabber Detect	RC	0	Jabber Detect. 1: Jabber condition detected 0: No Jabber occurred
1.0	Extended Capability	RO	1	1: Extended register capabilities, always 1

Note: RC: Read-cleared after read.

7.4.3. PHYID1 (PHY Identifier Register 1, Address 0x02)

Table 26. PHYID1 (PHY Identifier Register 1, Address 0x02)

Bit	Name	RW	Default	Description
2.15:0	OUI_MSB	RO	0000000000011100	Organizationally Unique Identifier Bit 3:18. Always 0000000000011100.

Note: Realtek OUI is 0x000732.

7.4.4. PHYID2 (PHY Identifier Register 2, Address 0x03)

Table 27. PHYID2 (PHY Identifier Register 2, Address 0x03)

Bit	Name	RW	Default	Description
3.15:10	OUI_LSB	RO	110010	Organizationally Unique Identifier Bit 19:24. Always 110010.
3.9:4	Model Number	RO	010001	Manufacture's Model Number
3.3:0	Revision Number	RO	0100	Revision Number

7.4.5. ANAR (Auto-Negotiation Advertising Register, Address 0x04)

Table 28. ANAR (Auto-Negotiation Advertising Register, Address 0x04)

Bit	Name	RW	Default	Description
4.15	NextPage	RW	0	1: Additional next pages exchange desired 0: No additional next pages exchange desired
4.14	RSVD	RO	0	Reserved.
4.13	Remote Fault	RW	0	1: Set Remote Fault bit 0: No remote fault detected
4.12	RSVD	RO	0	Reserved.
4.11	Asymmetric PAUSE	RW	0	1: Advertise support for asymmetric pause 0: No support for asymmetric pause
4.10	PAUSE	RW	0	1: Advertise support of pause frames 0: No support of pause frames
4.9	100Base-T4	RO	1	1: 100Base-T4 support 0: 100Base-T4 not supported
4.8	100Base-TX (Full)	RW	1	1: Advertise support of 100Base-TX full-duplex mode 0: Not advertised
4.7	100Base-TX (Half)	RW	1	1: Advertise support of 100Base-TX half-duplex mode 0: Not advertised
4.6	10Base-T (Full)	RW	1	1: Advertise support of 10Base-TX full-duplex mode 0: Not advertised
4.5	10Base-T (Half)	RW	1	1: Advertise support of 10Base-TX full-duplex mode 0: Not advertised
4.4:0	Selector Field	RO	00001	Indicates the RTL8211D/DG/DN supports IEEE 802.3

Note 1: The setting of Register 4 has no effect unless NWay is restarted or the link goes down.

Note 2: If 1000Base-T is advertised, then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed.

7.4.6. ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)

Table 29. ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)

Bit	Name	RW	Default	Description
5.15	Next Page	RO	0	Next Page Indication. Received Code Word Bit 15.
5.14	ACK	RO	0	Acknowledge. Received Code Word Bit 14.
5.13	Remote Fault	RO	0	Remote Fault indicated by Link Partner. Received Code Word Bit 13.
5.12:5	Technology Ability Field	RO	00000000	Received Code Word Bit 12:5.
5.4:0	Selector Field	RO	00000	Received Code Word Bit 4:0.

Note: Register 5 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

7.4.7. ANER (Auto-Negotiation Expansion Register, Address 0x06)

Table 30. ANER (Auto-Negotiation Expansion Register, Address 0x06)

Bit	Name	RW	Default	Description
6.15:5	RSVD	RO	0x000	Reserved.
6.4	Parallel Detection Fault	RC	0	1: A fault has been detected via the Parallel Detection function 0: A fault has not been detected via the Parallel Detection function
6.3	Link Partner Next Pageable	RO	0	1: Link Partner supports Next Page exchange 0: Link Partner does not support Next Page exchange
6.2	Local Next Pageable	RO	1	1: Local Device is able to send Next Page Always 1.
6.1	Page Received	RC	0	1: A New Page (new LCW) has been received 0: A New Page has not been received
6.0	Link Partner Auto-Negotiation Capable	RO	0	1: Link Partner supports Auto-Negotiation 0: Link Partner does not support Auto-Negotiation

Note: Register 6 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

7.4.8. ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)

Table 31. ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)

Bit	Name	RW	Default	Description
7.15	Next Page	RW	0	Next Page Indication. 0: No more next pages to send 1: More next pages to send Transmit Code Word Bit 15.
7.14	RSVD	RO	0	Transmit Code Word Bit 14.
7.13	Message Page	RW	1	Message Page. 0: Unformatted Page 1: Message Page Transmit Code Word Bit 13.
7.12	Acknowledge 2	RW	0	Acknowledge2. 0: Local device has no ability to comply with the message received 1: Local device has the ability to comply with the message received Transmit Code Word Bit 12.
7.11	Toggle	RO	0	Toggle Bit. Transmit Code Word Bit 11.
7.10:0	Message/ Unformatted Field	RW	0x001	Content of Message/Unformatted Page. Transmit Code Word Bit 10:0.

7.4.9. ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08)

Table 32. ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08)

Bit	Name	RW	Default	Description
8.15	Next Page	RO	0	Received Link Code Word Bit 15.
8.14	Acknowledge	RO	0	Received Link Code Word Bit 14.
8.13	Message Page	RO	0	Received Link Code Word Bit 13.
8.12	Acknowledge 2	RO	0	Received Link Code Word Bit 12.
8.11	Toggle	RO	0	Received Link Code Word Bit 11.
8.10:0	Message/Unformatted Field	RO	0x00	Received Link Code Word Bit 10:0.

Note: Register 8 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

7.4.10. GBCR (1000Base-T Control Register, Address 0x09)

Table 33. GBCR (1000Base-T Control Register, Address 0x09)

Bit	Name	RW	Default	Description
9.15:13	Test Mode	RW	0	Test Mode Select. 000: Normal Mode 001: Test Mode 1 - Transmit Jitter Test 010: Test Mode 2 - Transmit Jitter Test (MASTER mode) 011: Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100: Test Mode 4 - Transmit Distortion Test 101, 110, 111: Reserved
9.12	MASTER/SLAVE Manual Configuration Enable	RW	0	Enable Manual Master/Slave Configuration. 1: Manual MASTER/SLAVE configuration 0: Automatic MASTER/SLAVE
9.11	MASTER/SLAVE Configuration Value	RW	0	Advertise Master/Slave Configuration Value. 1: Manual configuration as MASTER 0: Manual configuration as SLAVE
9.10	Port Type	RW	0	Advertise Device Type Preference. 1: Prefer multi-port device (MASTER) 0: Prefer single-port device (SLAVE)
9.9	1000Base-T Full Duplex	RW	1	Advertise 1000Base-T Full Duplex Capability. 1: Advertise 0: Do not advertise
9.8	1000Base-T Half Duplex	RW	1	Advertise 1000Base-T Half Duplex Capability. 1: Advertise 0: Do not advertise
9.7:0	RSVD	RO	0	Reserved.

Note 1: Values set in register 9.12:8 have no effect unless Auto-Negotiation is restarted (Reg0.9) or the link goes down.

Note 2: Bits 9.11 and 9.10 are ignored when bit 9.12=0.

7.4.11. GBSR (1000Base-T Status Register, Address 0x0A)

Table 34. GBSR (1000Base-T Status Register, Address 0x0A)

Bit	Name	RW	Default	Description
10.15	MASTER/SLAVE Configuration Fault	RO, RC	0	Master/Slave Manual Configuration Fault Detected. 1: MASTER/SLAVE configuration fault detected 0: No MASTER/SLAVE configuration fault detected
10.14	MASTER/SLAVE Configuration Resolution	RO	0	Master/Slave Configuration Result. 1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE
10.13	Local Receiver Status	RO	0	Local Receiver Status. 1: Local Receiver OK 0: Local Receiver Not OK
10.12	Remote Receiver Status	RO	0	Remote Receiver Status. 1: Remote Receiver OK 0: Remote Receiver Not OK
10.11	Link Partner 1000Base-T Full Duplex Capability	RO	0	Link Partner 1000Base-T Full Duplex Capability. 1: Link Partner is capable of 1000Base-T full duplex 0: Link Partner is not capable of 1000Base-T full duplex
10.10	Link Partner 1000Base-T Half Duplex Capability	RO	0	Link Partner 1000Base-T Half Duplex Capability. 1: Link Partner is capable of 1000Base-T half duplex 0: Link Partner is not capable of 1000Base-T half duplex
10.9:8	RSVD	RO	00	Reserved.
10.7:0	Idle Error Count	RO, RC	0x00	MSB of Idle Error Counter. The counter stops automatically when it reaches 0xff.

Note 1: Values set in register 10.11:10 are not valid until register 6.1 is set to 1.

Note 2: Register 10 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

7.4.12. MACR (MMD Access Control Register, Address 0x0D)

Table 35. MACR (MMD Access Control Register, Address 0x0D)

Bit	Name	RW	Default	Description
13.15:14	Function	WO	0	00: Address 01: Data with no post increment 10: Data with post increment on reads and writes 11: Data with post increment on writes only
13.13:5	RSVD	RO	00000000	Reserved.
13.4:0	DEVAD	WO	0	Device Address.

Note 1: This register is used in conjunction with the MAADR (Register 14) to provide access to the MMD address space.

Note 2: If the MAADR accesses for address (Function=00), then it is directed to the address register within the MMD associated with the value in the DEVAD field.

Note 3: If the MAADR accesses for data (Function≠00), both the DEVAD field and MMD's address register direct the MAADR data accesses to the appropriate registers within the MMD.

7.4.13. MAADR (MMD Access Address Data Register, Address 0x0E)

Table 36. MAADR (MMD Access Address Data Register, Address 0x0E)

Bit	Name	RW	Default	Description
14.15:0	Address Data	RW	0x0000	13.15:14 = 00 → MMD DEVAD's address register 13.15:14 = 01, 10, or 11 → MMD DEVAD's data register as indicated by the contents of its address register

Note: This register is used in conjunction with the MACR (Register 13) to provide access to the MMD address space.

7.4.14. GBESR (1000Base-T Extended Status Register, Address 0x0F)

Table 37. GBESR (1000Base-T Extended Status Register, Address 0x0F)

Bit	Name	RW	Default	Description
15.15	1000Base-X FD	RO	0	0: Not 1000Base-X full duplex capable
15.14	1000Base-X HD	RO	0	0: Not 1000Base-X half duplex capable
15.13	1000Base-T FD	RO	1	1: 1000Base-T full duplex capable
15.12	1000Base-T HD	RO	1	1: 1000Base-T half duplex capable
15.11:0	RSVD	RO	0x000	Reserved.

7.4.15. PHYCR (PHY Specific Control Register, Address 0x10)

Table 38. PHYCR (PHY Specific Control Register, Address 0x10)

Bit	Name	RW	Default	Description
16.15	Disable RXC	RW	0	Disable RXC Clock Output
16.14:12	Select FPR Fail	RW	000	Select Signal for 'LPRFAIL' (10M Link Pulse Receive Status).
16.11	Assert CRS on Transmit	RW	0	1: Assert CRS on transmit 0: Never assert CRS on transmit
16.10	Force Link Good	RW	0	1: Force link good 0: Normal operation
16.9:8	RSVD	RW	01	Reserved.
16.7	Select Hcc	RW	0	0'b0: Select RX10M RTL circuit 1'b1: Select RX10M gate-level circuit
16.6	Enable Crossover	RW	1	1: Enable Auto-crossover mechanism
16.5	MDI Mode	RW	1	Used to Determine MDI/MDIX Mode when Disable Auto-Crossover. 1: MDI mode 0: MDIX mode
16.4	Disable CLK125	RW	0	1: CLK125 remains at logic Low 0: CLK125 Toggling Enabled
16.3:1	RSVD	RW	111	Reserved.
16.0	Disable Jabber	RW	0	1: Disable jabber function 0: Enable jabber function

7.4.16. PHYSR (PHY Specific Status Register, Address 0x11)

Table 39. PHYSR (PHY Specific Status Register, Address 0x11)

Bit	Name	RW	Default	Description
17.15:14	Speed	RO	01	Link Speed. 11: Reserved 01: 100Mbps 10: 1000Mbps 00: 10Mbps
17.13	Duplex	RO	0	Full/Half Duplex Mode. 1: Full duplex 0: Half duplex
17.12	Page Received	RC	0	New Page Received. 1: Page received 0: Page not received
17.11	Speed and Duplex Resolved	RO	0	Speed and Duplex Mode Resolved. 1: Resolved 0: Not resolved
17.10	Link (Real Time)	RO	0	Real Time Link Status. 1: Link OK 0: Link not OK
17.9:7	RSVD	RO	000	Reserved.
17.6	MDI Crossover Status	RO	0	MDI/MDI Crossover Status. 1: MDI Crossover 0: MDI
17.5:1	RSVD	RW	01110	Reserved.
17.0	Jabber (Real Time)	RO	0	Real Time Jabber Indication. 1: Jabber Indication 0: No jabber Indication

7.4.17. INER (Interrupt Enable Register, Address 0x12)

Table 40. INER (Interrupt Enable Register, Address 0x12)

Bit	Name	RW	Default	Description
18.15	Auto-Negotiation Error Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.14	Speed Change Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.13	Duplex Mode Change Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.12	Page Received Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.11	Auto-Negotiation Completed Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.10	Link Status Change Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.9	Symbol Error Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.8	False Carrier Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.7	RSVD	RW	1	Reserved.
18.6	MDI Crossover Change Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.5:2	RSVD	RW	1	Reserved.
18.1	Polarity Change Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.0	Jabber Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable

7.4.18. INSR (Interrupt Status Register, Address 0x13)

Table 41. INSR (Interrupt Status Register, Address 0x13)

Bit	Name	RW	Default	Description
19.15	Auto-Negotiation Error	RC	0	1: Auto-Negotiation Error 0: No Auto-Negotiation Error
19.14	Speed Change	RC	0	1: Link speed changed 0: Link speed not changed
19.13	Duplex Mode Change	RC	0	1: Duplex mode changed 0: Duplex mode not changed
19.12	Page Received	RC	0	1: Page (a new LCW) received 0: Page not received
19.11	Auto-Negotiation Completed	RC	0	1: Auto-Negotiation completed 0: Auto-Negotiation not completed
19.10	Link Status Change	RC	0	1: Link status changed 0: Link status not changed
19.9	Symbol Error	RC	0	1: Symbol error detected 0: No symbol error detected
19.8	False Carrier	RC	0	1: False carrier 0: No false carrier detected
19.7	RSVD	RC	0	Reserved.
19.6	MDI Crossover Change	RC	0	1: Crossover status changed 0: Crossover status not changed
19.5:2	RSVD	RC	0000	Reserved.
19.1	Polarity Change	RC	0	1: Polarity Changed 0: Polarity not changed <i>Note: This bit is valid only when 1000Base-T is enabled.</i>
19.0	Jabber	RC	0	1: Jabber detected 0: No jabber detected

7.4.19. RXERC (Receive Error Counter, Address 0x18)

Table 42. RXERC (Receive Error Counter, Address 0x18)

Bit	Name	RW	Default	Description
24.15:0	Receive Error Count	RC	0x0000	Receive Error Count.

Note: The RXERC register is read-cleared after a read.

7.4.20. PAGSEL (Page Select Register, Address 0x1F)

Table 43. PAGSEL (Page Select Register, Address 0x1F)

Bit	Name	RW	Default	Description
31.15:3	RSVD	RW	0	Reserved.
31.2:0	Pagesel	RW	000	Page Select Signal. 000: Page 0 (default page) 001: Page 1 010: Page 2 011: Page 3 100: Page 4 101: Page 5 110: Page 6 111: Extension page

7.4.21. SDSR (SerDes Register, ExtPage 140, Address 0x16)

Table 44. SDSR (SerDes Register, ExtPage 140, Address 0x16)

Bit	Name	RW	Default	Description
22.13:12	MAC SerDes Speed	RW	0	Bridge Mode Speed Select for SGMII Mode (RTL8211DN Only). 00: 10Mbps 01: 100Mbps 10: 1000Mbps

7.4.22. PC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)

Table 45. PC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)

Bit	Name	RW	Default	Description
3.0.15:11	RSVD	RW	0	Reserved.
3.0.10	Clock Stop Enable	RW	0	1: PHY may stop RXC in LPI 0: RXC not stoppable
3.0.9:0	RSVD	RW	0	Reserved.

7.4.23. PS1R (PCS Status1 Register, MMD Device 3, Address 0x01)

Table 46. PS1R (PCS Status 1 Register, MMD Device 3, Address 0x01)

Bit	Name	RW	Default	Description
3.1.15:12	RSVD	RO	0	Reserved.
3.1.11	TX LPI received	RO, LH	0	1: TX PCS has received LPI 0: LPI not received
3.1.10	RX LPI received	RO, LH	0	1: RX PCS has received LPI 0: LPI not received
3.1.9	TX LPI indication	RO	0	1: TX PCS is currently receiving LPI 0: TX PCS is not currently receiving LPI
3.1.8	RX LPI indication	RO	0	1: RX PCS is currently receiving LPI 0: RX PCS is not currently receiving LPI
3.1.7:0	RSVD	RO	0	Reserved

7.4.24. EEECR (EEE Capability Register, MMD Device 3, Address 0x14)

Table 47. EEECR (EEE Capability Register, MMD Device 3, Address 0x14)

Bit	Name	RW	Default	Description
3.20.15:3	RSVD	RO	0	Reserved.
3.20.2	1000BASE-T EEE	RO	0	1: EEE is supported for 1000Base-T EEE 0: EEE is not supported for 1000Base-T EEE
3.20.1	100BASE-TX EEE	RO	0	1: EEE is supported for 100Base-TX EEE 0: EEE is not supported for 100Base-TX EEE
3.20.0	RSVD	RO	0	Reserved.

7.4.25. EEEWER (EEE Wake Error Register, MMD Device 3, Address 0x16)

Table 48. EEEWER (EEE Wake Error Register, MMD Device 3, Address 0x16)

Bit	Name	RW	Default	Description
3.22.15:0	EEE Wake Error Counter	RC	0	Used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type.

7.4.26. EEEAR (EEE Advertisement Register, MMD Device 7, Address 0x3c)

Table 49. EEEAR (EEE Advertisement Register, MMD Device 7, Address 0x3c)

Bit	Name	RW	Default	Description
7.60.15:3	RSVD	RW	0	Reserved.
7.60.2	1000BASE-T EEE	RW	1	Advertise 1000Base-T EEE Capability. 1: Advertise 0: Do not advertise
7.60.1	100BASE-TX EEE	RW	1	Advertise 100Base-TX EEE Capability. 1: Advertise 0: Do not advertise
7.60.0	RSVD	RW	0	Reserved.

7.4.27. EEELPAR (EEE Link Partner Ability Register, MMD Device 7, Address 0x3d)

Table 50. EEELPAR (EEE Link Partner Ability Register, MMD Device 7, Address 0x3d)

Bit	Name	RW	Default	Description
7.61.15:3	RSVD	RO	0	Reserved.
7.61.2	LP 1000BASE-T EEE	RO	0	1: Link Partner is capable of 1000Base-T EEE 0: Link Partner is not capable of 1000Base-T EEE
7.61.1	LP 100BASE-TX EEE	RO	0	1: Link Partner is capable of 100Base-TX EEE 0: Link Partner is not capable of 100Base-TX EEE
7.61.0	RSVD	RO	0	Reserved.

8. Switching Regulator

The RTL8211D/DG/DN incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. The 1.05V switching regulator output pin (REG_OUT) should be connected only to DVDD10 and AVDD10 (do not provide this power source to other devices).

8.1. PCB Layout

- The input 3.3V power trace connected to VDDREG must be wider than 40mils
- The bulk de-coupling capacitors (Cin1 and Cin2) must be placed within 200mils (0.5cm) of VDDREG to prevent input voltage overshoot
- The output power trace out of REG_OUT must be wider than 60mils
- Lx (4.7 μ H) must be kept within 200mils (0.5cm) of REGOUT
- Cout1 and Cout2 must be kept within 200mils (0.5cm) of Lx to ensure stable output power and better power efficiency
- For switching regulator stability, the capacitor Cout1 and Cout2 must be a ceramic (X5R) capacitor. Cin1 and Cin2 are recommended to be ceramic capacitors
- Place Lx and Cin1 on the same layer as the RTL8211D/DG/DN. Do not use vias on VDDREG and REG_OUT traces

Note: Violation of the above rules will damage the IC.

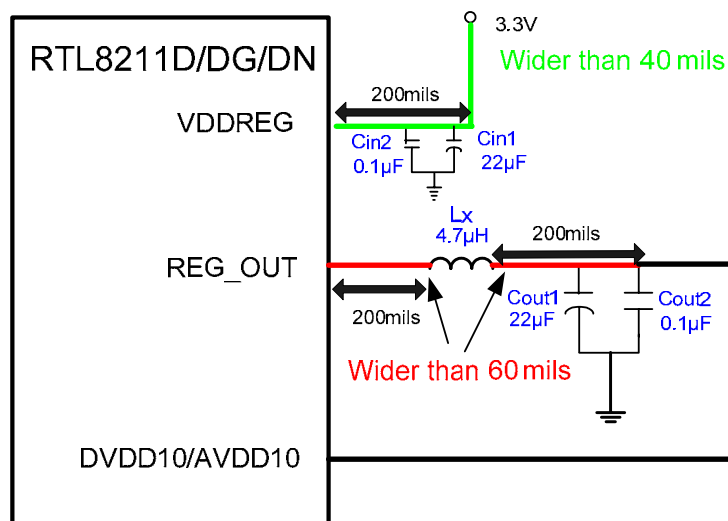


Figure 15. Switching Regulator

8.2. Inductor and Capacitor Parts List

Table 51. Inductor and Capacitor Parts List

Inductor Type	Inductance	ESR at 1MHz (mΩ)	Max I (mA)
4R7GTSD32	4.7μH	712	1100

Note 1: The ESR is equivalent to RDC or DCR. Lower ESR inductor values will promote a higher-efficiency switching regulator.

Note 2: The power inductor used by the switching regulator should be able to withstand 600mA of current.

Note 3: Typically, if the power inductor's ESR at 1MHz is below 0.8Ω, the switching regulator efficiency will be above 75%. However the actual switching regulator efficiency must be measured according to the method described in section 8.4 Efficiency Measurement, page 52.

Note 4: If the inductor does not meet this requirement, it may damage the switching regulator. Refer to the RTL8211D_DG_DN inductor Approved Vendor List (AVL) for details.

Capacitor Type	Capacitance	ESR at 1MHz (mΩ)
22μF 1210 X5R	22.15μF	24.90

Note: Cout1 and Cin1 must be X5R ceramic. Capacitors Cout2 and Cin2 are suggested to be ceramic, as lower ESR values will yield lower output voltage ripple.

8.3. Measurement Criteria

In order for the switching regulator to operate properly, the input and output voltage measurement criteria must be met. From the input side, the voltage overshoot cannot exceed 4V; otherwise the chip may be damaged. Note that the voltage signal must be measured directly at VDDREG, not at the capacitor. In order to reduce the input voltage overshoot, Cin1 and Cin2 must be placed close (< 200mils) to VDDREG. The following figures show what a good input voltage and a bad one look like.

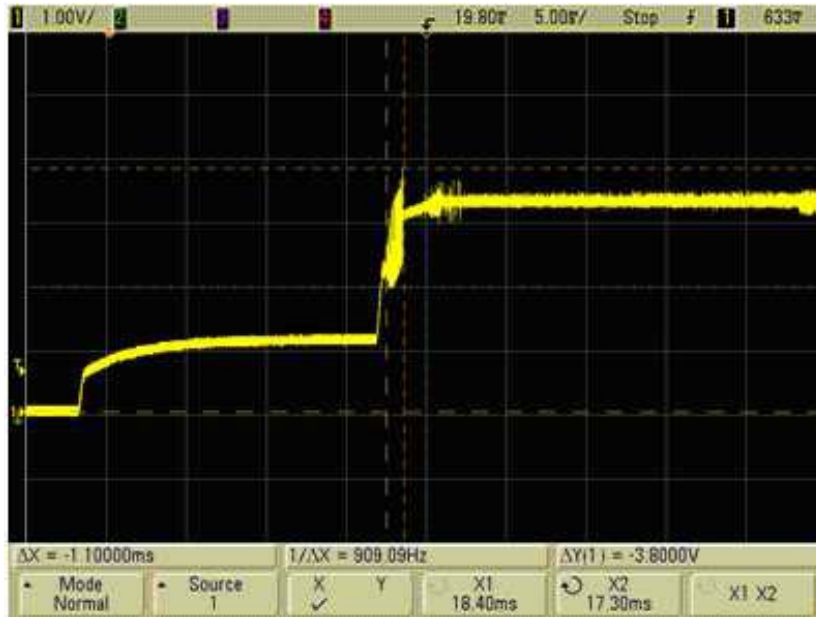


Figure 16. Input Voltage Overshoot <4V (Good)

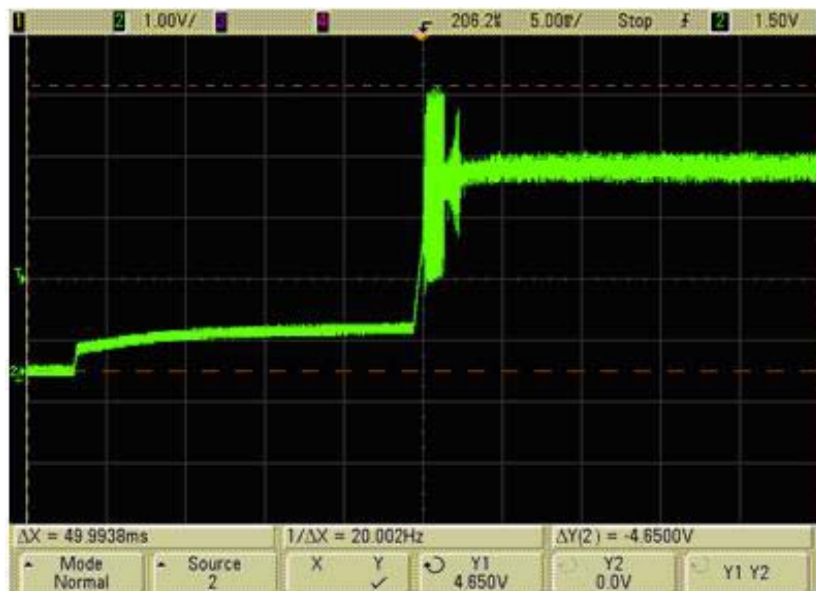


Figure 17. Input Voltage Overshoot >4V (Bad)

From the output side measured at REG_OUT, the voltage ripple must be within 100mV. Choosing different types and values of output capacitor (Cout1, Cout2) and power inductor (Lx) will seriously affect the efficiency and output voltage ripple of switching regulators. The following figures show the effects of different types of capacitors on the switching regulator's output voltage.

The blue square wave signal (top row) is measured at the output of REG_OUT before the power inductor (Lx). The yellow signal (second row) is measured after the power inductor (Lx), and shows there is a voltage ripple. The green signal (lower row) is the current. Data in the following figures was measured at 1000Mbps speed.



Figure 18. Ceramic 22 μ F 1210(X5R) (Good)

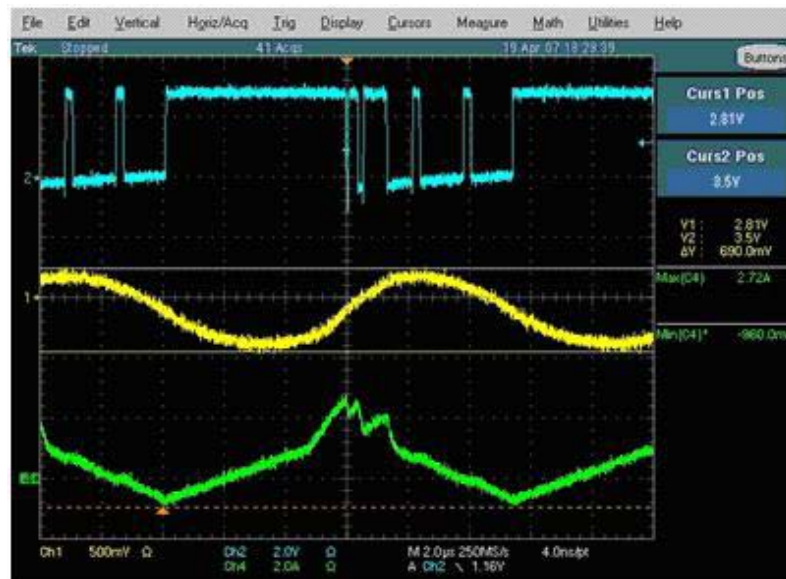


Figure 19. Ceramic 22 μ F 0805(Y5V) (Bad)

A ceramic 22 μ F (X5R) will have a lower voltage ripple compared to the electrolytic 100 μ F. The key to choosing a proper output capacitor is to choose the lowest ESR to reduce the output voltage ripple. Choosing a ceramic 22 μ F 0805 (Y5V) in this case will cause malfunction of the switching regulator.



Figure 20. Electrolytic 100 μ F (Ripple Too High)

The following figures show how different inductors affect the REG_OUT output waveform. The typical waveform should look like Figure 21, which has a square waveform with a dip at the falling edge and the rising edge. If the inductor is not carefully chosen, the waveform may look like Figure 22, where the waveform looks like a distorted square. This will cause insufficient current supply and will undermine the stability of the system at gigabit speed. Data in the following figures was measured at gigabit speed.

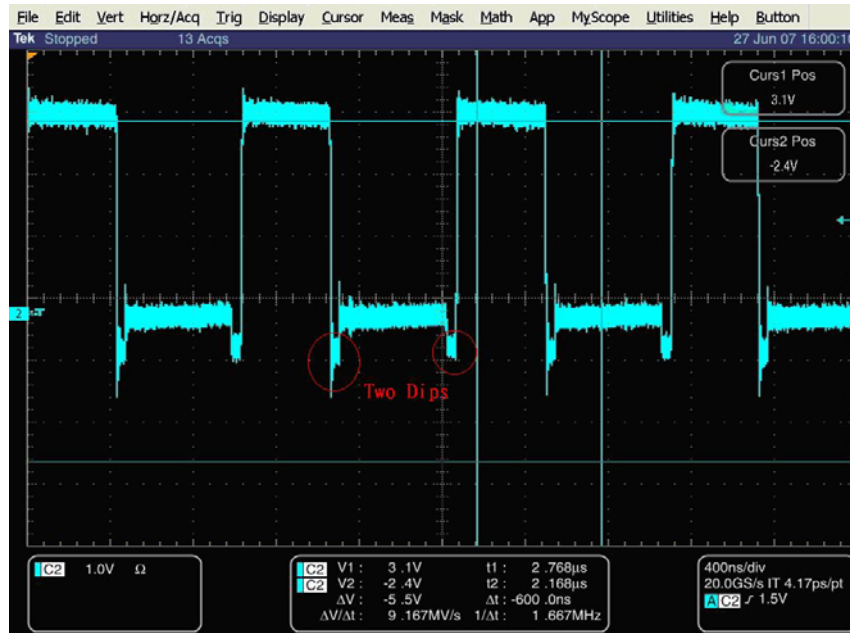


Figure 21. 4R7GTSD32 (Good)

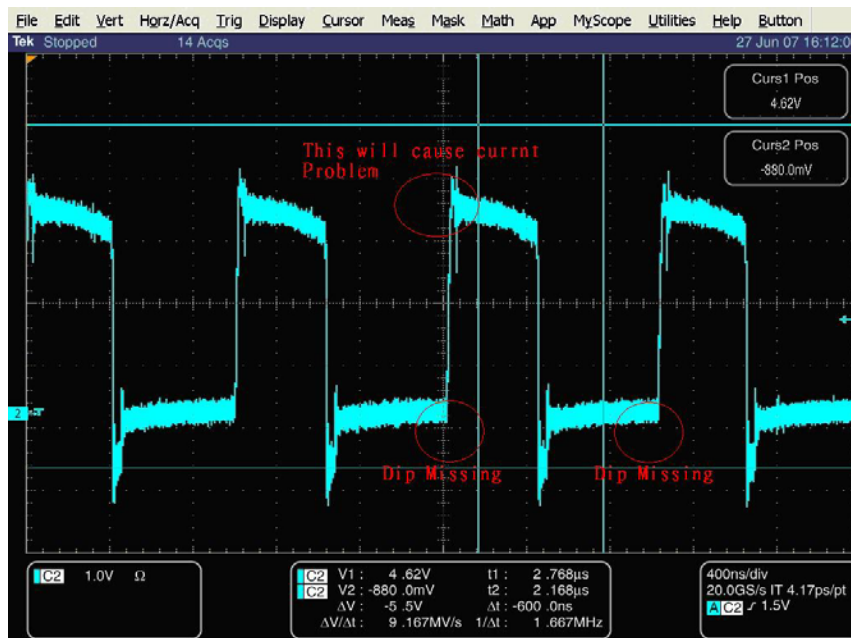


Figure 22. 1 μ H Bead (Bad)

8.4. Efficiency Measurement

The efficiency of the switching regulator is designed to be above 75% in gigabit traffic mode. It is very important to choose a suitable inductor before Gerber certification, as the Inductor ESR value will affect the efficiency of the switching regulator. An inductor with a lower ESR value will result in a higher-efficiency switching regulator.

The efficiency of the switching regulator is easily measured using the following method.

Figure 23 shows two checkpoints, checkpoint A (CP_A) and checkpoint B (CP_B). The switching regulator input current (I_{cpa}) should be measured at CP_A, and the switching regulator output current (I_{cpb}) should be measured at CP_B.

To determine efficiency, apply the following formula:

$$\text{Efficiency} = V_{cpb} \cdot I_{cpb} / V_{cpa} \cdot I_{cpa}$$

Where V_{cpb} is 1.05V; V_{cpa} is 3.3V. The measurements should be performed in gigabit traffic mode.

For example: The inductor used in the evaluation board is a GOTREND GTSD32-4R7M:

- The ESR value @ 1MHz is approximately 0.712ohm
- The measured I_{cpa} is 160mA at CP_A
- The measured I_{cpb} is 400mA at CP_B

These values are measured in gigabit traffic mode, so the efficiency of the GOTREND GTSD32-4R7M can be calculated as follows:

$$\text{Efficiency} = (1.05V \cdot 400mA) / (3.3V \cdot 160mA) = 0.80 = 80\%.$$

We strongly recommend that the efficiency should be measured when choosing an inductor for the switching regulator, and that the inductor should yield an efficiency rating higher than 75%. If the efficiency does not meet this requirement, there may be risk to the switching regulator reliability over the long term.

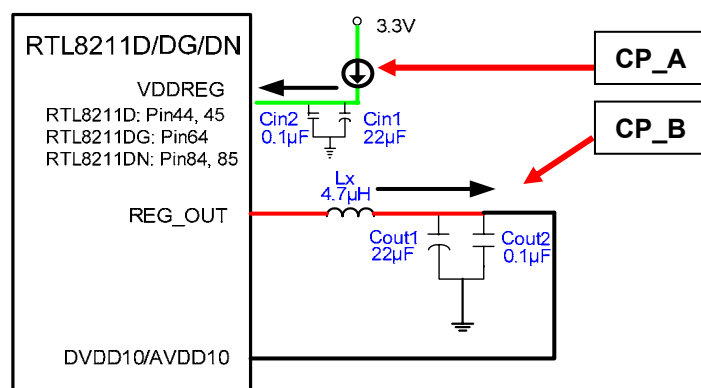


Figure 23. Switching Regulator Efficiency Measurement Checkpoint

8.5. Power Sequence

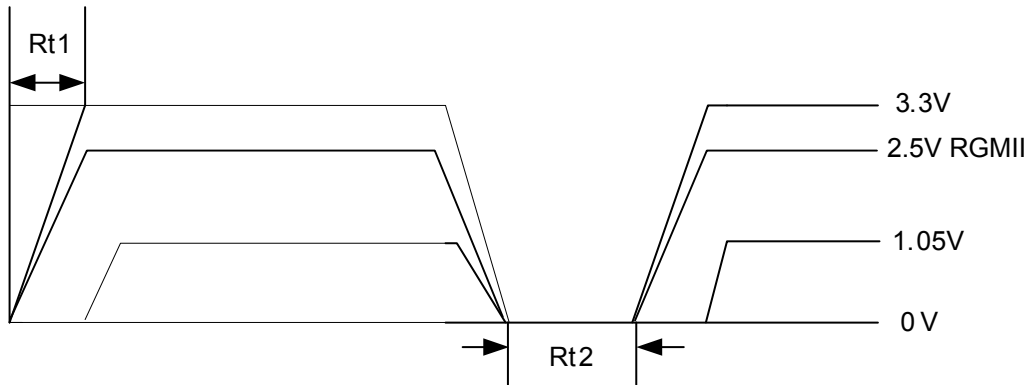


Figure 24. Power Sequence

Table 52. Power Sequence Parameter

Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	1	-	100	ms
Rt1	2.5V RGMII Rise Time	-	-	100	ms
Rt2	3.3V Off Time	200	-	-	ms

Note 1: The RTL8211D/DG/DN does not support fast 3.3V rising. The 3.3V rise time must be controlled over 1ms. If the rise time is too short, it will induce a peak voltage in VDDREG which may cause permanent damage to the switching regulator.

Note 2: If there is any action that involves consecutive ON/OFF toggling of the switching-regulator source (3.3V), the design must make sure the OFF state of both the switching-regulator source (3.3V) and output (1.05V) reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 200ms.

Note 3: The RTL8211D/DG/DN requires 500ms for power on reset, after which it can access the PHY register from MDC/MDIO. Refer to the power sequence application note for details.

9. Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 53. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
VDD33, AVDD33	Supply Voltage 3.3V	-0.4	3.7	V
AVDD10, DVDD10	Supply Voltage 1.05V	-0.1	1.26	V
VDD25 (RGMII 2.5V)	Supply Voltage 2.5V	-0.2	2.8	V
DCinput	Input Voltage	-0.5	Corresponding Supply Voltage + 0.5	V
DCoutput	Output Voltage	-0.3	Corresponding Supply Voltage + 0.5	V
NA	Storage Temperature	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

9.2. Recommended Operating Conditions

Table 54. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	DVDD33, AVDD33	2.97	3.3	3.63	V
	AVDD10, DVDD10	0.95	1.05	1.09	V
	2.5V GMII/RGMII	2.37	2.5	2.8	V
Ambient Operating Temperature T _A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

9.3. Crystal Requirements

Table 55. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F _{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F _{ref} Stability	Parallel Resonant Crystal Frequency Stability, Fundamental Mode, AT-Cut Type. T _a =0°C~70°C.	-30	-	+30	ppm
F _{ref} Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T _a =25°C.	-50	-	+50	ppm
F _{ref} Duty Cycle	Reference Clock Input Duty Cycle.	45	-	55	%
ESR	Equivalent Series Resistance.	-	-	30	Ω
DL	Drive Level.	-	-	0.5	mW
Jitter	Broadband Peak to Peak Jitter ^{1,2}		-	500	ps

Note 1: 25KHz to 25MHz RMS < 3ps.

Note 2: Broadband RMS < 9ps.

9.4. Oscillator Requirements

Table 56. Oscillator Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25	-	MHz
Frequency Stability	T _a = 0°C~70°C	-30	-	30	ppm
Frequency Tolerance	T _a = 25°C	-50	-	50	ppm
Duty Cycle	-	45	-	55	%
Broadband Peak to Peak Jitter ^{1,2}	-	-	-	500	ps
V _{p-p}	-	3.15	3.3	3.45	V
Rise Time (10%~90%)	-	-	-	10	ns
Fall Time (10%~90%)	-	-	-	10	ns
Operating Temperature Range	-	0	-	70	°C

Note 1: 25KHz to 25MHz RMS < 3ps.

Note 2: Broadband RMS < 9ps.

9.5. DC Characteristics

Table 57. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD33, AVDD33	3.3V Supply Voltage	-	2.97	3.3	3.63	V
RGMII I/O	2.5V GMII/RGMII Supply Voltage	-	2.37	2.5	2.8	V
DVDD10, AVDD10	1.05V Supply Voltage	-	0.98	1.05	1.09	V
Voh (3.3V)	Minimum High Level Output Voltage	-	0.9*VDD33	-	VDD33	V
Voh (2.5V)	Minimum High Level Output Voltage	-	0.9*VDD25	-	VDD25	V
Vol (3.3V)	Maximum Low Level Output Voltage	-	0	-	0.1*VDD33	V
Vol (2.5V)	Maximum Low Level Output Voltage	-	0	-	0.1*VDD25	V
Vih	Minimum High Level Input Voltage	-	1.8	-	-	V
Vil	Maximum Low Level Input Voltage	-	-	-	0.9	V
Iin	Input Current	Vin=VDD33 or GND	0	-	0.5	μA

9.5.1. SGMII DC Characteristics

Table 58. Differential Transmitter Output DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
V _{oh}	Output Voltage High	-	-	1000	mV
V _{ol}	Output Voltage Low	500	-	-	mV
V _{ring}	Output Ringing	-	-	10	%
V _{odl}	Output Differential Voltage	400	-	500	mV
V _{cm}	Output Offset Voltage	-	775	-	mV
R _o	Output Impedance (Single-End)	40	50	60	ohm
^R _o	Mismatch in a Pair	-	-	10	%
^ V _{odl}	Change in Vod between '0' and '1'	-	-	25	mV
^V _{od}	Change in Vos between '0' and '1'	-	-	25	mV
I _{sa} , I _{sb}	Output Current on Short to GND	-	-	40	mA
I _{sab}	Output Current when a/b are Shorted	-	-	12	mA
I _{xa} , I _{xb}	Power Off Leakage Current	-	-	10	mA

Table 59. Differential Receiver Input DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
V _i	Input Voltage Range	250	-	1000	mV
V _{idth}	Input Differential Threshold	-150	-	150	mV
V _{hyst}	Input Differential Hysteresis	25	-	-	mV
R _{in}	Receiver Differential Input Impedance	80	100	120	ohm

9.6. AC Characteristics

9.6.1. MDC/MDIO Timing

MDC/MDIO Timing – Management Port

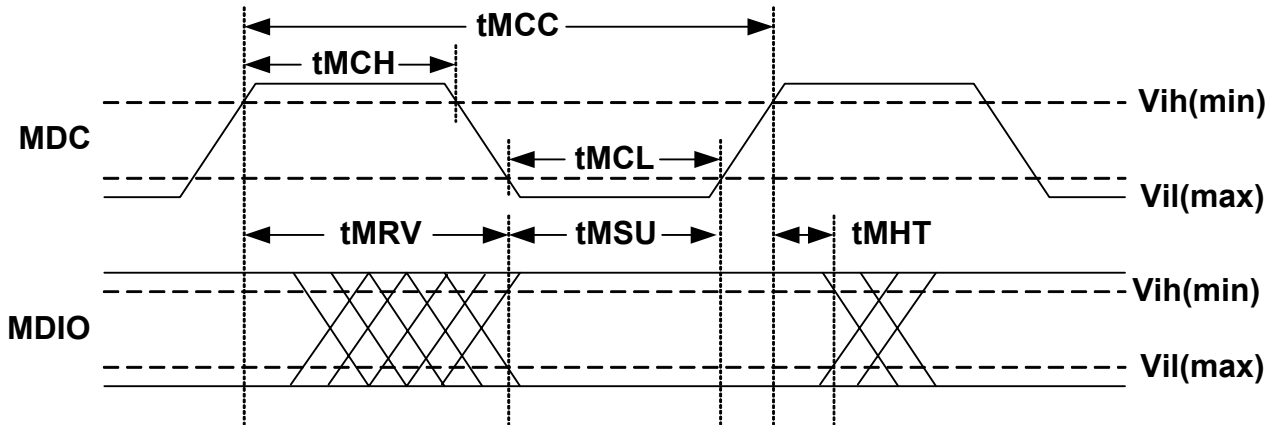


Figure 25. MDC/MDIO Management Timing Parameters

Table 60. MDC/MDIO Management Timing Parameters

Symbol	Description	Min	Max	Units
t_{MCC}	MDC Cycle Time	80	-	ns
t_{MCH}	MDC High Time	30	-	ns
t_{MCL}	MDC Low Time	30	-	ns
t_{MSU}	MDIO Setup Time	10	-	ns
t_{MHT}	MDIO Hold Time	10	-	ns
t_{MRV}	MDC Clock Rise to MDIO Valid	-	300	ns

9.6.2. MII Timing Modes

MII Timing – MII PORT – Transmit

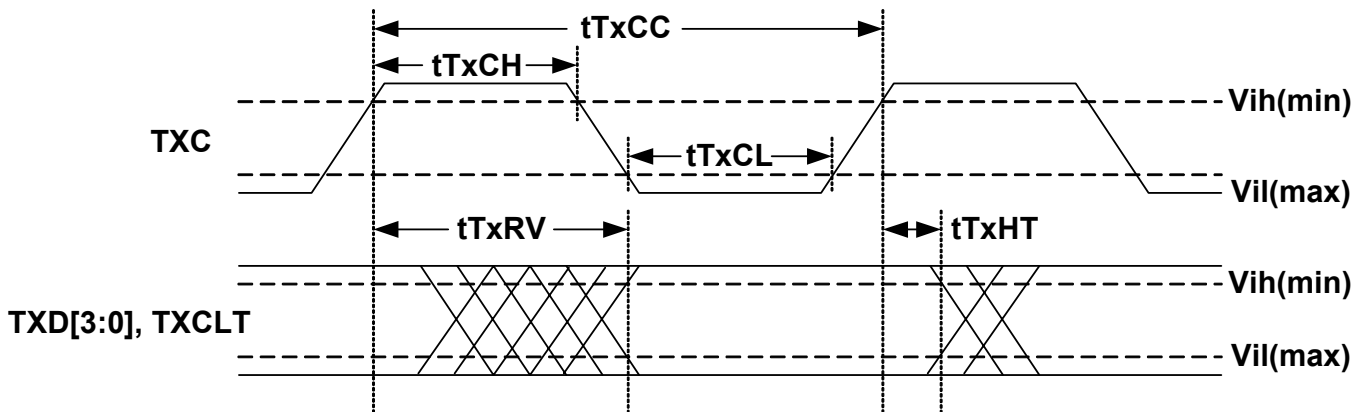
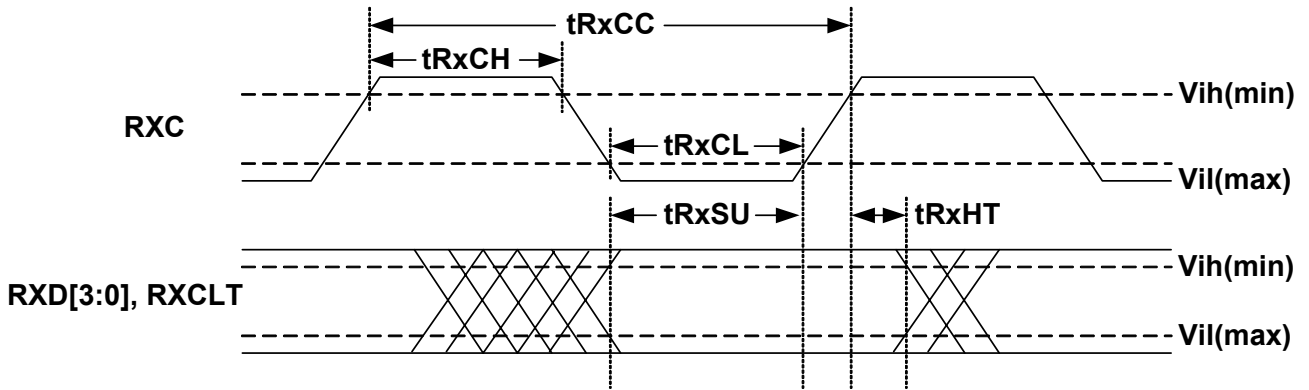


Figure 26. MII Timing – MII PORT – Transmit

Table 61. MII Transmit Timing Parameters

Symbol	Description	10MHz			100MHz			Units
		Min	Typical	Max	Min	Typical	Max	
t_{TxCC}	TX Clock Cycle	-	400	-	-	40	-	ns
t_{TxCH}	TX Clock High Time	140	-	260	14	-	26	ns
t_{TxCL}	TX Clock Low Time	140	-	260	14	-	26	ns
t_{TxRV}	TX Clock Rise to TxD, TXCLT Valid	-	-	20	-	-	20	ns
t_{TxHT}	TxD, TXCLT Hold Time	5	-	-	5	-	-	ns

MII Timing – MII PORT – Receive

Figure 27. MII Timing – MII PORT – Receive
Table 62. MII Receive Timing Parameters

Symbol	Description	10MHz			100MHz			Units
		Min	Typ	Max	Min	Typ	Max	
t_{RxCC}	RX Clock Cycle	-	400	-	-	40	-	ns
t_{RxCH}	RX Clock High Time	140	-	260	14	-	26	ns
t_{RxCL}	RX Clock Low Time	140	-	260	14	-	26	ns
t_{RxSU}	RxD, RXCLT Setup Time	10	-	20	10	-	20	ns
t_{RxHT}	RxD, RXCLT Hold Time	5	-	-	5	-	-	ns

9.6.3. GMII Timing Modes

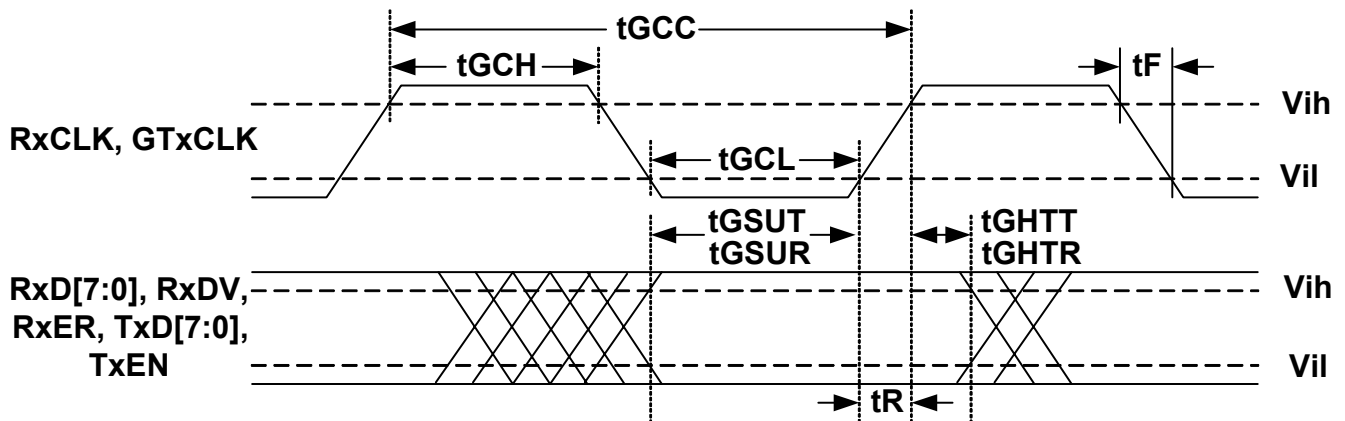
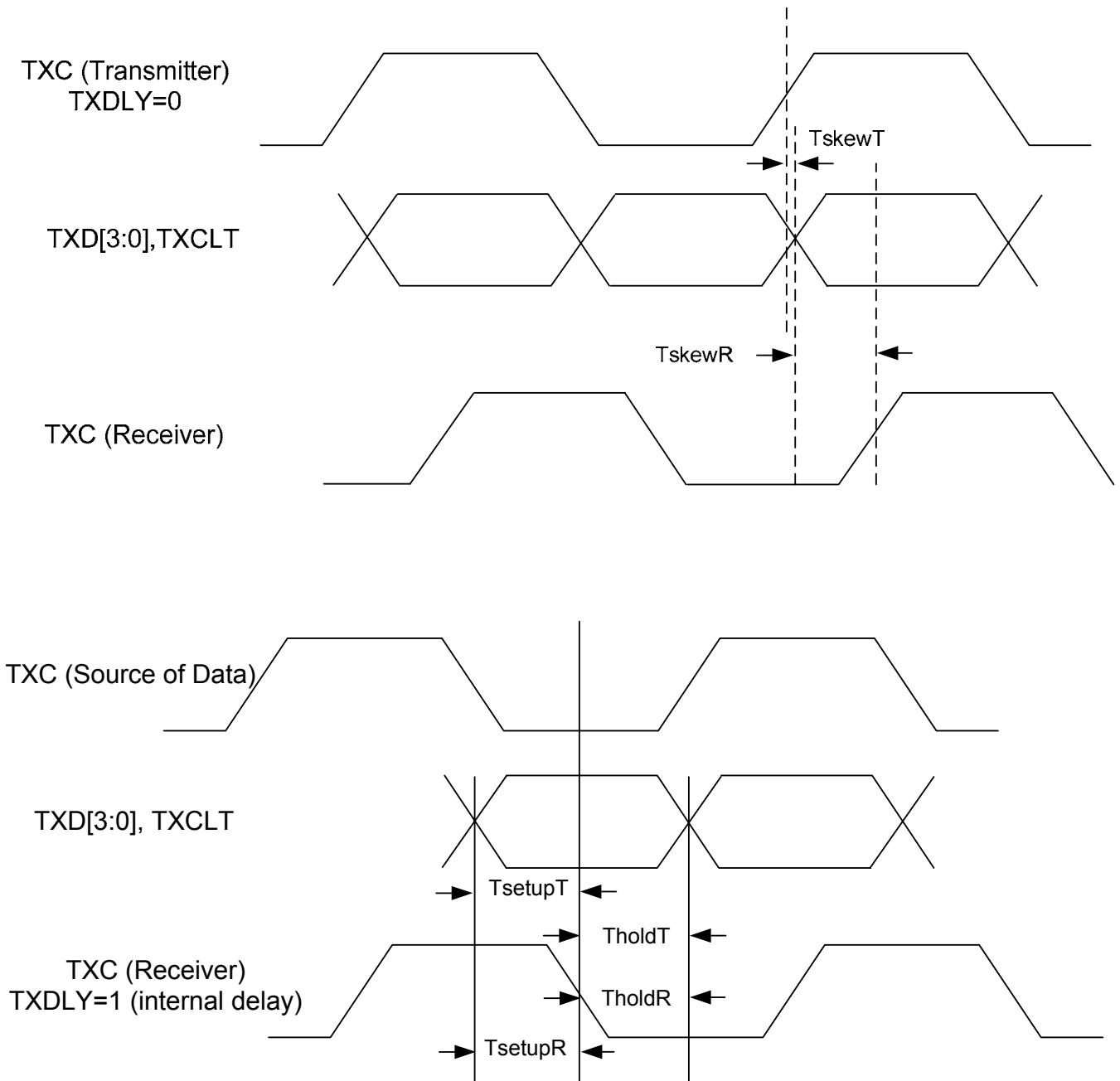


Figure 28. GMII Timing

Table 63. GMII Timing Parameters

Symbol	Description	Min	Typical	Max	Units
t _{GCC}	RxCLK Cycle Time	7.2	8	8.8	ns
t _{GCH}	GTxCLK, RxCLK High Time	2.5	-	-	ns
t _{GCL}	GTxCLK, RxCLK Low Time	2.5	-	-	ns
t _R	GTxCLK, RxCLK Rise Time	-	-	1	ns
t _F	GTxCLK, RxCLK Fall Time	-	-	1	ns
t _{GSUT}	TxD, TxEN Setup to ↑ of GTxCLK	2.5	-	-	ns
t _{GHTT}	TxD, TxEN Hold from ↑ of GTxCLK	0.5	-	-	ns
t _{GSUR}	RxD, RxDV, RxER Setup to ↑ of RxCLK	2	-	-	ns
t _{GHTR}	RxD, RxDV, RxER Hold from ↑ of RxCLK	0	-	-	ns

9.6.4. RGMII Timing Modes



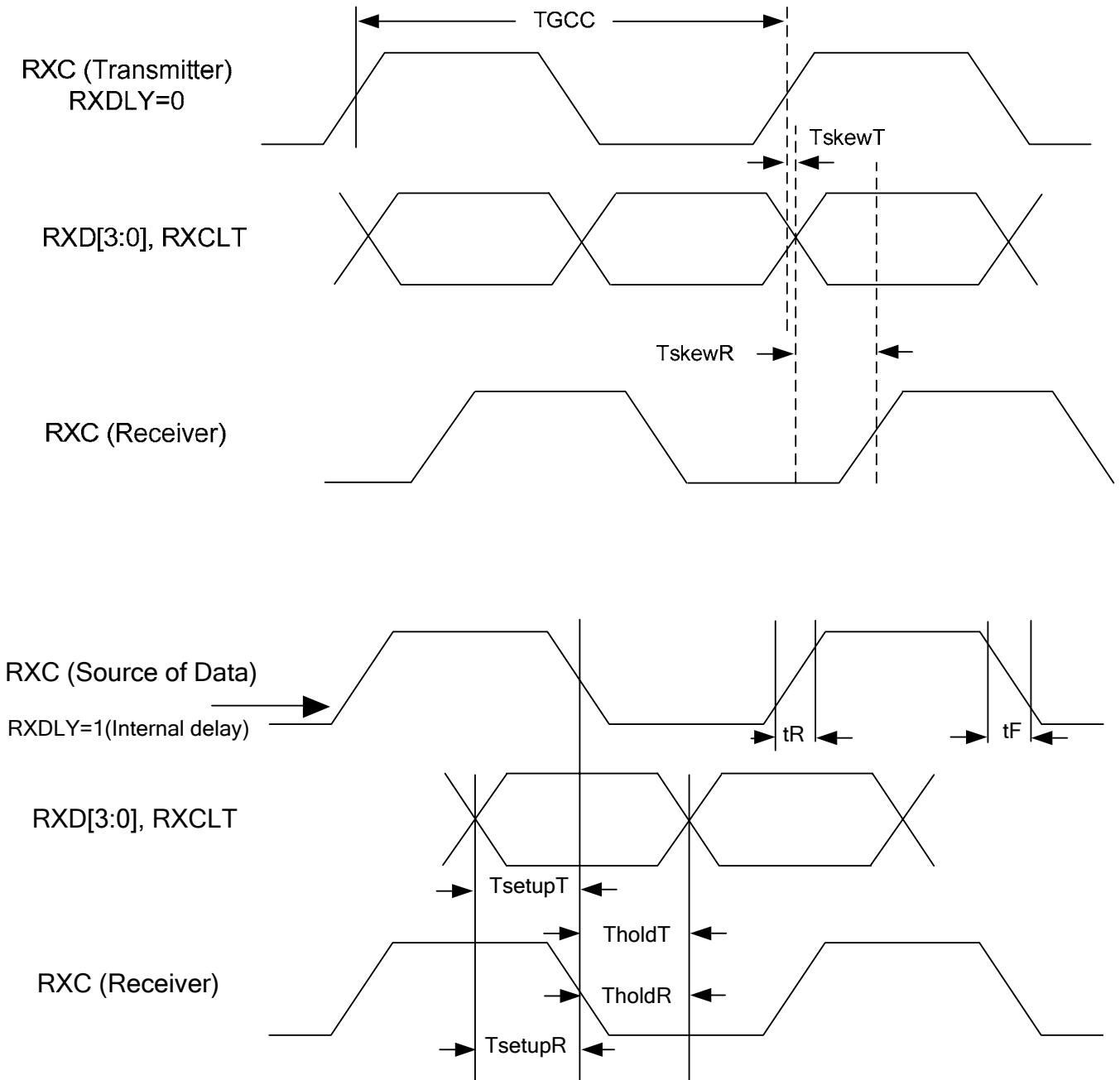


Figure 29. RGMII Timing Modes

Table 64. RGMII Timing Parameters

Symbol	Description	Min	Typical	Max	Units
TGCC	Clock Cycle Duration (1000Mbps)	7.2	8	8.8	ns
	Clock Cycle Duration (100Mbps)	36	40	44	ns
	Clock Cycle Duration (10Mbps)	360	400	440	ns
Duty_G	Duty Cycle for Gigabit	45	50	55	%
Duty_T	Duty Cycle for 10/100T	40	50	60	%
tR	RXC Rise Time (20%~80%)	-	-	0.75	ns
tF	RXC Fall Time (20%~80%)	-	-	0.75	ns
TsetupT	Data to Clock Output Setup (at Transmitter Integrated Delay)	1.2	2	-	ns
TholdT	Data to Clock Output Hold (at Transmitter Integrated Delay)	1.2	2	-	ns
TsetupR	Data to Clock Input Setup (at Receiver Integrated Delay)	1.0	2	-	ns
TholdR	Data to Clock Input Hold (at Receiver Integrated Delay)	1.0	2	-	ns
TskewT	Data to Clock Output Skew (at Transmitter)	-0.5	0	0.5	ns
TskewR	Data to Clock Input Skew (at Receiver)	1	1.8	2.6	ns

9.6.5. SGMII Timing Modes

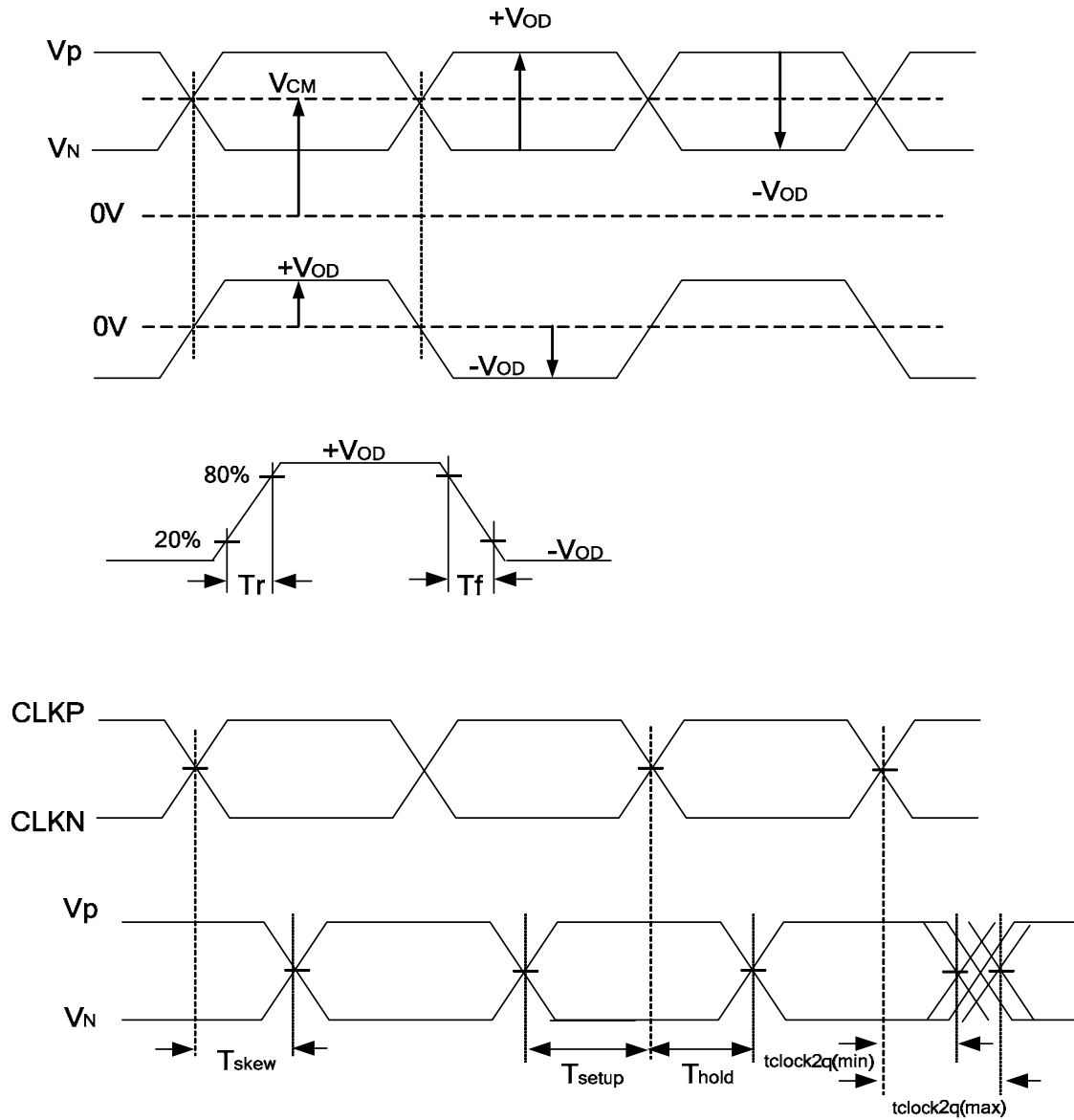


Figure 30. SGMII Timing Modes

Table 65. Differential Transmitter Output AC Timing

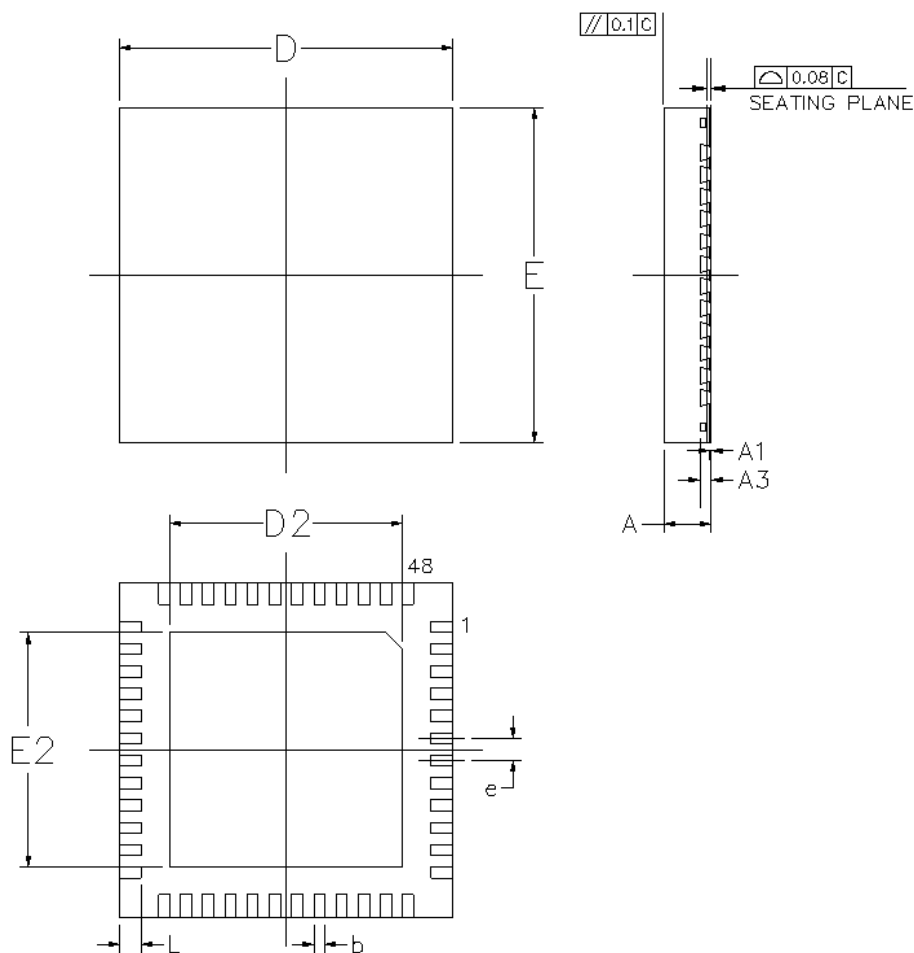
Symbol	Parameter	Min	Typical	Max	Units	Note
clock	Clock Signal Duty Cycle @ 625MHz	48	-	52	%	-
T _f	V _{OD} Fall Time (20%~80%)	80	-	120	ps	-
T _r	V _{OD} Rise Time (20%~80%)	80	-	120	ps	-
T _{skew}	Skew between Two Members of a Differential Pair	-	-	15	ps	-
t _{clock2q}	Clock to Data Relationship: From either edge of the clock to valid data	250	-	550	ps	-
-	Effective Clock Period	-	800	-	ps	-
-	Cycle to Cycle Clock Jitter	-	-	100	ps	peak to peak
-	Imperfect Duty Cycle	-	-	30	ps	peak to peak
-	Data Dependent Skew	-	-	70	ps	peak to peak
-	Static Package Skew	-	-	100	ps	peak to peak
-	Remaining Window	500	-	-	ps	peak to peak

Table 66. Differential Receiver Input AC Timing

Symbol	Parameter	Min	Typical	Max	Units	Note
T _{setup}	Setup Time (20%~80%)	250	-	550	ps	-
T _{hold}	Hold Time (20%~80%)	250	-	550	ps	-
-	Driver Window	500	-	-	ps	peak to peak
-	Static Package Skew	100	-	-	ps	peak to peak
-	Remaining Window	200	-	-	ps	peak to peak

10. Mechanical Dimensions

10.1. RTL8211D 48-Pin QFN Mechanical Dimensions



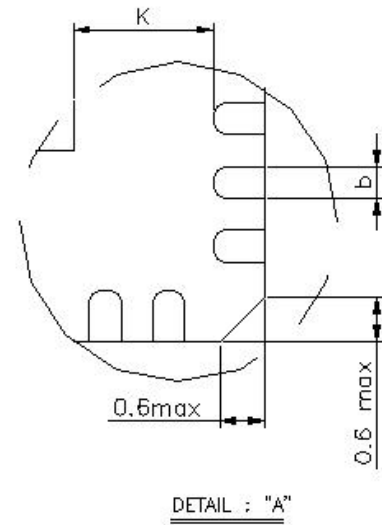
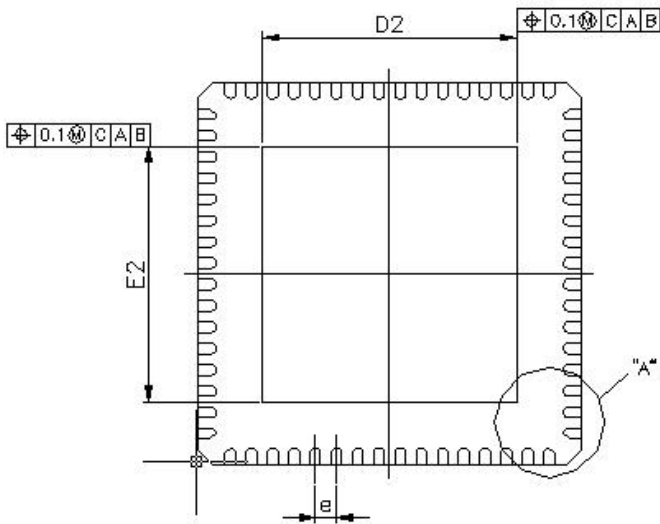
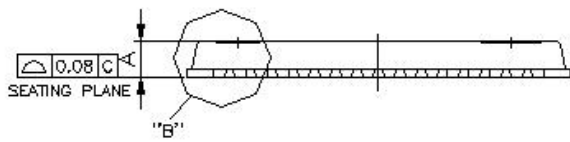
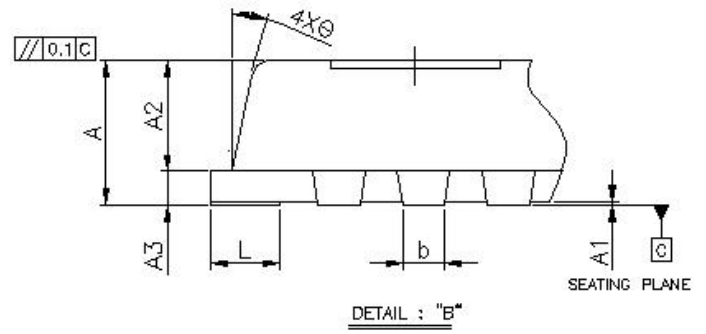
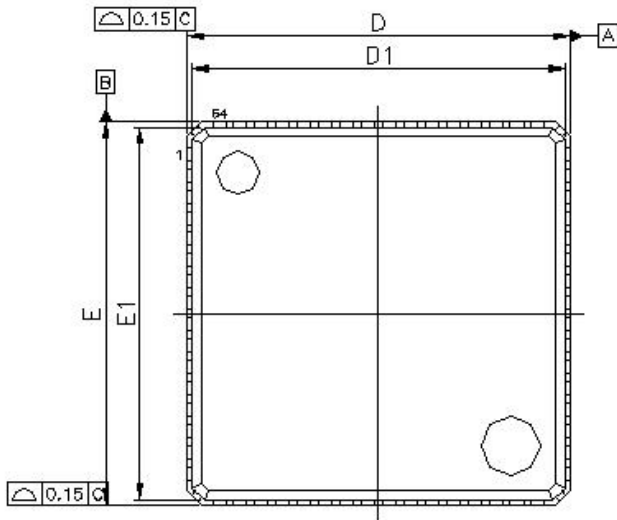
10.2. RTL8211D 48-Pin QFN Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A ₁	0.00	0.02	0.05	0.000	0.001	0.002
A ₃	0.20REF			0.008REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	6.00BSC			0.236BSC		
D2/E2	4.15	4.4	4.65	0.163	0.173	0.183
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).

Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

10.3. RTL8211DG 64-Pin QFN Mechanical Dimensions



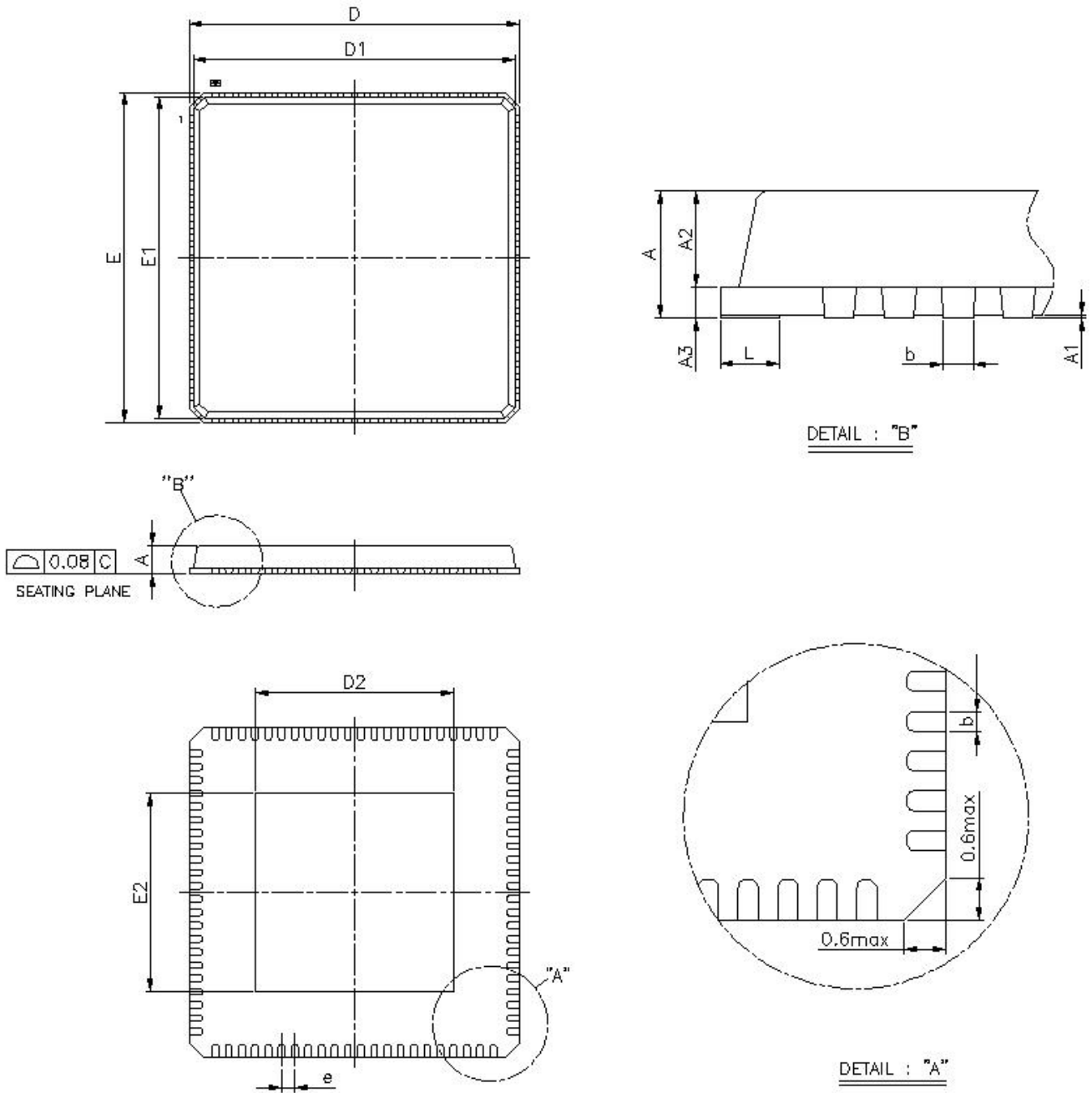
10.4. RTL8211DG 64-Pin QFN Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A ₁	0.00	0.02	0.05	0.000	0.001	0.002
A ₂	0.55	0.65	0.80	0.022	0.026	0.032
A ₃	0.20REF			0.008REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	9.00BSC			0.354BSC		
D ₁ /E ₁	8.75BSC			0.344BSC		
D ₂ /E ₂	5.25	5.5	5.75	0.206	0.216	0.226
e	0.50BSC			0.020BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	-	14°	0°	-	14°

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).

Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

10.5. RTL8211DN 88-Pin QFN Mechanical Dimensions



10.6. RTL8211DN 88-Pin QFN Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A ₁	0.00	0.02	0.05	0.000	0.001	0.002
A ₂	0.55	0.65	0.80	0.022	0.026	0.032
A ₃	0.20REF			0.008REF		
b	0.15	0.22	0.25	0.006	0.08	0.010
D/E	10.00BSC			0.394BSC		
D ₁ /E ₁	9.75BSC			0.384BSC		
D ₂ /E ₂	5.75	6.0	6.25	0.226	0.236	0.246
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).

Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

11. Ordering Information

Table 67. Ordering Information

Part Number	Package	Status
RTL8211D-VB-GR	48-Pin QFN with 'Green' Package with Au Bonding (supports RGMII not GMII)	Mass Production
RTL8211DG-VB-GR	64-Pin QFN with 'Green' Package with Au Bonding (supports RGMII and GMII)	Mass Production
RTL8211DN-VB-GR	88-Pin QFN with 'Green' Package with Au Bonding (supports RGMII, GMII, SGMII, and Fiber mode)	Mass Production

Note: See page 6, page 7, and page 8 for package identification.

Realtek Semiconductor Corp.

Headquarters

No. 2, Innovation Road II

Hsinchu Science Park, Hsinchu 300, Taiwan

Tel.: +886-3-578-0211 Fax: +886-3-577-6047

www.realtek.com