RTL8212-GR
RTL8212-N-GR

INTEGRATED 10/100/1000 DUAL GIGABIT ETHERNET TRANSCEIVER

DATASHEET

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USING THIS DOCUMENT
This document is intended for the hardware and software engineer's general information on the Realtek RTL8212 IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2005/08/10	First release.

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1. General Description

The RTL8212 integrates dual independent Gigabit Ethernet transceivers into a single IC and performs all the physical layer (PHY) functions for 10Base-T, 100Base-TX, and 1000Base-T Ethernet on category 3 (10Base-T) or category 5 UTP cable (except 1000Base-T half duplex operation).

The device includes the PCS, PMA, and PMD sub-layers. They perform encoding/decoding, clock/data recovery, digital adaptive equalization, echo cancellers, cross-talk elimination, line driver, as well as all other required support circuit functions. The device also integrates an internal hybrid that allows the use of inexpensive 1:1 transformer modules.

Each of the two independent transceivers features an industrial standard GMII, MII, and RGMII (Reduced Gigabit Media Independent Interface). To further reduce PCB trace complexity, the RTL8212 also provides an innovative 2.5Gbps serial interface – the Reduced Serial Gigabit Media Independent Interface (RSGMII). Both dual transceivers can simultaneously communicate with the MAC through the same RSGMII interface.

The RTL8212 adopts mixed mode 0.13µm CMOS technology and analog line driver architecture that offers lower power consumption than DAC architecture.

Two package types are available; a thermally-enhanced 128-pin EDHS-QFP (Exposed Drop-in Heat Sink QFP) package, and a QFN (Quad Flat No-Lead) 76-pin package.

2. Features

- Dual integrated 10/100/1000Base-T Gigabit Ethernet transceiver
- Supports full duplex at 10/100/1000Mbps, and half duplex at 10/100Mbps
- Supports 2.5V I/O (3.3V input tolerance) GMII and RGMII interfaces in 10/100/1000 mode (QFP-128 Package)
- Supports RSGMII (2.5Gbps serial high speed interface) in 10/100/1000 mode (QFP-128 Package)
- Crossover detection and auto correction at all 3 speeds
- Automatic detection and correction of wiring pair swaps, pair skew, and pair polarity
- Supports serial LED mode
- Line driver architecture with low power dissipation PAVE= 0.78W/port
- 3.3V, 1.8V, and 1.2V power supply (2.5V is generated by internal linear regulator for Digital I/O pads)
- Packages:
  - EDHS QFP-128, 14x20mm, 0.5mm lead pitch package
  - QFN-76, 9x9mm, 0.4mm pitch package
- 0.13 µm CMOS process

3. System Applications

- High density Gigabit Ethernet switches and routers

4. System Application Diagrams

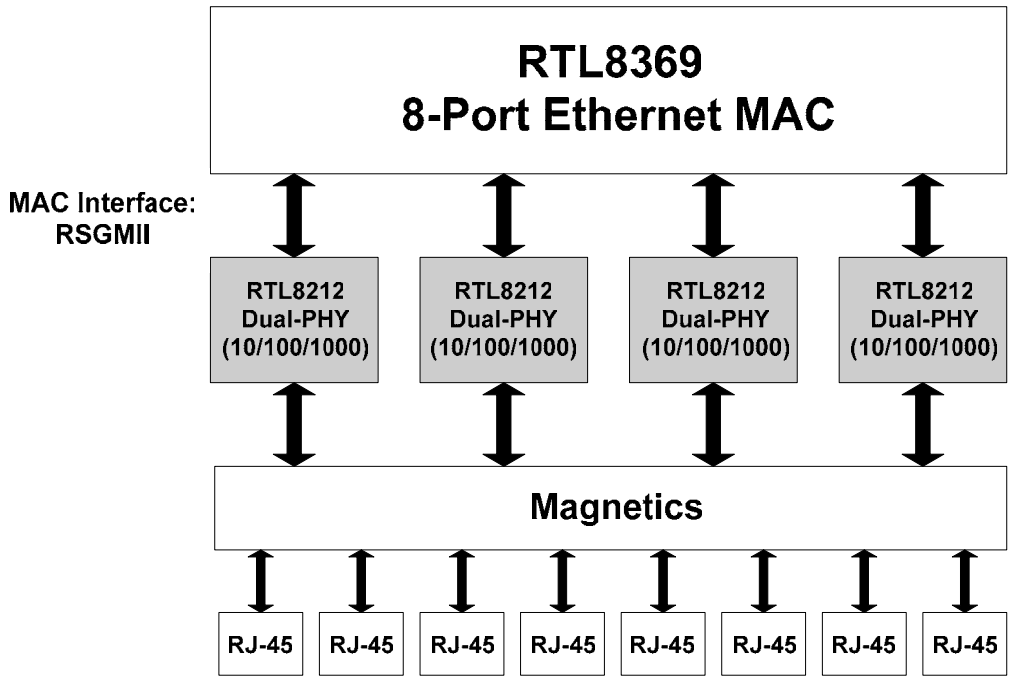


Figure 1. RTL8212 with 8-Port Gigabit MAC (RTL8369)

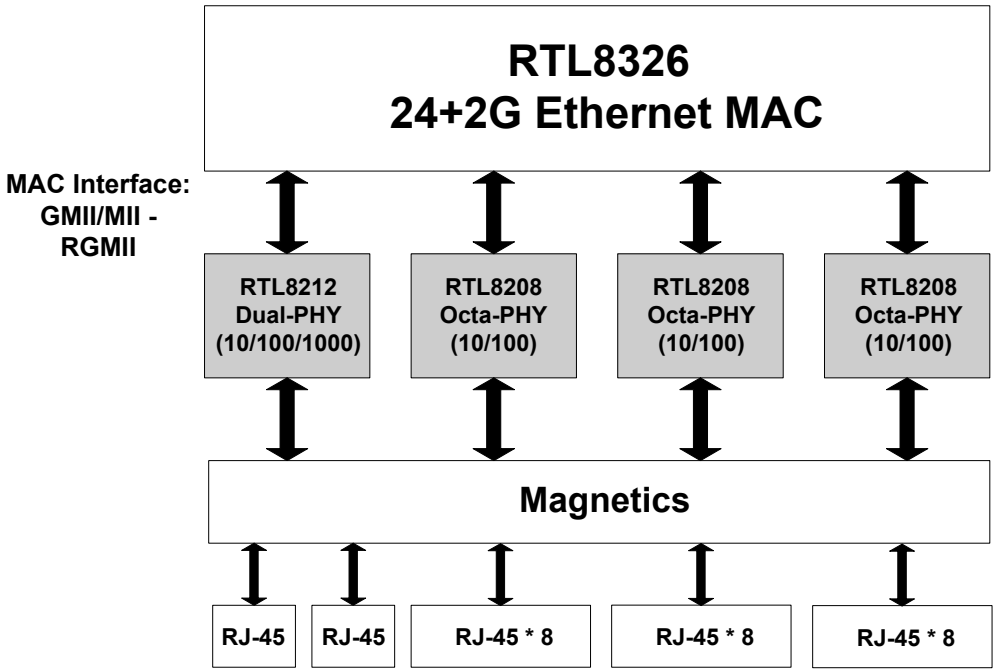


Figure 2. RTL8212 with 24+2G MAC (RTL8326)

5. Block Diagram

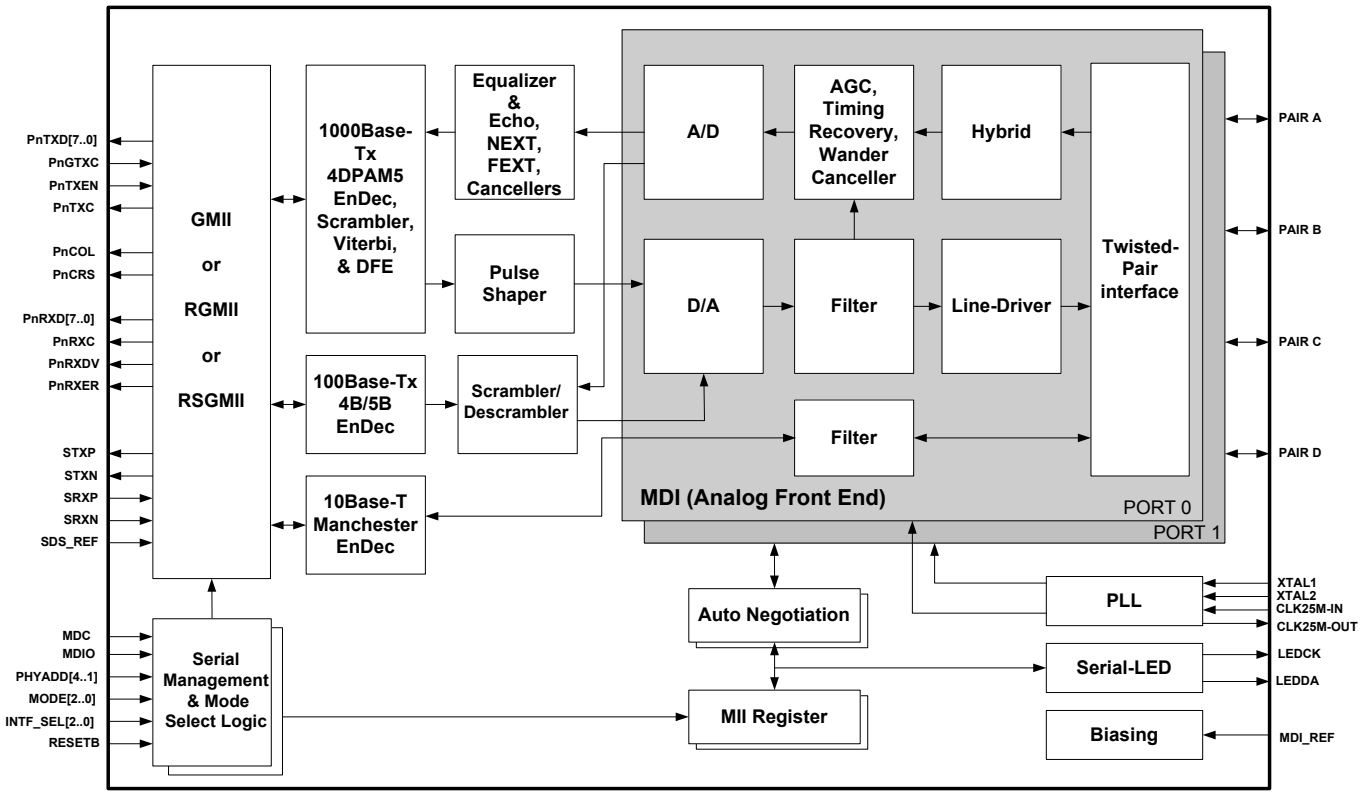


Figure 3. Block Diagram

6. Pin Assignments

6.1. EDHS QFP-128 Package

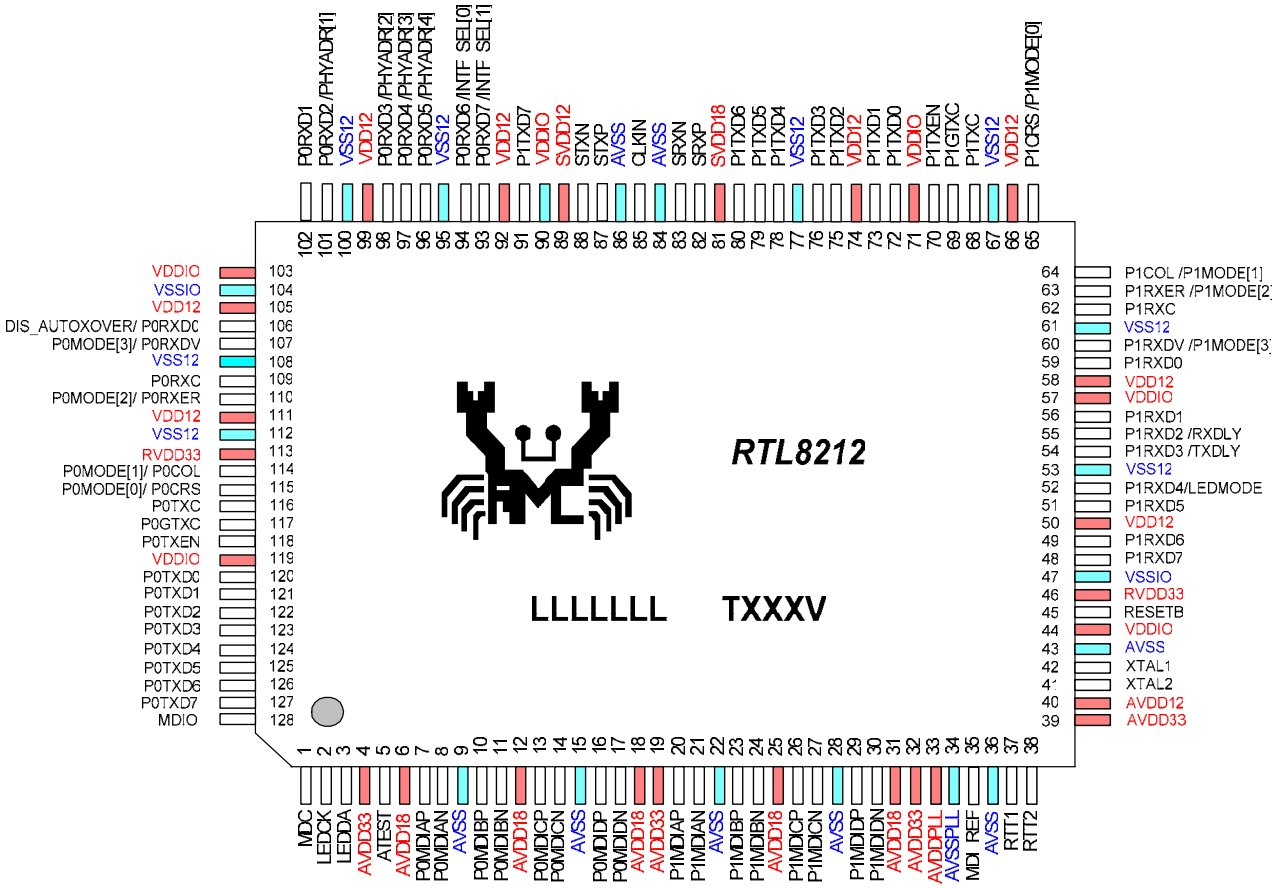


Figure 4. Pin Assignments (QFP-128)

6.2. Package Identification (EDHS QFP-128)

Green package is indicated by a ‘G’ in the location marked ‘T’ in Figure 4.

6.3. QFN-76 Package

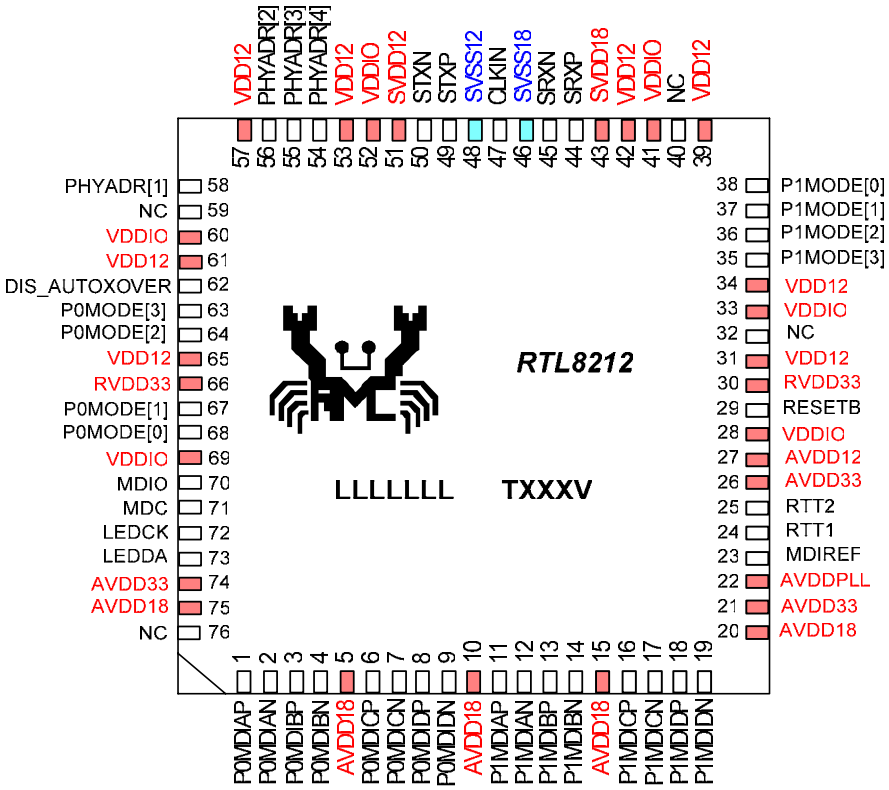


Figure 5. Pin Assignments (QFN-76)

6.4. Package Identification (QFN-76)

Green package is indicated by a ‘G’ in the location marked ‘T’ in Figure 5.

7. Pin Descriptions

Table 1. Pin Type Abbreviations

Pin Type	Definition
I	Input
O	Output
I/O	Bidirectional
B	Bias
PU	Internal pull-up
PD	Internal pull-down
PWR	Power
GND	Ground

Note: The RTL8212 is a dual-port Gigabit Ethernet transceiver. Each port, defined as Port0 and Port1, is independent of the other, and is identical in performance and functionality. In this document, these pins for each port are specified by the port number, pin name, and signal number, respectively.

For example, GMII transmit data pin 7 for port0 is shown as: P0TXD7

7.1. Media Dependent Interface Pins

Table 2. Media Dependent Interface Pins

QFN76 Pin#	QFP128 Pin#	Pin Name	Type	Description
1, 2 3, 4 6, 7 8, 9 11, 12 13, 14 16, 17 18, 19	7, 8 10, 11 13, 14 16, 17 20, 21 23, 24 26, 27 29, 30	P0MDIAP/N P0MDIBP/N P0MDICP/N P0MDIDP/N P1MDIAP/N P1MDIBP/N P1MDICP/N P1MDIDP/N	I/O	Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pair has an internal 100ohm termination resister.

7.2. GMII/MII Transmit Interface Pins

Table 3. GMII/MII Transmit Interface Pins

QFN76 Pin#	QFP128 Pin#	Pin Name	Type	Description
	117 69	P0GTXC P1GTXC	I	GMII Transmit Clock. 125MHz input clock. All transmit inputs must be synchronized to this clock during 1000Base-T operation. This clock can be stopped in 10/100Base-T modes, and also during Auto-Negotiation.
	116 68	P0TXC P1TXC	O	MII Transmit Clock. All transmit inputs must be synchronized to this clock during 10/100 operation. It provides a 25MHz clock reference in 100Base-TX mode, and 2.5MHz clock reference in 10Base-T. The 25MHz clock is the default rate.
	118 70	P0TXEN P1TXEN	I	GMII/MII Transmit Enable. The synchronous input indicates that valid data is being driven on the TXD bus. As the RTL8212 does not support 1000Base-T half-duplex mode, the carrier-extension symbol is not transmitted onto the cable. TXEN is synchronous to GTXC in 1000Base-T mode and synchronous to TXC in 10/100Base-TX mode.
	127 126 125 124 123 122 121 120 91 80 79 78 76 75 73 72	P0TXD7 P0TXD6 P0TXD5 P0TXD4 P0TXD3 P0TXD2 P0TXD1 P0TXD0 P1TXD7 P1TXD6 P1TXD5 P1TXD4 P1TXD3 P1TXD2 P1TXD1 P1TXD0	I_{PD}	GMII/MII Transmit Data Bus. The width of this synchronous input bus varies with the speed mode: 1000: TXD[7:0] are used. 10/100: TXD[3:0] are used; TXD[7:4] are ignored. TXD[7:0] is synchronous to GTXC in 1000Base-T mode and synchronous to TXC in 10/100Base-TX mode.

7.3. GMII/MII Receive Interface Pins

Table 4. GMII/MII Receive Interface Pins

QFN76 Pin#	QFP128 Pin#	Pin Name	Type	Description
	109 62	P0RXC P1RXC	O_{PD}	GMII/MII Receive Clock. The GMII/MII Receive output clock is used to synchronize received signals. Its frequency depends upon the link speed: 1000: 125MHz 100: 25MHz 10: 2.5MHz
	107 60	P0RXDV P1RXDV	O_{PD}	GMII/MII Receive Data valid. This synchronous output is asserted when valid data is driven on RXD. RXDV is synchronous to RXC.
	115 65	P0CRS P1CRS	O_{PD}	GMII/MII Carrier Sense. This asynchronous output is asserted when a non-idle condition is detected at the twisted-pair interface, and de-asserted when idle or a valid end of stream delimiter is detected. In 10/100Base-T half duplex, CRS is also asserted during transmission. CRS is asynchronous to TXC and RXC.
	114 64	P0COL P1COL	O_{PD}	GMII/MII Collision. This asynchronous output is asserted when a collision is detected in half-duplex modes. In full duplex mode, this out is forced low. COL is asynchronous to TXC, and RXC.
	110 63	P0RXER P1RXER	O_{PD}	GMII/MII Receive Error. When RXER and RXDV are both asserted, the symbol indicates an error symbol is detected on the cable. Since RTL8212 don't support 1000Base-T half-duplex mode, carrier-extension receive symbol (RXER is asserted with RXDV deasserted) is not valid. RXDV is synchronous to RXC.

QFN76 Pin#	QFP128 Pin#	Pin Name	Type	Description
	93 94 96 97 98 101 102 106 48 49 51 52 54 55 56 59	P0RXD7 P0RXD6 P0RXD5 P0RXD4 P0RXD3 P0RXD2 P0RXD1 P0RXD0 P1RXD7 P1RXD6 P1RXD5 P1RXD4 P1RXD3 P1RXD2 P1RXD1 P1RXD0	O_{PD}	GMII/MII Receive Data Bus. The width of this synchronous output bus varies with the speed mode: 1000: RXD[7:0] are used. 10/100: RXD[3:0] are used; RXD[7:4] are ignored. RXD[7:0] is synchronous to RXC.

7.4. RGMII Transmit Interface Pins

Table 5. RGMII Transmit Interface Pins

QFN76 Pin#	QFP128 Pin#	Pin Name	Type	Description
	117 69	P0GTXC P1GTXC	I	RGMII Transmit Clock. All transmit inputs must be synchronized to this clock. Its frequency, with +/- 50ppm tolerance, depends upon the link speed: 1000: 125MHz 100: 25MHz 10: 2.5MHz
	123 122 121 120 76 75 73 72	P0TXD3 P0TXD2 P0TXD1 P0TXD0 P1TXD3 P1TXD2 P1TXD1 P1TXD0	I_{PD}	RGMII Transmit Data Bus. In RGMII 1000Base-T mode, TXD[3..0] runs at a double data rate with bits[3..0] presented on the rising edge of the GTXC, and bits[7..4] presented on the falling edge of the GTXC. TXD[7..4] are ignored in this mode. In RGMII 10/100Base-T modes, the transmitted data nibble is presented on TXD[3..0] on the rising edge of GTXC and duplicated on the falling edge of GTXC.
	118 70	P0TXEN/ P0TXCTL P1TXEN/ P1TXCTL	I_{PD}	RGMII Transmit Control. In RGMII mode, TXEN is used as TXCTL. TXEN is presented on the rising edge of GTXC. A logical derivative of TXEN and TXER is presented on the falling edge of GTXC.

7.5. RGMII Receive Interface Pins

Table 6. RGMII Receive Interface Pins

QFN76 Pin#	QFP128 Pin#	Pin Name	Type	Description
	109 62	P0RXC P1RXC	O	RGMII Receive Clock. All RGMII receive outputs must be synchronized to this clock. Its frequency, with +/- 50ppm tolerance, depends upon the link speed: 1000: 125MHz 100: 25MHz 10: 2.5MHz
	98 101 102 106 54 55 56 59	P0RXD3 P0RXD2 P0RXD1 P0RXD0 P1RXD3 P1RXD2 P1RXD1 P1RXD0	O_{PD}	RGMII Receive Data Bus. In RGMII 1000Base-T mode, RXD[3..0] runs at a double data rate with bits[3..0] presented on the rising edge of the RXC and bits[7..4] presented on the falling edge of the RXC. RXD[7..4] are ignored in this mode. In RGMII 10/100Base_T modes, the received data nibble is presented on RXD[3..0] on the rising edge of RXC and duplicated on the falling edge of RXC.
	107 60	P0RXCTL/ P0RXDV P1RXCTL/ P1RXDV	O_{PD}	RGMII Receive Control. In RGMII mode, RXDV is used as RXCTL. RXEN is presented on the rising edge of RXC. A logical derivative of RXDV and RXER is presented on the falling edge of RXC.

7.6. RSGMII Interface Pins

Table 7. RSGMII Interface Pins

QFN76 Pin#	QFP128 Pin#	Pin Name	Type	Description
	82 83	SRXP SRXN	O	RSGMII Receive Pair. 2.5GHz differential serial output. The differential pair has an internal 100ohm termination resister.
	87 88	STXP STXN	I	RSGMII Transmit Pair. 2.5GHz differential serial input. The differential pair has an internal 100ohm termination resister.

7.7. Serial Management Interface Pins

Table 8. Serial Management Interface Pins

QFN76 Pin#	QFP128 Pin#	Pin Name	Type	Description
71	1	MDC	I	Management Data Clock. The clock reference for the serial management interface.
70	128	MDIO	I/O_{PU}	Management Data Input/Output. MDIO transfer management data; in and out of the device synchronous to the rising edge of MDC.
54	96	PHYADR[4]/ P0RXD5	O_{PD}	PHY Address Select. These pins are the four uppermost bits of the 5-bit IEEE-specified PHY address. The states of these four pins are latched during power-up or reset. The lowest bit of the 5-bit PHY address is hard-wired to each of the dual ports within the device. '0' represents Port0, and '1' represents Port1.
55	97	PHYADR[3]/ P0RXD4		
56	98	PHYADR[2]/ P0RXD3		
58	101	PHYADR[1]/ P0RXD2		

7.8. Serial LED Interface Pins

Table 9. Serial LED Interface Pins

QFN76 Pin#	QFP128 Pin#	Pin Name	Type	Description
72	2	LEDCK	O	Serial LED Clock. Reference output clock for serial LED interface. The 12.5MHz clock outputs periodically. Data is latched on the rising edge of LEDCK.
73	3	LEDDA	O	Serial LED Data Output. Serial bit stream of link status information.
32	52	LEDMODE/ P1RXD4	O_{PD}	Serial LED Mode Select. These pins are used to configure LED operation mode. The state of this pin is latched during power-up or reset. There are two LED display modes: 0: Mode 0 1: Mode 1

7.9. System Clock Interface Pins

Table 10. System Clock Interface Pins

QFN76 Pin#	QFP128 Pin#	Pin Name	Type	Description
	42	XTAL1	I	PHY Reference Clock Input. 25MHz +/- 50ppm tolerance crystal reference or oscillator input. When using a crystal, connect a loading capacitor from each pad to ground. This pin is not valid and should be pull-low when CLKIN is used. The maximum XTAL1 input voltage is 1.8 V.
	41	XTAL2	O	PHY Reference Clock Output. 25MHz +/- 50ppm tolerance crystal reference or oscillator output. This pin is not valid and should be floating when CLKIN is used.
47	85	CLKIN	I	25MHz Clock Input. 25MHz +/- 50ppm tolerance clock input. This pin is able to accept 25MHz clock signal generated from the MAC device when RSGMII is used. The maximum CLKIN input voltage is 1.8V.

7.10. Configuration and Control Pins

Table 11. Configuration and Control Pins

QFN76 Pin#	QFP128 Pin#	Pin Name	Type	Description
	93 94	INTF_SEL[1]/ P0RXD7 INTF_SEL[0]/ P0RXD6	O_{PD}	MAC Interface mode select. INTF_SEL[1:0] determines the MAC interface configuration for both port0 and port1: 00: RSGMII (default mode) 01: GMII 10: RGMII 11: Reserved
63 64 67 68 35 36 37 38	107 110 114 115 60 63 64 65	P0MODE[3]/ P0RXDV P0MODE[2]/ P0RXER P0MODE[1]/ P0COL P0MODE[0]/ P0CRS P1MODE[3]/ P1RXDV P1MODE[2]/ P1RXER P1MODE[1]/ P1COL P1MODE[0]/ P1CRS	O_{PD}	Auto-Negotiation Configuration. PxMODE[3:0] presets each port's advertise link ability (speed, duplex, and master/slave). The states of this pin is latched during power-up or reset. PxMODE[3:0] defined as: 0000=Auto-negotiation, advertise all capabilities, prefer MASTER. 0001=Auto-negotiation, advertise all capabilities, prefer SLAVE. 0010=Auto-negotiation, advertise only 100Base-TX half duplex. 0011=Auto-negotiation, advertise only 100Base-TX full duplex. 0100=Reserved. 0101=Reserved. 0110=Reserved. 0111=Reserved. 1000=Auto-negotiation, advertise only 1000Base-T full duplex, force MASTER. 1001=Auto-negotiation, advertise only 1000Base-T full duplex, force SLAVE. 1010=Auto-negotiation, advertise only 1000Base-T full duplex, prefer MASTER. 1011=Auto-negotiation, advertise only 1000Base-T full duplex, prefer SLAVE. 1100=Auto-negotiation, advertise all capabilities, force MASTER. 1101=Auto-negotiation, advertise all capabilities, force SLAVE. 1110=Auto-negotiation, advertise only 10Base-T half duplex. 1111=Auto-negotiation, advertise only 10Base-T full duplex.
	54	TXDLY/ P1RXD3	O_{PD}	GTXC Clock Delay Select. This pin enables GTXC input delay in RGMII mode.
	55	RXDLY/ P1RXD2	O_{PD}	RXC Clock Delay Select. This pin enables RXC output delay in RGMII mode.
62	106	DIS_AUTOX OVER/ P0RXD0	O_{PD}	1: Disable auto crossover detection 0: Enable auto crossover detection

7.11. Miscellaneous Pins

Table 12. Miscellaneous Pins

QFN76 Pin#	Q128 Pin#	Pin Name	Type	Description
29	45	RESETB	I	Hardware Reset. Active low reset signal. To complete the reset function, this pin must be asserted for at least 10ms. It must be pulled high for normal operation.
23	35	MDI_REF	I_B	MDI Bias Resistor. Adjusts the reference current for both PHYs. A resistor of 2.49KΩ±1% is connected between this pin and ground.
24	37	RTT1	O	Test Pin 1. Reserved pin for internal analog debugging. Connect to ground through a 1KΩ resistor. If debug is not important and there are board space constraints, this pin can be left floating.
25	38	RTT2	I	Test Pin 2. Reserved pin for internal analog debugging. Connect to ground through a 1KΩ resistor. If debug is not important and there are board space constrains, this pin can be left floating.
	5	ATEST	O	Analog Test Pin. Reserved pin for internal analog debugging. Connect to ground through a 1KΩ resistor. If debug is not important and there are board space constraints, this pin can be left floating.

7.12. Power and Ground Pins

Table 13. Power and Ground Pins

QFN76 Pin#	QFP128 Pin#	Pin Name	Type	Description
3.3V Power Supply				
21, 26, 74	4, 19 32, 39	AVDD33	PWR	Analog Power 3.3V.
30, 66	46, 113	RVDD33	PWR	Analog Power 3.3V for Internal Regulator.
1.8V Power Supply				
5, 10, 15, 20	6, 12 18, 25, 31	AVDD18	PWR	Analog Power 1.8V.
22	33	AVDDPLL	PWR	Analog Power 1.8V for PLL This pin is filtered with a low resistance series ferrite bead and 1000pF + 2.2uF shunt capacitors to ground.
43	81	SVDD18	PWR	Analog Power 1.8V for RSGMII.
1.2V Power Supply				
27	40	AVDD12	PWR	Analog Power 1.2V.
51	89	SVDD12	PWR	Analog Power 1.2V for RSGMII.
31, 34, 39, 42, 53, 57, 61, 65	50, 58, 66, 74, 92, 99, 105, 111	VDD12	PWR	Digital Power 1.2V for Digital Core.
2.5V Power Output Pin				
28, 33, 41, 52, 60, 69	44, 57, 71, 90, 103, 119	VDDIO	PWR	Digital I/O Power 2.5V. This power is generated from an internal regulator. Connect the following group of pins together QFP-128:Group(44,57,71) ,Group(90,103,119) QFN-76: Group(28,33,41),Group (52,60,69) If MII/GMII/RGMII not used, no external PCB trace is required. Only connect to ground through a decoupling capacitor.
Ground				
GND PAD	9, 15, 22, 28, 36, 43,	AVSS	GND	Analog ground.
GND PAD	34	AVSSPLL	GND	PLL ground.
GND PAD	53, 61, 67, 77, 95, 100, 108, 112	VSS12	GND	Digital Core ground.
GND PAD	47, 104	VSSIO	GND	Digital I/O ground.
46	84	SVSS18	PWR	Analog 1.8V GND for RSGMII.
48	86	SVSS12	PWR	Analog 1.2V GND for RSGMII.

8. Functional Description

8.1. MDI Interface

The RTL8212 uses a single common MDI interface to support 10Base-T, 100Base-Tx, and 1000Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used. Table 14 shows the mapping between the pairs and the RJ-45 signals.

Table 14. Mapping of Twisted-Pair Outputs to RJ-45 Connectors

Pairs	RJ-45 Connector
A	1 and 2
B	3 and 6
C	4 and 5
D	7 and 8

8.1.1. Crossover Detection and Auto Correction

The RTL8212 automatically determines whether or not it needs to crossover between pairs; removing the need for an external crossover cable. When connecting to a device that does not perform MDI crossover, the RTL8212 automatically switches its pin pairs to communicate with the connecting device. When connecting to a device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled by strap pin. The RTL8212 is set to MDI Crossover by default. The pin mapping in MDI and MDI Crossover mode is given in Table 15.

Table 15. Media Dependent Interface Pin Mapping

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	unused	unused	D	unused	Unused
D	D	unused	unused	C	unused	unused

8.1.2. Polarity Correction

The RTL8212 automatically corrects polarity errors on the receiver pairs in 10Base-T and 1000Base-T modes. In 100Base-Tx mode, the polarity does not matter.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

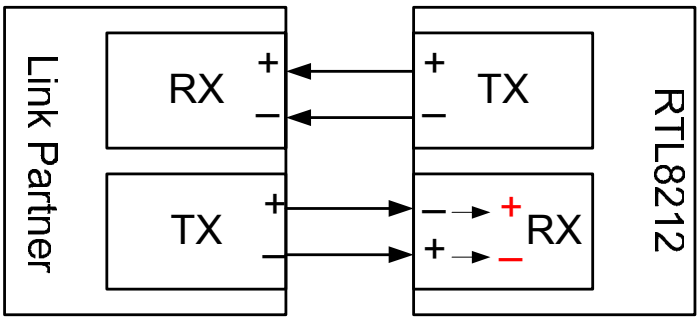


Figure 6. Conceptual Example of Polarity Correction

8.1.3. MAC Interface

The RTL8212 MAC interface supports GMII/MII, RGMII, and RSGMII (2.5Gbps serial interface). The MAC interface selection is set by INTF_SEL[1..0]. Table 16 shows the data rates supported through each interface, and Table 17 shows each MAC interface operation mode.

Table 16. Data Rates Supported Through Each Interface

MAC Interface	10Base-T	100Base-TX	1000Base-T
GMII			√
MII	√	√	
RGMII	√	√	√
RSGMII	√	√	√

Table 17. MAC Interface Modes of Operation

MAC Interface	Speed	Data Width	Clock Frequency	Clock Edge	Notes
GMII	1000	8 bits	125MHz	Rising	
MII	100	4 bits	25MHz	Rising	
	10	4 bits	2.5MHz	Rising	
RGMII	1000	4 bits	125MHz	Rising/Falling	
	100	4 bits	25MHz	Rising	1
	10	4 bits	2.5MHz	Rising	1
RSGMII	1000	1 bits	125MHz	Rising	2
	100	1 bits	125MHz	Rising	3
	10	1 bits	125MHz	Rising	3

Note 1: The data may be duplicated on the falling edge of the appropriate clock when the interface operates at 10 and 100Mbps speeds.

*Note 2: The internal PLL generates 20 sub-phase clock signals by dividing the 125MHz clock. The data can be latched on the rising edge of each sub-phase signal. The data bandwidth of the RSGMII interface is up to 2.5Gbps (125M*20*1).*

Note 3: Operation at 10 and 100Mbps uses respectively only 1% and 10% of the RSGMII Interface bandwidth.

8.2. Gigabit Media Independent Interface (GMII/MII)

Table 18 indicates the signal mapping of the RTL8212 to the Gigabit Media Independent Interface (GMII/MII). MII signaling to support 100Base-Tx and 10Base-T modes is implemented by sharing pins of the GMII interface. The interface supports GMII to copper connections at all three speeds. The GMII mode does not support carrier extension and packet concatenation in both the transmit and receive directions, due to no TXER pin.

Table 18. Gigabit Media Independent Interface

RTL8212 Pins	GMII	MII
GTXC	GTX_CLK	-
TXC	-	TXC
TXEN	TX_EN	TX_EN
TXD[7..4]	TXD[7..4]	-
TXD[3..0]	TXD[3..0]	TXD[3..0]
RXC	RX_CLK	RX_CLK
RXER	RX_ER	RX_ER
RXDV	RX_DV	RX_DV
RXD[7..4]	RXD[7..4]	-
RXD[3..0]	RXD[3..0]	RXD[3..0]
CRS	CRS	CRS
COL	COL	COL

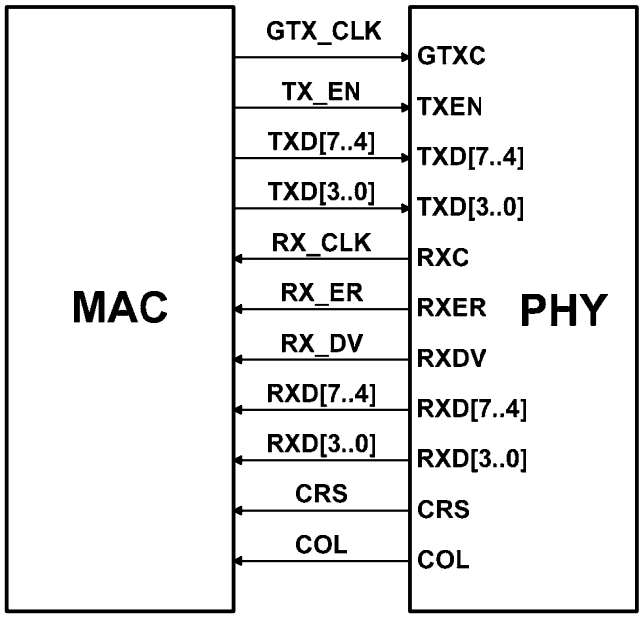


Figure 7. GMII Signal Diagram

In 1000Base-T operation, when GMII mode is selected, a 125MHz transmit clock is expected on GTXC, and RXC sources the 125MHz receive clock. At the same time, TXC sources 25MHz, 2.5MHz, or 0MHz depending on the MDI status.

In 10Base-T and 100Base-TX modes, when MII mode is selected, both TXC and RXC source 25MHz or 2.5MHz, respectively. TXD[3:0] and RXD[3:0] signals are used. GTXC and TXD[7..4] signals must be pulled high or low and must not be left floating. RXD[7..4] are driven low.

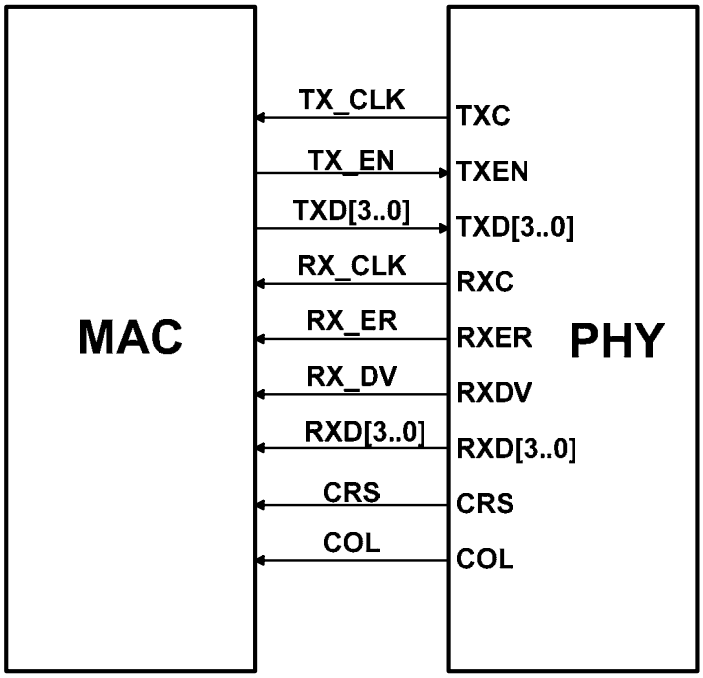


Figure 8. MII Signal Diagram

During the transition from one speed to another, a dead time of 1.5 clock cycles may occur in RXC and TXC (in order to ensure a glitch-free clock).

Note: The GMII and MII interfaces are enabled by hardware configuration bits INTF_SEL[1..0] that are latched at the end of hardware reset.

8.2.1. Reduced GMII (RGMII)

The RTL8212 supports the RGMII Rev. 2.0 specification. This interface reduces the interconnection between the MAC and the PHY to 12 pins. In order to accomplish this objective, the data paths and all associated control signals are reduced. Control signals are multiplexed and both edges of the clock are used.

For Gigabit operation, the transmit and receive clocks operate at 125MHz. For 10/100 operation, the clocks operate at 2.5MHz or 25MHz respectively. Once the RGMII is selected in all three speeds, transmit control is presented on both clock edges of GTXC (TXC). Receive control (RX_CTL) is presented on both clock edges of RXC (RXC).

The RGMII interface is selected by setting INTF_SEL[1..0] to '10'.

Table 19. MAC Interface Modes of Operation

RTL8212 Pins	RGMII	Description
GTXC	TXC	125MH, 25MHz, or 2.5MHz transmit clock, with +/- 50 ppm tolerance, based on the selected speed.
TXEN	TX_CTL	Transmit Control Signals. TX_EN is encoded on the rising edge of GTXC. TX_ER XOR TX_EN is encoded on the falling edge of GTXC.
TXD[3..0]	TD[3..0]	Transmit data. In 1000Base-T mode, bits 3:0 are presented on the rising edge of GTXC, and bits 7:4 is presented on the falling edge of GTXC. In 10/100 mode, bits 3:0 is presented on the rising edge of GTXC, and duplicated on the falling edge of GTXC.
RXC	RXC	125MH, 25MHz, or 2.5MHz receive clock, with +/- 50 ppm tolerance, based on the selected speed.
RXDV	RX_CTL	Receive Control Signals. RX_DV is encoded on the rising edge of RXC, RX_ER XOR RX_DV is encoded on the falling edge of RXC.
RXD[3..0]	RD[3..0]	Receive data. In 1000Base-T mode, bits 3:0 is presented on the rising edge of RXC, and bits 7:4 are presented on the falling edge of RXC. In 10/100 mode, bits 3:0 is presented on the rising edge of RXC, and duplicated on the falling edge of RXC.

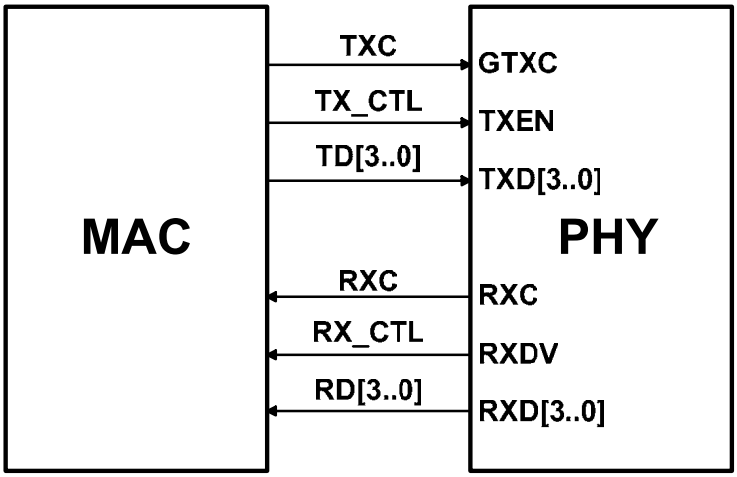


Figure 9. RGMII Signal Diagram

8.2.2. 10/100 Functionality

This interface can be used to implement the 10/100Mbps Ethernet Media Independent Interface (MII) by reducing the clock rate to 25MHz for 100Mbps operation and 2.5MHz for 10Mbps. The TXC will always be generated by the MAC and RXC will always be generated by the PHY. During packet reception, the RXC may be stretched on either the positive or negative pulse to accommodate the transition from the free running clock to a data-synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulses is allowed. No glitch of the clocks are allowed during speed transitions.

The interface will operate at 10 and 100Mbps speeds exactly the same way it does at Gigabit speed with the exception that the data may be duplicated on the falling edge of the appropriate clock.

The MAC must hold TXEN (TX_CTL) low until the MAC has ensured that TXEN (TX_CTL) is operating at the same speed as the PHY.

8.2.3. TX_CTL and RX_CTL Coding

To reduce power consumption of this interface, TX_ER and RX_ER are encoded in a manner that minimizes transitions during normal network operation. This is done via the following encoding method. *Note that the RTL8212 does not support Half-Duplex in 1000Base-T and the GMII_TX_ER signal is tied to logic low at all times, carrier extend and transmit errors never appear at the transmitting and receiving end.*

TX_CTL ← GMII_TX_ER (XOR) GMII_TX_EN

RX_CTL ← GMII_RX_ER (XOR) GMII_RX_DV

While receiving a valid frame with no errors, RX_DV=true is generated as a logic high on the rising edge of RXC, and RX_ER=false is generated as a logic high on the falling edge of RXC. When no frame is being received, RX_DV=false is generated as a logic low on the rising edge of RXC, and RX_ER=false is generated as a logic low on the falling edge of RXC.

When receiving a valid frame with errors, RX_DV=true is generated as a logic high on the rising edge of RXC, and RX_ER=true is generated as a logic low on the falling edge of RXC.

During normal frame transmission, the signal stays at high for both edges of TXC. During normal inter-frame, the signal stays low for both edges.

Table 20. TX_ER and TX_EN Encoding

TX_CTL	GMII_TX_EN	GMII_TX_ER	Description
0, 0	0	0	Normal inter-frame
1, 1	1	0	Normal data transmission

Note: As GMII_TX_ER is always tied to logic low in the RTL8212, no transmit error symbol or carrier extend symbol occurs in data transmission.

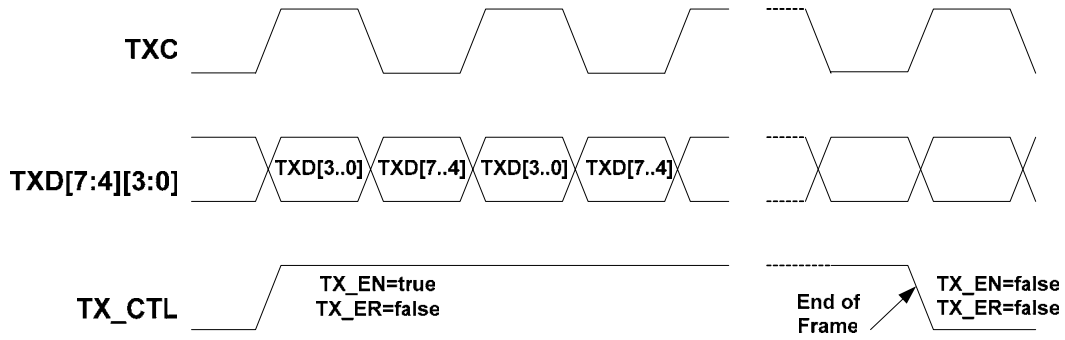


Figure 10. RGMII Data Transmission

Table 21. RX_ER and RX_DV Encoding

RX_CTL	GMII_RX_DV	GMII_RX_ER	Description
0, 0	0	0	Normal inter-frame
0, 1	0	1	Carrier sense
1, 1	1	0	Normal data reception
1, 0	1	1	Data reception error

Note 1: The MAC is designed to acquire the link status, speed and duplex mode of the PHY via MDC/MDIO polling, so the RTL8212 does not implement specific code onto RXD[3..0] to inform MAC of the PHY status during normal inter-frame.

Note 2: In addition to the encoding of RX_DV and RX_ER as indicated in Table 21, a value of 'FF' also exists on the RXD[7..0] simultaneously when the Carrier Sense symbol occurs.

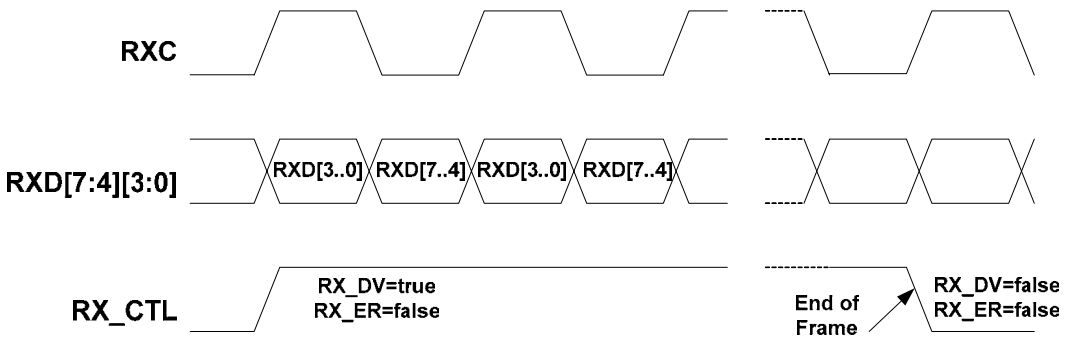


Figure 11. RGMII Data Reception Without Error

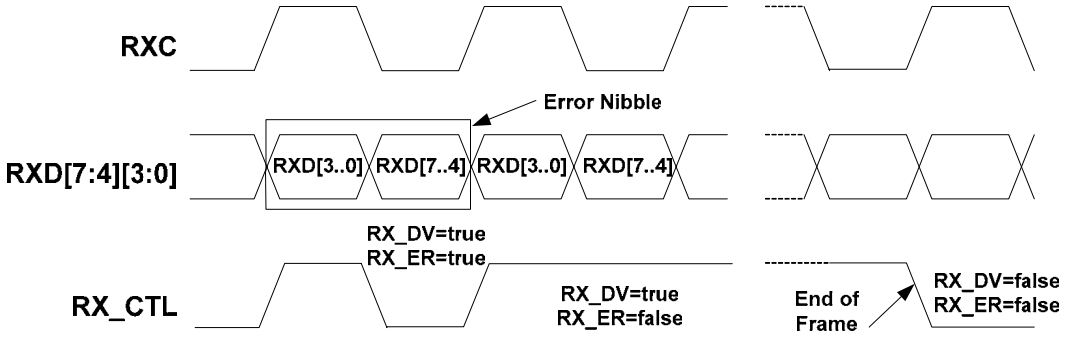


Figure 12. RGMII Data Reception With Error

8.2.4. In-Band Status

CRS is indicated where:

- RX_DV is true
- Where RX_DV is false, RX_ER is true, and a value of 'FF' exists on the RXD[7..0] bits simultaneously

Carrier Extend and Carrier Extend Error are not supported by the RTL8212. Collision is determined at the MAC by the assertion of TXEN being true while either CRS or RXDV are true. The PHY will not assert CRS as a result of TXEN being true.

8.2.5. Four RGMII Modes

The RTL8212 supports four different timing modes of operation. Hardware strapping pins TXDLY and RXDLY can be used to select between the four RGMII timing modes. Refer to Table 44, page 56, AC Characteristics for RGMII Mode timing.

Each bit adjusts the delays of data with respect to clock edges. For both inputs and outputs of the PHY the data can change either simultaneously with the clock edges, or the data can have setup and hold with respect to clock edges.

Table 22. RGMII Timing Modes

Mode	TXDLY	RXDLY	PHY Input GTXC vs. data	PHY Output RXC vs. data
Mode 0	0	0	Meet setup and hold time	Simultaneous with clock edge
Mode 1	0	1	Meet setup and hold time	Meet setup and hold time
Mode 2	1	0	Simultaneous with clock edge	Simultaneous with clock edge
Mode 3	1	1	Simultaneous with clock edge	Meet setup and hold time

8.3. Reduced Serial GMII (RSGMII)

To reduce PCB complexity and IC pin count, Realtek offers a proprietary interface; the Realtek Reduced Serial Gigabit Media Independent Interface (RSGMII). This innovative 2.5Gbps serial interface provides an up to 5 inch long MAC to PHY communication path. The RSGMII can carry the full duplex gigabit Ethernet data streams of two ports simultaneously, and recover clock from the data rather than use a dedicated clock. The RSGMII reduces the interconnection between the gigabit Ethernet PHY and MAC to only 4 pins. Figure 13 depicts the RSGMII interconnection.

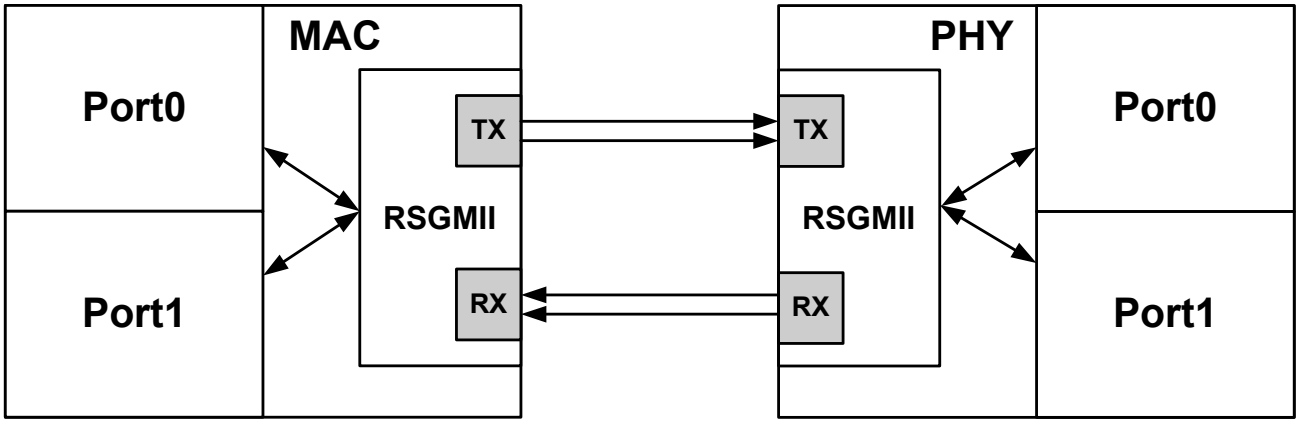


Figure 13. RSGMII Interconnection Diagram

The RSGMII interface runs at 2.5Gbps in 10M/100M/1000Mbps modes. Clearly, a 2.5Gbps data rate is excessive for interfaces operating at 10M/100Mbps. When operating in these conditions, the interface elongates each byte of data by 10 times for 100Mbps, and by 100 times for 10Mbps, through a rate adaptation block.

The data paths and all associated control signals are transmitted from each port and recovered at the receiver side via proprietary transmission encode/decode and Serial/De-serial translation.

Taking the Realtek RTL8369 and RTL8212 as examples (see Figure 14), the RTL8369 contains four RSGMII (4 pairs) and the RTL8212 contains one RSGMII (1 pair). The RTL8369 generates S*n*TX+/-, *n*=0-3 signals to four RTL8212's, and receives S*n*RX+/-, *n*=0-3 signals from four RTL8212's. Each RSGMII carries two gigabits of Ethernet data from PHY to MAC and MAC to PHY.

In traditional GMII applications, the MAC to PHY interface requires at least 20 pins to carry 1 port's bi-directional gigabit Ethernet traffic. A MAC to PHY RSGMII needs only 4 pins to carry two port's gigabit Ethernet traffic. This greatly improves PCB layout size and complexity in gigabit switch design.

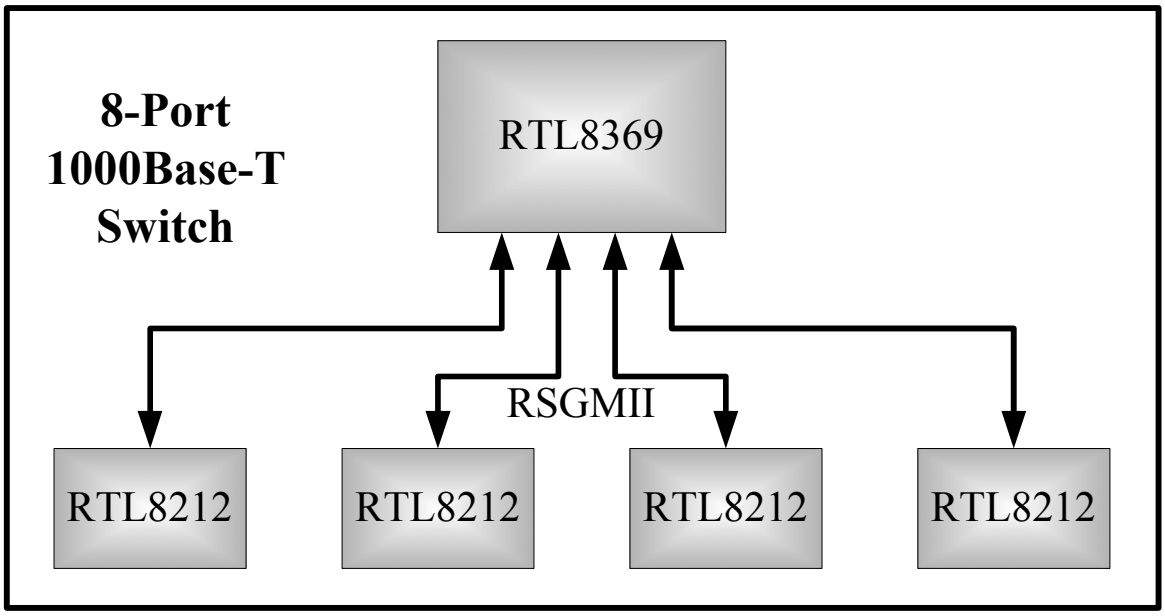


Figure 14. Realtek 8G Switch Application with RSGMII

8.3.1. RSGMII Data Transfer

At the receive side, GMII signals of the two gigabit Ethernet PHY ports enter at 10/100/1000Mbps, clocked at 2.5/25/125MHz. Each port passes these signals through Ethernet PHY receive rate adaptation to output data RXD[7..0] in the 125MHz clock domain. Both RXD are then sent to the individual PCS Transmit State Machine to generate proprietary encoded code-words ***A*** and ***B***. The PHY combines the code-words ***A*** and ***B*** generated from the two ports to a code-word ***C***, and converts it to a serial (bit by bit) stream for the Ethernet MAC at a 2.5Gbps data rate.

At the transmit side, the PHY de-serializes data to recover the encoded code-word ***C***. Next the synchronization block checks the code-word ***C*** to determine the synchronization status between links, and to realign if it detects a loss of synchronization.

The Ethernet PHY separates the synchronous code-word ***C,*** into ***A*** and ***B*** for each port. Each port's code-word is then recovered to the GMII signal in the 125MHz clock domain by passing through individual PCS Receive State Machines. Both the decoded GMII signals have to pass the PHY Transmit Rate Adaptation block to output data segments according to the port speed. The transmitting and receiving operation flow on the Ethernet MAC side is the same as the Ethernet PHY side. Figure 15 and Figure 16 show the functional block diagram at the PHY and MAC side respectively. They illustrate how the PCS layer is modified and incorporated at the PHY and MAC side within the RSGMII interface.

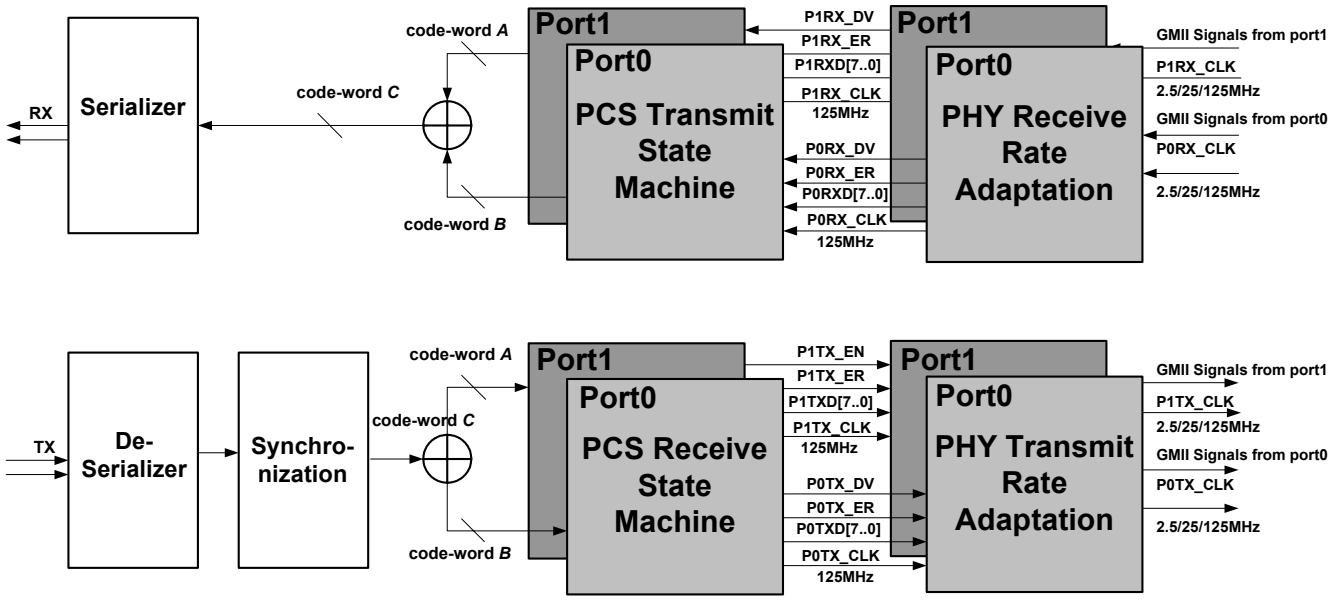


Figure 15. RSGMII Functional Block Diagram at Ethernet PHY Side

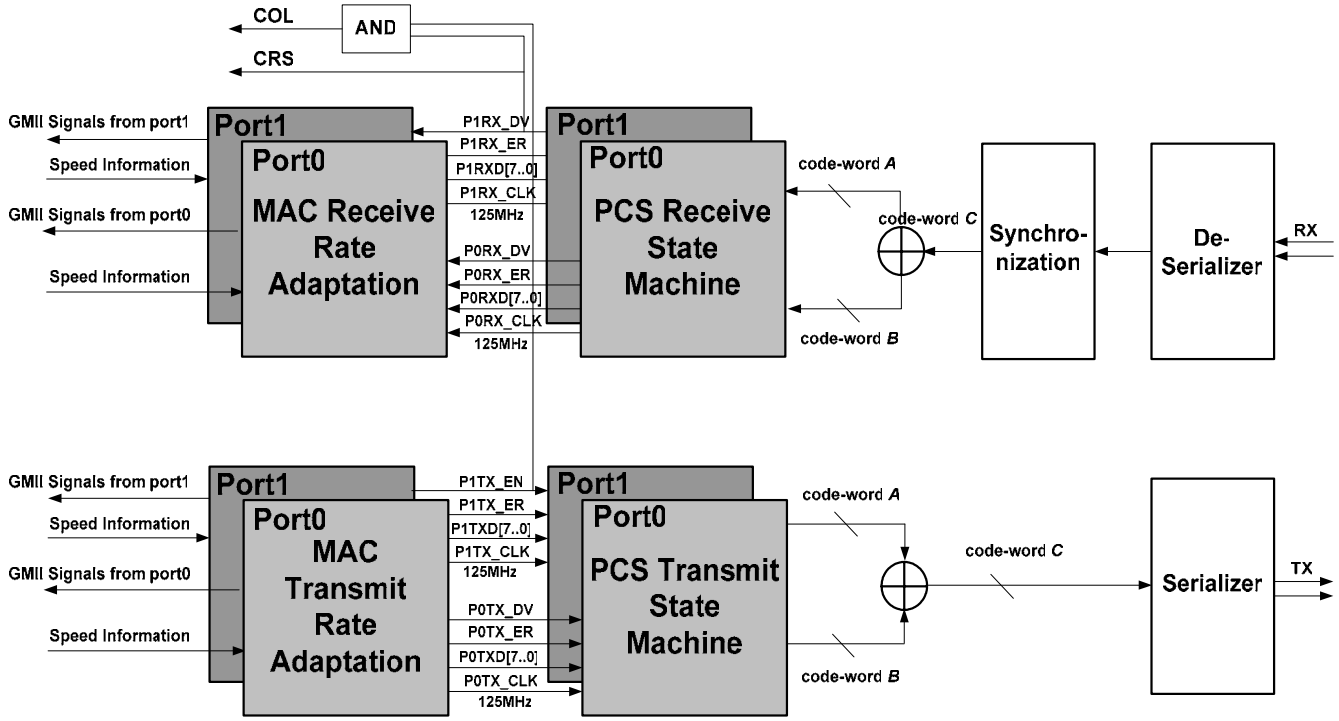


Figure 16. RSGMII Functional Block Diagram at Ethernet MAC Side

8.4. MDC/MDIO Management Interface

The RTL8212 supports the IEEE compliant Management Data Input/Output (MDIO) Interface. This is the only method that the MAC will acquire the statuses of PHY. The MII management interface registers are written and read serially, using the MDC/MDIO pins. Data transferred to and from the MDIO pins is synchronized with the MDC clock. All transfers are initiated by the MAC. A clock of up to 12.5MHz must drive the MDC pin of the RTL8212.

The MDIO frame structure starts with a 32-bit preamble, which is required by the RTL8212. Following bits include a start-of-frame marker, an op-code, a 10-bit address field, and a 16-bit data field. The address field is divided into two 5-bit segments. The first segment identifies the PHY address and the second identifies the register being accessed.

The four uppermost bits of the 5-bit PHY address are determined by the hardware strapping values during power up. The LSB of the PHY address is ‘0’ for Port0 and ‘1’ for Port1. The MDIO protocol provides both read and write operations. During a write operation, the MAC drives the MDIO line for the entire

frame. For a read operation, a turn-around time is inserted in the frame to allow the PHY to drive back to the MAC. The MDIO pin of the MAC must be put in a high-impedance during these bit times. Figure 17 and Figure 18, page 39 depict the MDIO read and write frame format respectively.

8.4.1. Preamble Suppression

The RTL8212 is permanently programmed for preamble suppression. A preamble of 32 bits is required only for the first read or write. The management preamble may be as short as 1 bit.

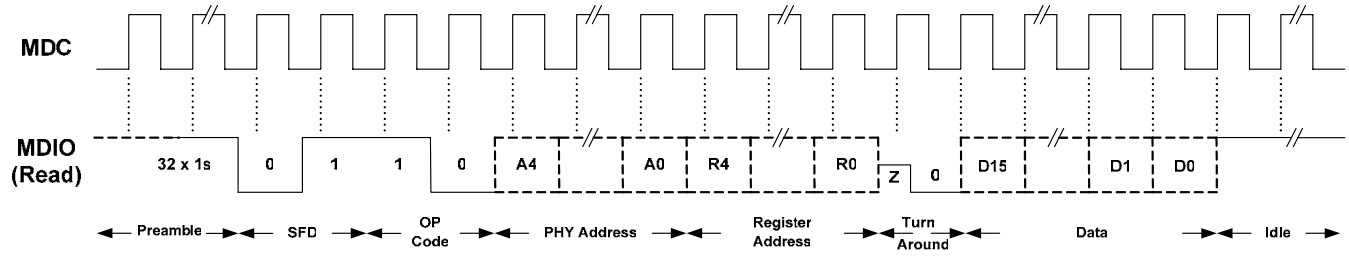


Figure 17. MDIO Read Frame Format

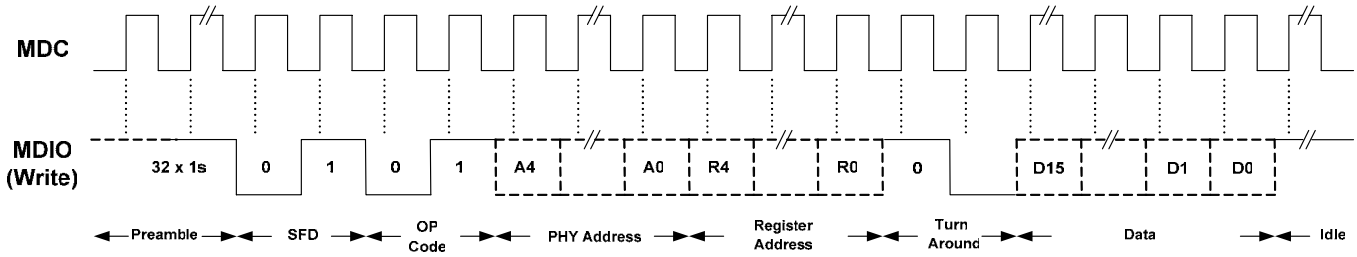


Figure 18. MDIO Write Frame Format

8.5. Hardware Configuration Interface

The RTL8212 is a dual port device. Configuration options like MAC interface, physical address, PHY operating mode are configured by using the configuration pins. These pins are shared with GMII/RGMII receive pins. Except for the PHY operating mode, both ports may be configured independently. Settings are implemented simultaneously after power-on reset. Table 23 shows the configuration definitions.

Table 23. Configuration Pin Definitions

Configuration	Description
INTF_SEL[1:0]	Interface Select: INTF_SEL[1:0] specifies the MAC interface operating mode for both ports. 00=RSGMII 01=GMII/MII 10=RGMII 11=Reserved
PHYADR[4:1]	PHY Address: PHYADR[4:1] sets the uppermost 4 bits of the 5-bit PHY address upon reset. The LSB is '0' for Port 0 and '1'for Port1.
LEDMODE	Serial LED Mode Select: LEDMODE specifies the serial LED display mode for both ports. There are two LED display modes in the RTL8212. 0=Mode 0 1=Mode 1
GTXCLK	GTXCLK Clock Delay Select: GTXCLK determines the GTXCLK input delay in RGMII mode. 0=Output data may change simultaneously with the GTXCLK edges 1=Output data can have setup time and hold time with respect to GTXCLK edges
RXCLK	RXCLK Clock Delay Select: RXCLK determines the RXCLK output delay in RGMII mode. 0=Output data may change simultaneously with the RXCLK edges 1=Output data can have setup time and hold time with respect to RXCLK edges

8.6. LED Configuration

The RTL8212 supports serial LED status streams for LED display. The forms of LED status streams are controlled by LEDMODE pins (see Table 24) which are latched upon reset. All LED statuses are represented as active-low.

Table 24. LED Mode

LED Mode	Output Sequences
0	Dup/Col, Link/Act, Spd1000, Spd100
1	Dup/Col, Spd1000/Act, (Spd100,Spd10)/Act

Table 25. LED Status

LED Status	Description
Col/Fulldup	Collision, Full duplex Indicator. Blinks every 43ms when collision occurs. Low for full duplex, and high for half duplex mode.
Link/Act	Link, Activity Indicator. Low for link established. Blinks every 43ms when the corresponding port is transmitting or receiving.
Spd1000	1000Mbps Speed Indicator. Low for 1000Mbps.
Spd1000/Act	1000Mbps Speed/Activity Indicator. Low for 1000Mbps. Blinks every 43ms when the corresponding port is transmitting or receiving.
(Spd100,Spd10)/Act	10/100Mbps, Speed/Activity Indicator. Low for 10/100Mbps. Blinks every 43ms when the corresponding port is transmitting or receiving.

8.6.1. LED System Application Examples

- 4 single-color LEDs: Link/Act, Spd1000, Spd100, Dup/Col (set LEDMODE=0)
- 3 single-color LEDs: Link/Act, Spd1000, Spd100 (set LEDMODE=0)
- 2 single-color, 1 bi-color LEDs: Link/Act, Dup/Col, Spd1000/Spd100 (set LEDMODE=0)
- 1 single-color, 1 bi-color LED: Dup/Col, Spd100/Spd10/100/Act (set LEDMODE=1)

8.6.2. Serial Stream Order

Every bit stream is output port by port, from port0 to port1 with Col/Fulldup as the first bit in a port stream.

Table 26. Serial Stream Order (Mode 0)

Clock	0	1	2	3	4	5	6	7
Mode 0	Port 0 Dup/Col	Port 0 Link/Act	Port 0 Spd1000	Port 0 Spd100	Port 1 Dup/Col	Port 1 Link/Act	Port 1 Spd1000	Port 1 Spd100
74164 Pin	H	G	F	E	D	C	B	A

Table 27. Serial Stream Order (Mode 1)

Clock	-	-	0	1	2	3	4	5
Mode 1	-	-	Port 0 Dup/Col	Port 0 Spd1000/Act	Port 0 Spd100/Act	Port 1 Dup/Col	Port 1 Spd1000/Act	Port 1 Spd100/Act
74164 Pin	H	G	F	E	D	C	B	A

8.7. System Clock Interface

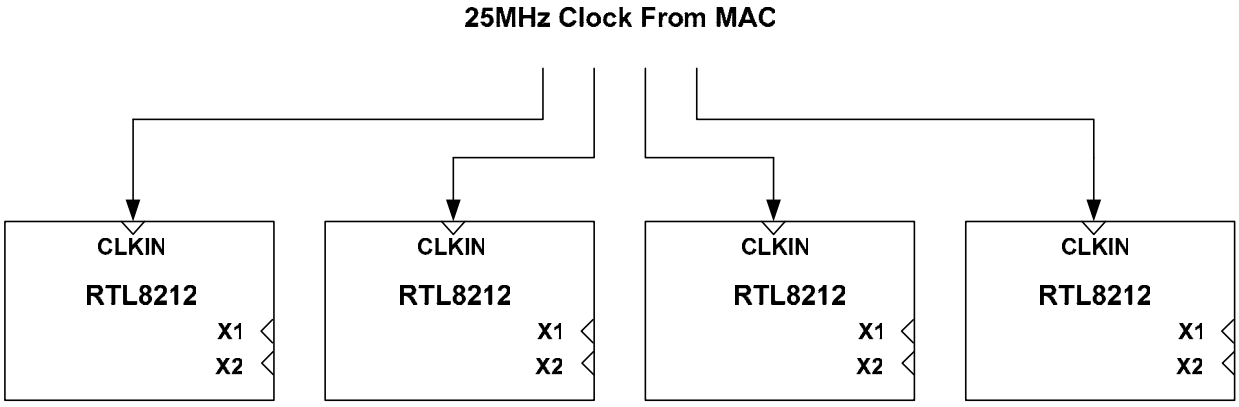


Figure 19. Clock Generated from MAC (RSGMII Mode)

Note: When CLKIN is used, pull the X1 pin low to GND.

8.8. Register Descriptions

The first six registers of the MII are defined by the MII specification. Other registers are defined by Realtek Semiconductor Corp. for internal use and are reserved for specific uses.

8.8.1. Register Symbols

RO: Read Only

RW: Read/Write

LL: Latch Low until cleared

LH: Latch High until cleared

SC: Self Clearing

8.8.2. MII Specification Defined Registers

Table 28. MII Specification Defined Registers

Register	Description	Default
0	Control Register.	0x1140
1	Status Register.	0x7949
2	PHY Identifier 1 Register.	0x001C
3	PHY Identifier 2 Register.	0xC912
4	Auto-Negotiation Advertisement Register.	0x01E1
5	Auto-Negotiation Link Partner Ability Register.	0x0000
6	Auto-Negotiation Expansion Register.	0x0000
7	Auto-Negotiation Page Transmit Register.	0x2001
8	Auto-Negotiation Link Partner Next Page Register.	0x0000
9	1000Base-T Control Register.	0x0F00
10	1000Base-T Status Register.	0x0000
15	Extended Status.	0x3000

8.8.3. Register0: Control

Table 29. Register0: Control

Bit(s)	Name	Description	Mode	Default
0.15	Reset	1=PHY reset 0=Normal operation This bit is self-clearing.	RW/SC	0
0.14	Loopback	This will loopback TXD to RXD and ignore all activity on the cable media. 1=Enable loopback 0=Normal operation	RW	0
0.13	Speed Selection[0]	[0.6,0.13] Speed Selection[1:0]. 11=Reserved 10=1000 Mbps 01=100 Mbps 00=10 Mbps *Note: The SMI: Serial Management Interface which is composed of MDC, MDIO, allows the MAC to manage the PHY.*	RW	0
0.12	Auto Negotiation Enable	This bit can be set through SMI (Read/Write). 1=Enable Auto-negotiation process 0=Disable Auto-negotiation process	RW	1
0.11	Power Down	1=Power down. All functions will be disabled except SMI read/write function 0=Normal operation	RW	0
0.10	Isolate	1=Electrically isolates the PHY from MII/GMII/RGMII/RSGMII. PHY is still able to respond to MDC/MDIO 0 = Normal operation	RW	0
0.9	Restart Auto Negotiation	1=Restart Auto-Negotiation process 0=Normal operation	RW/SC	0
0.8	Duplex Mode	1=Full duplex operation 0=Half duplex operation When Auto-Negotiation is enabled, this bit reflects the result of Auto-Negotiation (Read Only). When Auto-Negotiation is disabled, this bit can be configured through SMI (Read/Write).	RW	1
0.7	Collision Test	1=Collision test enabled 0=Normal operation When set, this bit will cause the COL signal to be asserted in response to the assertion of TXEN within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the de-assertion of TXEN.	RO	0
0.6	Speed Selection[1]	See bit 13.	RW	1
0.[5:0]	Reserved		RO	0

8.8.4. Register1: Status

Table 30. Register1: Status

Bit(s)	Name	Description	Mode	Default
1.15	100Base-T4	0=No 100Base-T4 capability The RTL8212 does not support 100Base-T4 mode. This bit should always be 0.	RO	0
1.14	100Base-X Full Duplex	1=100Base-X full duplex capable 0=Not 100Base-X full duplex capable	RO	1
1.13	100Base-X Half Duplex	1=100Base-X half duplex capable 0=Not 100Base-X half duplex capable	RO	1
1.12	10Mbps Full Duplex	1=10Mbps full duplex capable 0=Not 10Mbps full duplex capable	RO	1
1.11	10Mbps Half Duplex	1=10Mbps half duplex capable 0=Not 10Mbps half duplex capable	RO	1
1.10	100Base-T2 Full Duplex	0=No 100Base-T2 full duplex capability. The RTL8212 does not support 100Base-T2 mode. This bit should always be 0.	RO	0
1.9	100Base-T2 Half Duplex	0=No 100Base-T2 half duplex capability The RTL8212 does not support 100Base-T2 mode. This bit should always be 0.	RO	0
1.8	Extended Status	1=Extended status information in Register 15 The RTL8212 always supports Extended Status Register.	RO	1
1.7	Reserved	Reserved.	RO	0
1.6	MF Preamble Suppression	The RTL8212 will accept management frames with preamble suppressed.	RO	1
1.5	Auto-negotiate Complete	1=Auto-negotiation process completed. 0=Auto-negotiation process not completed.	RO	0
1.4	Remote Fault	1=Remote fault indication from link partner has been detected. 0=No remote fault indication detected. This bit will remain set until it is cleared by reading register 1 via management interface.	RO/LH	0
1.3	Auto-Negotiation Ability	1=Auto-negotiation capable (permanently =1) 0=Without Auto-negotiation capability.	RO	1
1.2	Link Status	1=Link has never failed since previous read 0=Link has failed since previous read If link fails, this bit will be set to 0 until bit is read.	RO/LL	0
1.1	Jabber Detect	1=Jabber detected 0=No Jabber detected Jabber is supported only in 10Base-T mode.	RO/LH	0
1.0	Extended Capability	1=Extended register capable. (permanently =1) 0=Not extended register capable	RO	1

8.8.5. Register2: PHY Identifier 1 Register

The PHY Identifier Registers #1 and #2 together form a unique identifier for the PHY section of this device. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management.

Table 31. Register2: PHY Identifier 1 Register

Reg. bit	Name	Description	Mode	Default
2.[15:0]	OUI	Composed of the 3rd to 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	001C h

8.8.6. Register3: PHY Identifier 2 Register

Table 32. Register3: PHY Identifier 2 Register

Reg. bit	Name	Description	Mode	Default
3.[15:10]	OUI	Assigned to the 19th through 24th bits of the OUI.	RO	110010
3.[9:4]	Model Number	Manufacturer's model number.	RO	010001
3.[3:0]	Revision Number	Manufacturer's revision number.	RO	0010

8.8.7. Register4: Auto-Negotiation Advertisement

This register contains the advertisement abilities of this device as they will be transmitted to its Link Partner during Auto-negotiation.

Table 33. Register4: Auto-Negotiation Advertisement

Reg. bit	Name	Description	Mode	Default
4.15	Next Page	1=Additional next pages exchange desired 0=No additional next pages exchange desired	RW	0
4.14	Reserved	Permanently =0	RO	0
4.13	Remote Fault	1=Set remote fault bit 0=Do not set remote fault bit	RW	0
4.12	Reserved	For future technology	RW	0
4.11	Asymmetric Pause	1=Advertises that the RTL8212 has asymmetric flow control capability 0=No asymmetric flow control capability	RW	0
4.10	Pause	1=Advertises that the RTL8212 has flow control capability. 0= No flow control capability.	RW	0
4.9	100Base-T4	1=100Base-T4 capable 0=Not 100Base-T4 capable (Permanently =0)	RO	0
4.8	100Base-TX-FD	1=100Base-TX full duplex capable 0=Not 100Base-TX full duplex capable	RW	1
4.7	100Base-TX	1=100Base-TX half duplex capable 0=Not 100Base-TX half duplex capable	RW	1
4.6	10Base-T-FD	1=10Base-TX full duplex capable 0=Not 10Base-TX full duplex capable	RW	1
4.5	10Base-T	1=10Base-TX half duplex capable 0=Not 10Base-TX half duplex capable	RW	1
4.[4:0]	Selector Field	[00001]=IEEE802.3	RO	00000

Note 1: The setting of Register 4 has no effect unless auto-negotiation is restarted or link down.
Note 2: If 1000Base-T is advertised, then the required next pages are automatically transmitted.

8.8.8. Register5: Auto-Negotiation Link Partner Ability

This register contains the advertised abilities of the Link Partner as received during Auto-negotiation. The content changes after a successful Auto-negotiation.

Table 34. Register5: Auto-Negotiation Link Partner Ability

Reg. bit	Name	Description	Mode	Default
5.15	Next Page	1=Link partner desires Next Page transfer 0=Link partner does not desire Next Page transfer	RO	0
5.14	Acknowledge	1=Link Partner acknowledges reception of FLP words 0=No acknowledgement by Link Partner	RO	0
5.13	Remote Fault	1=Remote Fault indicated by Link Partner 0=No remote fault indicated by Link Partner	RO	0
5.12	Reserved	Reserved.	RO	0
5.11	Asymmetric Pause	1=Asymmetric Flow control supported by Link Partner 0=No Asymmetric flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability. (read only).	RW	0
5.10	Pause	1=Flow control supported by Link Partner 0=No flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability. (read only)	RO	0
5.9	100Base-T4	1=100Base-T4 supported by Link Partner 0=100Base-T4 not supported by Link Partner	RO	0
5.8	100Base-TX-FD	1=100Base-TX full duplex supported by Link Partner 0=100Base-TX full duplex not supported by Link Partner	RO	0
5.7	100Base-TX	1=100Base-TX half duplex supported by Link Partner 0=100Base-TX half duplex not supported by Link Partner	RO	0
5.6	10Base-T-FD	1=10Base-TX full duplex supported by Link Partner 0=10Base-TX full duplex not supported by Link Partner	RO	0
5.5	10Base-T	1=10Base-TX half duplex supported by Link Partner 0=10Base-TX half duplex not supported by Link Partner	RO	0
5.[4:0]	Selector Field	[00001]=IEEE802.3 [00000]=No Information form Link Partner	RO	00000

8.8.9. Register6: Auto-Negotiation Expansion

Table 35. Register6: Auto-Negotiation Expansion

Reg. bit	Name	Description	Mode	Default
6.[15:5]	Reserved		RO	0
6.4	Parallel Detection Fault	1=A fault has been detected via the Parallel Detection function 0=No fault has been detected via the Parallel Detection function\	RO	0
6.3	Link Partner Next Page Ability	1=Link Partner is Next Page able 0=Link Partner is not Next Page able	RO	0
6.2	Local Next Page Ability	1= RTL8212 is Next Page able (permanently=1)	RO	1
6.1	Page Received	1=A New Page has been received 0=A New Page has not been received	RO/LH	0
6.0	Link Partner Auto-Negotiation Ability	If Auto-Negotiation is enabled, this bit means: 1=Link Partner is Auto-Negotiation able. 0=Link Partner is not Auto-Negotiation able	RO	0

8.8.10. Register7: Auto-Negotiation Page Transmit Register

Table 36. Register7: Auto-Negotiation Page Transmit Register

Reg. bit	Name	Description	Mode	Default
7.15	Next Page	1=Another next page desired 0=No next page to send	RW	0
7.14	Reserved		RO	0
7.13	Message Page	1=Message page	RW	1
7.12	Acknowledge 2	1=Local device has the ability to comply with the message received 0=Local device has no ability to comply with the message received.	RW	0
7.11	Toggle	Toggle bit.	RO	0
7.10:0	Message/Unformatted Field	Content of message/unformatted page.	RW	0x001

8.8.11. Register8: Auto-Negotiation Link Partner Next Page Register

Table 37. Register8: Auto-Negotiation Link Partner Next Page Register

Reg. bit	Name	Description	Mode	Default
8.15	Next Page	Received link code word bit 15.	RO	0
8.14	Acknowledge	Received link code word bit 14.	RO	0
8.13	Message Page	Received link code word bit 13.	RO	0
8.12	Acknowledge 2	Received link code word bit 12.	RO	0
8.11	Toggle	Received link code word bit 11.	RO	0
8.10:0	Message/Unformatted Field	Received link code word bit 10:0.	RO	0x000

8.8.12. Register9: 1000Base-T Control Register

Table 38. Register9: 1000Base-T Control Register

Reg. bit	Name	Description	Mode	Default
9.15:13	Test Mode	Test mode select: 000=Normal mode 001=Test mode 1 – Transmit waveform test 010=Test mode 2 – Transmit jitter test in MASTER mode 011=Test mode 3 – Transmit jitter test in SLAVE mode 100=Test mode 4 – Transmitter distortion test 101, 110, 111=Reserved	RW	000
9.12	MASTER/SLAVE Manual Configuration Enable	1=Enable MASTER/SLAVE manual configuration 0=Disable MASTER/SLAVE manual configuration	RW	0
9.11	MASTER/SLAVE Configuration Value	1=Configure PHY as MASTER during MASTER/SLAVE negotiation, only when 9.12 is set to logical one 0=Configure PHY as SLAVE during MASTER/SLAVE negotiation, only when 9.12 is set to logical one	RW	1
9.10	Port Type	1=Multi-port device 0=Single-port device	RW	1
9.9	1000Base-T Full Duplex	1=Advertise PHY is 1000Base-T full duplex capable 0=Advertise PHY is not 1000Base-T full duplex capable	RW	1
9.8	1000Base-T Half Duplex	1=Advertise PHY is 1000Base-T half duplex capable 0=Advertise PHY is not 1000Base-T half duplex capable	RW	0
9.7:0	Reserved	Reserved.	RW	0

8.8.13. Register10: 1000Base-T Status Register

Table 39. Register10: 1000Base-T Status Register

Reg. bit	Name	Description	Mode	Default
10.15	MASTER/SLAVE Configuration Fault	1=MASTER/SLAVE configuration fault detected 0=No MASTER/SLAVE configuration fault detected	RO	0
10.14	MASTER/SLAVE Configuration Fault Resolution	1=Local PHY configuration resolved to MASTER 0=Local PHY configuration resolved to SLAVE	RO	0
10.13	Local Receiver Status	1=Local receiver OK 0=Local receiver not OK	RO	0
10.12	Remote Receiver Status	1=Remote receiver OK 0=Remote receiver not OK	RO	0
10.11	Link Partner 1000Base-T Full Duplex	1=Link partner is capable of 1000Base-T full duplex 0=Link partner is not capable of 1000Base-T full duplex	RO	0
10.10	Link Partner 1000Base-T Half Duplex	1=Link partner is capable of 1000Base-T half duplex 0=Link partner is not capable of 1000Base-T half duplex	RO	0
10.9:8	Reserved	Reserved	RO	0
10.7:0	Idle Error Count	Idle error counter. The counter stops automatically when it reaches 0xFF	RO	0

8.8.14. Register15: Extended Status

Table 40. Register15: Extended Status

Reg. bit	Name	Description	Mode	Default
15.15	1000Base-X Full Duplex	0=1000Base-X full duplex not capable	RO	0
15.14	1000Base-X Half Duplex	0=1000Base-X half duplex not capable	RO	0
15.13	1000Base-T Full Duplex	1=1000Base-T full duplex capable	RO	1
15.12	1000Base-T Half Duplex	0=1000Base-T half duplex not capable	RO	0
15.11:0	Reserved	Reserved	RO	0

9. Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability may be affected. All voltages are specified reference to GND unless otherwise specified.

Table 41. Absolute Maximum Ratings

Parameter	Min	Max	Units
Storage Temperature	-55	+150	°C
Supply Voltage Referenced to VSS12 ,AVSS, AVSSPLL: VDD12, AVDD12, SVDD12 and AVDDPLL	GND-0.5	+1.32	V
Supply Voltage Referenced to AVSS: AVDD18 and SVDD18	GND-0.5	+1.98	V
Supply Voltage Referenced to AVSS: AVDD33, RVDD33	GND-0.5	+3.63	V
Digital Input Voltage	GND-0.5	VDDD	V
DC Output Voltage	GND-0.5	VDDD	V

9.2. Operating Range

Table 42. Operating Range

Parameter	Min	Max	Units
Ambient Operating Temperature (Ta)	0	+65	°C
1.2V VDDD, VDDA, and VDDIO Supply Voltage Range	1.14	1.26	V
1.8V VDDD, VDDA, and VDDIO Supply Voltage Range	1.71	1.89	V
3.3V VDDIO Supply Voltage Range	3.14	3.46	V

9.3. DC Characteristics

Table 43. DC Characteristics

Parameter	SYM	Condition	Min	Typical	Max	Units
Power Supply Current for Analog 1.2V	Icc	10Base-T, Idle	40	45	50	mA
		10Base-T, Peak continuous 100% utilization	40	45	50	
		100Base-TX, Idle	40	45	50	
		100Base-TX, Peak continuous 100% utilization	40	45	50	
		1000Base-T, Idle	40	45	50	
		1000Base-T, Peak continuous 100% utilization	40	45	50	
		Power saving	40	45	50	
Power Supply Current for Digital 1.2V	Icc	10Base-T, Idle	15	20	30	mA
		10Base-T, Peak continuous 100% utilization	15	20	30	
		100Base-TX, Idle	15	20	30	
		100Base-TX, Peak continuous 100% utilization	105	110	120	
		1000Base-T, Idle	105	110	120	
		1000Base-T, Peak continuous 100% utilization	450	460	480	
		Power saving	470	480	500	
			15	20	30	
Power Supply Current for Analog 1.8V	Icc	10Base-T, Idle	5	10	15	mA
		10Base-T, Peak continuous 100% utilization	5	10	15	
		100Base-TX, Idle	90	100	110	
		100Base-TX, Peak continuous 100% utilization	90	100	110	
		1000Base-T, Idle	190	200	210	
		1000Base-T, Peak continuous 100% utilization	190	200	210	
		Power saving	5	10	15	
Power Supply Current for Analog 3.3V	Icc	10Base-T, Idle	60	70	80	mA
		10Base-T, Peak continuous 100% utilization	230	240	250	
		100Base-TX, Idle	50	60	70	
		100Base-TX, Peak continuous 100% utilization	50	60	70	
		1000Base-T, Idle	110	120	150	
		1000Base-T, Peak continuous 100% utilization	110	120	150	
		Power saving	40	50	60	

Parameter	SYM	Condition	Min	Typical	Max	Units
Total Power Consumption for all ports	PS	10Base-T, Idle 10Base-T, Peak continuous 100% utilization 100Base-TX, Idle 100Base-TX,Peak continuous 100% utilization 1000Base-T, Idle 1000Base-T, Peak continuous 100% utilization Power saving	273 834 393 501 1293 1317 207	327 888 456 564 1362 1386 261	387 948 525 633 1509 1533 321	mW
TTL Input High Voltage	V_{ih}		2.0	-	-	V
TTL Input Low Voltage	V_{il}		-	-	0.8	V
TTL Input Current	I_{in}		-10	-	10	uA
TTL Input Capacitance	C_{in}		-	3	-	pF
Output High Voltage	V_{oh}		2.2	-	2.8	V
Output Low voltage	V_{ol}		0.0	-	0.4	V
Output Three State Leakage Current	$\|I_{OZ}\|$		-	-	10	µA

9.4. AC Characteristics

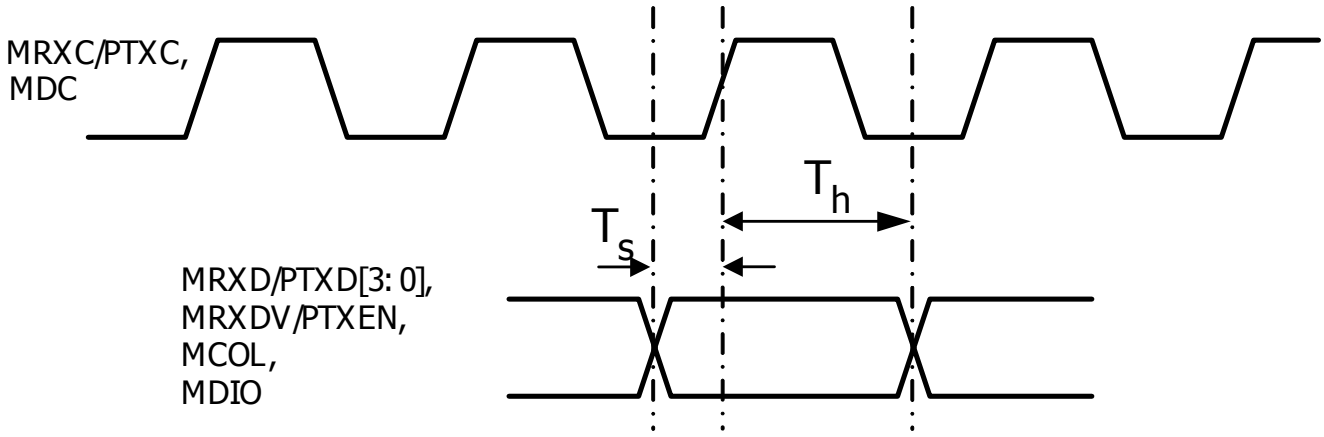


Figure 20. MII Interface Reception Data Timing

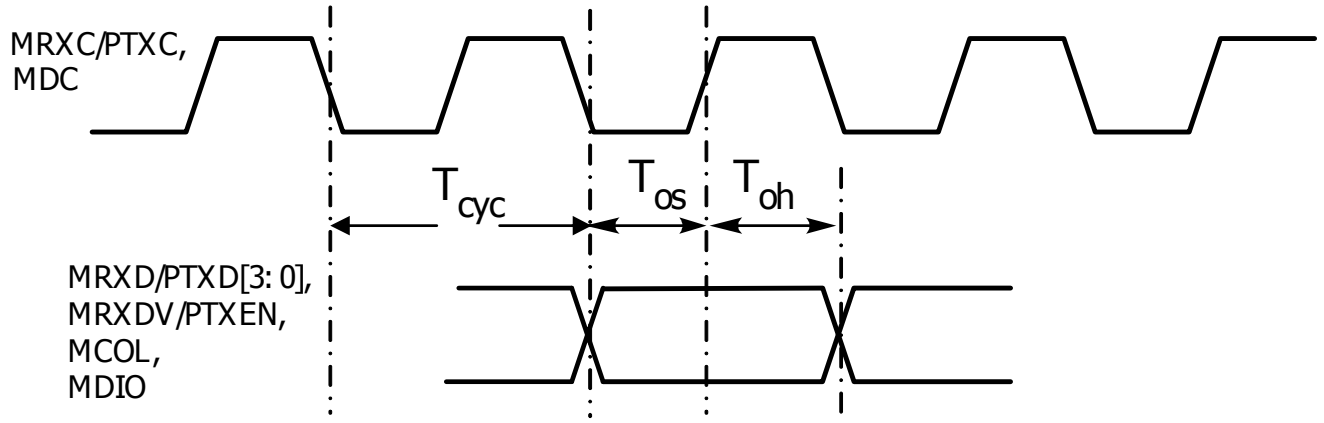


Figure 21. MII Interface Transmission Data Timing

Table 44. Digital Timing Characteristics

Parameter	SYM	Condition	I/O	Min	Typ	Max	Units
MII Mode Timing							
100BaseT RXC, TXC	T_{cyc}	RXC,TXC clock cycle time	O		40±50 ppm		ns
10BaseT RXC, TXC,	T_{cyc}	RXC,TXC clock cycle time	O		400±50 ppm		ns
RXD[3:0], RXDV, PCOL, Output Setup time	T_{os}	Output Setup time from RXC rising edge to RXD[3:0], RXDV, COL	O	21	23	25	ns
RXD[3:0], RXDV, COL, Output Hold time	T_{oh}	Output Hold time from RXC rising edge to RXD[3:0], RXDV, COL	O	13	15	18	ns
TXD[3:0], TXEN, Setup time	T_s	TXD[3:0], TXEN to TXC rising edge setup time	I	4			ns
TXD[3:0], TXEN, Hold time	T_h	TXD[3:0], TXEN to TXC rising edge hold time	I	2			ns
GMII Mode Timing							
RXC	T_{cyc}	RXC clock cycle time	O		100±50 ppm		ns
RXD[7:0],RXDV, COL Output Setup time	T_{os}	Output Setup time from RXC rising edge to RXD[0..7], RXDV, COL	O	5.4	6.6	-	ns
RXD[7:0], RXDV, COL Output Hold time	T_{oh}	Output Hold time from RXC rising edge to RXD[0..7], RXDV, COL	O	0.9	1.2	-	ns
RGMII Mode Timing							
RXC	T_{cyc}	RXC clock cycle time	O		100±50 ppm		ns
RXD[3:0],RXCTL Output Setup time (When RXDLY=1)	T_{os}	Output Setup time from RXC rising/falling edge to RXD[0..3], RXCTL	O	1.35	1.6	1.8	ns
RXD[3:0], RXCTL Output Hold time (When RXDLY=1)	T_{oh}	Output Hold time from RXC rising/falling edge to RXD[0..3], RXCTL	O	2.2	2.4	2.7	ns
RGMII Signal Rising Time	T_r	RGMII Signals 20% to 80% rising time	O			0.75	ns
RGMII Signal Rising Time	T_f	RGMII Signals 80% to 20% falling time	O			0.75	ns
LED Timing							
LED On Time	tLED on	While LED blinking	O		43		ms
LED Off Time	tLED off	While LED blinking	O		43		ms

10. Design and Layout Guide

In order to achieve maximum performance using the RTL8212, good design attention is required throughout the design and layout process. The following are some recommendations on how to implement a high performance system.

10.1. General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits (<100mV).
- Verify the ability of critical components, e.g. clock source and transformer, to meet application requirements.
- Use bulk capacitors (4.7µF-10µF) between the power and ground planes.
- Use 0.1µF de-coupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep de-coupling capacitors as close as possible to the RTL8212 (within 200 mil).
- The transformer should be placed as close as possible to the RTL8212 (within 12cm).
- The RJ-45 phone jack should be placed as close as possible to the transformer.
- Prevent right angles on all traces.

10.2. MII/GMII/RGMII Signal Layout Guidelines

- Keep inter trace spacing with 3 times of trace width, to reduce crosstalk. (For example, the width of signal trace is 6 mil, the inter trace spacing should be 18 mil or more).
- For traces longer than 5 inches guard traces should be place between signal traces, the guard traces should have many vias to GND.
- Place source termination resisters near output pins.

10.3. RSGMII Signal Layout Guidelines

- Ensure the differential pairs maintain 100 ohm impedance
  - (5/7/5 for 4 Layer PCB: Trace width 5 mil, inter-pair spacing 7 mil, dielectric layer thickness 4.4 mil)
  - (9/6/9 for 2 Layer PCB: Trace width 9 mil, inter-pair spacing 6 mil, dielectric layer thickness 59 mil)
- Separate the differential pair and other signals by at least 30mil.
- Keep intra-pair length mismatch less than 5mil.
- Place AC coupling capacitors near output pins of differential pairs.
- Route both traces of differential pairs symmetrically.
- Avoid vias on differential pairs.

10.4. Ethernet MDI Differential Signal Layout Guidelines

- Ensure the differential pairs maintain 100 ohm impedance and route both traces as identically as possible.
- Keep intra-pair length mismatch less than 50mil (From IC to transformer and Form Transformer to RJ-45).
- Avoid vias on differential pairs.
- Maintain a 30mil minimum gap between differential pairs.

10.5. Clock Circuit

- The clock should be 25M +/-50ppm with jitter less than 0.5ns.
- If possible, surround the clock by ground trace to minimize high-frequency emissions.

10.6. Power Planes

- Divide the power plane into 1.2V digital, 1.2V analog, 1.8V analog and 3.3V analog.
- Use 0.1µF decoupling capacitors and bulk capacitors between each power plane and ground plane.

10.7. Ground Plane

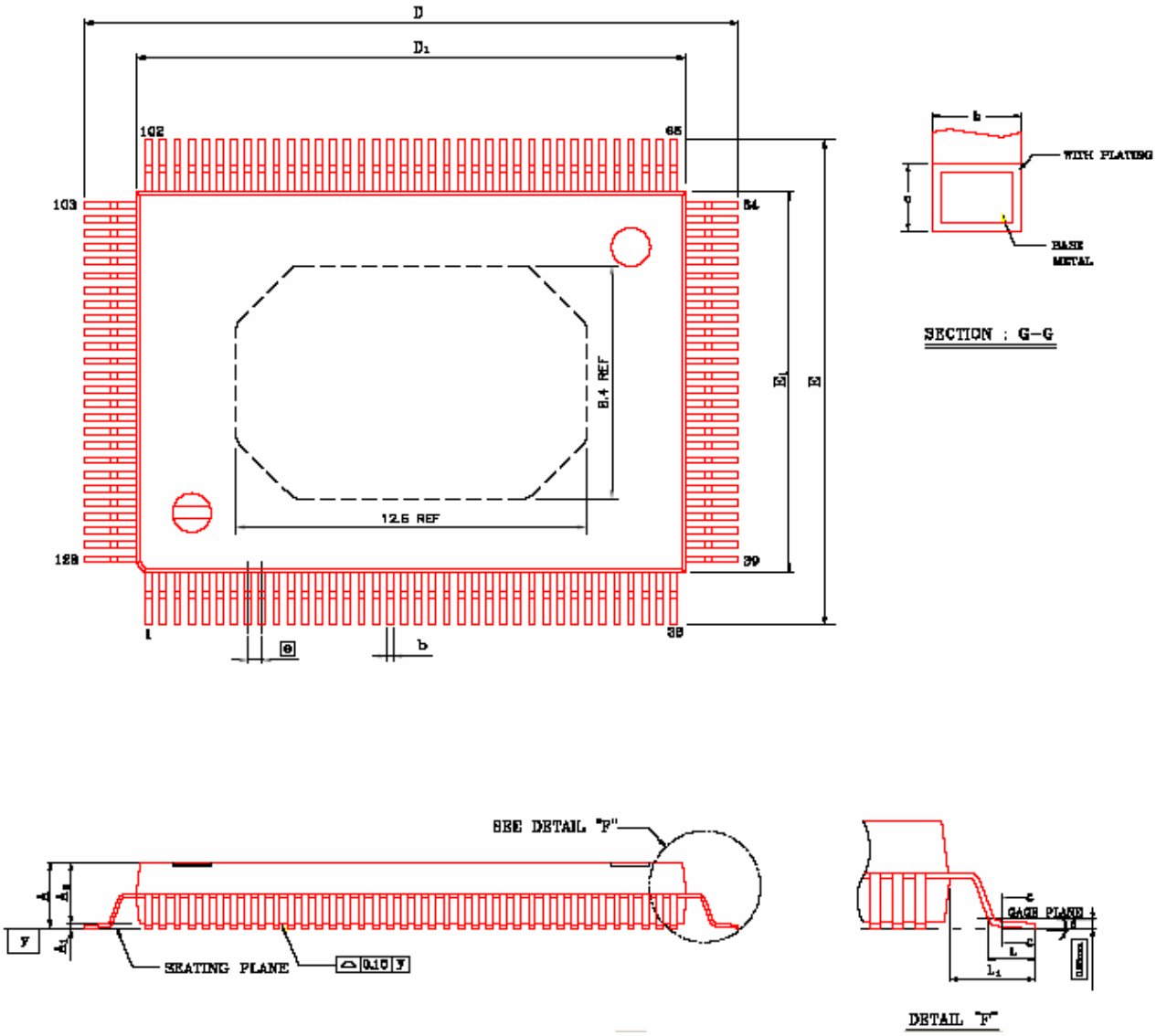
- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board.
- Isolate AVSS pin of RTL8212 (Pin 46,48 on QFN76) (Pin 84,86 on QFP128,if RSGMII interface selected) with system ground by beads.
- Place a moat (gap) between the system ground and chassis ground.
- Ensure the chassis ground area is voided at some point such that no ground loop exists on the chassis ground area.

10.8. Transformer Options

The RTL8212 uses a transformer with a 1:1 turn ratio. There are many venders offering transformer designs that meet the RTL8212's requirement. Such as Pulse H5014,Bothhand GS5014, Lankom LG4803S.

11. Mechanical Dimensions

11.1. EDHS-QFP-128 Dimensions



See the Mechanical Dimensions notes on the next page.

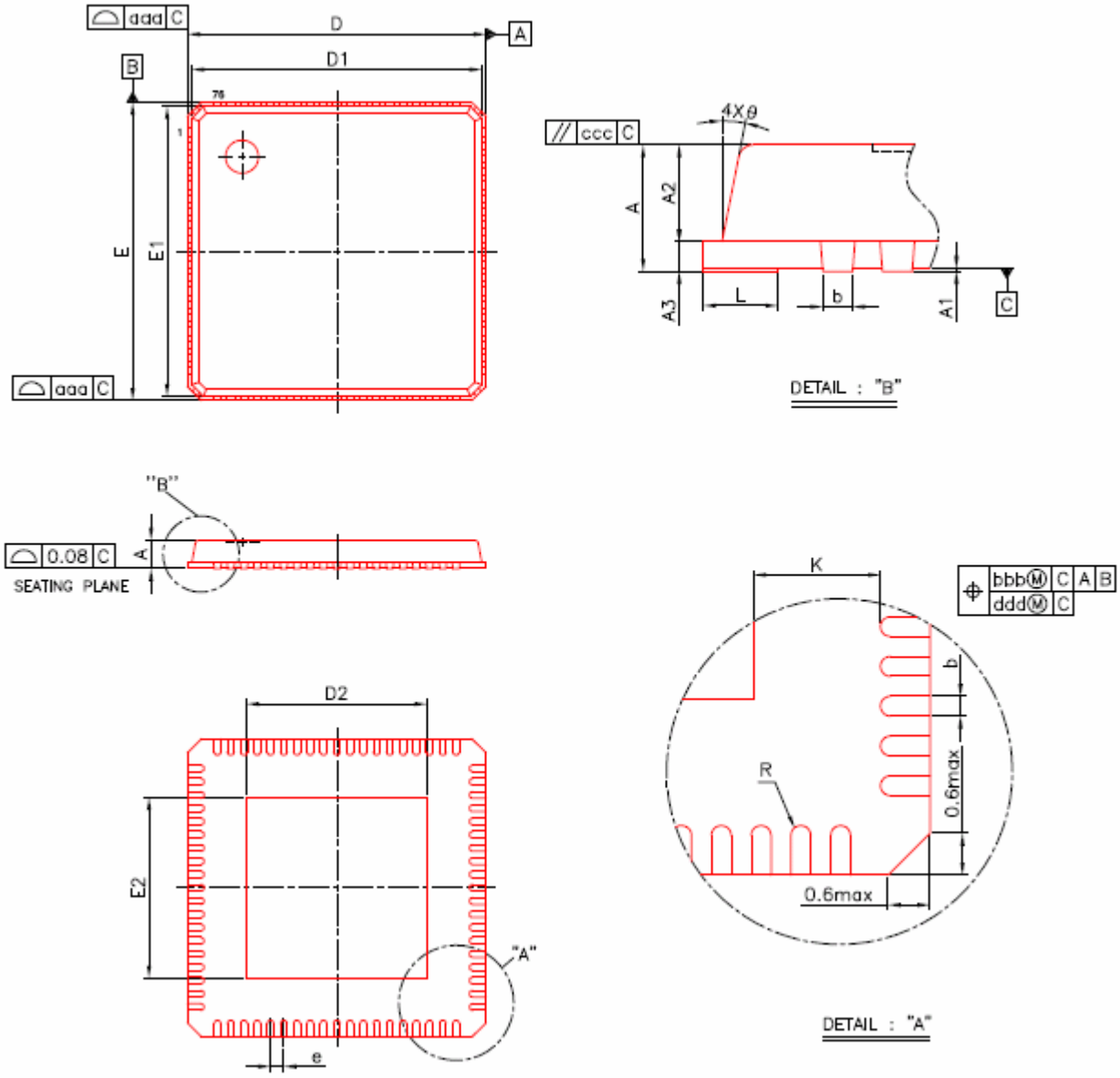
11.2. Notes for EDHS-QFP-128 Dimensions

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.134	—	—	3.40
A_1	0.010	—	—	0.25	—	—
A_2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	—	0.008	0.09	—	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.50 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L_1	0.063 BSC			1.60 BSC		
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

NOTE:

1. DIMENSIONS D_1 AND E_1 DO NOT INCLUDE MOLD PROTRUSION. BUT MOLD MISMATCH IS INCLUDED. ALLOWABLE PROTRUSION IS .25mm/.010" PER SIDE.
2. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION .08mm/.003". TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT .
3. CONTROLLING DIMENSION : MILLIMETER.

11.3. QFN-76 Dimensions



See the Mechanical Dimensions notes on the next page.

11.4. Notes for QFN-76 Dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	9.00 BSC			0.354 BSC		
D1	8.75 BSC			0.344 BSC		
D2	5.30	5.45	5.60	0.209	0.215	0.220
E	9.00 BSC			0.354 BSC		
E	8.75 BSC			0.344 BSC		
E2	5.30	5.45	5.60	0.209	0.215	0.220
e	0.40 BSC			0.016 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
θ	0°	---	12°	0°	---	12°
R	0.065	---	---	0.003	---	---
K	0.20	---	---	0.008	---	---
aaa	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
chamfer	---	---	0.60	---	---	0.024

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: PROPSED JEDEC MO-220.

12. Ordering Information

Table 45. Ordering Information

Part Number	Package	Status
RTL8212-GR	EDHS QFP-128 in 'Green' package	
RTL8212-N-GR	QFN-76 in 'Green' package	

Note: See page 13 and 14 for package identification information.

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