RTL8221B(I)-VB-CG
RTL8221B(I)-VM-CG

INTEGRATED 10/100/1000M/2.5G ETHERNET TRANSCEIVER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

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Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

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- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2020/07/30	First Release.

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1. General Description

The Realtek RTL8221B(I)-VB-CG/RTL8221B(I)-VM-CG (hereafter referred to as the RTL8221B(I)-VB/RTL8221B(I)-VM, except where differences exist) is a highly integrated Ethernet PHY transceiver that is compatible with 10BASE-Te, 100BASE-TX, 1000BASE-T, and 2.5GBASE-T, and is fully compatible with both the IEEE 802.3 standard and the NBASE-T™ Alliance PHY. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over CAT.5e UTP cable. The RTL8221B(I)-VM provides a MACsec feature of IEEE MAC Security Standard protocol. The integrated functionality with MACsec security engines separate egress and ingress traffic and provides data integrity check, confidentiality and replay protect.

The RTL8221B(I)-VB/RTL8221B(I)-VM uses state-of-the-art DSP technology and Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, MDI swap, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, RFI protection, thermal management, loopback diagnostic capability, and error correction are implemented in the RTL8221B(I)-VB/RTL8221B(I)-VM to provide robust transmission and reception capabilities.

Data transfer between MAC and PHY is via the SERDES (Serializer-Deserializer) interface, which supports SGMII, HiSGMII, and 2500Base-X. The RTL8221B(I)-VB/RTL8221B(I)-VM operates at various digital I/O voltages, including 3.3V and 1.8V.

2. Features

- Compatible with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
- Supports IEEE 802.3az (Energy Efficient Ethernet)
- Supports IEEE 802.3bz (2.5GBASE-T)
- Support MACsec compatible with IEEE 802.1AE, IEEE 802.1AEbn, IEEE 802.1AEbw (RTL8221B(I)-VM only)
- Supports Full Duplex flow control (IEEE 802.3x)
- Supports IEEE 802.3 optional ability (Energy Efficient Ethernet and Fast Retrain)
- Integrated 10M BASE-Te and 100M/1000M/2.5GBASE-T IEEE 802.3 compatible transceiver
- Supports 2.5G Lite (1G data rate) mode
- Auto-Negotiation with Extended Next Page capability (XNP)
- Compatible with NBASE-T™ Alliance PHY Specification
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Configurable MDI port ordering (MDI swap) for easy PCB layout
- Supports hardware CRC (Cyclic Redundancy Check) function
- Supports power down/link down power saving mode
- Supports clause 22 and Clause 45 MDC/MDIO management interface
- Supports rate adaptor for SerDes
- Selectable SERDES interface to MAC control (SGMII/HiSGMII/2500 BASE-X)
- Built-in Wake-on-LAN (WOL) over UTP
- Supports Interrupt function over UTP
- Supports Parallel Detection
- Supports PHYRSTB core power Turn-Off
- Baseline Wander Correction
- Selectable 3.3/1.8V signaling for MMD access
- Supports 25MHz crystal or external OSC
- Provides 25MHz clock source for MAC
- Provides 3 network customized LEDs with controllable LED Blinking Frequency and Duty Cycle
- Self-Loopback diagnostic capability
- Thermal management on PHY
- 48-pin QFN Green Package
- 22nm process with ultra-low power consumption
- Complete hardware support for Synchronous Ethernet and Precision Time Protocol (PTP) including IEEE 1588v1, v2, and 802.1AS
- Supports SPI Flash (up to 24MB flash size)
- Industrial grade manufacturing process (RTL8221BI-VB/ RTL8221BI-VM)

3. System Applications

- DTV (Digital TV)
- MAU (Media Access Unit)
- CNR (Communication and Network Riser)
- Game Console
- Printer and Office Machine
- DVD Player and Recorder
- Ethernet Hub
- Ethernet Switch
- Base Stations and Controllers
- Routers, DSLAMs, PON Equipment
- Test and Measurement Systems
- Industrial and Factory Automation Equipment
- Multimedia synchronization and Real Time Networking

3.1. System Application Diagram

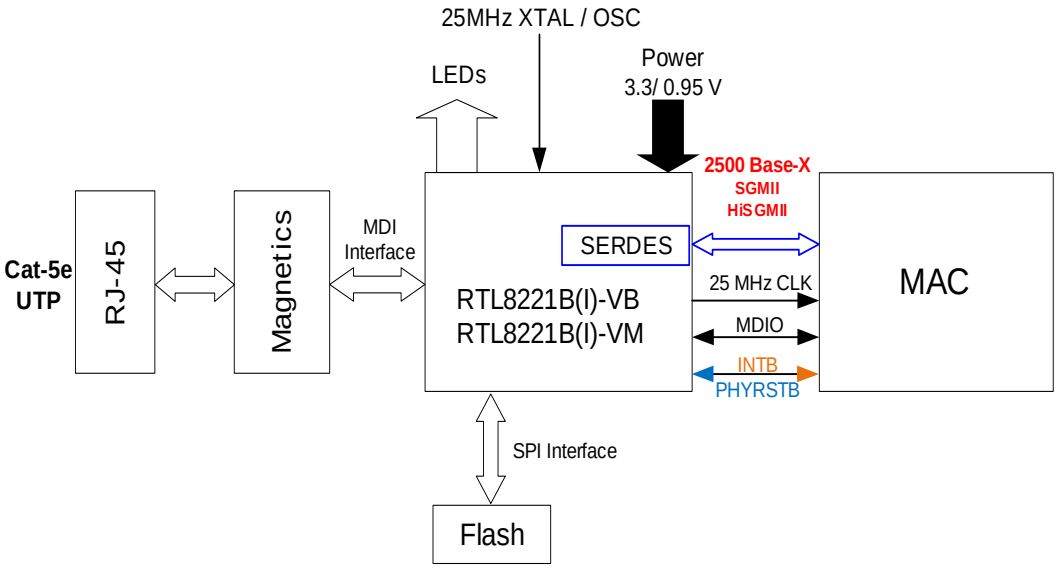


Figure 1. System Application Diagram

4. Block Diagrams

4.1. RTL8221B(I)-VB Block Diagram

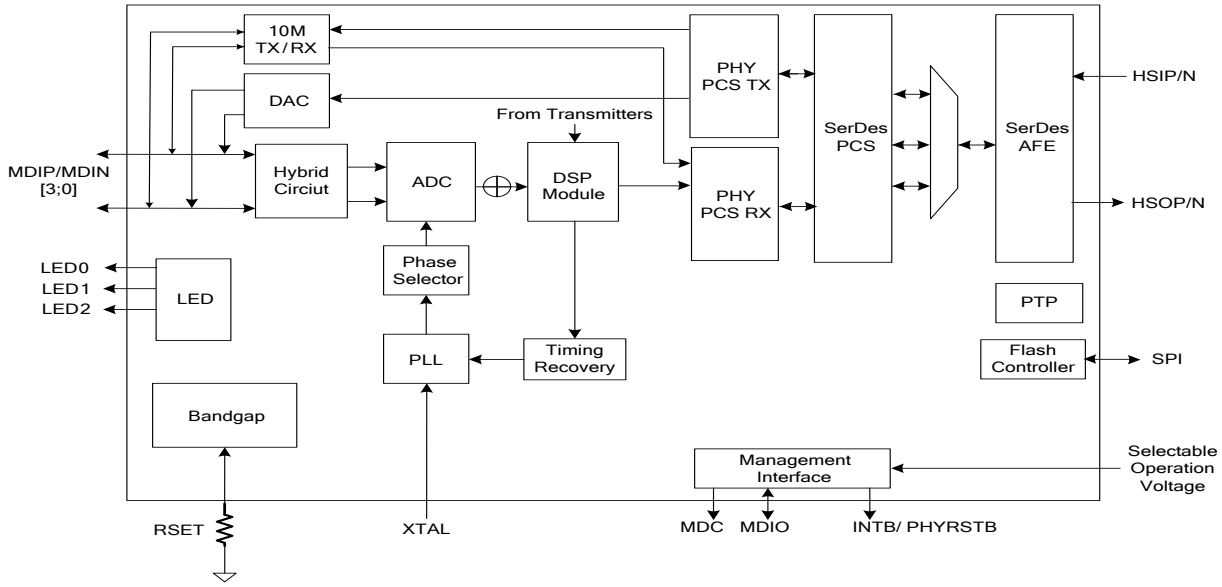


Figure 2. RTL8221B(I)-VB Block Diagram

4.2. RTL8221B(I)-VM Block Diagram

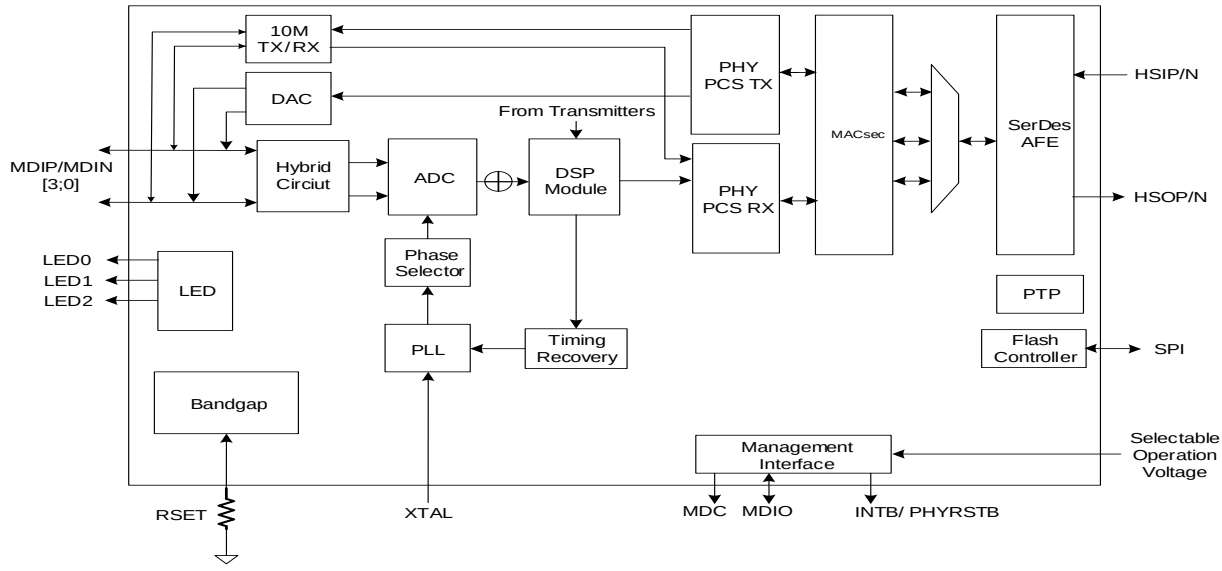


Figure 3. RTL8221B(I)-VM Block Diagram

5. Pin Assignments

5.1. RTL8221B(I)-VB/VM Pin Assignments

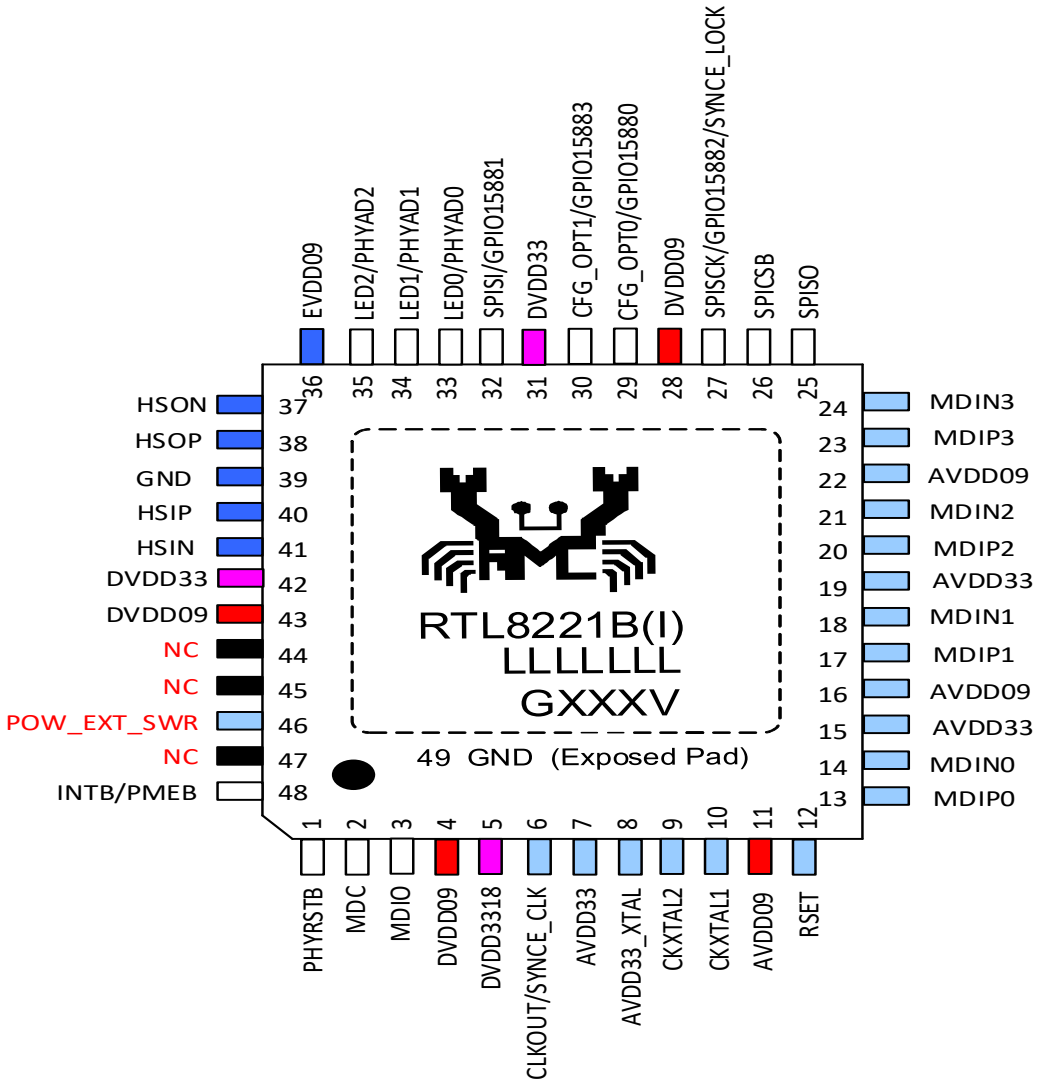


Figure 4. RTL8221B(I)-VB/VM Pin Assignments

5.2. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 4). The letter in the 'V' location indicates the IC version; 'B' is used for 'VB', and 'M' is used for 'VM'.

6. Pin Descriptions

Some pins have multiple functions. Refer to the Pin Assignment figures for a graphical representation.

I:	Input	LI:	Latched Input During Power up or Hardware Reset
O:	Output	IO:	Bi-Directional Input and Output
P:	Power	PD:	Internal Pull Down During Power On Reset
PU:	Internal Pull Up During Power On Reset	OD:	Open Drain
G:	Ground	I_c:	Operation Power Compatible Input

6.1. Transceiver Interface

Table 1. Transceiver Interface

Pin No.	Pin Name	Type	Description
13	MDIP0	IO	In MDI mode, this is the first pair in 2.5GBASE-T, 1000BASE-T, i.e., the BI_DA+/- pair, and is the transmit pair in 10BASE-Te and 100BASE-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10BASE-Te and 100BASE-TX. If MDI swap is set, this pair is BI_DD+/- in MDI mode and is BI_DC+/- in MDI crossover mode.
14	MDIN0	IO	
17	MDIP1	IO	In MDI mode, this is the second pair in 2.5GBASE-T, 1000BASE-T, i.e., the BI_DB+/- pair, and is the receive pair in 10BASE-Te and 100BASE-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10BASE-Te and 100BASE-TX. If MDI swap is set, this pair is BI_DC+/- in MDI mode and is BI_DD+/- in MDI crossover mode.
18	MDIN1	IO	
20	MDIP2	IO	In MDI mode, this is the third pair in 2.5GBASE-T, 1000BASE-T, i.e., the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair. If MDI swap is set, this pair is BI_DB+/- in MDI mode and is BI_DA+/- in MDI crossover mode.
21	MDIN2	IO	
23	MDIP3	IO	In MDI mode, this is the fourth pair in 2.5GBASE-T, 1000BASE-T, i.e., the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair. If MDI swap is set, this pair is BI_DA+/- in MDI mode and is BI_DB+/- in MDI crossover mode.
24	MDIN3	IO	

Note: BI_DA+/-, BI_DB+/-, BI_DC+/-, BI_DD+/- means the logical wire-pairs as described in IEEE 802.3 standard.
The MDI swap register /XFMR pin definition.

6.2. Clock

Table 2. Clock

Pin No.	Pin Name	Type	Description
10	CKXTAL1	I	25MHz Crystal Input. If a 25MHz oscillator is used, connect CKXTAL1 pin to the oscillator's output.
9	CKXTAL2	O	25MHz Crystal Output. Keep this pin floating if an external 25MHz oscillator drives CKXTAL1 pin.
6	CLKOUT	O	25MHz clock out for SOC. Keep this pin floating if do not use this clock.

6.3. SERDES

Table 3. SERDES

Pin No.	Pin Name	Type	Description
38	HSOP	O	SERDES Differential Output: serial interfaces to transfer data to an External device that supports the SERDES interface. The SERDES baud rate should be set by MAC via register before usage. SGMII: Supports 10M/100M/1G /2.5G lite Ethernet speed 2500Base-X/ HiSGMII: Supports 2.5G Ethernet speed The differential pair has an internal 100-ohm termination resistor. A pair of 0402- sized 0.1µF AC coupling capacitors must be placed near the RTL8221B(I)-VB/RTL8221B(I)-VM pin.
37	HSON	O	
40	HSIP	I	SERDES Differential Input: serial interfaces to receive data from an External device that supports the SERDES interface. The SERDES baud rate should be set by MAC via reg before usage. SGMII: Supports 10M/100M/1G/ 2.5G lite Ethernet speed 2500Base-X/ HiSGMII: Supports 2.5G Ethernet speed The differential pair has an internal 100-ohm termination resistor. A pair of 0402-sized 0.1µF AC coupling capacitors must be placed near the MAC pin.
41	HSIN	I	

Note: 2.5G lite is a Realtek proprietary feature. Refer to the SERDES application note for more details.

6.4. Reset

Table 4. Reset

Pin No.	Pin Name	Type	Description
1	PHYRSTB	Ic /PU	Hardware Reset. Active low. Pull up to 3.3V/1.8V for 3.3 V/1.8V I/O respectively. For a complete PHY reset, this pin must be asserted low for at least 10ms. All registers will be cleared after hardware reset.

Note: See section 7.26, page 44 for more details.

6.5. Hardware Configuration

Table 5. Hardware Configuration

Pin No.	Pin Name	Type	Description
33	PHYAD0	Ic/LI/PU	PHYAD[2:0]: PHY Address Configuration. These pins are only used as PHYAD[2:0] during power on process. Note the operation voltage for PHYAD[2:0]. *Note: All of the PHYAD0~PHYAD2 is shared with LED0~LED2.*
34	PHYAD1	Ic/LI/PD	
35	PHYAD2	Ic/LI/PD	
29	CFG_OPT0	LI/IO	Clock out. PU: 25MHz clock out in CLKOUT pin PD: Clock out disable
30	CFG_OPT1	LI/IO	MDI Swap. PU: MDI port 0 ~port3 mapping to ChD~ChA PD: MDI port 0 ~port3 mapping to ChA~ChD

Note: For more information, see section 7.18 Hardware Configuration, page 21.

6.6. LED Default Settings

Table 6. LED Default Settings

Pin No.	Pin Name	Type	Description
33	LED0	Ic/O/PU	Low=Link Up at 100Mbps and 10Mbps. Blinking=Transmitting or Receiving.
34	LED1	Ic/O/PD	High=Link Up at 1000Mbps. Blinking=Transmitting or Receiving.
35	LED2	Ic/O/PD	High=Link Up at 2.5Gbps. Blinking=Transmitting or Receiving.

Note 1: High/Low active depends on hardware configuration pins setting (see section 7.19, page 22).
Note 2: See section 0, page 37 for more LED setting details.

6.7. Reference

Table 7. Reference

Pin No.	Pin Name	Type	Description
12	RSET	O	Reference (External 2.49K ohms, 1% tolerance Resistor Reference required).

6.8. Power and Ground

Table 8. Power and Ground

Pin No.	Pin Name	Type	Description
11,16,22	AVDD09	P	Analog Core Power 0.95V.
7,15,19	AVDD33	P	Analog Power 3.3V.
8	AVDD33_XTAL	-	XTAL Power 3.3V.
4,28,43	DVDD09	P	Digital Core Power 0.95V.
5	DVDD3318	P	Specific digital I/O Power reference power pin. Connect to 3.3V or 1.8V.
31, 42	DVDD33	P	Digital Power 3.3V.
36	EVDD09	P	SERDES Core Power 0.95V.
39	GND	G	Ground.
49	E-Pad	G	Ground. Exposed Pad (E-Pad) is Analog and Digital Ground (see section 10, page 113).

6.9. Management and Application Interface

Table 9. Management and Application Interface

Pin No.	Pin Name	Type	Description
2	MDC	Ic	Management Data Clock. Support 3.3V/ 1.8V IO.
3	MDIO	Ic /O/PU	Input/Output of Management Data. An external 1.5K ohm pull up resistor is needed. Pull up to 3.3V/1.8V for 3.3 V/1.8V I/O respectively.
48	PMEB/INTB	Ic/O/OD	This pin is shared by two functions. Keep this pin pulled high if either of the functions is not used. Pull up to 3.3V/1.8V for 3.3 V/1.8V I/O respectively. 1. Interrupt Low active; Set low if the specified events occurred. 2. Power Management Event Low active; Set low if received a magic packet, Wake-Up frame, or wake up event. *Note 1: The behavior of this pin is level-triggered.* *Note 2: The function of INTB/PMEB can be assigned by MMD 31.0xD05C.0:* 1: Pin 48 functions as PMEB. 0: Pin 48 functions as INTB (default) *Note 3:For more detailed INTB/PMEB usage, see section 0, page 20.*

6.10. PTP Pins

Table 10. PTP Pins

Pin No.	Pin Name	Type	Description
29	GPIO15880	IO	Programmable Time Application interface. *Note 1: All of the GPIO1588 pins are share-pins.* *Note 2: GPIO15882 is shared with SyncE_lock. Set high if a SyncE_lock occurred. An external 4.7k ohm pull down resistor is needed.*
32	GPIO15881	IO	
27	GPIO15882/SYNCE_LOCK	IO	
30	GPIO15883	IO	
6	SYNCE_CLK	O	Generates synchronized 1588 clock.

6.11. SPI (Serial Peripheral Interface) Flash Pins

Table 11. SPI (Serial Peripheral Interface) Flash Pins

Pin No.	Pin Name	Type	Description
26	SPICSB	O	SPI Flash Chip Select.
25	SPISO	I	Input from SPI Flash Serial Data Output Pin.
32	SPISI	O	Output to SPI Flash Serial Data Input Pin. *Note: This is a share-pin with GPIO15881.*
27	SPISCK	O	SPI Flash Serial Data Clock. *Note: This is a share-pin with GPIO15882.*

6.12. Other Pins

Table 12. Other Pins

Pin No.	Pin Name	Type	Description
46	POW_EXT_SWR	O	Power control pin for external 0.95V SWR. 1(3.3V): Enable external 0.95V SWR 0: Disable external 0.95V SWR
44,45,47	NC	-	Not Connected Pin.

7. Function Description

7.1. Transmitter

2.5Gbps Mode

The RTL8221B(I)-VB/RTL8221B(I)-VM's PCS layer receives data bytes from the MAC through the SERDES interface and performs LDPC encoding to enhance error correction performance. After LDPC framing, each 4 bits are grouped to a PAM16 symbol through gray code mapping scheme. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT.5e cable at 200MBaud/s through a D/A converter.

1000Mbps Mode

The RTL8221B(I)-VB/RTL8221B(I)-VM's PCS layer receives data bytes from the MAC through the SERDES interface and performs generation of continuous code-groups through 4D-PAM5 coding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT.5 cable at 125MBaud/s through a D/A converter.

100Mbps Mode

The transmitted 4-bit nibbles passed from the MAC through the SERDES interface are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. The NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

10Mbps Mode

The transmitted 4-bit nibbles passed from the MAC through the SERDES interface, are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

7.2. Receiver

2.5Gbps Mode

Received bits from the media are first passed through the on-chip sophisticated hybrid circuit to eliminate the transmitted signal interference from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, such as adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, RFI cancellation, de-skew, and PAM16 decoding. Each 2048-bit-wide data is passed through a LDPC decoder and is sent to the SERDES interface. The Rx MAC retrieves the packet data and sends it to the Rx Buffer Manager.

1000Mbps Mode

Input signals from the media first pass through the on-chip sophisticated hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, such as adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the SERDES interface. The Rx MAC retrieves the packet data from the receive SERDES interface and sends it to the Rx Buffer Manager.

100Mbps Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the SERDES interface in 4-bit-wide nibbles.

10Mbps Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder, and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the SERDES interface.

7.3. Link Down Power Saving Mode

The RTL8221B(I)-VB/RTL8221B(I)-VM implements link-down power saving. This can greatly cut power consumption when the network cable is disconnected. The RTL8221B(I)-VB/RTL8221B(I)-VM automatically enters link down power saving mode 3 seconds after the cable is disconnected from it. Once it enters link down power saving mode, it transmits normal link pulses on its TX pins and continues to monitor the RX pins to detect incoming signals. After it detects an incoming signal, it wakes up from link down power saving mode and operates in normal mode according to the result of the connection.

7.4. Media Access Control Security (MACsec)

The RTL8221B(I)-VM integrated MACsec functionality is compatible with IEEE security standard 802.1AE and Extension 802.1AEbn and 802.1AEbw. The *MACsec Core* (MSC) encrypts packets with SecTag and ICV from a link layer and decrypts packets from a physical layer at the same time based on a selected cypher algorithm. In egress traffic, the packet from the link layer will first filter out the preamble, SFD and CRC through a pre-processor called the *Tx System Converter*. Then the pure data is encrypted by the MSC, and output to the post-processor called the *Tx Line Converter*, which reconstructs the preamble, SFD and CRC of the encrypted packet. Likewise, in ingress traffic, the encrypted packet received from the link partner into the physical layer, will filter out the preamble, SFD and CRC through the *Rx Line Converter*. Then the MSC decrypts the packet and passes it to the *Rx System Converter*, which reconstructs the preamble, SFD and CRC. The Tx converter and Rx converter have their own state machine and data FIFO for processing an incoming packet. Separately, they also collect statistic counters for different error type packets.

The MSC supports maximum 64 SAs (Security Association) individually in egress or ingress traffic and any SA information in the form of record format maintains security information such as cypher suite, and associate number (AN). Each active SA uses one of the SA matching rules (ex: DA/SA/ETHERTYPE) to determine the packet processes according to different flow types. The flow types include egress operation, ingress operation, bypass and drop action. Each matching rule defines the mapping of the flow type and SA index. Packets are encrypted and decrypted by the SA key identified by the SA index, after hitting the matching rule that corresponds to the egress or ingress operation. However, the flow type of the bypass and drop action do not need SA information.

MAC Security Entities (SecY) define the three interfaces: Common port, Controlled port and Uncontrolled port. Egress traffic goes from the Controlled and Uncontrolled port, to the Common port, and Ingress traffic goes from the Common port to the Controlled and Uncontrolled ports. According to the SA matching rules and flow type, the packet can be encrypted from the Controlled port with egress operation and unchanged from the Uncontrolled port with bypass operation to the Common port. Similarly, the packet can be decrypted from the Common port to the Controlled port with ingress operation and unchanged to the Uncontrolled port with bypass operation.

When the SA packet number reaches the maximum, the SA is considered as expired and is not allowed to protect other packets. If the next SA is available, the software needs to update the SA index to allow it to switch to the new SA. The MSC provides some registers to know which SA has expired, and the software can switch the SA or install a new SA before the current SA expires via this information.

Due to the encryption appending SecTag and ICV, it needs to reserve more inter-frame gap (IFG) time to fill the expanding payload and not reduce the original inter-frame gap. The Rate Adaptor provides a programmable inter-frame gap according to the length of SecTag and ICV. If the upper layer does not reserve IFG, the Rate Adaptor needs to be enabled when supporting the MACsec feature. The RTL8221B(I)-VM does not support MACsec and PTP (Precision Time Protocol) at the same time.

The MACsec features are briefly descripted as above. For a more detailed configuration of MACsec functions, refer to the RTL8221B(I)-VM MACsec Application Note.

7.5. Precision Time Protocol (PTP)

Precision Time Protocol (PTP) stands for a series of IEEE specifications, including IEEE 1588 Ver. 1, IEEE 1588 Ver. 2, and IEEE 802.1AS, that synchronize the time of day or a standard time across a network system. The PTP protocol is typically used in Audio Video Bridging (AVB) applications, industrial and factory automation applications, or test and measurement systems.

The fundamental concept of PTP is time-stamping specified PTP frames with high precision as close to the transmission media as possible. Time stamping in the PHY provides increased accuracy compared to time-stamping in the MAC or higher layers.

The PTP core consists of three main blocks:

- Packet Time Stamping
- Synchronized PTP Clock
- Time Application Interface (TAI)

By combining the above functions, the RTL8221B(I)-VB/8221B(I)-VM provides complete and accurate support for applications in a time-synchronous system.

The PTP features are briefly introduced below. For a more detailed configuration of PTP functions, refer to the RTL8221B(I)-VB/RTL8221B(I)-VM PTP Application Note.

7.5.1. Synchronized PTP Clock

Based on the PTP specification requirements, the integrated PTP clock consists of the following time fields: seconds (48 bits), nanoseconds (30 bits), and fractional nanoseconds (in units of 2^{-32} ns).

The RTL8221B(I)-VB/RTL8221B(I)-VM provides several ways to access and update this internal PTP clock. The methods are listed below:

- Direct Read/Write
- Step Adjustment
- Rate Adjustment

A Direct Write of the time value is done by setting a new value to all time fields. This function may be used when initializing a PTP synchronization that needs an immediate setting to a time value due to the local PTP time being far different to the Master clock time.

A Step Adjustment is an alternative method for making quick compensation to the PTP clock time. Note that the adjustment can be incremented and decremented.

When the local time is close to the PTP Master, Rate Adjustment is the better way to fine-tune the time setting. The Rate Adjustment allows for correction on the order of 2^{-32} ns per clock cycle. It can correct the offset over time accurately.

Refer to section 0

PTP_CLK_CFG (PTP Clock Config Register, MMD31, Address 0xE410), page 89, for detailed register settings.

7.5.2. Packet Time Stamping

The PTP packet parser continually monitors transmit/receive packet data in order to detect IEEE 1588 Ver. 1, Ver 2 or 802.1AS Event Messages. The PTP packets transported in Layer 2 Ethernet, IPv4/UDP, or IPv6/UDP packet formats can be recognized accordingly. Upon detection of a PTP Event Message, the RTL8221B(I)-VB/RTL8221B(I)-VM will capture the specific transmit/receive timestamp and provide it to the software at the upper layer through PTP_TRX_TS registers (see section 8.7.47, page 94). A PTP interrupt can be generated, if enabled, upon a transmit/receive timestamp ready.

In some transmission cases, the RTL8221B(I)-VB/RTL8221B(I)-VM supports One-Step operation. The egress timestamp of a Sync message is on-the-fly inserted to the Sync itself, with no need for Follow-Up messages.

A Hardware-assisted Timestamp Insertion feature is imbedded, which will insert receive timestamps directly into the next Follow-Up/Delay-Response packets via hardware; software does not need to access timestamp registers.

After gathering the timestamp information, the upper layer software can compute the difference between the local time and the PTP Master's central clock time, and use the three methods in section 0 to tune the local PTP clock, in order to match the master clock.

7.5.3. Time Application Interface (TAI)

When the end-point's PTP clock is synchronized to the PTP Master clock, its time information and local clock can be provided to peripheral time applications that need to work simultaneously with the central clock. The RTL8221B(I)-VB/RTL8221B(I)-VM features these time application interfaces in the following, via the PTP GPIO1588 pins and CLKOUT:

Event Capture interface:

- Monitors the selected GPIO1588, and records the timestamp of incoming pulses, or time alignment signals, similar to a stopwatch

Trigger Generate interface:

- Arms the selected GPIO1588 to generate a pulse, or periodic clock signal at a specific time, similar to an alarm clock. The periodic clock has configurable period and duty cycles
- Low-jitter synchronized 1588 clock output with frequency of 25MHz via the CLKOUT pin
- PTP clock input from the external reference clock source with 10M/25MHz via GPIO15881 (pin32)

The related TAI configurations can be set by PTP_TAI registers (section 8.7.41, page 91).

7.6. Energy Efficient Ethernet (EEE)

The RTL8221B(I)-VB/RTL8221B(I)-VM supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps, 100Mbps, and 1000Mbps and IEEE 802.3-2016 EEE at 2.5GBASE-T. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled. However, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported.

7.7. Radio Frequency Interference (RFI)

Among the many possible causes of interference when connecting two PHYs, RFI is the most common. The RTL8221B(I)-VB/RTL8221B(I)-VM is equipped with RFI cancellation ability. This allows the RTL8221B(I)-VB/RTL8221B(I)-VM to maintain data transmission in noisy environments and makes it immune to RFI strikes.

7.8. Fast Retrain (FR)

The RTL8221B(I)-VB/RTL8221B(I)-VM supports IEEE 802.3bz Fast Retrain in 2.5GBASE-T. It provides a protocol to quickly converge a Tx/Rx equalizer at both ends of the link when it is needed. If local Rx SNR is bad, or the link partner requests FR, FR is launched and it attempts to train the Tx/Rx equalizer before the link goes down. This protocol can reduce link up/link down wait time and provide better upper layer protocols and applications. It is especially useful when the RTL8221B(I)-VB/RTL8221B(I)-VM is used in noisy environments, or a short RFI happens to strike the link.

The RTL8221B(I)-VB/RTL8221B(I)-VM supports Negotiated Fast Retrain, which aims for the same target as IEEE FR but extends some timing specifications to allow better weak link recovery.

7.9. 2.5G Lite Mode

The RTL8221B(I)-VB/RTL8221B(I)-VM supports 2.5G Lite mode (data rate = 1000Mbps) which allows two link partners that both support 2.5G Lite mode to transmit at 1000Mbps data rate if only two pairs (AB pairs) can be detected in the CAT.5e UTP cable. This is a Realtek proprietary feature.

The Realtek proprietary 2.5G Lite mode also supports EEE and FR to save power and provide quick convergence. That is, 2.5G Lite mode supports the same functionality with 2.5GBASE-T but the data rate is only 1000Mbps.

7.10. Thermal Detect

When the RTL8221B(I)-VB/RTL8221B(I)-VM works in 2.5G and 2.5G Lite mode, built-in smart thermal management can sense temperature drift between the RTL8221B(I)-VB/RTL8221B(I)-VM IC and surrounding environment. With the aid of the thermal detect mechanism, the RTL8221B(I)-VB/RTL8221B(I)-VM can use smart power management.

To prevent package damage, the RTL8221B(I)-VB/RTL8221B(I)-VM could mask 2.5G or 2.5G Lite capability and notify the system via the INTB pin when an over-temperature event occurs. To resume 2.5G and 2.5G Lite capability, users should set MMD 31.0xA662.1:0 to 0. Users can adjust the threshold for over-temperature detection and current temperature from MMD 31.0xB54C.15:6. The thermal detect function default is enabled. The user can set MMD 31 0xA436,data=0x817D and MMD 31 0xA438.12=0 to disable this function.

The goal of smart power management is to give a balance between power consumption and Ethernet transceiver performance. This feature is especially useful when the RTL8221B(I)-VB/RTL8221B(I)-VM is deployed in thermally constrained environments.

7.11. Self-Loopback

The RTL8221B(I)-VB/RTL8221B(I)-VM provides a self-diagnosis capability. The self-diagnosis is achieved via several integrated loopback modes. These loopback modes help narrow down the cause of potential link failures within certain OSI reference model layers.

7.12. MDI SWAP

Different ICM (Integrated Combo Magnetics) might have opposite PHY side to cable side definitions. To accommodate this, the RTL8221B(I)-VB/RTL8221B(I)-VM supports MDI swap to prevent PCB trace routing from crossing. The swap can be done using the CFG_OPT1 pin config. The internal circuits will identify the data transmission path to guarantee correct Tx/Rx behavior.

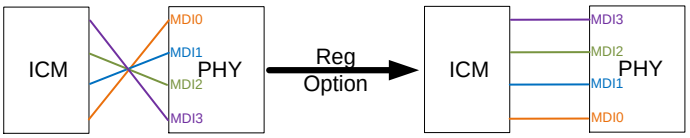


Figure 5. MDI Swap

Table 13. MDI swap

Pin Name	MDI	MDI + MDI Swap	MDIX	MDIX+ MDI Swap
MDIP0	BI_DA+	BI_DD+	BI_DB+	BI_DC+
MDIN0	BI_DA-	BI_DD-	BI_DB-	BI_DC-
MDIP1	BI_DB+	BI_DC+	BI_DA+	BI_DD+
MDIN1	BI_DB-	BI_DC-	BI_DA-	BI_DD-
MDIP2	BI_DC+	BI_DB+	BI_DD+	BI_DA+
MDIN2	BI_DC-	BI_DB-	BI_DD-	BI_DA-
MDIP3	BI_DD+	BI_DA+	BI_DC+	BI_DB+
MDIN3	BI_DD-	BI_DA-	BI_DC-	BI_DB-

7.13. Wake-On-LAN (WOL)

The RTL8221B(I)-VB/RTL8221B(I)-VM can monitor the network for a Wake-Up Frame or a Magic Packet, and notify the MAC via the INTB (Interrupt Event; 'B' means low active) pin when such a packet or event occurs. The system can then be restored to a normal state to process incoming jobs. The INTB pin needs to be connected with a 4.7k-ohm resistor and pulled up to the operation voltage. When the Wake-Up Frame or a Magic Packet is sent to the PHY, the INTB pin will be set low to notify the system to wake up. Refer to the RTL8221B(I)-VB/RTL8221B(I)-VM_Series_WOL_App_Note for details.

Magic Packet Wake-up occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8221B(I)-VB/RTL8221B(I)-VM, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8221B(I)-VB/RTL8221B(I)-VM
- The received Magic Packet does not contain a CRC error
- The Magic Packet pattern matches; i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet

A Wake-Up Frame event occurs only when the following conditions are met:

- The destination address of the received Wake-Up Frame is acceptable to the RTL8221B(I)-VB/RTL8221B(I)-VM, e.g., a broadcast, multicast, or unicast address to the current RTL8221B(I)-VB/RTL8221B(I)-VM
- The received Wake-Up Frame does not contain a CRC error
- The 16-bit CRC[1] of the received Wake-Up Frame matches the 16-bit CRC of the sample Wake-Up Frame pattern given by the local machine's OS. Or, the RTL8221B(I)-VB/RTL8221B(I)-VM is configured to allow direct packet wakeup, e.g., a broadcast, multicast, or unicast network packet. Non-specific packets are also supported

Note 1: 16-bit CRC: The RTL8221B(I)-VB/RTL8221B(I)-VM supports eight long Wake-Up frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet). CRC16 polynomial=x16+x12+x5+1.
Note 2: WOL feature supports only 1000Base-T, 100Base-TX, and 10BASE-Te. 2.5GBase-T is not supported.

7.14. Interrupt

The RTL8221B(I)-VB/RTL8221B(I)-VM provides an active low interrupt output pin (INTB) based on change of the PHY status. Every interrupt condition is represented by the read-only general interrupt status register (section 8.7.13 INSR (Interrupt Status Register, MMD 31.0xA4D4), page 79).

The interrupts can be individually enable or disable by setting or clearing bits in the interrupt enable register (section 8.7.12 INER (Interrupt Enable Register, MMD 31.0xA4D2), page78). When an enabled interrupt condition occurs, the interrupt pin is driven low, and the interrupts are self-cleared (INTB pin de-asserted) by reading the corresponding interrupt status registers through MDC/MDIO interface.

Note 1: The interrupt of the RTL8221B(I)-VB/RTL8221B(I)-VM is a level-triggered mechanism.
Note 2: The INTB and PMEB functions share the same pin, and can be determined by MMD 31.0xD05C.0.

7.15. SPI (Serial Peripheral Interface) Flash

SPI Flash is enabled by the RTL8221B(I)-VB/RTL8221B(I)-VM through the Chip Select pin, and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). The SPI flash utilizes an 8-bit instruction register. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low transition.

Compared to a parallel bus interface, the Serial Peripheral Interface provides simpler wiring and much less interaction (crosstalk) among the conductors in the cable. This minimizes the number of conductors, pins, and the IC package size, reducing the cost of making, assembling, and testing the electronics.

Table 14. SPI Flash Interface

SPI Flash	Description
SO	Input Data Bus.
SI	Output Data Bus.
SCK	SPI Flash Serial Data Clock.
CSB	SPI Flash Chip Select.

Note: The SPI flash`s density must be at least 2Mb for auto load.

7.16. INTB/PMEB Pin Usage

The INTB/PMEB pin 48 of the RTL8221B(I)-VB/RTL8221B(I)-VM is designed to notify in cases of both interrupt and WOL events. The default mode of this pin is INTB (MMD 31.0xD05C.0: 0). For general use, indication of a WOL event is also integrated into one of the interrupt events (MMD 31.0xA4D4.7 which is triggered when any specified WOL event occurs. However, the ‘Pulse Low’ waveform format is not supported during this mode; only the Active Low, level-triggered waveform is provided. Refer to the RTL8221B(I)-VB/RTL8221B(I)-VM_Series_WOL_App_Note for more information.

If PMEB mode is selected (MMD 31.0xD05C.0 = 1), pin 48 becomes a fully functional PMEB pin. Note that the interrupt function is disabled in this mode. Note also that the PMEB feature supports only 1000Base-T, 100Base-TX, and 10BASE-Te.

7.17. MDI Interface

This interface consists of four signal pairs; MDI0, MDI1, MDI2, and MDI3. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors to reduce BOM cost and PCB complexity. For 2.5GBASE-T and 1000BASE-T, all four pairs are used in both directions at the same time. For 10/100Mbps links and during auto-negotiation, only pairs MDI0 and MDI1 are used.

7.18. Hardware Configuration

The MDI port swap, CLKOUT and PHY address can be set by the CONFIG pins. The respective value mapping of CONFIG with the configurable vector is listed in Table 15. To set the CONFIG pins, an external pull-high or pull-low via resistor is required.

Table 15. CONFIG Pins vs. Configuration Register

CONFIG Pin	Configuration
PHYAD2	PHYAD[2]
PHYAD1	PHYAD[1]
PHYAD0	PHYAD[0]
CFG_OPT0	CLKOUT Enable
CFG_OPT1	MDI Swap

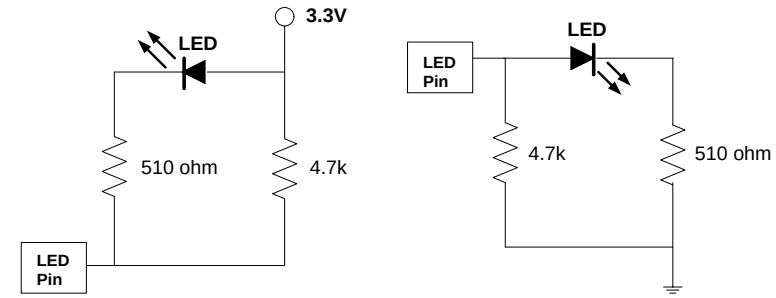
Table 16. Configuration Register Definitions

Configuration	Description
PHYAD[2:0]	PHY Address. PHYAD sets the PHY address for the device. The RTL8221B(I)-VB/RTL8221B(I)-VM supports PHY addresses from 0x01 to 0x7. *Note 1: An MDIO command with PHY address=0 is a broadcast from the MAC; each PHY device should respond. This function can be disabled by setting MMD31.0xA430, bit[13]=0.* *Note 2: The RTL8221B(I)-VB/RTL8221B(I)-VM with PHYAD[2:0]=3'b0 would automatically force PHY address = 1.*
CLKOUT enable	PCB PU in pin CFG_OPT0 means there is 25MHz clock out in CLKOUT pin; otherwise, clock Output is disabled. Register control: MMD31 0xBC60 bit[2]=1 for 25MHz output.
MDI Swap	PCB PD in pin CFG_OPT1 means MDIP0~MDIP3 mapping to ChA~ChD; otherwise, MDIP0 ~MDIP3 mapping to ChD~ChA.

7.19. LED and PHY Address Configuration

In order to reduce the pin count, the LED pins are duplexed with the PHYAD pins. As the Hardware Configuration shares the LED output pins, the external combinations required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD inputs upon power-on/reset.

For example, Figure 6 (left-side) shows, if a given PHYAD inputs are resistively pulled high then the corresponding LED outputs will be configured as an active low driver. On the right side, we can see that if a given PHYAD input is resistively pulled low then the corresponding output will be configured as an active high driver. The Hardware Configuration pins should not be connected to GND or VCC directly, but must be pulled high or low through a resistor (e.g., 4.7KΩ). If no LED indications are needed, the components of the LED path (LED+510Ω) can be removed.



PHYAD=Logical 1
LED Indication=Active low

PHYAD=Logical 0
LED Indication=Active High

Figure 6. LED and PHY Address Configuration

7.20. MAC/PHY Interface

The RTL8221B(I)-VB/RTL8221B(I)-VM supports most off-the-shelf MACs with the SERDES interface. The RTL8221B(I)-VB/RTL8221B(I)-VM supports SGMII, HiSGMII, and 2500Base-X mode between MAC and PHY layer. Setting MMD 30.0x697A.5:0 will set whether the RTL8221B(I)-VB/ RTL8221B(I)-VM SERDES mode setting is controlled by the RTL8221B(I)-VB/RTL8221B(I)-VM or by the MAC, based on PHY link speed and MAC ability.

Table 17 briefly lists the available different operation modes for the RTL8221B(I)-VB/RTL8221B(I)-VM. Refer to the RTL8221B(I)-VB/ RTL8221B(I)-VM_Series_SERDES_App_Note for details.

Table 17. SGMII/ HiSGMII/ 2500Base-X Mode

Mode	Ethernet PHY Speed	SERDES PCS Encoding	SERDES Speed	Data Replications
SGMII	10BASE-Te	8B/10B	1.25Gbps	100
	100Base-Tx			10
	1000Base-T			1
	2.5GBase-T Lite			1
HiSGMII	2.5GBase-T/ 2.5GNBase-T		3.125Gbps	1
2500Base-X				

7.20.1. SGMII

The Serial Gigabit Media Independent Interface (SGMII) is a standard interface that is used to carry frame data and link status information between a PHY and an Ethernet MAC. SGMII uses a differential pair for signals to provide signal integrity while minimizing system noise. The data signals operate at 1.25G/baud, however 10M/100M/1G Ethernet data transmissions are supported.

7.20.2. HiSGMII

The Hi-speed Serial Gigabit Media Independent Interface (HiSGMII) is a Realtek proprietary SERDES mechanism, which is an extension of the SGMII protocol. The data signals operate at 3.125G/baud, which is 2.5 times SGMII baud rate. Note that HiSGMII supports only 2.5G Ethernet data transmission. For more details, contact Realtek.

7.20.3. 2500Base-X

The 2500Base-X uses two data signals to convey frames between the PHY and Ethernet MAC. The differential signals operate at 3.125G/baud. All the protocols of 2500Base-X are exactly the same as 1000Base-X with a clock rate boost up to 2.5 times.

7.20.4. Management Interface

The management interface provides access to the internal registers through the MDC and MDIO pins as described in IEEE 802.3 section 45. The MDC signal, provided by the MAC, is the management data clock reference to the MDIO signal. The MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC. The MDIO pin needs a 1.5k Ohm pull-up resistor to maintain the MDIO high during idle and turnaround.

The RTL8221B(I)-VB/RTL8221B(I)-VM can share the same MDIO line. In switch/router applications, each port should be assigned a unique address during the hardware reset sequence, and it can only be addressed via that unique PHY address. For detailed information on the management registers, see section 8 Register Descriptions, page 46.

Table 18. Management Frame Format

	Management Frame Fields							
	Preamble	**ST**	**OP**	**PRTAD**	**DEVAD**	**TA**	**DATA**	**IDLE**
Address	1…1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1…1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1…1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Post-read-increment-address	1…1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

Table 19. Management Frame Descriptions

Name	**Description**
Preamble	32 Contiguous Logical 1's Sent by the MAC on MDIO, along with 32 Corresponding Cycles on MDC. This provides synchronization for the PHY.
ST	Start of Frame. Indicated by a 00 pattern. Frames that contain the ST=<01> pattern is defined in Clause 22 shall be ignored by the devices specified in Clause 45.
OP	Operation Code. 00: Address of the register to access 01: Write 11: Read 10: Post-read-increment-address
PRTAD	PHY Address. The port address is five bits, allowing 32 unique port addresses. The first port address bit to be transmitted and received is the MSB of the address. A station management entity must have a priori knowledge of the appropriate port address for each port to which it is attached, whether connected to a single port or to multiple ports.
DEVAD	Register Address. The device address is five bits, allowing 32 unique MMDs per port. The first device address bit transmitted and received is the MSB of the address.
TA	Turnaround. This is a 2-bit-time spacing between the register address and the data field of a frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY remain in a high-impedance state for the first bit time of the turnaround. The PHY drives a zero bit during the second bit time of the turnaround of a read transaction.

Name	Description
DATA	Data. For an address cycle, it contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, the field contains the data to be written to the register. For a read or post-read-increment-address frame, the field contains the contents of the register.
IDLE	Idle Condition. Not truly part of the management frame. This is a high impedance state. Electrically, the PHY's pull-up resistor will pull the MDIO line to a logical '1'.

Write, read, and post-read-increment-address frames shall access the register whose address is stored in the address register. Write and read frames shall not modify the contents of the address register. Upon receiving a post-read-increment-address frame and having completed the read operation, the MMD shall increment the address register by one. See the examples below:

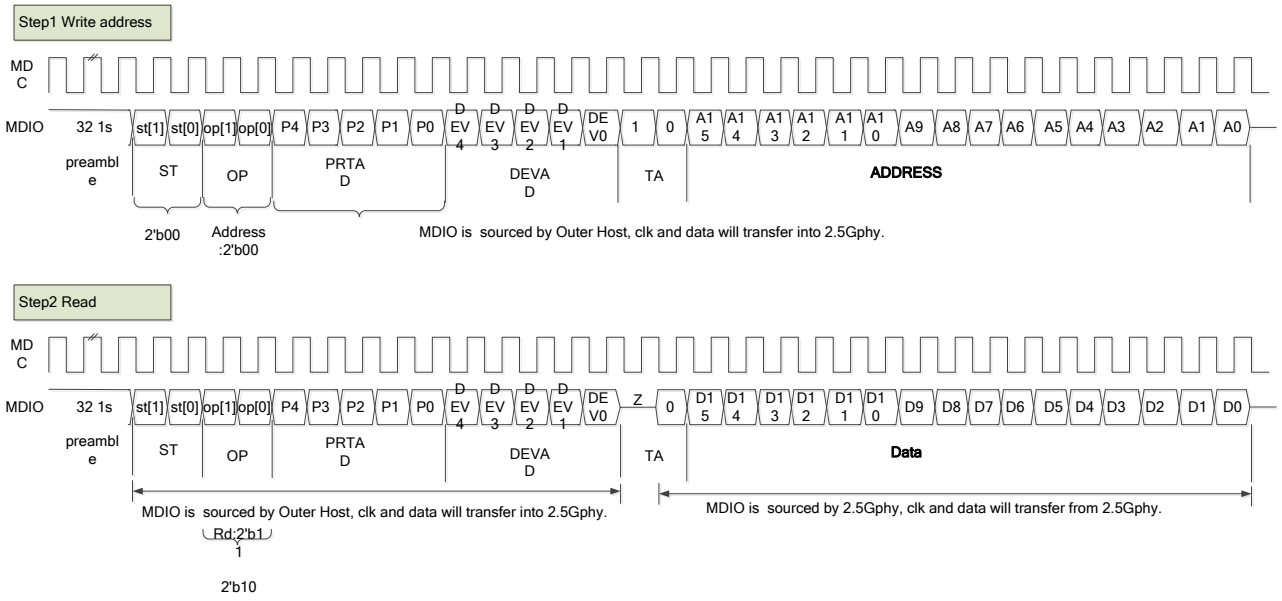


Figure 7. MDC/MDIO Read Timing

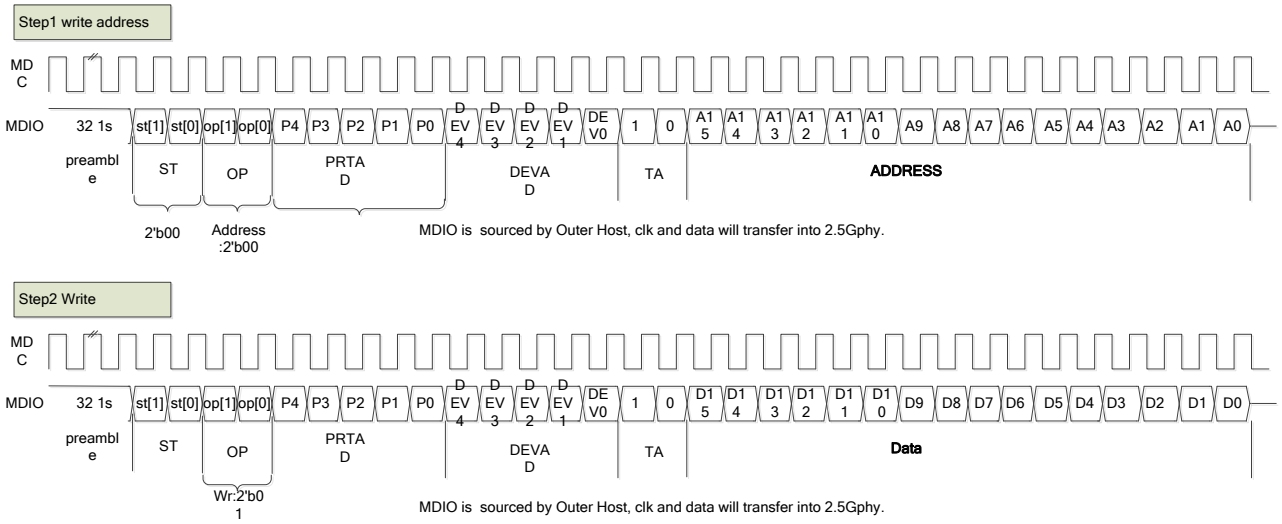


Figure 8. MDC/MDIO Write Timing

Clause 22 Access to Clause 45 MMD (MDIO Manageable Device)

RTL8221B(I)-VB/RTL8221B(I)-VM support clause 22 to access clause 45 MMD space using register 13 and register 14. The MMD access control register and Address/Data register definitions are shown in Table 20 and Table 21.

Table 20. MMD Access Control Register, Page 0 Register 13

Bit	Name	Type	Default	Description
15:14	mmd_op	RW	2'b0	mmd function. 00: address 01: data, no post increment 10: data, post increment on reads and writes 11: data, post increment on writes only
13:5	Reserved	RW	9'b0	Reserved.
4:0	mmd_devad	RW	5'b 0	mmd device address.

Table 21. MMD Access Control Register, Page 0 Register 14

Bit	Name	Type	Default	Description
15:0	mmd_addr_data	RW	15'b0	If mmd_op = 2'b00, mmd devad's address is read else mmd devad's data indicated by its address register is read.

Write Operation (Not support MMD 31 access)

Step 1. To register 13, write the mmd function field bit[15:14] to 00(address) and mmd device address bit[4:0] field with device address value.

Step 2. To register 14, write the MMD`s register address value.

Step 3. To register 13, write the mmd function field to 01(data, no post increment) and mmd device address field with device address value (as step 1).

Step 4. To register 14, write the content to be written to the selected MMD`s register.

Example: Write Data=0x1234 to MMD 7.0x6E00

Write Reg 13, Data=0x7 // set MMD as 7 and set Reg14 to be desired reg address

Write Reg 14, Data=0x6E00 // set Reg address as 0x6E00

Write Reg 13, Data=0x4007 // set MMD as 7 and let Reg14 to be desired reg data

Write Reg 14, Data=0x1234 // write 0x1234 to MMD7.0x6E00

Read Operation (MMD 31 access NOT supported)

Step 1. To register 13, write the mmd function field bit[15:14] to 00(address) and mmd device address bit[4:0] field with device address value.

Step 2. To register 14, write the MMD`s register address value.

Step 3. To register 13, write the mmd function field to 01(data, no post increment) and mmd device address field with device address value (as step 1).

Step 4. From register 14, read the content from the selected MMD`s register.

Example: Read Data from MMD 7.0x6E00

Write Reg 13, Data=0x7 // set MMD as 7 and set Reg14 to be desired reg address

Write Reg 14, Data=0x6E00 // set Reg address as 0x6E00

Write Reg 13, Data=0x4007 // set MMD as 7 and let Reg14 to be desired reg data

Read Reg 14 // Read Data from MMD 7.0x6E00

7.21. Auto-Negotiation

Auto-Negotiation is a mechanism to determine the fastest connection between two link partners. For copper media applications, it was introduced in IEEE 802.3u for Ethernet and Fast Ethernet, and then in IEEE 802.3 to address extended functions for 2.5G BASE-T. The RTL8221B(I)-VB/RTL8221B(I)-VM extends Auto-Negotiation ability to support NBASE-T Auto-Negotiation. It performs the following:

- Auto-Negotiation Priority Resolution
- Auto-Negotiation Master/Slave Resolution
- Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution
- Crossover Detection & Auto-Correction Resolution
- Speed Down

Upon de-assertion of a hardware reset, the RTL8221B(I)-VB/RTL8221B(I)-VM can be configured to have auto-negotiation enabled, or be set to operate in 10BASE-Te, 100BASE-TX, 1000BASE-T, or 2.5GBASE-T mode.

The auto-negotiation process is initiated automatically upon any of the following:

- Power-up
- Hardware reset (PHYRSTB pin)
- Software reset (MMD7.0x0000.15)
- Restart auto-negotiation (MMD 7.0x0000.9)
- Transition from power down to power up
- Entering the link fail state

Table 22. 1000BASE-T Base and Next Page Bit Assignments

Bit	Name	Bit Description	Register Location
Base Page			
D15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	MMD7.0x0010
D14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	
D13	RF	Remote Fault. 1: Indicates to its link partner that a device has encountered a fault condition	
D[12:5]	A[7:0]	Technology Ability Field. Indicates to its link partner the supported technologies specific to the selector field value.	
D[4:0]	S[4:0]	Selector Field. Always 00001. Indicates to its link partner that it is an IEEE 802.3 device.	

Bit	Name	Bit Description	Register Location
PAGE 0 (Message Next Page)			
M15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	MMD7.0x0016
M14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	
M13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page	
M12	Ack2	Acknowledge 2. 1: Indicates to its link partner that the device has the ability to comply with the message	
M11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	
M[10:0]	-	1000BASE-T Message Code (Always 8).	
PAGE 1 (Unformatted Next Page)			
U15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	MMD7.0x0016
U14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	
U13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page	
U12	Ack2	Acknowledge 2. 1: Indicates to its link partner that the device has the ability to comply with the message	
U11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	
U[10:5]	-	Reserved, transmit as 0.	
U4	-	1000BASE-T Half Duplex. 1: Half duplex 0: No half duplex	
U3	-	1000BASE-T Full Duplex. 1: Full duplex 0: No full duplex	
U2	-	1000BASE-T Port Type Bit. 1: Multi-port device 0: Single-port device	
U1	-	1000BASE-T Master-Slave Manual Configuration Value. 1: Master 0: Slave This bit is ignored if bit 9.12=0.	

Bit	Name	Bit Description	Register Location
U0	-	1000BASE-T Master-Slave Manual Configuration Enable. 1: Manual Configuration Enable This bit is intended to be used for manual selection in Master-Slave mode, and is to be used in conjunction with bit 9.11.	
PAGE 2 (Unformatted Next Page)			
U15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	MMD7.0x0016
U14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	
U13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page	
U12	Ack2	Acknowledge 2. 1: Indicates to its link partner that the device has the ability to comply with the message	
U11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	
U[10:0]	-	1000BASE-T Master-Slave Seed Bit[10:0].	

Table 23. 2.5GBASE-T and 1000BASE-T Extended Message Page Bit Assignments

Bit	Name	Bit Description	Register Location
D15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	MMD7.0x0016~7.0x0018
D14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	
D13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page	
D12	Ack2	Acknowledge 2. 1: Indicates to its link partner that the device has the ability to comply with the message	
D11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	
D[10:0]	-	Message Code (Always 9).	
Extended Next Page (Message Code Field and Flags Field)			
U[31:29]	-	Reserved, transmit as 0.	MMD7.0x0016~7.0x0018
U28	-	2.5GBASE-T Ability. 1: 2.5G BASE-T Ability 0: No 2.5G BASE-T Ability	
U27	-	Reserved.	
U26	-	Reserved.	

Bit	Name	Bit Description	Register Location
U25	-	Reserved.	
U24	-	Reserved.	
U23	-	1000BASE-T EEE. 1: 1000BASE-T EEE Ability 0: No 1000BASE-T EEE Ability	
U22	-	100BASE-Tx EEE. 1: 100BASE-Tx EEE Abilit 0: No 100BASE-Tx EEE Ability	
U21	-	Reserved.	
U20	-	LD PMA training Reset Request. 1: Reset PMA training PRBS every frame 0: Run PMA training PRBS continuously	
U19	-	Reserved.	
U18	-	PHY short reach mode. 1: Local PHY is in short reach mode 0: Local PHY is in normal mode	
U17	-	LD Loop Timing Ability. 1: Loop Timing Ability 0: No Loop Timing Ability	
U16	-	Reserved.	
U15	-	1000BASE-T Half Duplex. 1: Half duplex 0: No half duplex	
U14	-	1000BASE-T Full Duplex. 1: Full duplex 0: No full duplex	
U13	-	Port Type Bit. 1: Multi-port device 0: Single-port device	
U12	-	Reserved.	
U11	-	Reserved.	
U[10:0]	-	Master-Slave Seed Bit[10:0].	

Table 24. 2.5GBASE-T and 1000BASE-T Extended Next Page Bit Assignments

Bit	Name	Bit Description	Register Location
D[47:16]	-	Unformatted Code Field.	MMD7.0x0016~7.0x0018
D15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	
D14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	
D13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page	
D12	Ack2	Acknowledge 2. 1: Indicates to its link partner that the device has the ability to comply with the message	
D11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	
D[10:0]	-	Message Code (Always 9).	

Table 25. 2.5GNBASE-T OUI Tagged Extended Message Page Bit Assignments

Bit	Name	Bit Description	Register Location
D15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	N.A
D14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	
D13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page	
D12	Ack2	Acknowledge 2. 1: Indicates to its link partner that the device has the ability to comply with the message	
D11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	
D[10:0]	-	Message Code (Always 5).	
Extended Message Page (Message Code Field and Flags Field)			
D[31:27]	R	Reserved, transmit as 0.	N.A
D[26:16]	-	OUI Tag Code (Always 2000).	
Extended Message Page (Message Code Field and Flags Field)			
D[47:43]	R	Reserved, transmit as 0.	N.A
D[42:32]	-	OUI Tag Code (Always 463).	

Table 26. 2.5GNBASE-T OUI Tagged Extended Unformatted Page Bit Assignments

Bit	Name	Bit Description	Register Location
D15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	N.A
D14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	
D13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page	
D12	Ack2	Acknowledge 2. 1: Indicates to its link partner that the device has the ability to comply with the message	
D11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	
D[10:9]	-	OUI Tag Code (Always 2).	
D[8:0]	R	Reserved, transmit as 0.	
Extended Unformatted Page (Message Code Field and Flags Field)			
D[31:19]	R	Reserved, transmit as 0.	N.A
D18	V	Vendor specific (Always 0).	
D17	-	Reserved.	
D16	-	2.5GNBASE-T advertisement.	MMD31.0xA5EA.15
Extended Unformatted Page (Message Code Field and Flags Field)			
D[47:32]	R	Reserved, transmit as 0.	N.A

Table 27. CISCO Negotiated Fast Retrain OUI Tagged Extended Unformatted Page Bit Assignments

Bit	Name	Bit Description	Register Location
D15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	N.A
D14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	
D13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page	
D12	Ack2	Acknowledge 2. 1: Indicates to its link partner that the device has the ability to comply with the message	
D11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	
D[10:0]	-	Message Code (Always 5).	

Bit	Name	Bit Description	Register Location
Extended Message Page (Message Code Field and Flags Field)			
D[31:27]	R	Reserved, transmit as 0.	N.A
D[26:16]	-	OUI Tag Code (Always 0).	
Extended Message Page (Message Code Field and Flags Field)			
D[47:43]	R	Reserved, transmit as 0.	N.A
D[42:32]	-	OUI Tag Code (Always 266).	

Table 28. CISCO Negotiated Fast Retrain OUI Tagged Extended Unformatted Page Bit Assignments

Bit	Name	Bit Description	Register Location
D15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	N.A
D14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	
D13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page	
D12	Ack2	Acknowledge 2. 1: Indicates to its link partner that the device has the ability to comply with the message	
D11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	
D[10:9]	-	OUI Tag Code (Always 0).	
D[8:6]	-	OP Code (Always 4).	
D[5:3]	-	Version Code (Always 0).	
D2	-	THP on/off (Always 0).	
D1	-	Extended maxwait timer (Always 0).	
D0	-	nfr_disable_timer required (Always 0).	
Extended Unformatted Page (Message Code Field and Flags Field)			
D[31:16]	R	Reserved, transmit as 0.	N.A
Extended Unformatted Page (Message Code Field and Flags Field)			
D[47:32]	R	Reserved, transmit as 0.	N.A

7.21.1. Auto-Negotiation Priority Resolution

Upon the start of auto-negotiation, to advertise its capabilities each station transmits a 16-bit packet called a Link Code Word (LCW), within a burst of 17 to 33 Fast Link Pulses (FLP). A device capable of auto-negotiation transmits and receives the FLPs. The receiver must identify three identical LCWs before the information is authenticated and used in the arbitration process. The devices decode the base LCW and select capabilities with the highest common denominator supported by both devices.

To advertise 1000BASE-T capability, both link partners, sharing the same link medium, should engage in Next Page (1000BASE-T Message Page, Unformatted Page 1, and Unformatted Page 2) exchange or XNP exchange.

To advertise 2.5GBASE-T capability, both link partners, sharing the same link medium, should engage in XNP exchange. NBASE-T OUI tagged page exchange would be further needed if NBASE-T capability is to be advertised.

Auto-negotiation ensures that the highest priority protocol will be selected as the link speed based on the following priorities advertised through the Link Code Word (LCW) exchange. Refer to IEEE 802.3 Clause 28 and NBASE-T Physical Layer Specification v2.3 for detailed information.

1. 2.5GBASE-T Full Duplex (highest priority)
2. 2.5GNBASE-T Full Duplex
3. 1000BASE-T Full Duplex
4. 2.5GBASE-T Lite Full Duplex (1G data rate)
5. 100BASE-TX Full Duplex
6. 100BASE-TX Half Duplex
7. 10BASE-Te Full Duplex
8. 10BASE-Te Half Duplex (lowest priority)

Given the above Auto-negotiation HCD result and exchanged EEE/FR ability, the RTL8221B(I)-VB/RTL8221B(I)-VM will automatically determine the proper EEE/FR ability resolution.

7.21.2. Auto-Negotiation Master/Slave Resolution

To establish a valid 2.5GBASE-T or 1000BASE-T link, the Master/Slave mode of both link partners should be resolved through the auto-negotiation process:

- Master Priority
  - Multi-port > Single-port
  - Manual > Non-manual
- Determination of Master/Slave configuration from LCW
  - Manual_MASTER=U0*U1
  - Manual_SLAVE=U0*!U1
  - Single-port device=!U0*!U2
  - Multi-port device=!U0*U2

  Where: U0 is bit 0 of the Unformatted Page 1
  U1 is bit 1 of the Unformatted Page 1
  U2 is bit 2 of the Unformatted Page 1
- Where there are two stations with the same configuration, the one with higher Master-Slave seed SB[10:0] in the unformatted page 2 shall become Master.
- Master-Slave configuration process resolution:
  - Successful: Bit 10.15 Master-Slave Configuration Fault is set to logical 0, and Bit 10.14 is set to logical 1 for Master resolution, or set to logical 0 for Slave resolution.
  - Unsuccessful: Auto-Negotiation restarts.
  - Fault Detect: Bit 10.15 is set to logical 1 to indicate that a configuration fault has been detected. Auto-Negotiation restarts automatically. This happens when both stations are set to manual Master mode or manual Slave mode, or after seven attempts to configure the Master-Slave relationship through the seed method has failed.

7.21.3. Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution

Auto-negotiation is also used to determine the flow control capability between link partners. Flow control is a mechanism that can force a busy transmitting link partner to stop transmitting in a full duplex environment by sending special MAC control frames. In IEEE 802.3u, a PAUSE control frame had already been defined. However, in IEEE 802.3ab, a new ASY-PAUSE control frame was defined; if the MAC can only generate PAUSE frames but is not able to respond to PAUSE frames generated by the link partner, then it is called ASYMMETRIC PAUSE.

A PHY layer device such as the RTL8221B(I)-VB/RTL8221B(I)-VM is not directly involved in PAUSE resolution, but simply advertises and reports PAUSE capabilities during the Auto-Negotiation process. The MAC is responsible for final PAUSE/ASYMMETRIC PAUSE resolution after a link is established, and is responsible for correct flow control actions thereafter.

7.22. Speed Down

2.5GBASE-T is defined for CAT5e UTP cable. The cable may suffer from cable noise introduced from cable movement, power surge, RFI, or alien crosstalk. These noise sources may cause unpredictable link down or Rx failure. The RTL8221B(I)-VB/RTL8221B(I)-VM introduces a flexible mechanism called 'Speed Down'. When consecutive PHY control failure happens, the downshift mechanism will try to link at the second highest speed ability, as a lower speed will have higher SNR margin to accommodate the noisy environment.

7.23. LED Configuration

7.23.1. Customized LED Function

The RTL8221B(I)-VB/RTL8221B(I)-VM supports three LED pins, suitable for multiple types of applications that can directly drive the LEDs. The LED pins can be customized from the register. To change the LED settings, see Table 29 LED Register Table, which summarizes several configuration types (see also Table 30, page 37, and Table 31, page 40).

Table 29. LED Register Table

Pin	LINK Speed					Active (Tx/Rx)	Mode A/Mode B SEL*
	10Mbps	100Mbps	1000Mbps	2.5Gbps	1Gbps (2.5G lite)		
LED0	31.0xD032.0	31.0xD032.1	31.0xD032.2	31.0xD032.5	31.0xD032.7	31.0xD040.0	31.0xD040.5
LED1	31.0xD034.0	31.0xD034.1	31.0xD034.2	31.0xD034.5	31.0xD034.7	31.0xD040.1	
LED2	31.0xD036.0	31.0xD036.1	31.0xD036.2	31.0xD036.5	31.0xD036.7	31.0xD040.2	

**Mode A: Set MMD 31.0xD040.5 = 0. Only blinks when the LED setting is consistent with current PHY link Speed.*
Mode B: Set MMD 31.0xD040.5 = 1. All LEDs will blink regardless of their setting.

Table 30. Mode A LED Configuration

Pin	LINK Bit					Active (TX/RX) Bit	Description
	10Mbps	100Mbps	1000Mbps	2.5Gbps	1Gbps (2.5G lite)		
LED0 LED1 LED2	0	0	0	0	0	0	N/A
	0	0	0	0	0	1	N/A
	1	0	0	0	0	0	$Link_{10}$
	1	0	0	0	0	1	$Link_{10} + Act_{10}$
	0	1	0	0	0	0	$Link_{100}$
	0	1	0	0	0	1	$Link_{100} + Act_{100}$
	1	1	0	0	0	0	$Link_{10} + Link_{100}$
	1	1	0	0	0	1	$Link_{10} + Act_{10} + Link_{100} + Act_{100}$
	0	0	1	0	0	0	$Link_{1000}$
	0	0	1	0	0	1	$Link_{1000} + Act_{1000}$
	1	0	1	0	0	0	$Link_{10} + Link_{1000}$
	1	0	1	0	0	1	$Link_{10} + Act_{10} + Link_{1000} + Act_{1000}$

Pin	LINK Bit					Active (TX/RX) Bit	Description
	10Mbps	100Mbps	1000Mbps	2.5Gbps	1Gbps (2.5G lite)		
	0	1	1	0	0	0	$Link_{100} + Link_{1000}$
	0	1	1	0	0	1	$Link_{100} + Act_{100} + Link_{1000} + Act_{1000}$
	1	1	1	0	0	0	$Link_{10} + Link_{100} + Link_{1000}$
	1	1	1	0	0	1	$Link_{10} + Act_{10} + Link_{100} + Act_{100} + Link_{1000} + Act_{1000}$
	0	0	0	1	0	0	$Link_{2500}$
	0	0	0	1	0	1	$Link_{2500} + Act_{2500}$
	1	0	0	1	0	0	$Link_{10} + Link_{2500}$
	1	0	0	1	0	1	$Link_{10} + Act_{10} + Link_{2500} + Act_{2500}$
	0	1	0	1	0	0	$Link_{100} + Link_{2500}$
	0	1	0	1	0	1	$Link_{100} + Act_{100} + Link_{2500} + Act_{2500}$
	1	1	0	1	0	0	$Link_{10} + Link_{100} + Link_{2500}$
	1	1	0	1	0	1	$Link_{10} + Act_{10} + Link_{100} + Act_{100} + Link_{2500} + Act_{2500}$
	0	0	1	1	0	0	Link1000 + Link2500
	0	0	1	1	0	1	$Link_{1000} + Act_{1000} + Link_{2500} + Act_{2500}$
	1	0	1	1	0	0	$Link_{10} + Link_{1000} + Link_{2500}$
	1	0	1	1	0	1	$Link_{10} + Act_{10} + Link_{1000} + Act_{1000} + Link_{2500} + Act_{2500}$
	0	1	1	1	0	0	$Link_{100} + Link_{1000} + Link_{2500}$
	0	1	1	1	0	1	$Link_{100} + Act_{100} + Link_{1000} + Act_{1000} + Link_{2500} + Act_{2500}$
	1	1	1	1	0	0	$Link_{10} + Link_{100} + Link_{1000} + Link_{2500}$
	1	1	1	1	0	1	$Link_{10} + Act_{10} + Link_{100} + Act_{100} + Link_{1000} + Act_{1000} + Link_{2500} + Act_{2500}$
	0	0	0	0	1	0	$Link_{2500\ lite}$
	0	0	0	0	1	1	$Link_{2500\ lite} + Act_{2500\ lite}$
	1	0	0	0	1	0	$Link_{10} + Link_{2500\ lite}$
	1	0	0	0	1	1	$Link_{10} + Act_{10} + Link_{2500\ lite} + Act_{2500\ lite}$
	0	1	0	0	1	0	$Link_{100} + Link_{2500\ lite}$
	0	1	0	0	1	1	$Link_{100} + Act_{100} + Link_{2500\ lite} + Act_{2500\ lite}$
	1	1	0	0	1	0	$Link_{10} + Link_{100} + Link_{2500\ lite}$
	1	1	0	0	1	1	$Link_{10} + Act_{10} + Link_{100} + Act_{100} + Link_{2500\ lite} + Act_{2500\ lite}$
	0	0	1	0	1	0	$Link_{1000} + Link_{2500\ lite}$
	0	0	1	0	1	1	$Link_{1000} + Act_{1000} + Link_{2500\ lite} + Act_{2500\ lite}$

Pin	LINK Bit					Active (TX/RX) Bit	Description
	10Mbps	100Mbps	1000Mbps	2.5Gbps	1Gbps (2.5G lite)		
	1	0	1	0	1	0	$Link_{10}$ + $Link_{1000}$ + $Link_{2500\ lite}$
	1	0	1	0	1	1	$Link_{10}$ + Act_{10} + $Link_{1000}$ + Act_{1000} + $Link_{2500\ lite}$ + $Act_{2500\ lite}$
	0	1	1	0	1	0	$Link_{100}$ + $Link_{1000}$ + $Link_{2500\ lite}$
	0	1	1	0	1	1	$Link_{100}$ + Act_{100} + $Link_{1000}$ + Act_{1000} + $Link_{2500\ lite}$ + $Act_{2500\ lite}$
	1	1	1	0	1	0	$Link_{10}$ + $Link_{100}$ + $Link_{1000}$ + $Link_{2500\ lite}$
	1	1	1	0	1	1	$Link_{10}$ + Act_{10} + $Link_{100}$ + Act_{100} + $Link_{1000}$ + Act_{1000} + $Link_{2500\ lite}$ + $Act_{2500\ lite}$
	0	0	0	1	1	0	$Link_{2500\ lite}$ + $Link_{2500}$
	0	0	0	1	1	1	$Link_{2500\ lite}$ + $Act_{2500\ lite}$ + $Link_{2500}$ + Act_{2500}
	1	0	0	1	1	0	$Link_{10}$ + $Link_{2500\ lite}$ + $Link_{2500}$
	1	0	0	1	1	1	$Link_{10}$ + Act_{10} + $Link_{2500\ lite}$ + $Act_{2500\ lite}$ + $Link_{2500}$ + Act_{2500}
	0	1	0	1	1	0	$Link_{100}$ + $Link_{2500\ lite}$ + $Link_{2500}$
	0	1	0	1	1	1	$Link_{100}$ + Act_{100} + $Link_{2500\ lite}$ + $Act_{2500\ lite}$ + $Link_{2500}$ + Act_{2500}
	1	1	0	1	1	0	$Link_{10}$ + $Link_{100}$ + $Link_{2500\ lite}$ + $Link_{2500}$
	1	1	0	1	1	1	$Link_{10}$ + Act_{10} + $Link_{100}$ + Act_{100} + $Link_{2500\ lite}$ + $Act_{2500\ lite}$ + $Link_{2500}$ + Act_{2500}
	0	0	1	1	1	0	$Link_{1000}$ + $Link_{2500\ lite}$ + $Link_{2500}$
	0	0	1	1	1	1	$Link_{1000}$ + Act_{1000} + $Link_{2500\ lite}$ + $Act_{2500\ lite}$ + $Link_{2500}$ + Act_{2500}
	1	0	1	1	1	0	$Link_{10}$ + $Link_{1000}$ + $Link_{2500\ lite}$ + $Link_{2500}$
	1	0	1	1	1	1	$Link_{10}$ + Act_{10} + $Link_{1000}$ + Act_{1000} + $Link_{2500\ lite}$ + $Act_{2500\ lite}$ + $Link_{2500}$ + Act_{2500}
	0	1	1	1	1	0	$Link_{100}$ + $Link_{1000}$ + $Link_{2500\ lite}$ + $Link_{2500}$
	0	1	1	1	1	1	$Link_{100}$ + Act_{100} + $Link_{1000}$ + Act_{1000} + $Link_{2500\ lite}$ + $Act_{2500\ lite}$ + $Link_{2500}$ + Act_{2500}
	1	1	1	1	1	0	$Link_{10}$ + $Link_{100}$ + $Link_{1000}$ + $Link_{2500\ lite}$ + $Link_{2500}$
	1	1	1	1	1	1	$Link_{10}$ + Act_{10} +$Link_{100}$ + Act_{100} + $Link_{1000}$ + Act_{1000} + $Link_{2500\ lite}$ + $Act_{2500\ lite}$ + $Link_{2500}$ + Act_{2500}

Table 31. Mode B LED Configuration

Pin	LINK Bit					Active (TX/RX) Bit	Description
	10Mbps	100Mbps	1000Mbps	2.5Gbps	1Gbps (2.5G lite)		
LED0 LED1 LED2	0	0	0	0	0	0	N/A
	0	0	0	0	0	1	Act_{10} + Act_{100} + Act_{1000} + $Act_{2500\ lite}$ + Act_{2500}
	1	0	0	0	0	0	$Link_{10}$
	1	0	0	0	0	1	$Link_{10}$ + Act_{10} + Act_{100} + Act_{1000} + $Act_{2500\ lite}$ + Act_{2500}
	0	1	0	0	0	0	$Link_{100}$
	0	1	0	0	0	1	$Link_{100}$ + Act_{10} + Act_{100} + Act_{1000} + $Act_{2500\ lite}$ + Act_{2500}
	1	1	0	0	0	0	$Link_{10}$ + $Link_{100}$
	1	1	0	0	0	1	$Link_{10}$ + $Link_{100}$ + Act_{10} + Act_{100} + Act_{1000} + $Act_{2500\ lite}$ + Act_{2500}
	0	0	1	0	0	0	$Link_{1000}$
	0	0	1	0	0	1	$Link_{1000}$ + Act_{10} + Act_{100} + Act_{1000} + $Act_{2500\ lite}$ + Act_{2500}
	1	0	1	0	0	0	$Link_{10}$ + $Link_{1000}$
	1	0	1	0	0	1	$Link_{10}$ + $Link_{1000}$ + Act_{10} + Act_{100} + Act_{1000} + $Act_{2500\ lite}$ + Act_{2500}
	0	1	1	0	0	0	$Link_{100}$ + $Link_{1000}$
	0	1	1	0	0	1	$Link_{100}$ + $Link_{1000}$ + Act_{10} + Act_{100} + Act_{1000} + $Act_{2500\ lite}$ + Act_{2500}
	1	1	1	0	0	0	$Link_{10}$ + $Link_{100}$ + $Link_{1000}$
	1	1	1	0	0	1	$Link_{10}$ + $Link_{100}$ + $Link_{1000}$ + Act_{10} + Act_{100} + Act_{1000} + $Act_{2500\ lite}$ + Act_{2500}
	0	0	0	1	0	0	$Link_{2500}$
	0	0	0	1	0	1	$Link_{2500}$ + Act_{10} + Act_{100} + Act_{1000} + $Act_{2500\ lite}$ + Act_{2500}
	1	0	0	1	0	0	$Link_{10}$ + $Link_{2500}$
	1	0	0	1	0	1	$Link_{10}$ + $Link_{2500}$ + Act_{10} + Act_{100} + Act_{1000} + $Act_{2500\ lite}$ + Act_{2500}
	0	1	0	1	0	0	$Link_{100}$ + $Link_{2500}$
	0	1	0	1	0	1	$Link_{100}$ + $Link_{2500}$ + Act_{10} + Act_{100} + Act_{1000} + $Act_{2500\ lite}$ + Act_{2500}
	1	1	0	1	0	0	$Link_{10}$ + $Link_{100}$ + $Link_{2500}$
	1	1	0	1	0	1	$Link_{10}$ + $Link_{100}$ + $Link_{2500}$ + Act_{10} + Act_{100} + Act_{1000} + $Act_{2500\ lite}$ + Act_{2500}
	0	0	1	1	0	0	Link1000 + Link2500
	0	0	1	1	0	1	$Link_{1000}$ + $Link_{2500}$ + Act_{10} + Act_{100} + Act_{1000} + $Act_{2500\ lite}$ + Act_{2500}

Pin	LINK Bit					Active (TX/RX) Bit	Description
	10Mbps	100Mbps	1000Mbps	2.5Gbps	1Gbps (2.5G lite)		
	1	0	1	1	0	0	$Link_{10} + Link_{1000} + Link_{2500}$
	1	0	1	1	0	1	$Link_{10} + Link_{1000} + Link_{2500} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	0	1	1	1	0	0	$Link_{100} + Link_{1000} + Link_{2500}$
	0	1	1	1	0	1	$Link_{100} + Link_{1000} + Link_{2500} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	1	1	1	1	0	0	$Link_{10} + Link_{100} + Link_{1000} + Link_{2500}$
	1	1	1	1	0	1	$Link_{10} + Link_{100} + Link_{1000} + Link_{2500} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	0	0	0	0	1	0	$Link_{2500\ lite}$
	0	0	0	0	1	1	$Link_{2500\ lite} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	1	0	0	0	1	0	$Link_{10} + Link_{2500\ lite}$
	1	0	0	0	1	1	$Link_{10} + Link_{2500\ lite} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	0	1	0	0	1	0	$Link_{100} + Link_{2500\ lite}$
	0	1	0	0	1	1	$Link_{100} + Link_{2500\ lite} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	1	1	0	0	1	0	$Link_{10} + Link_{100} + Link_{2500\ lite}$
	1	1	0	0	1	1	$Link_{10} + Link_{100} + Link_{2500\ lite} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	0	0	1	0	1	0	$Link_{1000} + Link_{2500\ lite}$
	0	0	1	0	1	1	$Link_{1000} + Link_{2500\ lite} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	1	0	1	0	1	0	$Link_{10} + Link_{1000} + Link_{2500\ lite}$
	1	0	1	0	1	1	$Link_{10} + Link_{1000} + Link_{2500\ lite} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	0	1	1	0	1	0	$Link_{100} + Link_{1000} + Link_{2500\ lite}$
	0	1	1	0	1	1	$Link_{100} + Link_{1000} + Link_{2500\ lite} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	1	1	1	0	1	0	$Link_{10} + Link_{100} + Link_{1000} + Link_{2500\ lite}$
	1	1	1	0	1	1	$Link_{10} + Link_{100} + Link_{1000} + Link_{2500\ lite} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	0	0	0	1	1	0	$Link_{2500\ lite} + Link_{2500}$

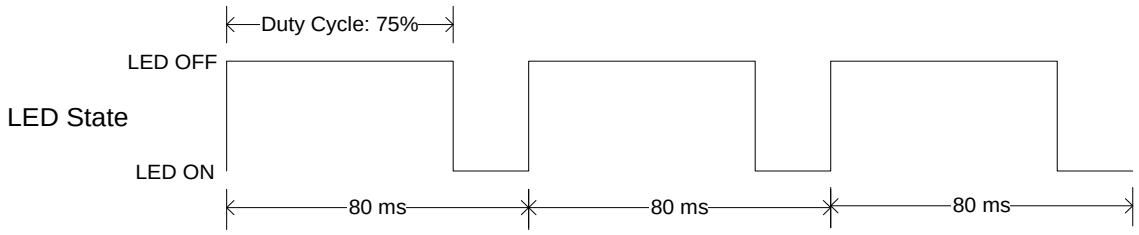
Pin	LINK Bit					Active (TX/RX) Bit	Description
	10Mbps	100Mbps	1000Mbps	2.5Gbps	1Gbps (2.5G lite)		
	0	0	0	1	1	1	$Link_{2500\ lite} + Link_{2500} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	1	0	0	1	1	0	$Link_{10} + Link_{2500\ lite} + Link_{2500}$
	1	0	0	1	1	1	$Link_{10} + Link_{2500\ lite} + Link_{2500} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	0	1	0	1	1	0	$Link_{100} + Link_{2500\ lite} + Link_{2500}$
	0	1	0	1	1	1	$Link_{100} + Link_{2500\ lite} + Link_{2500} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	1	1	0	1	1	0	$Link_{10} + Link_{100} + Link_{2500\ lite} + Link_{2500}$
	1	1	0	1	1	1	$Link_{10} + Link_{100} + Link_{2500\ lite} + Link_{2500} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	0	0	1	1	1	0	$Link_{1000} + Link_{2500\ lite} + Link_{2500}$
	0	0	1	1	1	1	$Link_{1000} + Link_{2500\ lite} + Link_{2500} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	1	0	1	1	1	0	$Link_{10} + Link_{1000} + Link_{2500\ lite} + Link_{2500}$
	1	0	1	1	1	1	$Link_{10} + Link_{1000} + Link_{2500\ lite} + Link_{2500} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	0	1	1	1	1	0	$Link_{100} + Link_{1000} + Link_{2500\ lite} + Link_{2500}$
	0	1	1	1	1	1	$Link_{100} + Link_{1000} + Link_{2500\ lite} + Link_{2500} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$
	1	1	1	1	1	0	$Link_{10} + Link_{100} + Link_{1000} + Link_{2500\ lite} + Link_{2500}$
	1	1	1	1	1	1	$Link_{10} + Link_{100} + Link_{1000} + Link_{2500\ lite} + Link_{2500} + Act_{10} + Act_{100} + Act_{1000} + Act_{2500\ lite} + Act_{2500}$

7.23.2. LED Blinking Frequency Control

The RTL8221B(I)-VB/RTL8221B(I)-VM supports LED blinking frequency control via MMD 31.0xD040 (see Table 32). The LED state is shown in Figure 9.

Table 32. LED Blinking Frequency Control (Register 31.53312)

Bit	RW	Description
11:10	RW	LED Blinking Frequency. 0: 240ms 1: 160ms (Default) 2: 80ms 3: Link Speed Dependent
9:8	RW	LED Blinking Duty Cycle. 0: 12.5% 1: 25% 2: 50% (Default) 3: 75%



Note: Assume the LED is in low active.

Figure 9. LED Blinking Frequency Example

7.24. Polarity Correction

The RTL8221B(I)-VB/RTL8221B(I)-VM automatically corrects polarity errors on the receive pairs in 2.5GBASE-T, 2.5GNBASE-T, 2.5G Lite, 1000BASE-T and 10BASE-Te modes. In 100BASE-TX mode polarity is irrelevant. In 1000BASE-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. Users may manually do polarity correction via the register if polarity is known beforehand. The polarity becomes unlocked only when the receiver loses lock.

In 10BASE-Te mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10BASE-Te link is up. The polarity becomes unlocked when the link is down.

7.25. Power

The system vendor needs to supply four steady power sources to the RTL8221B(I)-VB/RTL8221B(I)-VM (3.3V, 1.8V, and 0.95V) with correct power sequence (see section 8.8 Power Sequence, page 98). The RTL8221B(I)-VB/RTL8221B(I)-VM implements an option for the digital I/O and MDIO/MDC power. The default digital I/O and MDIO/MDC voltage is 3.3V with support for 1.8V.

7.26. PHY Reset (Hardware Reset)

The RTL8221B(I)-VB/RTL8221B(I)-VM has a PHYRSTB pin to reset the chip. For a complete PHY reset, this pin must be asserted low for at least 10ms (Tgap in Figure 10) to properly shut down an external power source via the POW_EXT_SWR pin. Wait for internal circuits settle time before accessing PHY registers (*68ms is recommended, as the 0.95V power rail rise time is less than 10ms).* All registers will return to default values after a hardware reset.

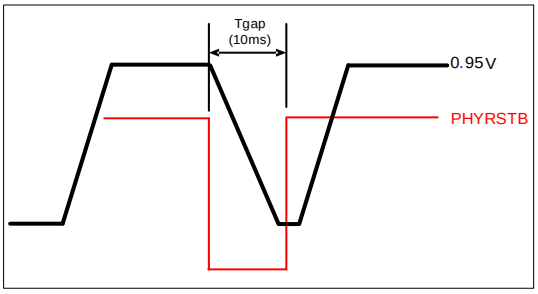


Figure 10. PHY Reset Timing

7.27. Rate Adaptor

The RTL8221B(I)-VB/RTL8221B(I)-VM's rate adaptor feature is used for auto rate matching of HiSGMII to Ethernet. The rate adaptor operates in two modes as described below:

1. **Normal Mode (Rate adaptor disable)**

The SerDes speed follows the Ethernet link speed change. When a packet is received from the SOC or link partner, the packet will be directly output, without buffering.

It supports five Ethernet speeds: 2.5G/1G/500M/100M/10M.

2. **Rate Adaptor (Enable)**

The SerDes speed is fixed at 2.5Gbps and the Ethernet speed cannot be higher than the SerDes speed. SOC does not follow the Ethernet link speed and cannot change the SerDes speed in this mode. There is a data flow control mechanism to ensure correct data transmission.

Note: When rate adaptor mode is enabled, the RTL8221B(I)-VB/8221B(I)-VM cannot support MAC mode EEE function. In rate adaptor mode, the RTL8221B(I)-VB/8221B(I)-VM only supports PHY mode EEE.

Feature List

- Supports Fix interframe gap (12Byte)
- Supports jumbo frames size up to 16KByte
- Supports early TX for SerDes send data to Ethernet
- Supply flow control to send pause/release packet when FIFO near full/empty
- Supports pause packet detect from SerDes and Ethernet direction
- Supports FIFO almost full/empty threshold dynamic adjustment

8. Register Descriptions

8.1. Register Access Types

Table 33. Register Access Types

Type	Description
LH	Latch high. If the status is high, this field is set to '1' and remains set.
RC	Read-cleared. The register field is cleared after read.
RO	Read only.
WO	Write only.
RW	Read and Write.
SC	Self-cleared. Writing a '1' to this register field causes the function to be activated immediately, and then the field will be automatically cleared to '0'.

8.2. MMD Register Mapping and Definition

Table 34. MMD Register Mapping and Definition

Device	MMD Name	Description
1	PMA/PMD	PMA/PMD Control Register.
3	PCS	PCS Control Register.
7	Auto-Negotiation	Auto-Negotiation Register.
30	Vendor specific 1	SERDES Control Register.
31	Vendor specific 2	PHY Control Register.
Otherwise	Reserved	Reserved.

8.3. PMA/PMD MMD Mapping and Definition

Table 35. PMA/PMD MMD Register Mapping and Definitions

Register Address	Register Name	Subclause
1.0x0000	PMA/PMD control 1	45.2.1.1
1.0x0001	PMA/PMD status 1	45.2.1.2
1.0x0002	PMA/PMD device identifier 1	45.2.1.3
1.0x0003	PMA/PMD device identifier 2	45.2.1.3
1.0x0004	PMA/PMD speed ability	45.2.1.4
1.0x000B	PMA/PMD extended ability	45.2.1.10
1.0x0015	2.5G PMA/PMD extended ability	45.2.1.14
1.0x0081	Multi-GBASE-T status	45.2.1.62
1.0x0082	Multi-GBASE-T pair swap and polarity	45.2.1.63
1.0x0083	Multi-GBASE-T TX power backoff and PHY short reach setting	45.2.1.64
1.0x0084	Multi-GBASE-T test mode	45.2.1.65
1.0x0091	Multi-GBASE-T skew delay 1	45.2.1.78
1.0x0092	Multi-GBASE-T skew delay 2	45.2.1.78
1.0x0093	Multi-GBASE-T fast retrain status and control	45.2.1.79
Otherwise	Reserved	Reserved

8.3.1. PMA/PMD Control 1 Register MMD 1.0x0000)

Table 36. PMA/PMD Control 1 Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0000.15	Reset	RW, SC	0	Reset. 1: PMA/PMD reset 0: Normal operation This action may change the internal PHY state and the state of the physical link associated with the PHY.
1.0x0000.14	Reserved	RO	0	Value always 0.

<table>
<tr><th>Bit</th><th>Name</th><th>Type</th><th>Default</th><th>Description</th></tr>
<tr><td>1.0x000
0.13</td><td>Speed selection (LSB)</td><td>RW</td><td>0</td><td>Speed Select Bit 0.
In forced mode, i.e., when Auto-Negotiation is disabled, bits 0.6 and 0.13 can be used to determine device speed selection. See mmd 31.0.0 for detailed description.
<table>
<tr><th>1.0.6</th><th>1.0.13</th><th>Speed Enabled</th></tr>
<tr><td>1</td><td>1</td><td>Bits 5:2 select speed</td></tr>
<tr><td>1</td><td>0</td><td>1000Mbps</td></tr>
<tr><td>0</td><td>1</td><td>100Mbps</td></tr>
<tr><td>0</td><td>0</td><td>10Mbps</td></tr>
</table></td></tr>
<tr><td>1.0x000
0.12</td><td>Reserved</td><td>RO</td><td>0</td><td>Value always 0.</td></tr>
<tr><td>1.0x000
0.11</td><td>Low power</td><td>RW</td><td>0</td><td>Power Down.
1: Power down (only Management Interface and logic are active; link is down)
0: Normal operation</td></tr>
<tr><td>1.0x000
0.10:7</td><td>Reserved</td><td>RO</td><td>4’b0</td><td>Value always 0.</td></tr>
<tr><td>1.0x000
0.6</td><td>Speed selection (MSB)</td><td>RW,
SC</td><td>1</td><td>Speed Select Bit 1.
In forced mode, i.e., when Auto-Negotiation is disabled, the bits 0.6 and 0.13 can be used to determine device speed selection. See mmd 31.0.0 for a detailed description.
<table>
<tr><th>1.0.6</th><th>1.0.13</th><th>Speed Enabled</th></tr>
<tr><td>1</td><td>1</td><td>Bits 5:2 select speed</td></tr>
<tr><td>1</td><td>0</td><td>1000Mbps</td></tr>
<tr><td>0</td><td>1</td><td>100Mbps</td></tr>
<tr><td>0</td><td>0</td><td>10Mbps</td></tr>
</table></td></tr>
<tr><td>1.0x000
0.5:2</td><td>Speed selection</td><td>RW</td><td>4’b 0110</td><td>5 4 3 2
0 1 1 0: 2.5Gb/s
Otherwise: Reserved.</td></tr>
<tr><td>1.0x000
0.1</td><td>PMA remote loopback</td><td>RW</td><td>0</td><td>1: Enable PMA remote loopback mode
0: Disable PMA remote loopback mode</td></tr>
<tr><td>1.0x000
0.0</td><td>PMA local loopback</td><td>RW</td><td>0</td><td>1: Enable PMA local loopback mode
0: Disable PMA local loopback mode</td></tr>
</table>

Note 1: To make bits speed selection bits effective, 1.0x0000.13 & 1.0x0000.6 or 1.0x0000.5:2 must have consistent setting, i.e., only one speed could be set among these bits.

Note 2: PMA remote loopback is not supported by the RTL8221B(I)-VB/RTL8221B(I)-VM thus its value would not affect the system operation.

Note 3: PMA local loopback is supported by the RTL8221B(I)-VB/RTL8221B(I)-VM. Note that the RTL8221B(I)-VB/8221B(I)-VM provides several loopback modes for self-diagnosis purposes. Only one loopback mode should be set at one time. Triggering more than 2 loopback modes at the same time might cause a system crash.

8.3.2. PMA/PMD Status 1 Register (MMD 1.0x0001)

Table 37. PMA/PMD Status 1 Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0001.15:8	Reserved	RO	8'b 0	Value always 0.
1.0x0001.7	PMA Fault	RO	0	1: Fault condition detected 0: Fault condition not detected
1.0x0001.6:3	Reserved	RO	4'b 0	Value always 0.
1.0x0001.2	Receive link status	RO, LL	0	1: PMA/PMD receive link up 0: PMA/PMD receive link down
1.0x0001.1	Low-power ability	RO	1	1: PMA/PMD supports low-power mode 0: PMA/PMD does not support low-power mode
1.0x0001.0	Reserved	RO	0	Value always 0.

8.3.3. PMA/PMD Device Identifier 1 Register (MMD 1.0x0002)

Table 38. PMA/PMD Device Identifier 1 Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0002.15:0	Realtek OUI [21:6]	RO	0x1C	Realtek OUI, bit 21 to bit 6.

8.3.4. PMA/PMD Device Identifier 2 Register (MMD 1.0x0003)

Table 39. PMA/PMD Device Identifier 2 Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0003.15:10	Realtek OUI [5:0]	RO	0x32	Realtek OUI, bit 5 to bit 0.
1.0x0003.9:4	Model number	RO	0x4	Value always 4 for RTL8221B(I)-VB/RTL8221B(I)-VM series.
1.0x0003.3	sample classification	RO	0x0	0: ES sample 1:MP sample
1.0x0003.2:0	Revision number	RO	0x1	1:RTL8221B-VB 2: RTL8221B-VM

8.3.5. PMA/PMD Speed Ability Register (MMD 1.0x0004)

Table 40. PMA/PMD Speed Ability Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0004.15	Reserved	RO	0	Value always 0.
1.0x0004.14	Reserved	RO	0	Reserved.
1.0x0004.13	2.5G capable	RO	1	1: PMA/PMD is capable of operating at 2.5 Gb/s 0: PMA/PMD is not capable of operating at 2.5 Gb/s
1.0x0004.12:10	Reserved	RO	3'b 0	Value always 0.
1.0x0004.9	Reserved	RO	0	Reserved.
1.0x0004.8	Reserved	RO	0	Reserved.
1.0x0004.7	Reserved	RO	0	Reserved.
1.0x0004.6	10M capable	RO	1	1: PMA/PMD is capable of operating at 10 Mb/s 0: PMA/PMD is not capable of operating at 10 Mb/s

Bit	Name	Type	Default	Description
1.0x0004.5	100M capable	RO	1	1: PMA/PMD is capable of operating at 100 Mb/s 0: PMA/PMD is not capable of operating at 100 Mb/s
1.0x0004.4	1000M capable	RO	1	1: PMA/PMD is capable of operating at 1000 Mb/s 0: PMA/PMD is not capable of operating at 1000 Mb/s
1.0x0004.3	Reserved	RO	0	Value always 0.
1.0x0004.2	10PASS-TS capable	RO	0	1: PMA/PMD is capable of operating at 10PASS-TS 0: PMA/PMD is not capable of operating at 10PASS-TS
1.0x0004.1	2BASE-TL capable	RO	0	1: PMA/PMD is capable of operating at 2BASE-TL 0: PMA/PMD is not capable of operating at 2BASE-TL
1.0x0004.0	Reserved	RO	0	Reserved.

8.3.6. PMA/PMD Extended Ability Register (MMD 1.0x000B)

Table 41. PMA/PMD Extended Ability Register Bit Definitions Bit Definitions

Bit	Name	Type	Default	Description
1.0x000B.15	Reserved	RO	0	Value always 0.
1.0x000B.14	2.5G extended abilities	RO	1	1: PMA/PMD has 2.5G extended abilities listed in register 1.21 0: PMA/PMD does not have 2.5G extended abilities
1.0x000B.13:11	Reserved	RO	3'b 0	Value always 0.
1.0x000B.10	Reserved	RO	0	Reserved.
1.0x000B.9	P2MP ability	RO	0	1: PMA/PMD has P2MP abilities listed in register 1.12 0: PMA/PMD does not have P2MP abilities
1.0x000B.8	10BASE-Te ability	RO	1	1: PMA/PMD is able to perform 10BASE-Te 0: PMA/PMD is not able to perform 10BASE-Te
1.0x000B.7	100BASE-TX ability	RO	1	1: PMA/PMD is able to perform 100BASE-TX 0: PMA/PMD is not able to perform 100BASE-TX
1.0x000B.6	1000BASE-KX ability	RO	0	1: PMA/PMD is able to perform 1000BASE-KX 0: PMA/PMD is not able to perform 1000BASE-KX
1.0x000B.5	1000BASE-T ability	RO	1	1: PMA/PMD is able to perform 1000BASE-T 0: PMA/PMD is not able to perform 1000BASE-T
1.0x000B.4	Reserved	RO	0	Reserved.
1.0x000B.3	Reserved	RO	0	Reserved.
1.0x000B.2	Reserved	RO	0	Reserved.
1.0x000B.1	Reserved	RO	0	Reserved.
1.0x000B.0	Reserved	RO	0	Reserved.

8.3.7. 2.5G PMA/PMD Extended Ability Register (MMD 1.0x0015)

Table 42. 2.5G/5G PMA/PMD Extended Ability Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0015.15:2	Reserved	RO	14'b 0	Value always 0.
1.0x0015.1	Reserved	RO	0	Reserved.
1.0x0015.0	2.5GBASE-T ability	RO	1	1: PMA/PMD is able to perform 2.5GBASE-T 0: PMA/PMD is not able to perform 2.5GBASE-T

8.3.8. Multi-GBASE-T Status Register (MMD 1.0x0081)

Table 43. Multi-GBASE-T Status Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0081.15:1	Reserved	RO	15'b 0	Value always 0.
1.0x0081.0	LP information valid	RO	0	1: Link partner information is valid in 10G/ 5G/ 2.5GBASE-T 0: Link partner information is invalid in 10G/ 5G/ 2.5GBASE-T

8.3.9. Multi-GBASE-T Pair Swap and Polarity Register (MMD 1.0x0082)

Table 44. Multi-GBASE-T Pair Swap and Polarity Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0082.15:12	Reserved	RO	4'b 0	Value always 0.
1.0x0082.11	Pair D polarity	RO	0	1: Polarity of pair D is reversed 0: Polarity of pair D is not reversed
1.0x0082.10	Pair C polarity	RO	0	1: Polarity of pair C is reversed 0: Polarity of pair C is not reversed
1.0x0082.9	Pair B polarity	RO	0	1: Polarity of pair B is reversed 0: Polarity of pair B is not reversed
1.0x0082.8	Pair A polarity	RO	0	1: Polarity of pair A is reversed 0: Polarity of pair A is not reversed
1.0x0082.7:2	Reserved	RO	6'b 0	Value always 0.
1.0x0082.1:0	MDI/MDI-X connection	RO	2'b 0	bit1 bit0. 1 1: No crossover 1 0: Reserved 0 1: Reserved 0 0: Pair A/B and pair C/D crossover

8.3.10. Multi-GBASE-T TX Power Backoff and PHY Short Reach Setting Register (MMD 1.0x0083)

Table 45. Multi-GBASE-T TX Power Backoff and PHY Short Reach Setting Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0083.15:13	Link partner TX power backoff setting	RO	3'b 0	15 14 13 1 1 1: 14 dB 1 1 0: 12 dB 1 0 1: 10 dB 1 0 0: 8 dB 0 1 1: 6 dB 0 1 0: 4 dB 0 0 1: 2 dB 0 0 0: 0 dB
1.0x0083.12:10	TX power backoff setting	RO	3'b 0	12 11 10 1 1 1: 14 dB 1 1 0: 12 dB 1 0 1: 10 dB 1 0 0: 8 dB 0 1 1: 6 dB 0 1 0: 4 dB 0 0 1: 2 dB 0 0 0: 0 dB
1.0x0083.9:1	Reserved	RO	9'b 0	Value always 0.
1.0x0083.0	Short reach mode	RW	4'b 0	1: PHY is operating in short reach mode 0: PHY is not operating in short reach mode

8.3.11. Multi-GBASE-T Test Mode Register (MMD 1.0x0084)

Table 46. Multi-GBASE-T Test Mode Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0084.15:13	Test mode control	RW	3'b0	15 14 13 1 1 1: Test mode 7 1 1 0: Test mode 6 1 0 1: Test mode 5 1 0 0: Test mode 4 0 1 1: Test mode 3 0 1 0: Test mode 2 0 0 1: Test mode 1 0 0 0: Normal operation
1.0x0084.12:10	Transmitter test frequencies	RW	3'b001	12 11 10 1 1 1: Reserved 1 1 0: Dual tone 5 1 0 1: Dual tone 4 1 0 0: Dual tone 3 0 1 1: Reserved 0 1 0: Dual tone 2 0 0 1: Dual tone 1 0 0 0: Reserved
1.0x0084.9:0	Reserved	RO	10'b 0	Value always 0.

8.3.12. Multi-GBASE-T Skew Delay 1 Register (MMD 1.0x0091)

Table 47. Multi-GBASE-T Skew Delay 1 Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0091.15	Reserved	RO	0	Value always 0.
1.0x0091.14:8	Skew delay B	RO	7'b 0	Skew delay for pair B.
1.0x0091.7:0	Reserved	RO	8'b 0	Value always 0.

8.3.13. Multi-GBASE-T Skew Delay 2 Register (MMD 1.0x0092)

Table 48. Multi-GBASE-T Skew Delay 2 Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0092.15	Reserved	RO	0	Value always 0.
1.0x0092.14:8	Skew delay D	RO	7'b0	Skew delay for pair D.
1.0x0092.7	Reserved	RO	0	Value always 0.
1.0x0092.6:0	Skew delay C	RO	7'b0	Skew delay for pair C.

8.3.14. Multi-GBASE-T Fast Retrain Status and Control Register (MMD 1.0x0093)

Table 49. Multi-GBASE-T Fast Retrain Status and Control Register Bit Definitions

Bit	Name	Type	Default	Description
1.0x0093.15:11	LP fast retrain count	RO, LH, RC	5'b0	Counts the number of fast retrains requested by the link partner.
1.0x0093.10:6	LD fast retrain count	RO, LH, RC	5'b0	Counts the number of fast retrains requested by the local device.
1.0x0093.5	Reserved	RO	0	Value always 0.
1.0x0093.4	Fast retrain ability	RO	0	1: Fast retrain capability is supported 0: Fast retrain capability is not supported
1.0x0093.3	Fast retrain negotiated	RO	0	1: Fast retrain capability was negotiated 0: Fast retrain capability was not negotiated
1.0x0093.2:1	Fast retrain signal type	RW	2'b 01	11: Reserved 10: PHY signals Link Interruption during fast retrain 01: PHY signals Local Fault during fast retrain 00: PHY signals IDLE during fast retrain
1.0x0093.0	Fast retrain enable	RW	1	1: Fast retrain capability is enabled 0: Fast retrain capability is disabled

8.4. PCS Registers

Table 50. PCS Registers Mapping and Definitions

Register Address	Register Name	Subclause
3.0x0000	PCS control 1	45.2.3.1
3.0x0001	PCS status 1	45.2.3.2
3.0x0004	PCS speed ability	45.2.3.4
3.0x0014	EEE control and capability	45.2.3.9
3.0x0015	EEE control and capability 2	45.2.3.9
3.0x0016	EEE wake error counter	45.2.3.10
Otherwise	Reserved	Reserved.

8.4.1. PCS Control 1 Register (MMD 3.0x0000)

Table 51. PCS control 1 Register Bit Definitions

Bit	Name	Type	Default	Description
3.0x0000.15	Reset	RW	0	1: PCS reset 0: Normal operation
3.0x0000.14	Loopback	RW	0	1: Enable loopback mode 0: Disable loopback mode
3.0x0000.13	Speed selection	RO	0	13 6 1 1: Bits 5:2 select speed 0 x: Unspecified x 0: Unspecified
3.0x0000.12	Reserved	RO	0	Value always 0.
3.0x0000.11	Low power	RW	0	1: Low-power mode 0: Normal operation
3.0x0000.10	Clock stop enable	RW	0	1: The PHY may stop the clock during LPI 0: Clock not stoppable
3.0x0000.9:7	Reserved	RO	3'b 0	Value always 0.
3.0x0000.6	Speed selection	RO	1	13 6 1 1: Bits 5:2 select speed 0 x: Unspecified x 0: Unspecified
1.0x0000.5:2	Speed selection	RO	4'b 0111	5 4 3 2 0 1 1 1: 2.5Gb/s Otherwise: Reserved
1.0x0000.1:0	Reserved	RO	2'b 0	1: Enable PMA remote loopback mode 0: Disable PMA remote loopback mode

Note 1: 3.0x0000.13 & 3.0x0000.6 or 3.0x0000.5:2 will have no effect when Auto-Negotiation is 0. That is, they are unlike 1.0x0000.13& 1.0x0000.6 or 1.0x0000.5:2.
Note 2: PCS loopback is supported by the RTL8221B(I)-VB/RTL8221B(I)-VM. Note that the RTL8221B(I)-VB/ RTL8221B(I)-VM provides several loopback modes for self-diagnosis purposes. Only one loopback mode should be set at one time. Triggering more than 2 loopback modes at the same time might cause a system crash.

8.4.2. PCS Status 1 Register (MMD 3.0x0001)

Table 52. PCS Status 1 Register Bit Definitions

Bit	Name	Type	Default	Description
3.0x0001.15:12	Reserved	RO	4'b 0	Value always 0.
3.0x0001.11	Tx LPI received	RO, LH	0	1: Tx PCS has received LPI 0: LPI not received
3.0x0001.10	Rx LPI received	RO, LH	0	1: Rx PCS has received LPI 0: LPI not received
3.0x0001.9	Tx LPI indication	RO	0	1: Tx PCS is currently receiving LPI 0: PCS is not currently receiving LPI
3.0x0001.8	Rx LPI indication	RO	0	1: Rx PCS is currently receiving LPI 0: PCS is not currently receiving LPI
3.0x0001.7	Fault	RO	1	1: Fault condition detected 0: No fault condition detected
3.0x0001.6	Clock stop capable	RO	0	1: The MAC may stop the clock during LPI 0: Clock not stoppable
3.0x0001.5:3	Reserved	RO	0	Value always 0.
3.0x0001.2	PCS receive link status	RO, LL	0	1: PCS receive link up 0: PCS receive link down
3.0x0001.1	Low-power ability	RO	0	1: PCS supports low-power mode 0: PCS does not support low-power mode
3.0x0001.0	Reserved	RO	0	Value always 0.

8.4.3. PCS Speed Ability Register (MMD 3.0x0004)

Table 53. PCS Speed Ability Register Bit Definitions

Bit	Name	Type	Default	Description
3.0x0004.15:8	Reserved	RO	8'b 0	Value always 0.
3.0x0004.7	Reserved	RO	0	Reserved.
3.0x0004.6	2.5G capable	RO	1	1: PCS is capable of operating at 2.5 Gb/s 0: PCS is not capable of operating at 2.5 Gb/s
3.0x0004.5:4	Reserved	RO	2'b 0	Value always 0.
3.0x0004.3	Reserved	RO	0	Reserved.
3.0x0004.2	Reserved	RO	0	Reserved.
3.0x0004.1	10PASS-TS/2BASE-TL capable	RO	0	1: PCS is capable of operating at the 10P/2B PCS 0: PCS is not capable of operating at the 10P/2B PCS
3.0x0004.0	Reserved	RO	0	Reserved.

8.4.4. EEE Control and Capability Register (MMD 3.0x0014)

Table 54. EEE Control and Capability Register Bit Definitions

Bit	Name	Type	Default	Description
3.0x0014.15:5	Reserved	RO	0	Value always 0.
3.0x0014.4	1000BASE-KX EEE	RO	0	1: EEE is supported for 1000BASE-KX 0: EEE is not supported for 1000BASE-KX
3.0x0014.3	Reserved	RO	0	Value always 0.
3.0x0014.2	1000BASE-T EEE	RO	1	1: EEE is supported for 1000BASE-T 0: EEE is not supported for 1000BASE-T
3.0x0014.1	100BASE-TX EEE	RO	1	1: EEE is supported for 100BASE-TX 0: EEE is not supported for 100BASE-TX
3.0x0014.0	Reserved	RO	0	Value always 0.

8.4.5. EEE Control and Capability 2 Register (MMD 3.0x0015)

Table 55. EEE Control and Capability 2 Register Bit Definitions

Bit	Name	Type	Default	Description
3.0x0015.15:1	Reserved	RO	15'b 0	Value always 0.
3.0x0015.0	2.5GBASE-T EEE	RO	1	1: EEE is supported for 2.5GBASE-T 0: EEE is not supported for 2.5GBASE-T

8.4.6. EEE Wake Error Counter (MMD 3.0x0016)

Table 56. EEE Wake Error Counter Bit Definitions

Bit	Name	Type	Default	Description
3.0x0016.15:0	EEE wake time fault counter	RO, SC	16'b0	Count EEE wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type.

8.5. Auto-Negotiation Registers

Table 57. Auto-Negotiation Registers Mapping and Definitions

Register Address	Register Name	Subclause
7.0x0000	AN control	45.2.7.1
7.0x0001	AN status	45.2.7.2
7.0x0010	AN advertisement	45.2.7.6
7.0x0013	AN LP base page ability register	45.2.7.7
7.0x0016 through 7.0x0018	AN XNP transmit	45.2.7.8
7.0x0020	Multi-GBASE-T AN control	45.2.7.10
7.0x0021	Multi-GBASE-T AN status	45.2.7.11
7.0x003C	EEE advertisement	45.2.7.13
7.0x003D	EEE LP ability	45.2.7.14
7.0x003E	EEE advertisement 2	45.2.7.14
7.0x003F	EEE link partner ability 2	45.2.7.14
7.0x0040	Multi-GBASE-TBASE-T AN control 2	45.2.7.14
7.0x0041	Multi-GBASE-TBASE-T AN status 2	45.2.7.14
otherwise	Reserved	Reserved

8.5.1. AN Control Register (MMD 7.0x0000)

Table 58. AN Control Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0000.15	AN reset	RW	0	1: AN reset 0: AN normal operation
7.0x0000.14	Reserved	RO	0	Value always 0.
7.0x0000.13	Extended Next Page control	RW	1	1: Extended Next Pages are enabled 0: Extended Next Pages are disabled
7.0x0000.12	Auto-Negotiation enable	RW	1	1: Enable Auto-Negotiation process 0: Disable Auto-Negotiation process
7.0x0000.11:10	Reserved	RO	0	Value always 0.
7.0x0000.9	Restart Auto-Negotiation	RW, SC	0	1: Restart Auto-Negotiation process 0: Auto-Negotiation in process, disabled, or not supported
7.0x0000.8:0	Reserved	RO	0	Value always 0.

8.5.2. AN Status Register (MMD 7.0x0001)

Table 59. AN Status Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0001.15:10	Reserved	RO	6'b 0	Value always 0.
7.0x0001.9	Parallel detection fault	RO	0	1: A fault has been detected via the parallel detection function 0: A fault has not been detected via the parallel detection function
7.0x0001.8	Reserved	RO	0	Value always 0.
7.0x0001.7	Extended Next Page status	RO	0	1: Extended Next Page format is used 0: Extended Next Page is not allowed
7.0x0001.6	Page received	RO	0	1: A page has been received 0: A page has not been received
7.0x0001.5	Auto-Negotiation complete	RO	0	1: Auto-Negotiation process completed 0: Auto-Negotiation process not completed
7.0x0001.4	Remote fault	RO	0	1: remote fault condition detected 0: no remote fault condition detected
7.0x0001.3	Auto-Negotiation ability	RO	1	1: PHY is able to perform Auto-Negotiation 0: PHY is not able to perform Auto-Negotiation
7.0x0001.2	Link status	RO	0	1: Link is up 0: Link is down
7.0x0001.1	Reserved	RO	0	Value always 0.
7.0x0001.0	Link partner Auto-Negotiation ability	RO	0	1: LP is able to perform Auto-Negotiation 0: LP is not able to perform Auto-Negotiation

8.5.3. AN Advertisement Register (MMD 7.0x0010)

Table 60. AN Advertisement Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0010.15	Next Page	RW	0	1: Additional next pages exchange desired 0: No additional next pages exchange desired
7.0x0010.14	Acknowledge	RO	0	Value always 0, writes ignored.
7.0x0010.13	Remote fault	RW	0	1: Set Remote Fault bit 0: No remote fault detected
7.0x0010.12	XNP	RW	1	1: Extended Next Page format is used 0: Extended Next Page is not allowed
7.0x0010.11	Asymmetric PAUSE	RW	0	1: Advertise support of asymmetric pause 0: No support of asymmetric pause
7.0x0010.10	PAUSE	RW	0	1: Advertise support of pause frames 0: No support of pause frames
7.0x0010.9	100BASE-T4	RO	0	1: 100BASE-T4 support 0: 100BASE-T4 not supported
7.0x0010.8	100BASE-TX (Full)	RW	1	1: Advertise support of 100BASE-TX full-duplex mode 0: Not advertised
7.0x0010.7	100BASE-TX (Half)	RW	1	1: Advertise support of 100BASE-TX half-duplex mode 0: Not advertised

Bit	Name	Type	Default	Description
7.0x0010.6	10BASE-Te (Full)	RW	1	1: Advertise support of 10BASE-TeX full-duplex mode 0: Not advertised
7.0x0010.5	10BASE-Te (Half)	RW	1	1: Advertise support of 10BASE-TeX half-duplex mode 0: Not advertised
7.0x0010.4:0	Selector field	RO	5'b00001	Indicates the RTL8221B(I)-VB/RTL8221B(I)-VM supports IEEE 802.3.

8.5.4. AN LP Base Page Ability Register (MMD 7.0x0013)

Table 61. AN LP Base Page Ability Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0013.15	Next Page	RO	0	1: Link partner support for transmission and reception of additional link coed word encodings 0: No additional next pages exchange desired
7.0x0013.14	Acknowledge	RO	0	1: Link partner has successfully received Link Code Word
7.0x0013.13	Remote fault	RO	0	1: Link partner Indicate to local device that a fault condition has occurred
7.0x0013.12	XNP	RO	0	1: Link partner supports Extended Next Page 0: Extended Next Page is not supported
7.0x0013.11	Asymmetric PAUSE	RO	0	1: Link partner support Asymmetric PAUSE operation for full duplex links 0: No support of asymmetric pause
7.0x0013.10	PAUSE	RO	0	1: Link partner support PAUSE operation for full duplex links 0: No support of pause frames
7.0x0013.9	100BASE-T4	RO	0	1: Link partner support 100BASE-T4 capability 0: 100BASE-T4 not supported
7.0x0013.8	100BASE-TX (Full)	RO	0	1: Link partner support 100BASE-TX full duplex capability 0: Not advertised
7.0x0013.7	100BASE-TX (Half)	RO	0	1: Link partner support 100BASE-TX half duplex capability 0: Not advertised
7.0x0013.6	10BASE-Te (Full)	RO	0	1: Link partner support 10BASE-Te full duplex capability 0: Not advertised
7.0x0013.5	10BASE-Te (Half)	RO	0	1: Link partner support 10BASE-Te half duplex capability 0: Not advertised
7.0x0013.4:0	Selector field	RO	5'b00000	Indicates the link partner supports IEEE 802.3.

8.5.5. AN XNP Transmit Register (MMD 7.0x0016~7.0x0018)

Table 62. AN XNP Transmit Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0016.15	Next Page	RW	0	1: Additional next pages exchange desired 0: No additional next pages exchange desired
7.0x0016.14	Reserved	RO	0	1: Link partner has successfully received Link Code Word
7.0x0016.13	Message Page	RW	0	1: XNP message page coding 0: XNP unformatted page coding
7.0x0016.12	Acknowledge 2	RW	0	1: Will comply with message 0: Cannot comply with message
7.0x0016.11	Toggle	RO	0	1: Previous value of the transmitted link codeword equaled 1 0: Previous value of the transmitted link codeword equaled 0
7.0x0016.10:0	Message/Unformatted Code Field	RW	11'b 0	If 7.0x0016.13 is 1, then these bits are random seed used for master/slave decision and is RO. Otherwise these bits should be self-defined.
7.0x0017.15:0	Unformatted Code Field 1	RW	16'b 0	Self-defined message used to advertise ability during Auto-Negotiation process.
7.0x0018.15:0	Unformatted Code Field 2	RW	16'b 0	Self-defined message used to advertise ability during Auto-Negotiation process.

8.5.6. Multi-GBASE-TBASE-T AN Control 1 Register (MMD 7.0x0020)

Table 63. Multi-GBASE-TBASE-T AN Control 1 Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0020.15	MASTER-SLAVE manual config enable	RW	0	1: Enable MASTER-SLAVE manual configuration 0: Disable MASTER-SLAVE manual configuration Default value is 0.
7.0x0020.14	MASTER-SLAVE config value	RW	0	1: Configure PHY as MASTER 0: Configure PHY as SLAVE Default value is 0.
7.0x0020.13	Port type	RW	0	1: Multiport device 0: single-port device
7.0x0020.12	Reserved	RW	0	Reserved.
7.0x0020.11:9	Reserved	RO	3'b 0	Value always 0.
7.0x0020.8	Reserved	RO	0	Value always 0.
7.0x0020.7	2.5GBASE-T ability	RW	0	1: Advertise PHY as 2.5GBASE-T capable 0: Do not advertise PHY as 2.5GBASE-T capable
7.0x0020.6	Reserved	RW	0	Reserved.
7.0x0020.5	2.5GBASE-T Fast retrain ability	RW	0	1: Advertise PHY as 2.5GBASE-T fast retrain capable 0: Do not advertise PHY as 2.5GBASE-T fast retrain capable
7.0x0020.4:3	Reserved	RO	2'b 0	Value always 0.

Bit	Name	Type	Default	Description
7.0x0020.2	LD PMA training reset request	RW	0	1: Local device requests that link partner reset PMA training PRBS every frame 0: Local device requests that link partner run PMA training PRBS continuously
7.0x0020.1	Reserved	RW	0	Reserved.
7.0x0020.0	LD loop timing ability	RW	1	1: Advertise PHY as capable of loop timing 0: Do not advertise PHY as capable of loop timing

8.5.7. Multi-GBASE-TBASE-T AN Status 1 Register (MMD 7.0x0021)

Table 64. Multi-GBASE-TBASE-T AN Status 1 Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0021.15	MASTER-SLAVE manual config enable	RO, LH, SC	0	1: MASTER-SLAVE configuration fault detected 0: No MASTER-SLAVE configuration fault detected
7.0x0021.14	MASTER-SLAVE config value	RO	0	1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE
7.0x0021.13	Local receiver status	RO	0	1: Local receiver OK 0: Local receiver not OK
7.0x0021.12	Remote receiver status	RO	0	1: Remote receiver OK 0: Remote receiver not OK
7.0x0021.11	Link partner 10GBASE-T capability	RO	0	1: Link partner is able to operate as 10GBASE-T 0: Link partner is not able to operate as 10GBASE-T This bit is guaranteed to be valid only when the Page received bit (7.0x0001.6) has been set to 1.
7.0x0021.10	LP loop timing ability	RO	0	1: Link partner is capable of loop timing 0: Link partner is not capable of loop timing
7.0x0021.9	LP PMA training reset request	RO	0	1: Link partner requests that local device reset PMA training PRBS every frame 0: Link partner requests that local device run PMA training PRBS continuously
7.0x0021.8:7	Reserved	RO	2’b 0	Value always 0.
7.0x0021.6	Link partner 5GBASE-T capability	RO	0	1: Link partner is able to operate as 5GBASE-T 0: Link partner is not able to operate as 5GBASE-T
7.0x0021.5	Link partner 2.5GBASE-T capability	RO	0	1: Link partner is able to operate as 2.5GBASE-T 0: Link partner is not able to operate as 2.5GBASE-T
7.0x0021.4	5GBASE-T Fast retrain ability	RO	0	1: Link partner is capable of 5GBASE-T fast retrain 0: Link partner is not capable of 5GBASE-T fast retrain
7.0x0021.3	2.5GBASE-T Fast retrain ability	RO	0	1: Link partner is capable of 2.5GBASE-T fast retrain 0: Link partner is not capable of 2.5GBASE-T fast retrain
7.0x0021.2	Reserved	RO	0	Value always 0.
7.0x0021.1	10GBASE-T Fast retrain ability	RO	0	1: Link partner is capable of 10GBASE-T fast retrain 0: Link partner is not capable of 10GBASE-T fast retrain
7.0x0021.0	Reserved	RO	0	Value always 0.

8.5.8. EEE Advertisement Register (MMD 7.0x003C)

Table 65. EEE Advertisement Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x003C.15:7	Reserved	RO	9'b 0	Value always 0.
7.0x003C.6	Reserved	RO	0	Reserved.
7.0x003C.5	Reserved	RO	0	Reserved.
7.0x003C.4	1000BASE-KX EEE	RO	0	1: Advertise that 1000BASE-KX has EEE capability 0: Do not advertise that 1000BASEKX has EEE capability
7.0x003C.3	Reserved	RO	0	Reserved.
7.0x003C.2	1000BASE-T EEE	RW	1	1: Advertise that 1000BASE-T has EEE capability 0: Do not advertise that 1000BASE-T has EEE capability
7.0x003C.1	100BASE-TX EEE	RW	1	1: Advertise that 100BASE-TX has EEE capability 0: Do not advertise that 100BASETX has EEE capability in
7.0x003C.0	Reserved	RO	0	Value always 0.

8.5.9. EEE Link Partner Ability Register (MMD 7.0x003D)

Table 66. EEE Link Partner Ability Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x003D.15:14	Reserved	RO	2'b 0	Value always 0.
7.0x003D.13:10	Reserved	RO	4'b 0	Value always 0.
7.0x003D.9	Reserved	RO	0	Value always 0.
7.0x003D.8:7	Reserved	RO	2'b 0	Value always 0.
7.0x003D.6	10GBASE-KR EEE	RO	0	1: Link partner is advertising EEE capability for 10GBASE-KR 0: Link partner is not advertising EEE capability for 10GBASE-KR
7.0x003D.5	10GBASE-KX4 EEE	RO	0	1: Link partner is advertising EEE capability for 10GBASE-KX4 0: Link partner is not advertising EEE capability for 10GBASE-KX4
7.0x003D.4	1000BASE-KX EEE	RO	0	1: Link partner is advertising EEE capability for 1000BASE-KX 0: Link partner is not advertising EEE capability for 1000BASE-KX
7.0x003D.3	10GBASE-T EEE	RO	0	1: Link partner is advertising EEE capability for 10GBASE-T 0: Link partner is not advertising EEE capability for 10GBASE-T
7.0x003D.2	1000BASE-T EEE	RO	0	1: Link partner is advertising EEE capability for 1000BASE-T 0: Link partner is not advertising EEE capability for 1000BASE-T
7.0x003D.1	100BASE-TX EEE	RO	0	1: Link partner is advertising EEE capability for 100BASE-TX 0: Link partner is not advertising EEE capability for 100BASE-TX
7.0x003D.0	Reserved	RO	0	Value always 0.

8.5.10. EEE Advertisement 2 Register (MMD 7.0x003E)

Table 67. EEE Advertisement 2 Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x003E.15:2	Reserved	RO	14'b 0	Value always 0.
7.0x003E.1	Reserved	RW	0	Reserved.
7.0x003E.0	2.5GBASE-T EEE	RW	0	1: Advertise that the 2.5GBASE-T has EEE capability 0: Do not advertise that the 2.5GBASE-T has EEE capability

8.5.11. EEE Link Partner Ability 2 Register (MMD 7.0x003F)

Table 68. EEE Link Partner Ability 2 Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x003F.15:2	Reserved	RO	14'b 0	Value always 0.
7.0x003F.1	5GBASE-T EEE	RO	0	1: Link partner is advertising that the 5GBASE-T has EEE capability 0: Link partner is not advertising that the 5GBASE-T has EEE capability
7.0x003F.0	2.5GBASE-T EEE	RO	0	1: Link partner is advertising that the 2.5GBASE-T has EEE capability 0: Link partner is not advertising that the 2.5GBASE-T has EEE capability

8.5.12. Multi-GBASE-TBASE-T AN Control 2 Register (MMD 7.0x0040)

Table 69. Multi-GBASE-TBASE-T AN Control 2 Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0040.15:4	Reserved	RO	12'b 0	Value always 0.
7.0x0040.3	2.5GBASE-T THP Bypass Request	RW	1	1: Local device requests link partner to initially reset THP during fast retrain 0: Local device requests link partner not to initially reset THP during fast retrain
7.0x0040.2	Reserved	RW	1	Reserved.
7.0x0040.1:0	Reserved	RO	2'b 0	Value always 0.

8.5.13. Multi-GBASE-TBASE-T AN Status 2 Register (MMD 7.0x0041)

Table 70. Multi-GBASE-TBASE-T AN Status 2 Register Bit Definitions

Bit	Name	Type	Default	Description
7.0x0041.15:4	Reserved	RO	12'b 0	Value always 0.
7.0x0041.3	2.5GBASE-T Link Partner THP Bypass Request	RO	0	1: Link partner requests local device to initially reset THP during fast retrain 0: Link partner requests local device not to initially reset THP during fast retrain
7.0x0041.2	Reserved	RO	0	Reserved.
7.0x0041.1:0	Reserved	RO	2'b 0	Value always 0.

8.6. SERDES Registers Mapping and Definitions

Table 71. SERDES Registers Mapping and Definitions

Register Address	Register Name	Subclause
30.0x697A	SERDES OPTION	-
30.0x6A04	SERDES Control 1 Register	-
30.0x7580	SERDES Control 3 Register	-
30.0x7581	SERDES Control 4 Register	-
30.0x7582	SERDES Control 5 Register	-
30.0x7587	SERDES Control 6 Register	-
30.0x758B	SERDES Control 7 Register	-
30.0x758C	SERDES Control 8 Register	-
30.0x758D	SERDES Control 9 Register	-
Otherwise	Reserved	Reserved

8.6.1. SERDES OPTION 1 Register (MMD 30.0x697A)

Table 72. SERDES Control 1 Register Bit Definitions

Bit	Name	RW	Default	Description
30.0x697A.15	Link down option	RW	0	0: Link down 1: Set Link ok and sds_mode to related mode
30.0x697A.14:6	Reserved	RW	-	Reserved.
30.0x697A.5:0	SDS option mode	RW	0x03	Serdes option mode. 0:2500Base-X+SGMII 1:HiSGMII+SGMII 2:2500Base-X 3:HiSGMII Otherwise: Reserved.

8.6.2. SERDES Control 1 Register (MMD 30.0x6A04)

Table 73. SERDES Control 1 Register Bit Definitions

Bit	Name	RW	Default	Description
30.0x6A04.15:11	Reserved	RO	10'b0	Value always 0.
30.0x6A04.10:8	MDIO select	RW	3'b110	3'b100: SERDES control is selected as SGMII mode 3'b101: SERDES control is selected as HiSGMII/ 2500BASE-X mode
30.0x6A04.7:0	Reserved	RO	0x03	Value always 0.

8.6.3. SERDES Control 3 Register (MMD 30.0x7580)

Table 74. SERDES Control 3 Register Bit Definitions

Bit	Name	RW	Default	Description
30.0x7580.15	SERDES PHY Mode	RW	1	0: MAC-side SERDES 1: PHY-side SERDES
30.0x7580.14:7	Reserved	RO	8'b0	Value always 0.
30.0x7580.6	SERDES Isolation	RW	0	1: Activate isolation cell to isolate analog SERDES signal 0: Normal analog SERDES signal transfer
30.0x7580.5	SERDES Force Link Down	RW	0	1: Force SERDES link down 0: Normal SERDES operation
30.0x7580.4:0	SERDES Mode	RW	5'b 01101	SERDES Speed Setting. 5'b00010: SGMII 5'b10010: HiSGMII 5'b10110: 2500BASE-X 5'b11111: SERDES off Otherwise: Reserved.

8.6.4. SERDES Control 4 Register (MMD 30.0x7581)

Table 75. SERDES Control 4 Register Bit Definitions

Bit	Name	RW	Default	Description
30.0x7581.15:5	Reserved	RO	11'b 0	Value always 0.
30.0x7581.4	SERDES Clock Enable	RW	0	1: SERDES clock enable 0: SERDES clock disable *Follow the SERDES application note to set this bit. Misuse of this bit may lead to SERDES malfunction.*
30.0x7581.3	Reserved	RO	0	Value always 0.
30.0x7581.2	Mac TxRx Idle	RW	0	1: SERDES PCS goes into deep power saving mode 0: SERDES PCS is in normal operation mode
30.0x7581.1	SERDES Rx Disable	RW	0	1: Force to close SERDES RX 0: SERDES RX is in normal operation
30.0x7581.0	SERDES Tx Disable	RW	0	1: Force to close SERDES TX 0: SERDES TX is in normal operation

8.6.5. SERDES Control 5 Register (MMD 30.0x7582)

Table 76. SERDES Control 5 Register (Ethernet Link Status) Bit Definitions

Bit	Name	RW	Default	Description
30.0x7582.15	Reserved	RO	0	Value always 0.
30.0x7582.14	EEE Ability	RW	0	1: Both local and link-partner Ethernet PHY have EEE capability of current speed 0: At least one of local or link-partner does not advertise EEE capability in current link

<table>
<tr><th>Bit</th><th>Name</th><th>RW</th><th>Default</th><th>Description</th></tr>
<tr><td>30.0x7582.13:12</td><td>Port Speed_h</td><td>RW</td><td>2’b0</td><td>Ethernet speed setting bit 13:12.
<table>
<tr><th>13:12</th><th>1:0</th><th>Speed Enabled</th></tr>
<tr><td rowspan="3">00</td><td>00</td><td>10M</td></tr>
<tr><td>01</td><td>100M</td></tr>
<tr><td>10</td><td>1000M</td></tr>
<tr><td>01</td><td>11</td><td>2.5G Lite</td></tr>
<tr><td>01</td><td>01</td><td>2.5G</td></tr>
</table>
Other combinations are reserved.</td></tr>
<tr><td>30.0x7582.11</td><td>Enable 1000M EEE</td><td>RW</td><td>0</td><td>1: Ethernet PHY has 1000M EEE ability
0: Ethernet PHY has no 1000M EEE ability</td></tr>
<tr><td>30.0x7582.10</td><td>Enable 100M EEE</td><td>RW</td><td>0</td><td>1: Ethernet PHY has 100M EEE ability
0: Ethernet PHY has no 100M EEE ability1</td></tr>
<tr><td>30.0x7582.9</td><td>Auto-Negotiation fault</td><td>RW</td><td>0</td><td>1: A fault occurred during Auto-Negotiation
0: No fault occurred during Auto-Negotiation</td></tr>
<tr><td>30.0x7582.8</td><td>Master mode</td><td>RW</td><td>0</td><td>1: Master mode, only valid when in 2.5G/ Giga mode
0: Slave mode, only valid when in 2.5G/ Giga mode</td></tr>
<tr><td>30.0x7582.7</td><td>Auto-Negotiation enable</td><td>RW</td><td>0</td><td>1: Ethernet PHY enable Auto-Negotiation
0: Ethernet PHY disable Auto-Negotiation</td></tr>
<tr><td>30.0x7582.6</td><td>Tx flow control enable</td><td>RW</td><td>0</td><td>1: Tx flow control enable
0: Tx flow control disable</td></tr>
<tr><td>30.0x7582.5</td><td>Rx flow control enable</td><td>RW</td><td>0</td><td>1: Rx flow control enable
0: Rx flow control disable</td></tr>
<tr><td>30.0x7582.4</td><td>Ethernet Link OK</td><td>RW</td><td>0</td><td>1: real-time link status: link up
0: real-time link status: link down</td></tr>
<tr><td>30.0x7582.3</td><td>Reserved</td><td>RO</td><td>0</td><td>Value always 0.</td></tr>
<tr><td>30.0x7582.2</td><td>Full duplex</td><td>RW</td><td>0</td><td>1: Current link is full duplex, only valid when in 100M/ 10M mode
0: Current link is half duplex, only valid when in 100M/ 10M mode</td></tr>
<tr><td>30.0x7582.1:0</td><td>Port Speed_l</td><td>RW</td><td>2’b0</td><td>Ethernet speed setting bit 1:0.
<table>
<tr><th>13:12</th><th>1:0</th><th>Speed Enabled</th></tr>
<tr><td rowspan="3">00</td><td>00</td><td>10M</td></tr>
<tr><td>01</td><td>100M</td></tr>
<tr><td>10</td><td>1000M</td></tr>
<tr><td>01</td><td>11</td><td>2.5G Lite</td></tr>
<tr><td>01</td><td>01</td><td>2.5G</td></tr>
</table>
Other combinations are reserved.</td></tr>
</table>

8.6.6. SERDES Control 6 Register (MMD 30. 0x7587)

Table 77. SERDES Control 6 Register Bit Definitions

Bit	Name	RW	Default	Description
30.0x7587.15:3	Reserved	RO	13'b 0	Value always 0.
30.0x7587.2	SERDES Reg Setting Lock	RW	0	1: Restore analog SERDES register default value when doing a SERDES reset 0: Keep SERDES register value even after SERDES reset
30.0x7587.1:0	Reserved	RO	2'b 0	Value always 0.

8.6.7. SERDES Control 7 Register (MMD 30.0x758B)

Table 78. SERDES Control 7 Register Bit Definitions

Bit	Name	RW	Default	Description
30.0x758B.15:3	Reserved	RO	13'b 0	Value always 0.
30.0x758B.2	SERDES Reg Reset	RW	1	1: Keep SERDES register current value 0: Reset SERDES register
30.0x758B.1	Reserved	RO	0	Value always 0.
30.0x758B.0	SERDES ResetB	RW	0	1: Keep SERDES circuit current status 0: Reset SERDES circuit

8.6.8. SERDES Control 8 Register (MMD 30.0x758C)

Table 79. SERDES Control 8 Register Bit Definitions

Bit	Name	RW	Default	Description
30.0x758C.15:1	Reserved	RO	15'b 0	Value always 0.
30.0x758C.0	SERDES Signal Detect	RO	0	1: SERDES detect signal 2: SERDES does not detect signal

8.6.9. SERDES Control 9 Register (MMD 30.0x758D)

Table 80. SERDES Control 9 Register Bit Definitions

Bit	Name	RW	Default	Description
30.0x758D.15:4	Reserved	RO	0x1	Value always 0.
30.0x758D.3	SERDES Link Change	WC	0	1: When SERDES links up 0: When SERDES does not link
30.0x758D.2	SERDES All Channel OK	RO	0	SERDES channel total link status. 1: All SERDES channel link OK 0: Otherwise
30.0x758D.1	SERDES Link OK	RO	0	SERDES channel link status. 1: SERDES channel link OK 0: SERDES channel link not OK
30.0x758D.0	Reserved	RO	0	Value always 0.

8.7. PHY Control Registers Mapping and Definitions

Table 81. PHY Control Registers Mapping and Definitions

Register Address	Register Name	Subclause
31.0xA400	FEDCR	-
31.0xA402	FESR	-
31.0xA40C	ANER	-
31.0xA40E	ANNPTR	-
31.0xA410	ANNPRR	-
31.0xA412	GBCR	-
31.0xA414	GANLPAR	-
31.0xA43A	INER	-
31.0xA430	PHYCR1	-
31.0xA432	PHYCR2	-
31.0xA434	PHYSR	-
31.0xA468	PHYSCR	-
31.0xA4D2	INER	-
31.0xA4D4	INSR	-
31.0xA5B4	FSS	-
31.0xA5EA	SANAR1	-
31.0xA6D8	SANAR2	-
31.0xA5F6	LPSANAR1	-
31.0xA6D2	LPSANAR2	-
31.0xA654	NANRR	-
31.0xB48C	TSRR	-
31.0xB54C	TSSR	-
31.0xD030	LCR1	-
31.0xD032	LCR2	-
31.0xD034	LCR3	-
31.0xD036	LCR4	-
31.0xD040	LCR6	-
31.0xD044	LCR7	-
31.0xD046	LCR8	-
31.0xD05C	INTBCR	-
31.0xE400	PTP_CTL	-
31.0xE402	PTP_INER	-
31.0xE404	PTP_INSR	-
31.0xE406	SYNCE_CTL	-
31.0xE408	PTP_GEN_CFG	-
31.0xE410	PTP_CLK_CFG	-
31.0xE412	PTP_CFG_NS_LO	-
31.0xE414	PTP_CFG_NS_HI	-
31.0xE416	PTP_CFG_S_LO	-
31.0xE418	PTP_CFG_S_MI	-
31.0xE41A	PTP_CFG_S_HI	-

Register Address	Register Name	Subclause
31.0xE420	PTP_TAI_CFG	-
31.0xE424	PTP_TAI_STA	-
31.0xE426	PTP_TAI_TS_NS_LO	-
31.0xE428	PTP_TAI_TS_NS_HI	-
31.0xE42A	PTP_TAI_TS_S_LO	-
31.0xE42C	PTP_TAI_TS_S_HI	-
31.0xE430	PTP_TRX_TS_STA	-
31.0xE432	PTP_TAI_TRIG_CFG	-
31.0xE434	PTP_TAI_TRIG_CFG	-
31.0xE436	PTP_TAI_TRIG_CFG	-
31.0xE438	PTP_TAI_TRIG_CFG	-
31.0xE440	PTP_TRX_TS_INFO	-
31.0xE442	PTP_TRX_TS_SH	-
31.0xE444	PTP_TRX_TS_SID	-
31.0xE446	PTP_TRX_TS_NS_LO	-
31.0xE448	PTP_TRX_TS_NS_HI	-
31.0xE44A	PTP_TRX_TS_S_LO	-
31.0xE44C	PTP_TRX_TS_S_MI	-
31.0xE44E	PTP_TRX_TS_S_HI	-
31.0xE450	SyncE_Lock_CFG	-
31.0xE500	PTP_CTL	-
Otherwise	Reserved	Reserved

8.7.1. FEDCR (Fast Ethernet Duplex Control Register, MMD 31.0xA400)

Table 82. Fast Ethernet Duplex Control Register Advertisement Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xA400.15:9	Reserved	RW	0x8	Reserved.
31.0xA400.8	Duplex	RW	1'b 0	1: Full duplex 0: Half duplex This bit is only valid when local or link partner apply force mode to establish link @ 100Base-Tx or 10BASE-Te. If both sides apply Auto-Negotiation to establish link, then Auto-Negotiation capability advertisement will override this bit.
31.0xA400.7:0	Reserved	RW	0x40	Reserved.

8.7.2. FESR (Fast Ethernet Status Register, MMD 31.0xA402)

Table 83. Fast Ethernet Status Register Advertisement Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xA402.15	100Base-T4	RO	1'b 0	100Base-T4 Capability. The RTL8221B(I)-VB/RTL8221B(I)-VM series does not support 100Base-T4 mode. This bit should always be 0.
31.0xA402.14	100Base-TX (full)	RO	1'b 1	100Base-TX Full Duplex Capability. 1: Device is able to perform 100Base-TX in full duplex mode 0: Device is not able to perform 100Base-TX in full duplex mode
31.0xA402.13	100Base-TX (half)	RO	1'b 1	100Base-TX Half Duplex Capability. 1: Device is able to perform 100Base-TX in half duplex mode 0: Device is not able to perform 100Base-TX in half duplex mode
31.0xA402.12	10BASE-Te (full)	RO	1'b 1	10BASE-Te Full Duplex Capability. 1: Device is able to perform 10BASE-Te in full duplex mode 0: Device is not able to perform 10BASE-Te in full duplex mode
31.0xA402.11	10BASE-Te (half)	RO	1'b 1	10BASE-Te Half Duplex Capability. 1: Device is able to perform 10BASE-Te in half duplex mode 0: Device is not able to perform 10BASE-Te in half duplex mode
31.0xA402.10	10BASE-Te2 (full)	RO	1'b 0	10BASE-Te2 Full Duplex Capability. The RTL8221B(I)-VB/RTL8221B(I)-VM series do not support 10BASE-Te2 mode and this bit should always be 0.
31.0xA402.9	10BASE-Te2 (half)	RO	1'b 0	10BASE-Te2 Half Duplex Capability. The RTL8221B(I)-VB/RTL8221B(I)-VM series do not support 10BASE-Te2 mode. This bit should always be 0.
31.0xA402.8	1000Base-T Extended Status	RO	1	1000Base-T Extended Status Register. 1: Extended status information 0: No extended status information
31.0xA402.7	Uni-directional ability	RO	1	Uni-Directional Ability. 1: PHY able to transmit without linkok 0: PHY not able to transmit without linkok
31.0xA402.6	Preamble Suppression	RO	0	Preamble Suppression Capability. 1: PHY will accept mdc/mdio frames with preamble suppressed 0: PHY will not accept mdc/mdio frames with preamble suppressed
31.0xA402.5	Auto-Negotiation Complete	RO	0	Auto-Negotiation Complete. 1:Auto-Negotiation process complete 0: Auto-Negotiation process not complete

Bit	Name	Type	Default	Description
31.0xA402.4	Remote Fault	RC,LH	0	Remove Fault. 1: Remote fault condition detected (cleared on read or by reset) 0: No remote fault condition detected
31.0xA402.3	Auto-Negotiation Ability	RO	1	Auto Configured Link. 1:Device is able to perform Auto-Negotiation 0: Device is not able to perform Auto-Negotiation
31.0xA402.2	Link Status	RO	0	Link Status. 1: Linked 0: Not Linked This register indicates whether the link was lost since the last read. For the current link status, either read this register this register twice or read 31.0xA434.2 link (real time).
31.0xA402.1	Jabber Detect	RC,LH	0	Jabber Detect. 1:Jabber condition detected 0:No Jabber occurred
31.0xA402.0	Extended Capability	RO	1	1:Exrended register capabilities, always 1

8.7.3. ANER (Auto-Negotiation Expansion Register, MMD 31.0xA40C)

Table 84. Auto-Negotiation Expansion Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xA40C.15:7	Reserved	RO	0x000	Reserved.
31.0xA40C.6	RX NP location ability	RO	1	Received next page storage location ability. 1: Received next page storage location is specified by MMD 31.0xA40C. 5 0: Received next page storage location is not specified by MMD 31.0xA40C. 5
31.0xA40C.5	RX NP location	RO	1	Received next page storage location. 1: Link partner next pages are stored in MMD 31.0xA410 0: Reserved
31.0xA40C.4	Parallel Detection Fault	RC, LH	0	1: A fault has been detected via the Parallel Detection function 0: A fault has not been detected via the Parallel Detection function
31.0xA40C.3	Link Partner Next Page Able	RO	0	1: Link Partner supports Next Page exchange 0: Link Partner does not support Next Page exchange
31.0xA40C.2	Local Next Page Able	RO	1	1: Local Device is able to send Next Page Always 1
31.0xA40C.1	Page Received	RC, LH	0	1: A New Page (new LCW) has been received 0: A New Page has not been received
31.0xA40C.0	Link Partner Auto-Negotiation capable	RO	0	1: Link Partner supports Auto-Negotiation 0: Link Partner does not support Auto-Negotiation

Note: MMD 31.0xA40C is not valid until the Auto-Negotiation complete bit MMD 7.0x0001.5 indicates completed.

8.7.4. ANNPTR (Auto-Negotiation Next Page Transmit Register, MMD 31.0xA40E)

Table 85. Auto-Negotiation Next Page Transmit Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xA40E.15	Next Page	RW	0	Next Page Indication. 0: No more next pages to send 1: More next pages to send Transmit Code Word Bit 15.
31.0xA40E.14	Reserved	RO	0	Transmit Code Word Bit 14.
31.0xA40E.13	Message Page	RW	1	Message Page. 0: Unformatted Page 1: Message Page Transmit Code Word Bit 13.
31.0xA40E.12	Acknowledge 2	RW	0	Acknowledge2. 0: Local device has no ability to comply with the message received 1: Local device has the ability to comply with the message received Transmit Code Word Bit 12.
31.0xA40E.11	Toggle	RO	0	Toggle Bit. Transmit Code Word Bit 11.
31.0xA40E.10:0	Message/Unformatted Field	RW	0x001	Content of Message/Unformatted Page. Transmit Code Word Bit 10:0.

8.7.5. ANNPRR (Auto-Negotiation Next Page Receive Register, MMD 31.0xA410)

Table 86. Auto-Negotiation Next Page Receive Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xA410.15	Next Page	RO	0	Received Link Code Word Bit 15.
31.0xA410.14	Acknowledge	RO	0	Received Link Code Word Bit 14.
31.0xA410.13	Message Page	RO	0	Received Link Code Word Bit 13.
31.0xA410.12	Acknowledge 2	RO	0	Received Link Code Word Bit 12.
31.0xA410.11	Toggle	RO	0	Received Link Code Word Bit 11.
31.0xA410.10:0	Message/Unformatted Field	RO	0x00	Received Link Code Word Bit 10:0.

Note: Register MMD31.0xA410 is not valid until the Auto-Negotiation complete bit MMD 7.0x0001.5 indicates completed.

8.7.6. GBCR (1000Base-T Control Register, MMD 31.0xA412)

Table 87. 1000Base-T Control Register Advertisement Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xA412.15:13	Giga Test Mode	RW	3'b 0	Giga Test Mode Select. 3'b000: Normal Mode 3'b001: Test Mode 1 – Transmit waveform test 3'b010: Test Mode 2 – Transmit jitter test in master mode 3'b011: Test Mode 3 – Transmit jitter test in slave mode 3'b100: Test Mode 4 – Transmit distortion test Otherwise reserved.
31.0xA412.12:10	Reserved	RO	3'b 0	Value always 0.
31.0xA412.9	1000BASE-T Full Duplex Capability	RW	0	1: Advertise PHY as 1000BASE-T full duplex capable 0: Do not advertise PHY as 1000BASE-T full duplex capable
31.0xA412.8:0	Reserved	RO	9'b 0	Value always 0.

8.7.7. GANLPAR (Giga Auto-Negotiation Link Partner Ability Register, MMD 31.0xA414)

Table 88. Giga Auto-Negotiation Link Partner Ability Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xA414.15:12	Reserved	RO	4'b 0	Value always 0.
31.0xA414.11	Link Partner 1000BASE-T Full Duplex ability	RO	0	1: Link partner is able to operate as 1000BASE-T full duplex 0: Link partner is not able to operate as 1000BASE-T full duplex
31.0xA414.10	Link Partner 1000BASE-T Half Duplex ability	RO	0	1: Link partner is able to operate as 1000BASE-T half duplex 0: Link partner is not able to operate as 1000BASE-T half duplex
31.0xA414.9:0	Reserved	RO	10'b 0	Value always 0.

8.7.8. PHYCR1 (PHY Specific Control Register 1, MMD 31. 0xA430)

Table 89. PHY Specific Control Register 1 Bit Definitions

Bit	Name	Type	Default	Description
31.0xA430.15:14	Reserved	RO	0	Value always 0.
31.0xA430.13	PHYAD_0 Enable	RW	1	1: A broadcast from MAC (A command with PHY address=0) is valid. MDC/MDIO will respond to this command
31.0xA430.12	ALDPS XTAL-OFF Enable	RW	0	1: Enable XTAL off when in ALDPS mode (valid when Bit 31.0xA430.2=1)
31.0xA430.11:10	Reserved	RO	0	Value always 0.
31.0xA430.9	MDI Mode Manual Configuration Enable	RW	0	1: Enable Manual Configuration of MDI mode
31.0xA430.8	MDI Mode	RW	1	Set the MDI/MDIX mode. 1: MDI 0: MDIX This bit will take effect only when Bit 31.0xA430.9=1.
31.0xA430.7:5	Reserved	RO	0x4	Value always 0.
31.0xA430.4	Preamble Check Enable	RW	1	1: Check preamble when receiving an MDC/MDIO command
31.0xA430.3	Jabber Detection Enable	RW	1	1: Enable Jabber Detection
31.0xA430.2	ALDPS Enable	RW	0	1: Enable Link Down Power Saving Mode
31.0xA430.1:0	Reserved	RO	2'b3	Value always 0.

Note: The method to disable auto-crossover and force MDI or MDIX mode is as follows:
Step 1: Set Bit 9=1 (Manual Configuration of MDI mode) and set Bit 8=1 (MDI) or 0 (MDIX).
Step 2: Perform a PHY reset.

8.7.9. PHYCR2 (PHY Specific Control Register 2, MMD 31. 0xA432)

Table 90. PHY Specific Control Register 2 Bit Definitions

Bit	Name	Type	Default	Description
31.0xA432.15:14	Reserved	RW	0	Reserved.
31.0xA432.13:12	CLK125_src	RW	0	CLK125 pin output source. 2'b00: 125MHz free run clock generated from internal PLL. 2'b01: UTP Recoverd Receive clock for Sync Ethernet use. (Valid if in UTP mode) 2'b10: Fiber Recoverd Receive clock for Sync Ethernet use. (Valid if in FIBER mode) 2'b11: PTP clock output (Valid if ptp_en = 1) / Spread Spectrum clock (valid if clk125_ssc_en)
31.0xA432.11	CLK125_freq	RW	1	CLK125 pin clock output frequency select. 0: 25 MHz 1: 125 MHz
31.0xA432.10:9	Reserved	RW	0	Reserved.
31.0xA432.8	aldps_phymode_en	RW	0	1: Enable phymode ALDPS

Bit	Name	Type	Default	Description
31.0xA432.7	clk125_ssc_en	RW	0	1: Enable spread spectrum clock of clk125
31.0xA432.6	ctap_short_en	RW	1	1: Short 4-channel transformer common mode to central tap
31.0xA432.5	eee_phymode_en	RW	0	1: Enable phymode eee
31.0xA432.4	eee10_en	RW	1	1: Enable 10M eee capaibility
31.0xA432.3	ssc_en	RW	0	1: Enable spread spectrum clock
31.0xA432.2	eeep_tx_phymode_en	RW	0	1: Enable phymode eeep
31.0xA432.1	Reserved	RO	-	Reserved.
31.0xA432.0	en_clk125	RW	1	1: Enable clk125

Note 1: The method to enable PHY mode EEE is as follows:
Step 1: Set Bit 5=1
Step 2: Perform a NWAY re-start

Note 2: The method to enable 10M PHY mode EEEP is as follows:
Step 1: Set Bit 2=1
Step 2: Set 31.0x0C842.2=1
Step 3: Perform a NWAY re-start

8.7.10. PHYSR (PHY Specific Status Register, MMD 31.0xA434)

Table 91. PHY Specific Status Register Bit Definitions

<table>
<tr><th>Bit</th><th>Name</th><th>Type</th><th>Default</th><th>Description</th></tr>
<tr><td>31.0xA434.15</td><td>Reserved</td><td>RO</td><td>0</td><td>Value always 0.</td></tr>
<tr><td>31.0xA434.14</td><td>ALDPS State</td><td>RO</td><td>0</td><td>Link Down Power Saving Mode.
1: Reflects local device entered Link Down Power Saving Mode, i.e., cable not plugged in (reflected after 3 sec)
0: With cable plugged in</td></tr>
<tr><td>31.0xA434.13</td><td>MDI Plug</td><td>RO</td><td>0</td><td>MDI Status.
1: Plugged
0: Unplugged</td></tr>
<tr><td>31.0xA434.12</td><td>Auto-Negotiation Enable</td><td>RO</td><td>1</td><td>Auto-Negotiation Status.
1: Enable
0: Disable</td></tr>
<tr><td>31.0xA434.11</td><td>Master Mode</td><td>RO</td><td>0</td><td>Device is in Master/Slave Mode.
1: Master mode
0: Slave mode</td></tr>
<tr><td>31.0xA434.10:9</td><td>Speed_h</td><td>RO</td><td>2’b 11</td><td>Ethernet Speed.
<table>
<tr><th>Speed_h</th><th>Speed_l</th><th>Speed Enabled</th></tr>
<tr><td rowspan="3">00</td><td>00</td><td>10M</td></tr>
<tr><td>01</td><td>100M</td></tr>
<tr><td>10</td><td>1000M</td></tr>
<tr><td>01</td><td>11</td><td>2.5G Lite</td></tr>
<tr><td>01</td><td>01</td><td>2.5G</td></tr>
</table>
Other combinations are reserved.</td></tr>
</table>

Bit	Name	Type	Default	Description
31.0xA434.8	EEE capability	RO	0	1: Both local and link-partner have EEE capability for current link speed
31.0xA434.7	Rx Flow Enable	RO	0	Rx Flow Control. 1: Enable 0: Disable
31.0xA434.6	Tx Flow Enable	RO	0	Tx Flow Control. 1: Enable 0: Disable
31.0xA434.5:4	Speed_1	RO	2'b0	Link Speed. 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps
31.0xA434.3	Duplex	RO	0	Full/Half Duplex Mode. 1: Full duplex 0: Half duplex
31.0xA434.2	Link (Real Time)	RO	0	Real Time Link Status. 1: Link OK 0: Link not OK
31.0xA434.1	MDI Crossover Status	RO	1	MDI/MDI Crossover Status. 1: MDI 0: MDI Crossover
31.0xA434.0	Jabber (Real Time)	RO	0	Real Time Jabber Indication. 1: Jabber Indication 0: No Jabber Indication

Note 1: Bit 11 is valid only when in 2.5G, Giga, or 2.5G Lite mode.
Note 2: Bit 8 asserts at 10M speed when local device is EEE capable.

8.7.11. PHYSCR (PHY Special Config Register, MMD 31.0xA468)

Table 92. PHY Special Config Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xA468.15:2	Reserved	RO	0	Value always 0.
31.0xA468.1	PHY Special Config Done	RW	1	1: Write 1 to indicate the special PHY parameter configuration has been done
31.0xA468.0	Reserved	RO	1	Value always 1.

8.7.12. INER (Interrupt Enable Register, MMD 31.0xA4D2)

Table 93. Interrupt Enable Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xA4D2.15:11	Reserved	RW	00000	Reserved.
31.0xA4D2.10	Jabber Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the jabber interrupt event in the INTB pin.
31.0xA4D2.9	ALDPS State Change Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the ALDPS state change interrupt event in the INTB pin.
31.0xA4D2.8	Reserved	RW	0	Reserved.
31.0xA4D2.7	PME (Power Management Event of WOL)	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the PME interrupt event in the INTB pin.
31.0xA4D2.6	Reserved	RW	0	Reserved.
31.0xA4D2.5	PHY Register Accessible Interrupt	RW	1	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the PHY register access interrupt event in the INTB pin.
31.0xA4D2.4	Link Status Change Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the link status change interrupt event in the INTB pin.
31.0xA4D2.3	Auto-Negotiation Completed Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the auto-negotiation completed interrupt event in the INTB pin.
31.0xA4D2.2	Page Received Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the page received interrupt event in the INTB pin.
31.0xA4D2.1	Reserved	RW	0	Reserved.
31.0xA4D2.0	Auto-Negotiation Error Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the auto-negotiation error interrupt event in the INTB pin.

8.7.13. INSR (Interrupt Status Register, MMD 31.0xA4D4)

Table 94. Interrupt Status Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xA4D4.15:11	Reserved	RO	5'b 0	Value always 0.
31.0xA4D4.10	Jabber	RO, RC	0	1: Jabber detected 0: No jabber detected
31.0xA4D4.9	ALDPS State Change	RO, RC	0	1: ALDPS state changed 0: ALDPS state not changed
31.0xA4D4.8	Reserved	RO	0	Value always 0.
31.0xA4D4.7	PME (Power Management Event of WOL)	RO, RC	0	1: WOL event occurred 0: WOL event did not occur
31.0xA4D4.6	Reserved	RO	0	Value always 0.
31.0xA4D4.5	PHY Register Accessible	RO, RC	0	1: Can access PHY Register through MDC/MDIO 0: Cannot access PHY Register through MDC/MDIO
31.0xA4D4.4	Link Status Change	RO, RC	0	1: Link status changed 0: Link status not changed
31.0xA4D4.3	Auto-Negotiation Completed	RO, RC	0	1: Auto-Negotiation completed 0: Auto-Negotiation not completed
31.0xA4D4.2	Page Received	RO, RC	0	1: Page (a new LCW) received 0: Page not received
31.0xA4D4.1	Reserved	RO	0	Value always 0.
31.0xA4D4.0	Auto-Negotiation Error	RO, RC	0	1: Auto-Negotiation Error 0: No Auto-Negotiation Error

Note 1: Both WOL and PMEB features support only 1000Base-T, 100Base-TX, and 10BASE-Te. 2.5GBase-T is not supported.

8.7.14. FSS (Force Speed Status Register, MMD 31.0xA5B4)

Table 95. Force Speed Status Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xA5B4.15:4	Reserved	RO	0x800	Value always 0x800.
31.0xA5B4.3:0	Force Speed Status	RO	4'b0010	4'b0100: 2.5GBASE-T; 4'b 0011: 1000BASE-T; 4'b 0010: 100BASE-TX; 4'b 0001: 10BASE-Te 4'b 0000: Force Speed Resolution Error These bits are only valid when MMD7.0x0000.12 is turned off. The force speed is set according to MMD1.0x0000.13 & 1.0x0000.6:2.

8.7.15. SANAR1 (Special Auto-Negotiation Advertisement Register 1, MMD 31.0xA5EA)

Table 96. Special Auto-Negotiation Advertisement Register 1 Bit Definitions

Bit	Name	Type	Default	Description
31.0xA5EA.15	Bypass 2.5GNBASE-T ability in Auto-Negotiation	RW	0	1: Do not advertise PHY as 2.5GNBASE-T capable 0: Advertise PHY as 2.5GNBASE-T capable
31.0xA5EA.14	Bypass CISCO Negotiated Fast Retrain ability in Auto-Negotiation	RW	1	1: Do not advertise PHY as CISCO Negotiated Fast Retrain capable 0: Advertise PHY as CISCO Negotiated Fast Retrain capable
31.0xA5EA.13:1	Reserved	RO	0x1300	Value always 0x1300.
31.0xA5EA.0	2.5GBASE-T Lite ability	RW	0	1: Do not advertise PHY as 2.5GBASE-T Lite capable 0: Advertise PHY as 2.5GNBASE-T Lite capable This is a Realtek proprietary feature. Only available when link partner also has the same ability.

8.7.16. SANAR2 (Special Auto-Negotiation Advertisement Register 2, MMD 31.0xA6D8)

Table 97. Special Auto-Negotiation Advertisement Register 2 Bit Definitions

Bit	Name	Type	Default	Description
31.0xA6D8.15:5	Reserved	RO	11'b 0	Value always 0.
31.0xA6D8.4	2.5GBASE-T Lite EEE ability	RW	0	1: Advertise PHY as 2.5GBASE-T Lite EEE capable 0: Do not advertise PHY as 2.5GBASE-T Lite EEE capable
31.0xA6D8.3	2.5GBASE-T Lite Fast Retrain Bypass THP	RW	1	1: Do not apply THP during 2.5GBASE-T Lite Fast Retrain 0: Apply THP during 2.5GBASE-T Lite Fast Retrain
31.0xA6D8.2:1	Reserved	RO	2'b 10	Value always 2'b 10.
31.0xA6D8.0	2.5GBASE-T Lite Fast Retrain ability	RW	0	1: Advertise PHY as 2.5GBASE-T Lite fast retrain capable 0: Do not advertise PHY as 2.5GBASE-T Lite fast retrain capable

8.7.17. LPSANAR1 (Link Partner Special Auto-Negotiation Advertisement Register 1, MMD 31.0xA5F6)

Table 98. Link Partner Special Auto-Negotiation Advertisement Register 1 Bit Definitions

Bit	Name	Type	Default	Description
31.0xA5F6.15:1	Reserved	RO	15'b 0	Value always 0.
31.0xA5F6.0	Link Partner 2.5GBASE-T Lite capability	RW	0	1: Link partner is capable of 2.5GBASE-T Lite 0: Link partner is not capable of 2.5GBASE-T Lite

8.7.18. LPSANAR2 (Link Partner Special Auto-Negotiation Advertisement Register 2, MMD 31.0xA6D2)

Table 99. Link Partner Special Auto-Negotiation Advertisement Register 2 Bit Definitions

Bit	Name	Type	Default	Description
31.0xA6D2.15:11	Reserved	RO	5'b 0	Value always 0.
31.0xA6D2.10	Link Partner 2.5GBASE-T Lite Fast Retrain capability	RW	0	1: Link partner is capable of 2.5GBASE-T Lite Fast Retrain 0: Link partner is not capable of 2.5GBASE-T Lite Fast Retrain
31.0xA6D2.9	Reserved	RO	0	Value always 0.
31.0xA6D2.8	Link Partner 2.5GBASE-T Lite Fast Retrain bypass THP	RW	0	1: Link partner request do not apply THP during 2.5GBASE-T Lite Fast Retrain 0: Link partner request apply THP during 2.5GBASE-T Lite Fast Retrain
31.0xA6D2.7	Reserved	RO	0	Value always 0.
31.0xA6D2.6	Link Partner 2.5GBASE-T Lite EEE capability	RW	0	1: Link partner is capable of 2.5GBASE-T Lite EEE 0: Link partner is not capable of 2.5GBASE-T Lite EEE
31.0xA6D2.5:0	Reserved	RO	6'b 0	Value always 0.

8.7.19. NANRR (NBASE-T Auto-Negotiation Result Register, MMD 31.0xA654)

Table 100. NBASE-T Auto-Negotiation Result Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xA654.15:14	Reserved	RO	2'b 0	Value always 0.
31.0xA654.13	HCD is NBASE-T	RO	0	1: Current HCD is 2.5GNBASE-T 0: Current HCD is NOT 2.5GNBASE-T
31.0xA654.12	CISCO Negotiated Fast Retrain Ability	RO	0	1: Advertise PHY as CISCO Negotiated Fast Retrain capable 0: Do not advertise CISCO negotiated fast retrain capable
31.0xA654.11:0	Reserved	RO	12'b 0	Value always 0.

8.7.20. TSRR (Thermal Sensor Result Register, MMD 31.0xBD84)

Table 101. Thermal Sensor Result Register Bit Definitions-1

Bit	Name	Type	Default	Description
31.0xBD84.15:10	Reserved	RO	0	-
31.0xBD84.9:0	ts_out_sync	RO	0	Thermal sensor temperature(s10.1f). The current temperature in degree ℃ could be derived by: If ts_out_sync<=2^9, Tj=ts_out_sync/2 If ts_out_sync>2^9, Tj= -((2^9)-(ts_out_sync-2^9))/2 *Note: ts_out_sync should be translated into decimal.*

8.7.21. TSSR (Thermal Sensor Setting Register, MMD 31.0xB54C)

Table 102. Thermal Sensor Setting Register Bit Definitions-2

Bit	Name	Type	Default	Description
31.0xB54C.15:6	rg_overtemp_thrd	RW	10'h0bb	Over-Temperature Threshold. Set over-temperature detection threshold.
31.0xB54C.:5	Reserved	RO	0	Value always 0.
31.0xB54C.4	rg_en_intr_at_overtemp	RW	1	Over-Temperature Interrupt. 1: PHY generate an interrupt when over-temperature is detected 0: PHY DO NOT generate an interrupt when over-temperature is detected
31.0xB54C.3	rg_en_dwnspd_at_overtemp	RW	1	Over-Temperature Speed Mask. 1: Enable PHY mask 2.5G/ 2.5G lite capability when over-temperature is detected 0: Disable PHY mask 2.5G/ 2.5G lite capability when over-temperature is detected
31.0xB54C.2:1	Internal use	RW	2'b0	-
31.0xB54C.0	Reserved	RW	1	-

Note: The settings in this register are valid only when 31.0xB54C.0 = 1. When link Ethernet at 2.5G speed.

8.7.22. LCR1 (LED Control Register 1, MMD 31.0xD030)

Table 103. LED Control Register 1 Bit Definitions

Bit	Name	Type	Default	Description
31.0xD030.11:8	Led2 Speed	RO	4'b1100	LED2 Link Indication: Ethernet links. 4'b0000: 10M 4'b0001: 100M 4'b0010: 1000M 4'b0101: 2.5G 4'b0111: 2.5G lite Otherwise: Reserved.
31.0xD030.7:4	Led1 Speed	RO	4'b1100	LED1 Link Indication: Ethernet Links. 4'b0000: 10M 4'b0001: 100M 4'b0010: 1000M 4'b0101: 2.5G 4'b0111: 2.5G Lite Otherwise: Reserved.
31.0xD030.3:0	Led0 Speed	RO	4' b1100	LED0 Link Indication: Ethernet links. 4'b0000: 10M 4'b0001: 100M 4'b0010: 1000M 4'b0101: 2.5G 4'b0111: 2.5G lite Otherwise: Reserved.

8.7.23. LCR2 (LED Control Register 2, MMD 31.0xD032)

Table 104. LED Control Register 2 Bit Definitions

Bit	Name	Type	Default	Description
31.0xD032.15:8	Reserved	RO	8'b 0	Value always 0.
31.0xD032.7	LED0 2.5G lite	RW	0	1: LED0 Ethernet link select at 2.5G lite
31.0xD032.6	Reserved	RO	0	Value always 0.
31.0xD032.5	LED0 2.5G	RW	0	1: LED0 Ethernet link select at 2.5G
31.0xD032.4:3	Reserved	RO	2'b 0	Value always 0.
31.0xD032.2	LED0 1G	RW	0	1: LED0 Ethernet link select at 1G
31.0xD032.1	LED0 100M	RW	0	1: LED0 Ethernet link select at 100M
31.0xD032.0	LED0 10M	RW	1	1: LED0 Ethernet link select at 10M

8.7.24. LCR3 (LED Control Register 3, MMD 31.0xD034)

Table 105. LED Control Register 3 Bit Definitions

Bit	Name	Type	Default	Description
31.0xD034.15:8	Reserved	RO	8'b 0	Value always 0.
31.0xD034.7	LED1 2.5G lite	RW	0	1: LED1 Ethernet link select at 2.5G lite
31.0xD034.6	Reserved	RO	0	Value always 0.
31.0xD034.5	LED1 2.5G	RW	0	1: LED1 Ethernet link select at 2.5G
31.0xD034.4:3	Reserved	RO	2'b 0	Value always 0.
31.0xD034.2	LED1 1G	RW	0	1: LED1 Ethernet link select at 1G
31.0xD034.1	LED1 100M	RW	1	1: LED1 Ethernet link select at 100M
31.0xD034.0	LED1 10M	RW	0	1: LED1 Ethernet link select at 10M

8.7.25. LCR4 (LED Control Register 4, MMD 31. 0xD036)

Table 106. LED Control Register 4 Bit Definitions

Bit	Name	Type	Default	Description
31.0xD036.15:8	Reserved	RO	8'b 0	Value always 0.
31.0xD036.7	LED2 2.5G lite	RW	0	1: LED2 Ethernet link select at 2.5G lite
31.0xD036.6	Reserved	RO	0	Value always 0.
31.0xD036.5	LED2 2.5G	RW	0	1: LED2 Ethernet link select at 2.5G
31.0xD036.4:3	Reserved	RO	2'b 0	Value always 0.
31.0xD036.2	LED2 1G	RW	1	1: LED2 Ethernet link select at 1G
31.0xD036.1	LED2 100M	RW	0	1: LED2 Ethernet link select at 100M
31.0xD036.0	LED2 10M	RW	0	1: LED2 Ethernet link select at 10M

8.7.26. LCR6 (LED Control Register 6, MMD 31.D040)

Table 107. LED Control Register 6 Bit Definitions

Bit	Name	Type	Default	Description
31.0xD040.15	LED Blink Speed Up	RW	0	1: Speed up blink frequency 0: Normal blink frequency (as user specified)
31.0xD040.14	LED Reset	RW	0	1: Reset LED reg 0: Keep current LED reg setting
31.0xD040.13:12	EEE LPI On Time	RW	2'b 11	LED LPI ON Time. 00: 20ms 01: 100ms 10: 200ms 11: 400ms
31.0xD040.11:10	LED Blink Duty	RW	2'b 10	LED blink duty cycle. 2'b00: 12.5% 2'b01: 25% 2'b10: 50% 2'b11: 75%

Bit	Name	Type	Default	Description
31.0xD040.9:8	LED Blink Freq	RW	2'b 01	LED blink frequency control. 2'b00: 20ms 2'b01: 40ms 2'b10: 60ms 2'b11: 40ms (default)
31.0xD040.7:6	Reserved	RO	2'b 0	Value always 0.
31.0xD040.5	LED modeA/modeB Sel	RW	0	1: LED blink pattern mode B 0: LED blink pattern mode A
31.0xD040.4	LED Enable 10M LPI	RW	1	1: Fake LPI when links at 10M 0: No fake LPI when links at 10M
31.0xD040.2	LED2 act	RW	1	1: LED2 active blink 0: LED2 blinks only when link speed matches LED setting
31.0xD040.1	LED1 act	RW	1	1: LED1 active blink 0: LED1 blinks only when link speed matches LED setting
31.0xD040.0	LED0 act	RW	1	1: LED0 active blink 0: LED0 blinks only when link speed matches LED setting

8.7.27. LCR 7 (LED Control Register 7 2, MMD 31.0D044)

Table 108. LED Control Register 7 Bit Definitions

Bit	Name	Type	Default	Description
31.0xD044.15:8	Reserved	RO	8'b 0	Value always 0.
31.0xD044.6	LED2 Enable	RW	1	LED2 Enable. 1: Enable
31.0xD044.5	LED1 Enable	RW	1	LED1 Enable. 1: Enable
31.0xD044.4	LED0 Enable	RW	1	LED0 Enable. 1: Enable
31.0xD044.2	LED2 Polar	RW	1	LED2 polarity. 0: Active low 1: Active high
31.0xD044.1	LED1 Polar	RW	1	LED1 polarity. 0: Active low 1: Active high
31.0xD044.0	LED0 Polar	RW	1	LED0 polarity. 0: Active low 1: Active high

8.7.28. LCR 8 (LED Control Register 8, MMD 31.0xD046)

Table 109. LED Control Register 8 Bit Definitions

Bit	Name	Type	Default	Description
31.0xD046.15:4	Reserved	RO	12'b 0	Value always 0.
31.0xD046.2	LED2 Traffic	RO	0	LED2 setting speed has traffic. 1: Traffic 0: Idle
31.0xD046.1	LED1 Traffic	RO	0	LED1 setting speed has traffic. 1: Traffic 0: Idle
31.0xD046.0	LED0 Traffic	RO	0	LED0 setting speed has traffic. 1: Traffic 0: Idle

8.7.29. INTBCR (INTB Pin Control Register, MMD 31.0xD05C)

Table 110. INTB Pin Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xD05C.15:1	Reserved	RO	15'b 0	Value always 0.
31.0xD05C.0	INTB/PMEB Selection	RW	0	Pin 48 of the RTL8221B(I)-VB/RTL8221B(I)-VM functions as: 1: PMEB 0: INTB

8.7.30. PTP_CTL (PTP Control Register, MMD31, Address 0xE400)

Table 111. PTP_CTL Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE400.15:13	RSVD	RO	000	Reserved.
31.0xE400.12	UDP_CHKSUM Update	RW	0	Enable auto-correction of UDP Checksum if One-Step Timestamp Insertion is enabled. Only effective to IPv6/UDP packets. 0: Set 0x0000 to the UDP Checksum field 1: Re-compute the UDP Checksum
31.0xE400.11	P_DRFU_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to PDelaly_Resp_Follow_Up messages.
31.0xE400.10	P_DR_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to PDelay_Resp messages.
31.0xE400.9	DR_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to Delay_Resp messages.
31.0xE400.8	FU_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to Follow_Up messages.
31.0xE400.7	P_DR_1STEP Enable	RW	0	Enable One-Step Timestamp Insertion (t3-t2) to Pdelay_Response messages.
31.0xE400.6	SYNC_1STEP Enable	RW	0	Enable One-Step Timestamp Insertion (t1) to Sync messages.
31.0xE400.5	AVB_802.1AS Support	RW	0	1: AVB 802.1AS standard support
31.0xE400.4	PTPv2_Layer2 Support	RW	0	1: PTPv2 Layer 2 packets support
31.0xE400.3	PTPv2_UDPIPV4 Support	RW	0	1: PTPv2 UDP/IPv4 packets support
31.0xE400.2	PTPv2_UDPIPV6 Support	RW	0	1: PTPv2 UDP/IPv6 packets support
31.0xE400.1	PTPv1 Support	RW	0	1: PTPv1 packets support
31.0xE400.0	PTP_Enable	RW	0	PTP function enable. *Note: Issue a Software Reset (MMD 7.0x0000.15) after setting this bit in order to enable/disable PTP function.*

8.7.31. PTP_INER (PTP Interrupt Enable Register, MMD31, Address 0xE402)

Table 112. PTP_INER Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE402.15:4	RSVD	RO	0x000	Reserved.
31.0xE402.3	Tx Timestamp Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Transmit Timestamp ready interrupt.
31.0xE402.2	Rx Timestamp Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Receive Timestamp ready interrupt.
31.0xE402.1	TrigGen Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Trigger Generate complete interrupt.
31.0xE402.0	EventCap Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Event Capture timestamp ready interrupt.

8.7.32. PTP_INSR (PTP Interrupt Status Register, MMD31, Address 0xE404)

Table 113. PTP_INSR Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE404.15:4	RSVD	RO	0x000	Reserved.
31.0xE404.3	Tx Timestamp Interrupt	RO, RC	0	1: Transmit Timestamp ready interrupt detected
31.0xE404.2	Rx Timestamp Interrupt	RO, RC	0	1: Receive Timestamp ready interrupt detected
31.0xE404.1	TrigGen Interrupt	RO, RC	0	1: Trigger Generate complete interrupt detected
31.0xE404.0	EventCap Interrupt	RO, RC	0	1: Event Capture timestamp ready interrupt detected

8.7.33. SYNCE_CTL (Sync-E Control Register, MMD31, Address 0xE406)

Table 114. SYNCE_CTL Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE406.15:1	RSVD	RO	0	Reserved.
31.0xE406.0	SyncE Enable	RW	0	Sync-E function Enable. *Note: Issue a Software Reset (MMD 7.0x0000.15) after setting this bit in order to enable/disable Sync-E function.*

8.7.34. PTP_GEN_CFG (PTP General Config Control Register, MMD31, Address 0xE408)

Table 115. PTP_GEN_CFG Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE408.15:1	RSVD	RO	0	Reserved.
31.0xE408.0	PTP IBTR CLR Mode	RW	0	1: ptp intr status register is write 1 clear 0: ptp intr status register is read clear

8.7.35. PTP_CLK_CFG (PTP Clock Config Register, MMD31, Address 0xE410)

Table 116. PTP_CLK_CFG Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE410.15:7	RSVD	RO	0	Reserved.
31.0xE410.6:5	ptp_clkin_freq_sel	RW	0	PTP CLKIN Frequency Select. 01: 25MHz 00: 10MHz 10: Reserved 11: Reserved *Note: Issue a Software Reset (MMD 7.0x0000.15) in order to allow the setting to take effect.*
31.0xE410.4	ptp_clkin_en	RW	0	PTP CLKIN function enable. *Note: Issue a Software Reset (MMD 7.0x0000.15) in order to allow the setting to take effect.*
31.0xE410.3:1	ptp_clkadj_mod	RW	0	PTP Clock Adjustment Mode Select. 000: No function 001: Reserved - Issue Direct Read/Write to PTP_Local_Time through PTP_Time_Config registers. 010: Direct Read 011: Direct Write - Issue Step Adjustment to PTP_Local_Time through PTP_Time_Config registers. 100: Increment Step 101: Decrement Step - Issue Rate Adjustment Read/Write to PTP_Rate_Adj_Amt through PTP_Time_Config_ns registers [21:0]. A 2's complement representation should be used if a negative rate adjustment is needed. 110: Rate Read 111: Rate Write
31.0xE410.0	ptp_clkadj_mod_set	RW, SC	0	PTP Clock Adjustment Mode Set. 1: Activate the selected clock adjustment mode as related parameters are properly inserted

8.7.36. PTP_CFG_NS_LO (PTP Time Config Nano-Sec Low Register, MMD31, Address 0xE412)

Table 117. PTP_CFG_NS_LO Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE412.15:0	PTP_Time_Config_ns[15:0]	RW	0x0000	Time configuration nano-sec field [15:0] / Rate adjustment multiplier field [15:0]. A 2's complement representation should be used if a negative rate adjustment is needed.

8.7.37. PTP_CFG_NS_HI (PTP Time Config Nano-Sec High Register, MMD31, Address 0xE414)

Table 118. PTP_CFG_NS_HI Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE414.15:14	RSVD	RO	00	Reserved.
31.0xE414.13:0	PTP_Time_Config_ns[29:16]	RW	0	Time configuration nano-sec field_ns [29:16]/ Rate adjustment multiplier field [21:16]; [21]: Rate adjustment Sign bit (1: higher rate; 0: lower rate); [29:22]: No effect when write, Reflect Sign Extension result when read. A 2's complement representation should be used if a negative rate adjustment is needed.

8.7.38. PTP_CFG_S_LO (PTP Time Config Sec Low Register, MMD31, Address 0xE416)

Table 119. PTP_CFG_S_LO Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE416.15:0	PTP_Time_Config_s[15:0]	RW	0x0000	Time configuration sec field [15:0].

8.7.39. PTP_CFG_S_MI (PTP Time Config Sec Mid Register, MMD31, Address 0xE418)

Table 120. PTP_CFG_S_MI Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE418.15:0	PTP_Time_Config_s[31:16]	RW	0x0000	Time configuration sec field [31:16].

8.7.40. PTP_ CFG_S_HI (PTP Time Config Sec High Register, MMD31, Address 0xE41A)

Table 121. PTP_S_HI Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE41A.15:0	PTP_Time_Config_s[47:32]	RW	0x0000	Time configuration sec field [47:32].

8.7.41. PTP_TAI_CFG (PTP Application I/F Config Register, MMD31, Address 0xE420)

Table 122. PTP_TAI_CFG Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE420.15:9	RSVD	RO	0000000	Reserved.
31.0xE420.8	trig_mod_sel	RW	0	Trigger Generate mode select. Trigger(s) start at time specified in TAI_TS_RW registers. Valid if tai_func_sel = 01. 0: Single pulse. The pulse width can be set by pulse_amt fields 1: Periodic pulses. The pulse period and duty cycle can be set by pulse_amt (31.0xE432.8:0 and 31.0xE434.15:0) and pulse_with (31.0xE436.0 and 31.0xE438.15:0) fields, see section 8.7.48~8.7.51
31.0xE420.7	trig_iflate	RW	0	Trigger-if-Late Control. Valid if tai_func_sel (31.0xE420.2:1) = 01. 1: Allow an immediate Trigger when setting a time value that is earlier than the current time
31.0xE420.6	evnt_rf_det	RW	0	Event Capture rising/falling edge detect selection. Valid if tai_func_sel (31.0xE420.2:1) = 10. 0: Detection of a rising edge 1: Detection of a falling edge SW should take care of the high/low level of GPIO1588 with this setting.
31.0xE420.5	evnt_overwr_en	RW	1	Event Capture timestamp overwrite enable. Valid if tai_func_sel = 10. 0: Keep the old value 1: Cause the event timestamp to be overwritten if a new event is detected at the specific GPIO1588 though the upper layer has not yet read the old event timestamp
31.0xE420.4:3	tai_gpio_num	RW	00	The GPIO1588 number that is going to be armed.
31.0xE420.2:1	tai_func_sel	RW	00	PTP Application Interface function select of selected GPIO1588. 00: Disable function 01: Trigger Generate 10: Event Capture 11: Trigger start time/Event timestamp read (according to current GPIO1588 settings)
31.0xE420.0	tai_cfg_set	RW, SC	0	PTP Application Interface configuration set. Setting this bit will issue a TAI Configuration ‘Set’ to the selected GPIO1588 via tai_gpio_num.

8.7.42. PTP_TAI_STA (PTP TAI Status Register, MMD31, Address 0xE424)

Table 123. PTP_TAI_STA Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE424.15	tai_gpio15880_func	RO	0	Indicate GPIO15880's function. 0: Trigger Generate 1: Event Capture
31.0xE424.14	tai_gpio15880_en	RO	0	GPIO15880 function is enabled.
31.0xE424.13	update tai_gpio15880_notify	RO/COR	0	Indicate if a Trigger is generated or Event Detected at GPIO15880.
31.0xE424.12	tai_gpio15880_err	RO/COR	0	Indicate that Trigger-start-time is earlier than the current time / an old Event timestamp value is kept at GPIO15880.
31.0xE424.11	tai_gpio15881_func	RO	0	Indicate GPIO15881's Function. 0: Trigger Generate 1: Event Capture
31.0xE424.10	tai_gpio15881_en	RO	0	GPIO15881 function is enabled.
31.0xE424.9	tai_gpio15881_notify	RO	0	Indicate if a Trigger is generated or Event detected at GPIO15881.
31.0xE424.8	tai_gpio15881_err	RO	0	Indicate that Trigger-start-time is earlier than the current time / an old Event timestamp value is kept at GPIO15881.
31.0xE424.7	tai_gpio15882_func	RO/COR	0	Indicate GPIO 2's Function. Valid if TAI_GPIO15882_En = 1. 0: Trigger Generate 1: Event Capture
31.0xE424.6	tai_gpio15882_en	RO/COR	0	GPIO15882 function is enabled.
31.0xE424.5	tai_gpio15882_notify	RO	0	Indicate if a Trigger is generated or Event detected at GPIO15882.
31.0xE424.4	tai_gpio15882_err	RO	0	Indicate that Trigger-start-time is earlier than the current time / an old Event timestamp value is kept at GPIO15882.
31.0xE424.3	tai_gpio15883_func	RO/COR	0	Indicate GPIO15883's Function. Valid if TAI_GPIO15883_En = 1. 0: Trigger Generate 1: Event Capture
31.0xE424.2	tai_gpio15883_en	RO/COR	0	GPIO15883 function is enabled.
31.0xE424.1	tai_gpio15883_notify	RO/COR	0	Indicate if a Trigger is generated or Event Detected at GPIO15883.
31.0xE424.0	tai_gpio15883_err	RO/COR	0	Indicate that Trigger-start-time is earlier than the current time / an old Event timestamp value is kept at GPIO15883.

8.7.43. PTP_TAI_TS_NS_LO (PTP TAI Timestamp Nano-Sec Low Register, MMD31, Address 0xE426)

Table 124. PTP_TAI_TS_NS_LO Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE426.15:0	TAI_TS_ns[15:0]	RW	0x0000	TAI timestamp Read/Write interface nanosec field [15:0].

8.7.44. PTP_TAI_TS_NS_HI (PTP TAI Timestamp Nano-Sec High Register, MMD31, Address 0xE428)

Table 125. PTP_TAI_TS_NS_HI Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE428.15:14	RSVD	RO	00	Reserved.
31.0xE428.13:0	TAI_TS_ns[29:16]	RW	0	TAI timestamp Read/Write interface nanosec field [29:16].

8.7.45. PTP_TAI_TS_S_LO (PTP TAI Timestamp Sec Low Register, MMD31, Address 0xE42A)

Table 126. PTP_S_LO Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE42A.15:0	TAI_TS_s[15:0]	RW	0x0000	TAI timestamp Read/Write interface sec field [15:0].

8.7.46. PTP_TAI_TS_S_HI (PTP TAI Timestamp Sec High Register, MMD31, Address 0xE42C)

Table 127. PTP_S_MI Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE42C.15:0	TAI_TS_s[31:16]	RW	0x0000	TAI timestamp Read/Write interface sec field [31:16].

8.7.47. PTP_TRX_TS_STA (PTP TXRX TS Status Register, MMD31, Address 0xE430)

Table 128. PTP_TXRX_TS_STA Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE430.15	txts_sync_rdy	RO	0	Sync message Transmit timestamp ready.
31.0xE430.14	txts_dlyreq_rdy	RO	0	Delay Request Transmit timestamp ready.
31.0xE430.13	txts_pdlyreq_rdy	RO	0	PDelay Request Transmit timestamp ready.
31.0xE430.12	txts_pdlyrsp_rdy	RO	0	PDelay Response Transmit timestamp ready.
31.0xE430.11	rxts_sync_rdy	RO	0	Sync message Receive timestamp ready.
31.0xE430.10	rxts_dlyreq_rdy	RO	0	Delay Request Receive timestamp ready.
31.0xE430.9	rxts_pdlyreq_rdy	RO	0	PDelay Request Receive timestamp ready.
31.0xE430.8	rxts_pdlyrsp_rdy	RO	0	PDelay Response Receive timestamp ready.
31.0xE430.7:5	RSVD	RO	0	Reserved.
31.0xE430.4	trxts_overwr_en	RW	1	Transmit/Receive timestamp overwrite enable. When a new PTP packet comes which needs to be timestamped, HW will: 0: Keep the old timestamp value 1: Overwrite the old timestamp value if the older one has not been read by the upper layer
31.0xE430.3:2	trxts_msgtype_sel	RW	00	Message Type of Transmit/Receive timestamp select. 00: Sync 01: Delay Request 10: PDelay Request 11: PDelay Response
31.0xE430.1	trxts_sel	RW	0	Transmit/Receive timestamp read select. 0: Tx 1: Rx
31.0xE430.0	trxts_rd	RW/SC	0	Transmit/Receive timestamp read enable. Issue a read from Tx/Rx timestamp.

8.7.48. PTP_TAI_TRIG_CFG (PTP TAI Trigger Config Register, MMD31, Address 0xE432)

Table 129. PTP_TAI_TRIG_CFG Control Register Bit Definitions (0xE432)

Bit	Name	Type	Default	Description
31.0xE432.15:9	RSVD	RO	0x00	Reserved.
31.0xE432.8:0	pulse_amt_24_16	RW	0x00	Period of periodic pulses in unit of 40 ns base. Period = pulse_amt * 40 ns. Note the pulse_amt must not be set less than 2.

8.7.49. PTP_TAI_TRIG_CFG (PTP TAI Trigger Config Register, MMD31, Address 0xE434)

Table 130. PTP_TAI_TRIG_CFG Control Register Bit Definitions (0xE434)

Bit	Name	Type	Default	Description
31.0xE434.15:0	pulse_amt_15_0	RW	0x0002	Period of periodic pulses in unit of 40 ns base. Period = pulse_amt * 40 ns.

8.7.50. PTP_TAI_TRIG_CFG (PTP TAI Trigger Config Register, MMD31, Address 0xE436)

Table 131. PTP_TAI_TRIG_CFG Control Register Bit Definitions (0xE436)

Bit	Name	Type	Default	Description
31.0xE436.15:12	single_trig_pulse_width	RW	0001	Pulse width of single trigger pulse in unit of 40 ns base. Note the single_trig_pulse_width must be set greater than 0.
31.0xE436.11:9	RSVD	RO	000	Reserved.
31.0xE436.8:0	prd_trig_pulse_width_24_16	RW	0x00	Pulse width of periodic trigger pulse in unit of 40 ns base. Note the range of prd_trig_pulse_width must be in 1 ~ (pulse_amount - 1).

8.7.51. PTP_TAI_TRIG_CFG (PTP TAI Trigger Config Register, MMD31, Address 0xE438)

Table 132. PTP_TAI_TRIG_CFG Control Register Bit Definitions (0xE438)

Bit	Name	Type	Default	Description
31.0xE438.15:0	prd_trig_pulse_width_15_0	RW	0x0001	Pulse width of periodic trigger pulse in unit of 40 ns base. Note the range of prd_trig_pulse_width must be in 1 ~ (pulse_amount - 1).

8.7.52. PTP_TRX_TS_INFO (PTP TxRx Timestamp Info Register, MMD31, Address 0xE440)

Table 133. PTP_TRX_TS_INFO Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE440.15:12	trxts_transspec	RO	0000	Transmit/Receive timestamp Transport Specific field.
31.0xE440.11:8	trxts_msgtype	RO	0000	Transmit/Receive timestamp Message Type field.
31.0xE440.7:4	RSVD	RO	0000	Reserved.
31.0xE440.3:0	trxts_ptpver	RO	0000	Transmit/Receive timestamp PTP Version field.

8.7.53. PTP_TRX_TS_SH (PTP TxRx Timestamp Source Hash Register, MMD31, Address 0xE442)

Table 134. PTP_TRX_TS_SH Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE442.15:0	trxts_srchash	RO	0x0000	Transmit/Receive timestamp Source Port ID Hash field.

8.7.54. PTP_TRX_TS_SID (PTP TxRx Timestamp Seq ID Register, MMD31, Address 0xE444)

Table 135. PTP_TRX_TS_SID Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE444.15:0	trxts_seqid	RO	0x0000	Transmit/Receive timestamp Sequence ID field.

8.7.55. PTP_ TRX_TS_NS_LO (PTP TxRx Timestamp Nano-Sec Low Register, MMD31, Address 0xE446)

Table 136. PTP_ TRX_TS NS_LO Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE446.15:0	TXRX_TS_ns[15:0]	RO	0x0000	Transmit/Receive timestamp nanosec field [15:0].

8.7.56. PTP_ TRX_TS_NS_HI (PTP TxRx Timestamp Nano-Sec High Register, MMD31, Address 0xE448)

Table 137. PTP_ TRX_TS NS_HI Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE448.15:14	RSVD	RO	00	Reserved.
31.0xE448.13:0	TXRX_TS_ns[29:16]	RW	0	Transmit/Receive timestamp nanosec field [29:16].

8.7.57. PTP_ TRX_TS_S_LO (PTP TxRx Timestamp Sec Low Register, MMD31, Address 0xE44A)

Table 138. PTP_ TRX_TS S_LO Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE44A.15:0	TXRX_TS_s[15:0]	RW	0x0000	Transmit/Receive timestamp sec field [15:0].

8.7.58. PTP_ TRX_TS_ S_MI (PTP TxRx Timestamp Sec Mid Register, MMD31, Address 0xE44C)

Table 139. PTP_ TRX_TS S_MID Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE44C.15:0	TXRX_TS_s[31:16]	RW	0x0000	Transmit/Receive timestamp sec field [31:16].

8.7.59. PTP_ TRX_TS_S_HI (PTP TxRx Timestamp Sec High Register, MMD31, Address 0xE44E)

Table 140. PTP_ TRX_TS S_LO Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE44E.15:0	TXRX_TS_s[47:32]	RW	0x0000	Transmit/Receive timestamp sec field [47:32].

8.7.60. SyncE_Lock_CFG (SyncE Lock Config Control Register, MMD31, Address 0xE450)

Table 141. SyncE_Lock_CFG Control Register Bit Definitions

Bit	Name	Type	Default	Description
31.0xE450.15:4	RSVD	RO	0x000	Reserved.
31.0xE450.3:0	rg_synce_lock_en	RW	0100	SyncE lock enable.

8.7.61. PTP_CTL (PTP Control Register, MMD31, Address 0xE500)

Table 142. PTP_CTRL Control Register Bit Definitions (0xE500)

Bit	Name	Type	Default	Description
31.0xE500.15	ptp_clkin_sel	RW	0	PTP CLKIN source select. 0: Clock from GPIO15881 pin 1: Reserved
31.0xE500.14	ptp_clkin_en_internal	RW	0	1'b1: Enable ptp clk input internally
31.0xE500.13:12	ptp_clkin_freq_internal	RW	0	ptp clk input frequency selection internally. 2'b00: 10MHz 2'b01: 25MHz 2'b10: Reserved 2'b11: Reserved
31.0xE500.11	ptp_clk_follow_sys_en	RW	0	1'b1: ptp clock follow sysclk, this will force dll_up_ptp/dll_dn_ptp follow dll_up/dn of sysclk
31.0xE500.10	frc_clk_ext_en	RW	0	1'b1: Force clk_ext enable without deglith
31.0xE500.9	ptp_en_internal	RW	0	1'b1: Enable ptp circuit internally
31.0xE500.8	tr_dll_en	RW	1	1'b1: Enable tr dll_up/dn
31.0xE500.7	tr_dll_swap	RW	0	1'b1: Swap tr dll_up/dn
31.0xE500.6	ptp_dll_swap	RW	0	1'b1: Swap ptp dll_up/dn
31.0xE500.5	ptp_fulldup_en	RW	0	1'b1: Enable ptp when full duplex 1'b0: Enable ptp discard duplex
31.0xE500.4	ptp_no_eee_en	RW	0	1'b1: Enable ptp when no eee cap 1'b0: Enable ptp discard eee cap
31.0xE500.3	ptp_linkok_en	RW	0	1'b1: Enable ptp when linkok 1'b0: Enable ptp discard linkok
31.0xE500.2:0	ptp_rateadj_kf	RW	0	ptp rate adjustment tracking ratio for clock input mode. Ratio = 2^(-19+kf)

8.8. Power Sequence

The power supply of the RTL8221B(I)-VB/RTL8221B(I)-VM series should follow the power sequence below to ensure the internal circuits work properly. If there is any action that involves consecutive ON/OFF toggling of the SWR, the design must make sure the OFF state of both the SWR output reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 50ms. Note that the output DC level should fall in the ± 5% of the target voltage.

To ensure the power sequence control, connect Pin 46 (POW_EXT_SWR) to SWR for RTL8221B(I)-VB/RTL8221B(I)-VM to control 0.95V power-on timing. Under this scenario, the enable time of 0.95V would be well controlled by RTL8221B(I)-VB/VM series. Thus the main objective is to ensure the 3.3V -> 1.8V (if DVDD3318 is connected to 1.8V) power sequence. Care must be taken that if different power modules are used for different power domains; at any time the below relationships of power rail output voltage should be strictly followed:

3.3V power rail > 1.8V power rail

8.9. Power Sequence Parameters

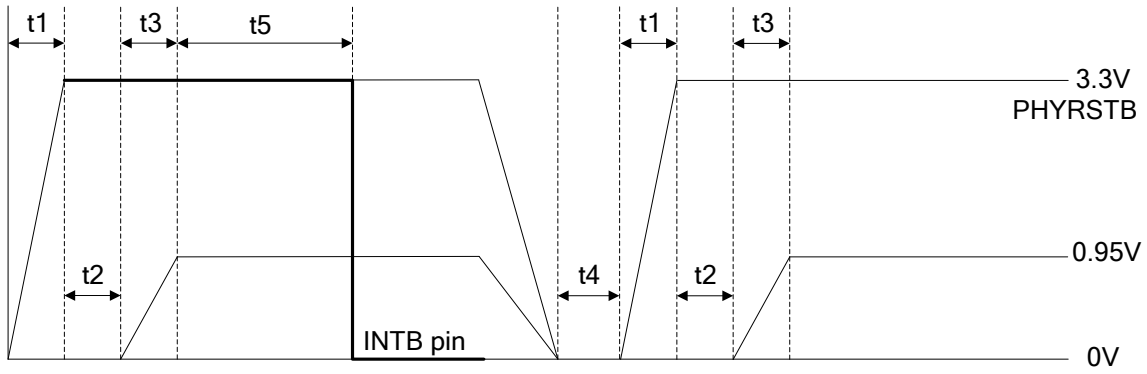


Figure 11. Power Sequence

Table 143. Power Sequence Parameters

Symbol	Description	Min	Typical	Max	Unit
t1	3.3V Rise Time	0.5	-	10	ms
t2	0.95V SWR Enable time	(Note 2)	-	-	ms
t2	0.95V SWR Enable time (bypass POW_EXT_SWR pin)	0	-	-	ms
t3	0.95V Rise	0.5	-	5	ms
t4	On/Off Interval	50	-	-	ms
t5 (note 3)	Core logic ready time	-	-	55	ms

Note 1: The loosest counting of t1 would be the rising time required for the power rail to output from 0V to 90% of target voltage.
Note 2: t2 should be well controlled by the RTL8221B(I)-VB/RTL8221B(I)-VM.
Note 3: The RTL8221B(I)-VB/RTL8221B(I)-VM can be accessed by MDC/MDIO after t5 (without SPI flash).

The output DC level tolerance is ± 5% of the target voltage therefore the loosest counting of t1 would be the rising time required for the power rail to output from 0V to 90% target voltage.

- **0.5ms < Rise Time < 10ms and monotonic ramp:**

No action to take.

- **0.1ms < Rise Time < 0.5 ms and monotonic ramp:**

If the rise time is between 0.1ms~0.5ms and the power supply is in monotonic ramp, the customer MUST ensure that there is at least three times as much margin for inrush current to the RTL8221B(I)-VB/RTL8221B(I)-VM series, so as to be safely under the system's power supply OCP threshold.

For example: Assume customer supply power rise time of the RTL8221B(I)-VB/RTL8221B(I)-VM is 0.374ms. The system power supply OCP is 9A. The inrush current of other devices is 5.64A. The inrush current to the RTL8221B(I)-VB/RTL8221B(I)-VM series must be less than 1.12A; otherwise, an unanticipated system OCP may be triggered. It can be expressed in the following formula: Inrush current to the RTL8221B(I)-VB/RTL8221B(I)-VM < (System power supply OCP - inrush current of other devices) / 3.

- **Rise Time < 0.1 ms or non-monotonic ramp:**

Under this scenario, there is risk of an unanticipated ESD trigger event, which may cause permanent damage. As well as an unanticipated ESD trigger event, the power supply source with rise time < 0.1ms or > 100ms or non-monotonic ramp may possibly cause permanent damage. If there is any action that involves consecutive ON/OFF toggling of the power source, the design must make sure the OFF state of all power domains reaches 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 50ms.

9. Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 144. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
AVDD33, DVDD33	Supply Voltage 3.3V	-0.3	3.63	V
DVDD09, AVDD09, EVDD09	Supply Voltage 0.95V	-0.2	1.05	V
DVDD3318	Input Voltage (3.3V or 1.8V)	-0.3	DVD3318*1.1	V
NA	Storage Temperature	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

9.2. Recommended Operating Conditions

Table 145. Recommended Operating Conditions

Description	Supply Voltage	Minimum	Typical	Maximum	Unit
Supply Voltage	3.3	3.14	3.3	3.46	V
	1.8	1.71	1.8	1.89	V
	0.95	0.92	0.95	0.98	V
Ambient Operating Temperature T_A RTL8221B-VB/RTL8221B-VM	-	0	-	70	°C
Ambient Operating Temperature T_A RTL8221BI-VB/ RTL8221BI-VM	-	-40	-	85	°C
Maximum Junction Temperature	-	-	-	125	°C
Power ripple (note)	DVDD33	-	-	30	mV p-p
	AVDD33	-	-	15	mVp-p
	AVDD09	-	-	15	mVp-p
	DVDD09,EVDD09	-	-	30	mVp-p

Note: In order to achieve maximum performance when using the RTL8221B(I)-VB/RTL8221B(I)-VM, a good power source should have power noise less than 15mV peak-to-peak (using pigtail cable) for analog power domains. If the power rail is supplied by SWR, then the SWR should operate in PWM (or CCM) mode to achieve this target. The switching frequency must be greater than 1Mhz and the noise ripple from the SWR must be kept to a minimum. The switching frequency noise must be under -67dBm (FFT) for analog power domain. The details of power noise measurement including measure points, measure instrument, measurement setup, and measurement criteria are illustrated in the layout guide.

9.3. Electrostatic Discharge Performance

Table 146. Electrostatic Discharge Performance

Test Item	Results
HBM ESD	All Pins: ｜2KV｜
MM ESD	All Pins: ｜100V｜
CDM ESD	All Pins: ｜200V｜
Latch Up	I/O Pin: 100mA Power Pin: 1.5xVDD

9.4. Crystal Requirements

A 25MHz parallel resonant crystal can be used as the reference clock source to replace the 25MHz Oscillator. The crystal must be connected to CKXTAL1 and CKXTAL2 pins. Shunt each crystal lead to ground with a 27pF capacitor.

Table 147. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F_{ref} Tolerance (RTL8221B-VB,VM)	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=0°C~70°C.	-50	-	+50	ppm
F_{ref} Tolerance (RTL8221BI-VB,VM)	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=-40°C~85°C.	-50	-	+50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	70	Ω
V_{ih}_CKXTAL	Crystal Output High Level.	1.4	-	-	V
V_{il}_CKXTAL (Note2)	Crystal Output Low Level.	-	-	0.4	V
Operating Temperature	-	-40	-	85	°C
Package (Note3)	-	-	SMD	-	-

Note 1: Fref Tolerance +/- 50ppm including effects of aging of the first year, external crystal capacitors, and PCB layout.
Note 2: Based on XTAL drive level spec to choose the appropriate resistor on CKXTAL2 pin to meet Vih and Vil requirement.
Note 3: MUST use SMD type crystal for the RTL8221B(I)-VB/RTL8221B(I)-VM.

9.5. Oscillator/External Clock Requirements

Table 148. Oscillator/External Clock Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25	-	MHz
Frequency Tolerance RTL8221B-VB/ RTL8221B-VM	Ta=0°C~70°C	-50	-	50	ppm
Frequency Tolerance RTL8221BI-VB/ RTL8221BI-VM	Ta=-40°C~85°C	-50	-	50	ppm
Duty Cycle	-	40	-	60	%
RMS Jitter [1]	10kHz~20MHz	-	-	2	ps
V_{ih}	-	1.1	-	-	V
V_{il}	-	-	-	0.4	V
Rise Time (10%~90%)	-	-	-	11	ns
Fall Time (10%~90%)	-	-	-	11	ns
Operating Temperature	-	-40	-	85	°C

Note 1: Frequency Tolerance +/- 50ppm including effects of aging of the first year, external crystal capacitors, and PCB layout. The phase noise of 25MHz clock input should be at least that as shown in Figure 12.

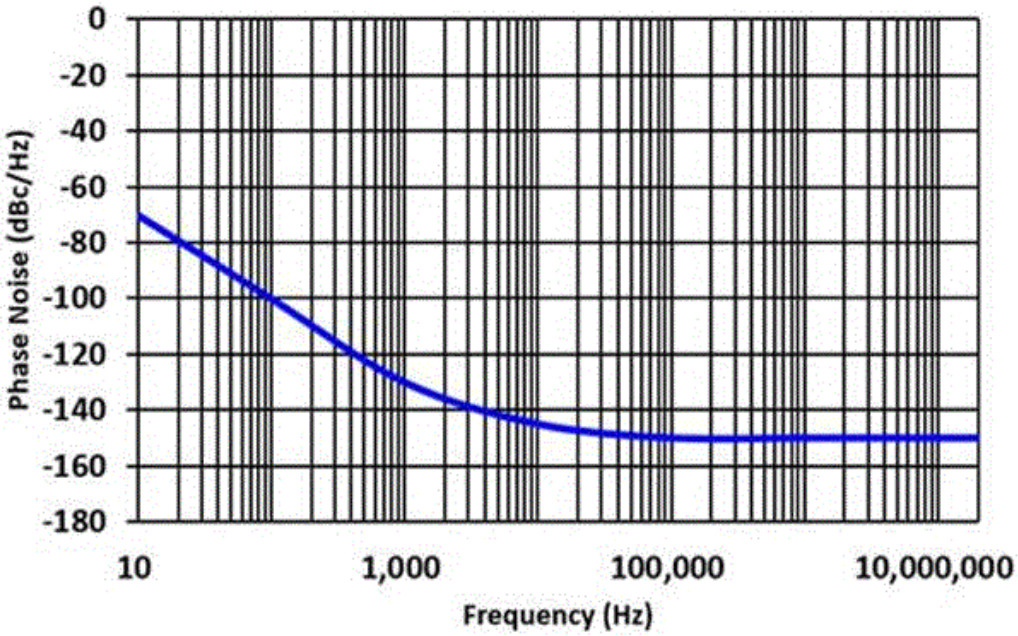


Figure 12. Phase Noise

9.6. DC Characteristics

Table 149. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
DVDD33, AVDD33	3.3V Supply Voltage	-	3.14	3.3	3.46	V
DVDD3318	MDIO, MDC,PHYRSTB, INTB Operation Voltage	DVDD3318 @ 3.3V	3.14	3.3	3.46	V
		DVDD3318 @ 1.8V	1.71	1.8	1.89	
DVDD09, AVDD09, EVDD09	0.95V Supply Voltage	-	0.92	0.95	0.98	V
Voh	Minimum High Level Output Voltage	3.3V domain	2.4	3.3	VDD33 + 0.3	V
		1.8V domain	0.9*VDD18	1.8	VDD18 + 0.3	
Vol	Maximum Low Level Output Voltage	3.3V domain	-0.3	0	0.4	V
		1.8V domain	-0.3		0.1*VDD18	
Vih	Minimum High Level Input Voltage	3.3V domain	2.0	3.3	VDD33+0.3	V
		1.8V domain	0.65*VDD18	1.8	VDD18+0.3	
Vil	Maximum Low Level Input Voltage	3.3V domain	-0.3	0	0.8	V
		1.8V domain	-0.3		0.35*VDD18	
Iin	Input Current	Vin=VDD33 or GND	0	-	0.5	µA
Icc	Average Operating Supply Current (Note 2)	3.3V domain	-	88	100	mA
		0.95V domain	-	364	650	

Note 1: Pins not mentioned above remain at 3.3V.
Note 2: The Maximum Operating Supply Current was measured under the specific conditions of 100 meter Cat5e, +5% of all power rails and Ta = 85℃. Power consumed by all peripheral components is not calculated in the above table. This will help PCB designer have a better understanding on each power rail budget.

9.7. Thermal Characteristics

Table 150. Thermal Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
θ_{JA}	Junction-to-ambient thermal resistance $\theta_{JA} = (T_J - T_A)/P_H$	No air flow	-	19.06	-	°C/W
Ψ_{JT}	Junction-to-top-center thermal characterization parameter $\Psi_{JT} = (T_J - T_T)/P_H$	No air flow	-	0.28	-	°C/W

Note: T_J = junction temperature (°C), T_A = ambient temperature (°C), T_T = temperature on the top-center of the package (°C), P_H = total power dissipation (W).

The preceding thermal characteristics are based on customized PCB information as shown in Table 151.

Table 151. PCB Information

PCB Type	Customized PCB
PCB layers	4
PCB dimensions	119.9 mm X 56 mm
Cu coverage (%)	L1: 61% L2: 85% L3: 83% L4: 80%
External heat sink	No

Ψ_{JT} is better than θ_{JA} and θ_{JC} (Junction-to-case thermal resistance) on the estimation of the junction temperature (T_J). The temperature on the top-center of the package (T_T) is effected by not only the ambient temperature (T_A) but also the PCB conditions. Also, P_H includes the power dissipation from the top, bottom and sides of the package, but θ_{JC} assumes that all the power is dissipated only from the top of the package. Thus, θ_{JC} is appropriate for the package attached with the external heat sink. In an actual environment, Ψ_{JT} brings a closer value to the actual T_J by measuring T_T.

9.8. SERDES Characteristics

9.8.1. HiSGMII and 2500Base-X Differential Transmitter Characteristics

Table 152. HiSGMII and 2500Base-X Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	-	320	-	ps	320ps ± 100ppm
T_X1	Eye Mask	-	-	0.15	UI	CDR BW=3.125G/1667 @1st order
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	150	-	-	mV	-
T_Y2	Eye Mask	-	-	400	mV	-
$V_{TX-OFFSET}$	Output Offset Voltage	600	800	1000	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	700	900	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.7	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.3	UI	$T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.3UI
$T_{TX-RISE}$	Rise Time	0.15	-	-	UI	20% ~ 80%
$T_{TX-FALL}$	Fall Time	0.15	-	-	UI	20% ~ 80%
R_{TX}	Differential Resistance	80	100	120	Ohm	-
C_{TX}	AC Coupling Capacitor	80	100	120	nF	-
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

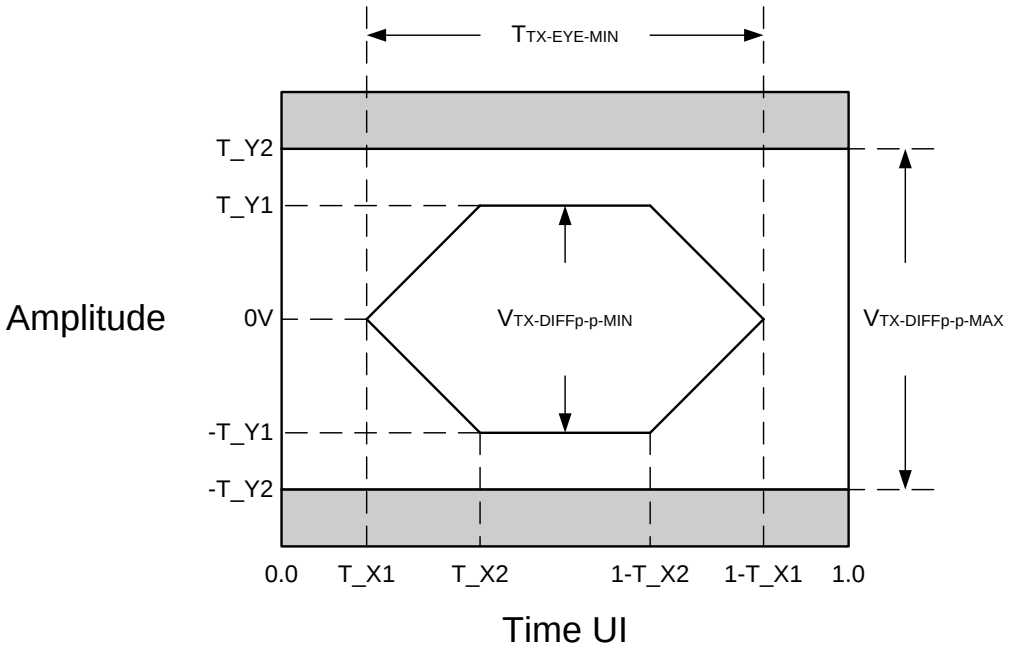


Figure 13. HiSGMII and 2500Base-X Differential Transmitter Eye Diagram

9.8.2. HiSGMII and 2500Base-X Differential Receiver Characteristics

Table 153. HiSGMII and 2500Base-X Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	-	320	-	ps	320ps ± 100ppm
R_X1	Eye Mask	-	-	0.3	UI	-
R_Y1	Eye Mask	100	-	-	mV	-
R_Y2	Eye Mask	-	-	600	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	200	-	1200	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.4	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.6	UI	TRX-JITTER-MAX=1 - TRX-EYE-MIN =0.6UI
R_{RX}	Differential Resistance	80	100	120	ohm	-

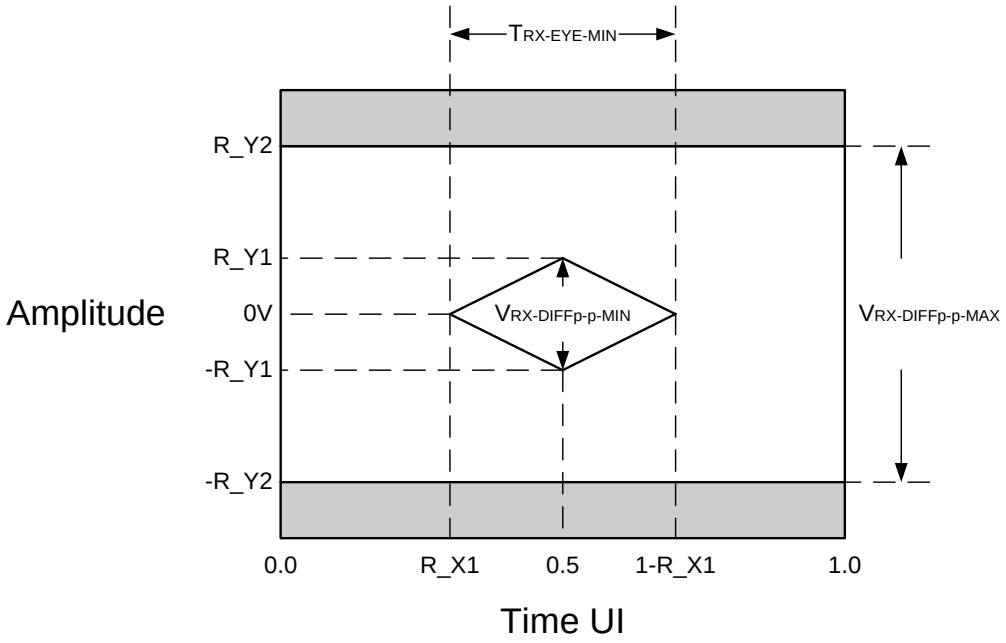


Figure 14. HiSGMII and 2500Base-X Differential Receiver Eye Diagram

9.8.3. SGMII Differential Transmitter Characteristics

Table 154. SGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.76	800	800.24	ps	800ps ± 300ppm
T_X1	Eye Mask	-	-	0.15	UI	CDR BW=1.25G/1667 @1st order
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	300	-	-	mV	-
T_Y2	Eye Mask	-	-	450	mV	-
$V_{TX-OFFSET}$	Output Offset Voltage	600	800	1000	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	600	800	900	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.7	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.3	UI	$T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.3UI
$T_{TX-RISE}$	Rise Time	0.125	-	0.25	UI	20% ~ 80%
$T_{TX-FALL}$	Fall Time	0.125	-	0.25	UI	20% ~ 80%
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling Capacitor	80	100	120	nF	-
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

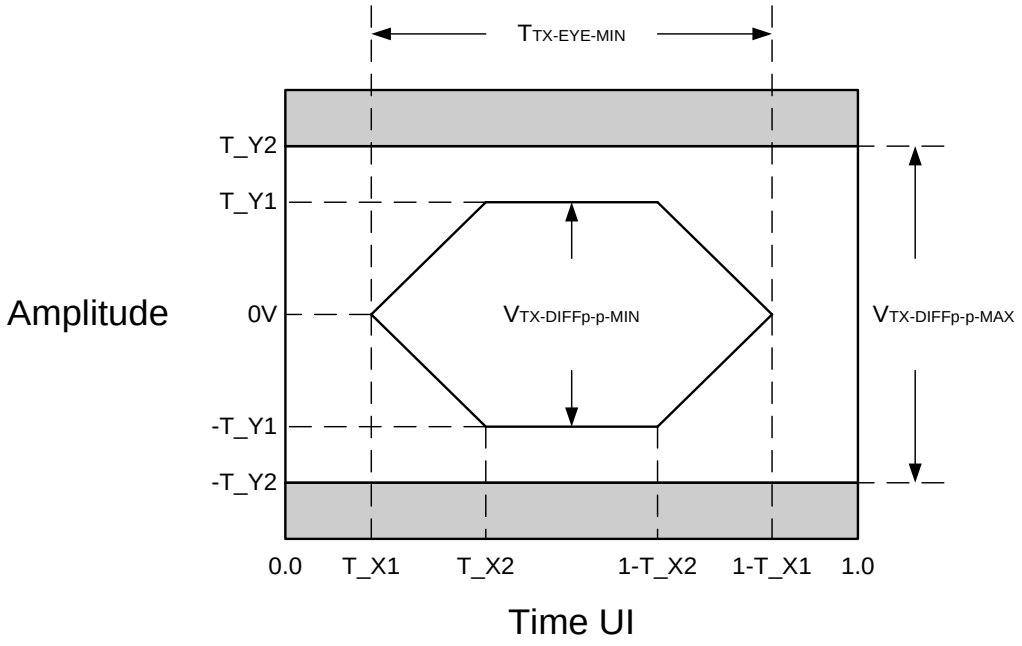


Figure 15. SGMII Differential Transmitter Eye Diagram

9.8.4. SGMII Differential Receiver Characteristics

Table 155. SGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.76	800	800.24	ps	800ps ± 300ppm
R_X1	Eye Mask	-	-	0.3	UI	-
R_Y1	Eye Mask	100	-	-	mV	-
R_Y2	Eye Mask	-	-	1000	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	200	-	2000	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.4	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.6	UI	$T_{RX-JITTER-MAX}$=1 - $T_{RX-EYE-MIN}$ =0.6UI
R_{RX}	Differential Resistance	80	100	120	ohm	-

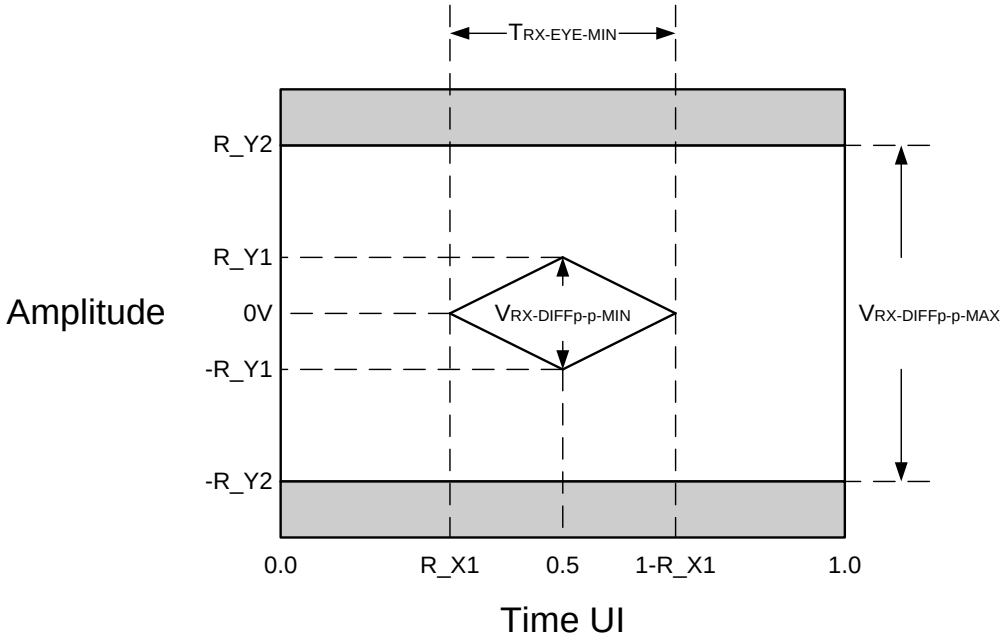


Figure 16. SGMII Differential Receiver Eye Diagram

9.9. AC Characteristics

9.9.1. MDC/MDIO Timing

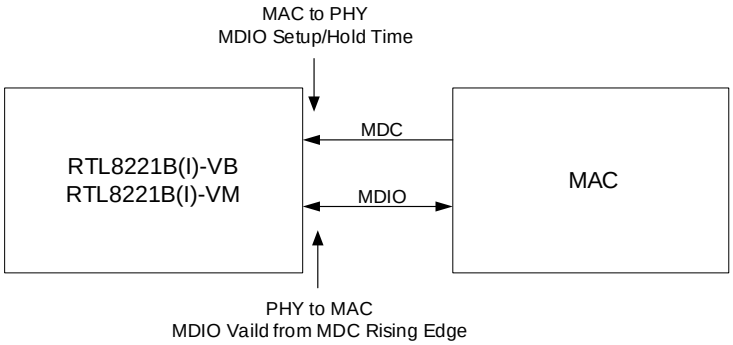


Figure 17. MDC/MDIO Setup, Hold Time, and Valid from MDC Rising Edge Time Definitions

MDC/MDIO Timing – Management Port

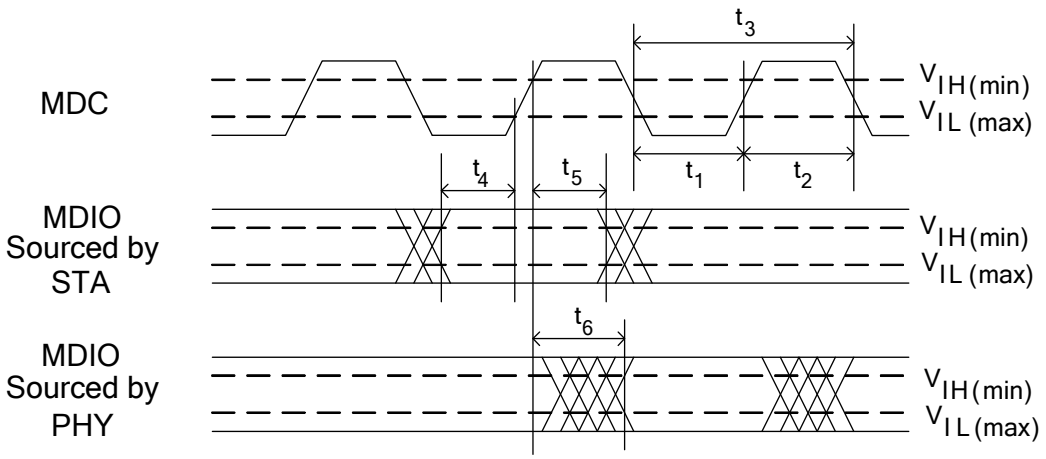


Figure 18. MDC/MDIO Management Timing Parameters

Table 156. MDC/MDIO Management Timing Parameters

Symbol	Description	Minimum	Maximum	Unit
t1	MDC Low Pulse Width	32	-	ns
t2	MDC High Pulse Width	32	-	ns
t3	MDC Period	80	-	ns
t4	MDIO Setup to MDC Rising Edge	10	-	ns
t5	MDIO Hold Time from MDC Rising Edge	10	-	ns
t6	MDIO Valid from MDC Rising Edge	0	45	ns

The MDC shall provide a minimum of 10ns of setup time and a minimum of 10ns of hold time referenced to the rising edge of MDC when STA sources the MDIO signal. The MDC to the output delay shall be a minimum of 0ns, and a maximum of 45ns measured at the STA, when MMD sources the MDIO signal.

9.9.2. SPI Flash Commands

9.9.2.1 SPI Flash Commands

Table 157. SPI Flash Commands

Command	Operation Code	Action
WREN	06h	Write Enable
WRDI	04h	Write Disable
RDID	9Fh	Read Manufacturer and Product ID
RDSR	05h	Read Status Register
WRSR	01h	Write Status Register
Read	03h	Read
Page Program	02h	Page Program
Sector Erase (4K)	20h	Erase The Selected Sector
Block Erase (64K)	D8h	Erase The Selected Block
Chip Erase	60h or C7h	Erase Whole Chip

9.9.2.2 SPI Flash Command Sequence

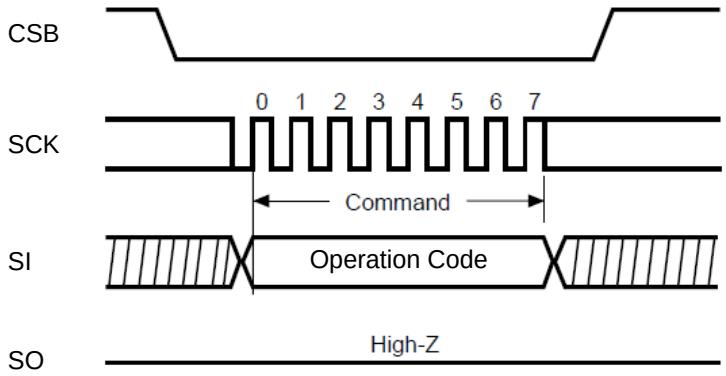


Figure 19. WREN/WRDI Command Sequence

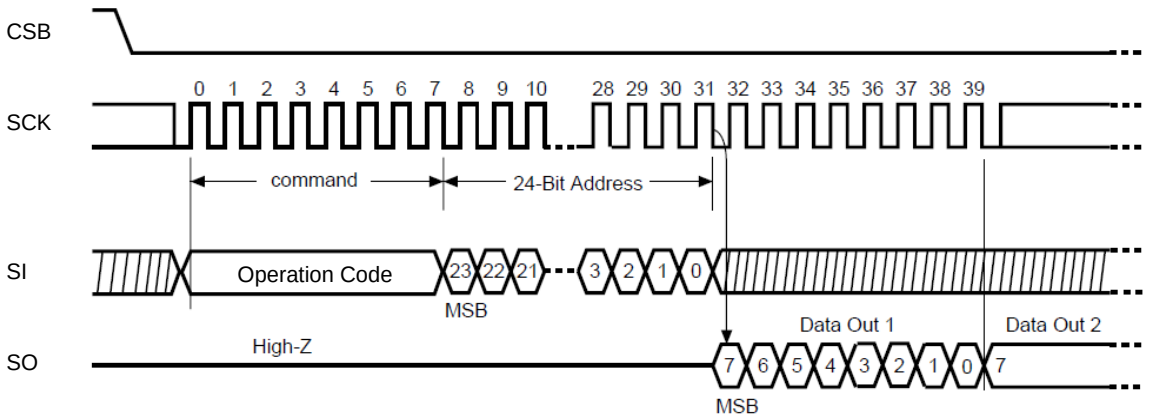


Figure 20. Read Command Sequence

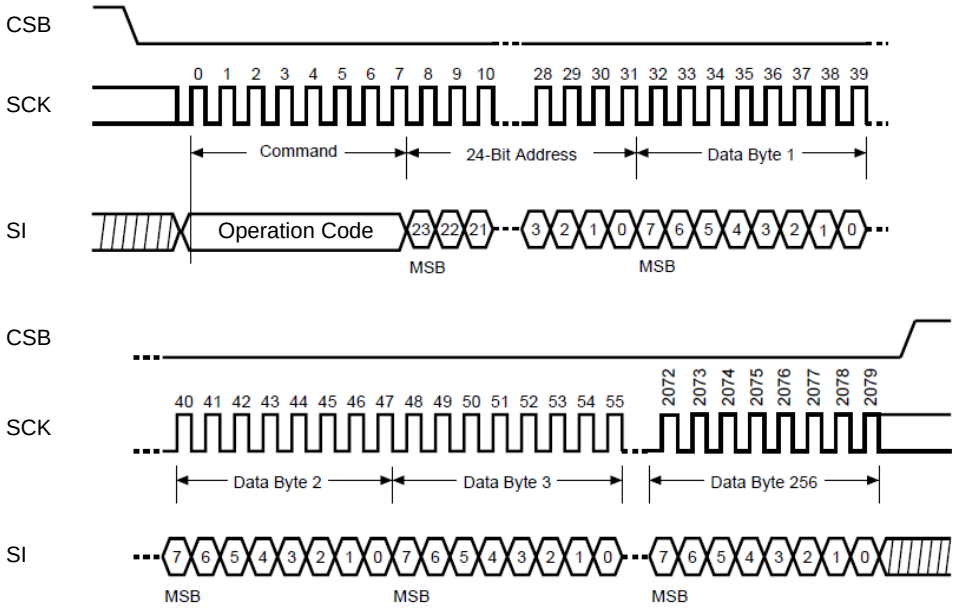


Figure 21. Page Program Command Sequence

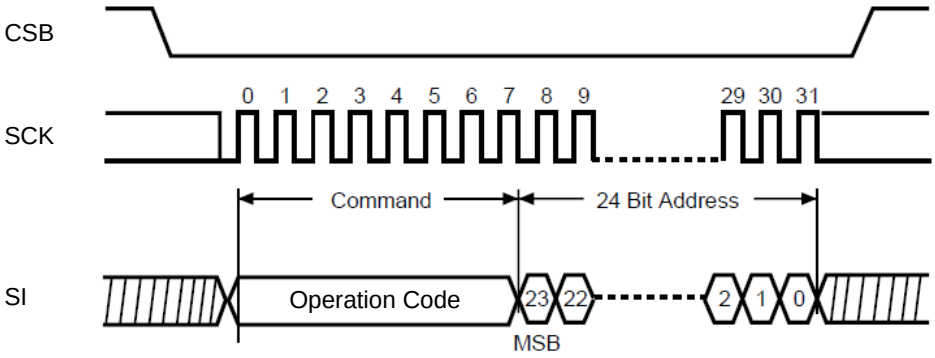


Figure 22. Sector/Block Erase Command Sequence

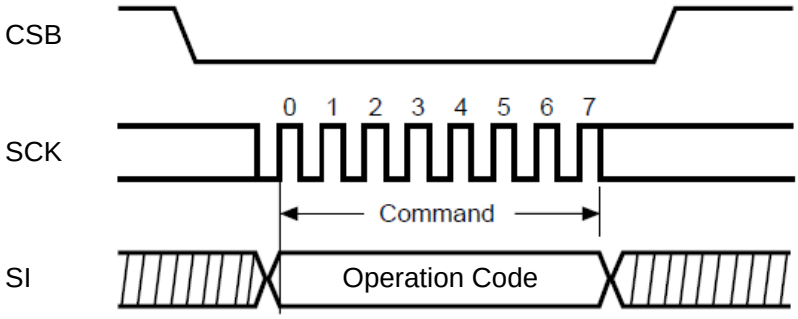
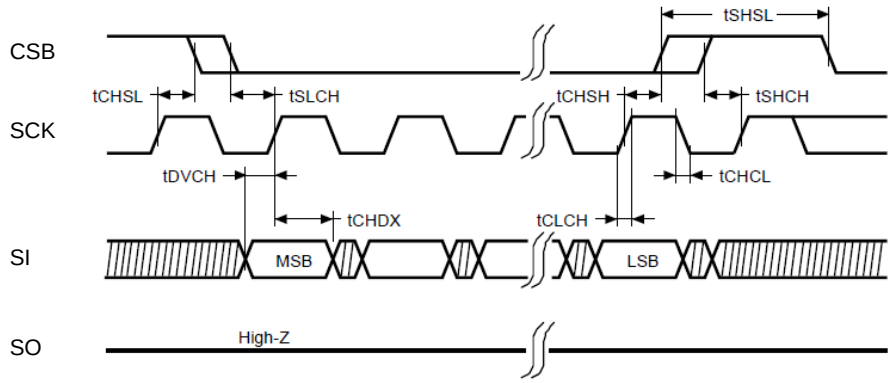


Figure 23. Chip Erase Command Sequence

9.9.3. SPI Flash Interface Timing

Write Timing



Read Timing

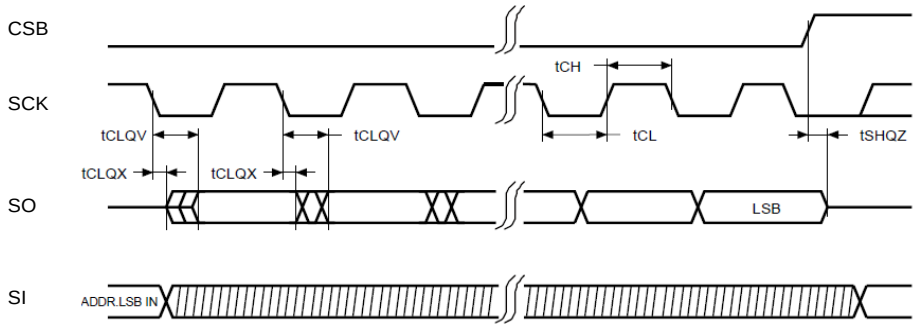
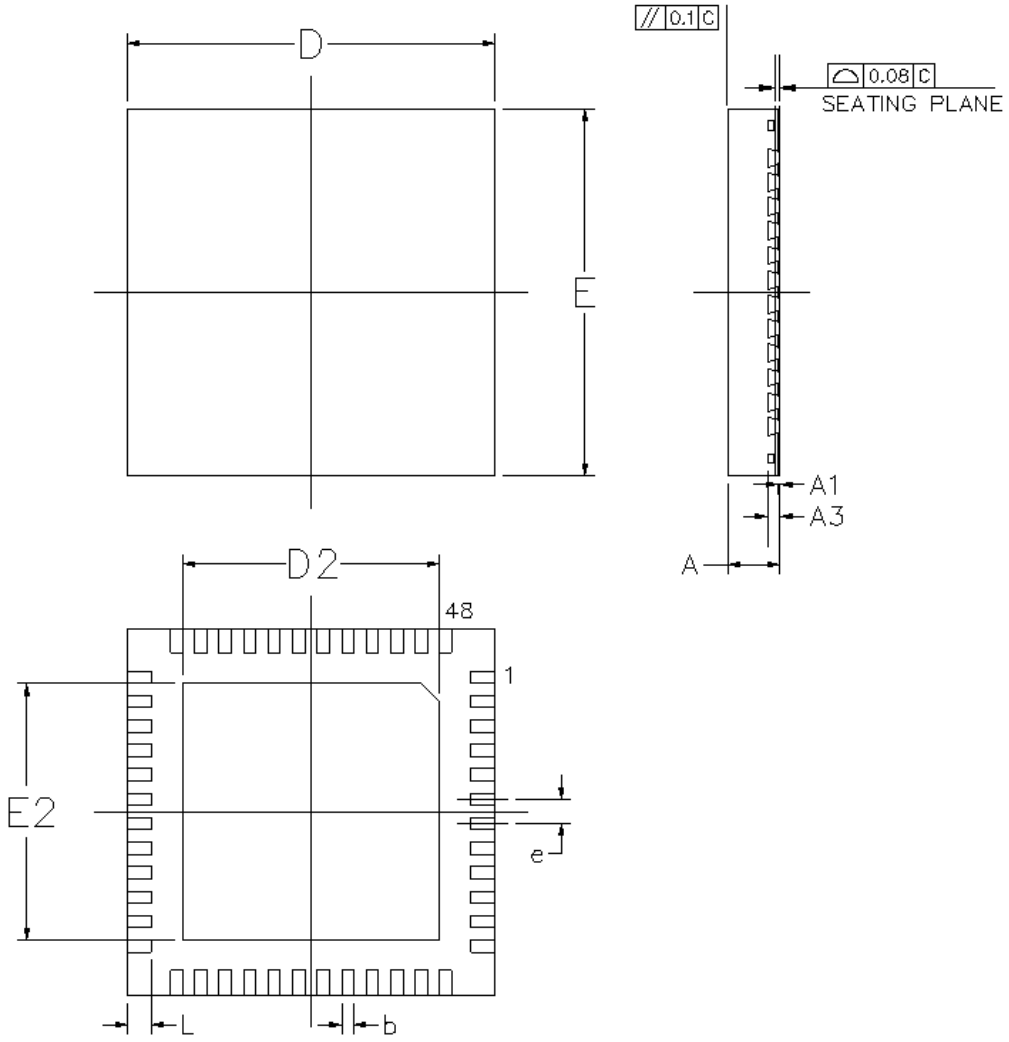


Figure 24. SPI Flash Interface Timing

Table 158. SPI Flash Access Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
fSCK	Clock Frequency for all instructions except Read data (fC)	DC	-	6	MHz
fRSCK	Clock Frequency for the READ instructions (fR)	DC	-	32	MHz
tCH	Clock High Time (fC)	128	-	-	ns
	Clock High Time (fR)	-	16	-	ns
tCL	Clock Low Time (fC)	40	-	-	ns
	Clock Low Time (fR)	-	16	-	ns
tCLCH	Clock Rise Time	0.1	-	-	V/ns
tCHCL	Clock Fall Time	0.1	-	-	V/ns
tDVCH	SI Setup Time	32	-	-	ns
tCHDX	SI Hold Time	96	-	-	ns
tSHQZ	SO Disable Time	-	-	-	ns
tCLQV	Clock Low to SO Valid	-	-	10	ns
tCLQX	SO Hold Time	0	-	-	ns

10. Mechanical Dimensions



10.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		6.00BSC			0.236BSC	
D2/E2	4.04	4.29	4.55	0.159	0.169	0.179
e		0.40BSC			0.016BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes: CONTROLLING DIMENSION: MILLIMETER (mm).
REFERENCE DOCUMENT: JEDEC MO-220.

11. Ordering Information

Table 159. Ordering Information

Part Number	Package
RTL8221B-VB-CG	48-Pin QFN with 'Green' Package
RTL8221B-VM-CG	48-Pin QFN with 'Green' Package
RTL8221BI-VB-CG	48-Pin QFN with 'Green' Package. Industrial grade
RTL8221BI-VM-CG	48-Pin QFN with 'Green' Package. Industrial grade

Note: See page 5 for package identification.

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