Realtek 8/6-Port 10/100 Mbps Ethernet Switch Controller with Embedded memory

The RTL8308/8306 chip is a **128-pin low cost and ultra low power consumption** 8/6-port 10/100M Ethernet switch controller integrated both with a **2M bits embedded DRAM** as packet buffer and a 16K entries of address table. The RTL8308 supports reduced MII (RMII) interface. **Only single 50MHz oscillator is needed** in a switch system to save your Bill Of Material. In addition, the RTL8308/8306 provides a LED display specially to indicate a network loop existence.

1. Features

- Support eight/six 10/100Mbps Ethernet ports with RMII interface
- Provided non-blocking and non-head-of-line-blocking forwarding
- **50MHz 2M bits DRAM is built in** as packet storage buffer. Page based buffer management to efficiently utilize the internal packet buffer
- **Ultra low power consumption with less than 180mA** at 3.3V operating voltage
- **Embedded 16K entries of look-up table** and 128 entries of CAM
- Support address hashing or direct mapping for look-up table. 128-entry CAM is used to eliminate the hash collision problem
- Support full and half duplex operations
- Link, speed and duplex status are auto-detected via MDIO
- Flow control fully supported:
  - Half-duplex: back pressure
  - Full-duplex: IEEE 802.3X
- Auto-negotiated Full-duplex flow control by writing the ability via MDIO to external PHY
- Support store-and-forward and cut-through
- Provide a LED display especially to indicate a network loop existence
- Broadcast storm control
- **Reversible PHYAD order** for diverse PHY
- 24C02 interface
- 128-pin PQFP, 0.35 um, 3.3V CMOS technology

2. General Description

The RTL8308/8306 provides eight/six 10/100 Mbps RMII Ethernet ports. Each port can operate in 10 Mbps or 100 Mbps data rate, and in full or half duplex mode. Speed, duplex and link status can be acquired by periodically polling the status of the PHY devices via MDIO.

2M (or 32K x 64) bits, or 256K bytes DRAM operating in 50MHz clock is built-in as packet storage buffer. To efficiently utilize the packet buffer, the RTL8308/8306 divides the 256K bytes DRAM into 1K pages of storage spaces, i.e., per page contains 256 bytes. For Ethernet packets, the maximum of seven pages are used and the minimum is one.

Address look-up table consists of two spaces. One is a 16K entries of hash table and another is a 128 entries of CAM. The RTL8308/8306 uses address hashing algorithm or direct mapping method to search destination MAC address and record source MAC address from and to the hash table. If hashed or mapped location is not empty, the RTL8308/8306 will compare the destination MAC address with the contents of the CAM for address searching and store source MAC address to CAM for learning.

The RTL8308/8306 supports IEEE 802.3x full duplex flow control and half duplex back pressure congestion control. The IEEE 802.3x flow control's ability is auto-negotiated between remote device and the RTL8308/8306 by writing the flow control ability via MDIO to external connected PHY and restart the auto-negotiation process. For half duplex, the RTL8308/8306 adopts a special back pressure design, forwarding one packet successfully after 28 force collisions, to avoid the connected repeater being partitioned due to lots of collisions. The full/half duplex flow control ability can be enable or disable via ENFCTRL pin.

The RTL8308 provides reversible PHYAD order feature to connect diverse external PHY devices via EEPROM's setting. But 8306 doesn't support this function.

The RTL8308/8306 is capable to auto-detect the network loop (or bridge loop). When a loop is detected, the loop LED is displayed. This capability can be enabled or disabled via ENLOOP pin.

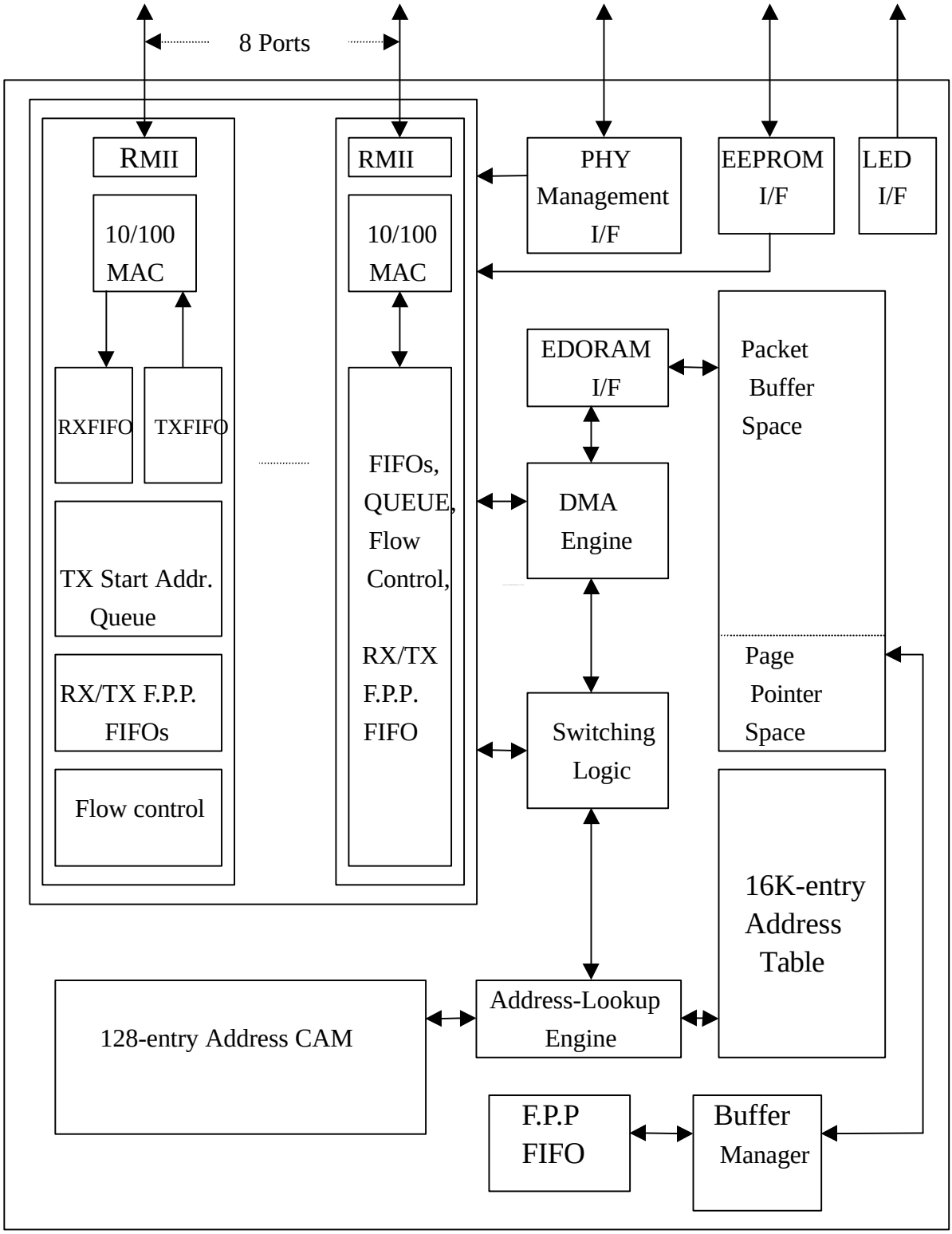
The RTL8308/8306 supports non-blocking 148800 packets/second wire speed forwarding rate and special design to resolve the head-of-line-blocking problem.

The RTL8308/8306 can enable broadcast storm control via ENBRDCTRL pin. Each port will drop

broadcast packet (DID is ff ff ff ff ff ff) after receiving continuous 64 broadcast packets. The counter will be reset as 0 every 800ms or when receiving any non-broadcast packet(DID is not ff ff ff ff ff ff) .

The RTL8308/8306 uses 2-wire 24C02 interface to access external serial EEPROM.

3. Block Diagram



4. Functional Description

Reset

After power on reset, the RTL8308/8306 will determine some features from ENFCTRL, ENBRDCTRL and ENLOOP pins, auto-load the content of 24C02 serial EEPROM, and write abilities to connected PHY management registers via MDC/MDIO. It is most important that the RTL8308/8306 and connected PHYs have to use the same reset signal source. Otherwise, it is not guaranteed to work properly.

RMII interface

The RTL8308/8306 provides 10/100 Mbps low pin count RMII interface for use between PHY and RTL8308/8306. The RMII is capable of supporting 10Mbps and 100Mbps data rates. A single clock reference, 50MHz, sourced from an external clock input is used for receive and transmit. It also provides independent 2 bit wide (di-bit) transmit and receive data paths. As the REFCLK is 10 times the data rate in 10Mbps mode each data di-bit must be output on TXD[1:0] and input on RXD[1:0] for ten consecutive REFCLK cycles. The RTL8308/8306 can regenerate the COL signal of the MII internally by ANDing TXEN and CRS as recovered from CRSDV. Note that TXEN cannot be ANDed directly with CRSDV since CRSDV may toggle at the end of the frame to provide separation of RXDV and CRS.

RMII Specification Signals are as below,

Signal Name	Direction (with respect to the PHY)	Direction (with respect to the RTL8308/8306)	Use
REFCLK	Input	Input	Synchronous clock reference for receive, transmit and control interface.
CRSDV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Date
TXEN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data

Serial Management Interface MDC/MDIO

The RTL8308/8306 supports PHY management through the serial MDIO and MDC signal lines. After power on reset, the RTL8308/8306 write abilities to the advertisement register 4 of connected PHY and restart the auto-negotiation process through MDIO using PHY address increasingly from 01000b to 01111b. After restarting auto-negotiation, the RTL8308/8306 will continuously poll the link status and link partner's ability which including speed, duplex and flow control of the PHY devices via MDIO. The following is the management frame format

	Management frame fields							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1 ..1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1 ..1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Reversible PHYAD order

The RTL8308 provides the reversible PHYAD order feature to connect diverse external PHY devices. The addresses of port [A] till [H] are corresponding to PHYAD 01000b till 01111b or to PHYAD 01111b till 01000b depending on the value of PHYAD_RV in EEPROM. But RTL8306 does not support this feature.

Address Search and Learning

The RTL8308/8306 supports address hashing or direct mapping algorithm to search destination MAC address and learn source MAC address. The aging time of the learnt source MAC address is 300 seconds or 5 minutes. The either mode can be selected via 24C02.

Address hashing mode

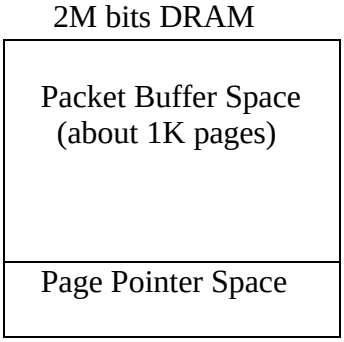
When a packet is receiving, firstly the RTL8308/8306 hashes the ***destination*** MAC address to get a location index to the 16K-entry hash table and at the same time compares the destination MAC address with the contents of the 128-entry CAM. If the hash indexed location is valid or the CAM comparison is match, this receiving packet will be forwarded to the corresponding destination port. Otherwise, the RTL8308/8306 broadcasts the packet. Next the RTL8308/8306 hashes the ***source*** MAC address to get a location index to the hash table, if the hash indexed location has been occupied, i.e., hash collision occurs, the new source MAC address will be relocated into the 128-entry CAM accordingly. Using this eliminates the hash collision problem.

Address direct mapping mode

In this mode, the RTL8308/8306 uses the last 14 bits of sequence number of MAC to index to the 16K-entry look-up table.

Buffer Management

The embedded DRAM is divided into two parts. One is Packet Buffer Space for storing received packet data and the other is Page Pointer Space managed by buffer manager. The Packet Buffer Space consists of about 1k storage units in page. Each page is comprised of a 8-byte Header information, including next page pointer and receive byte count, and 248 bytes of data. The page pointers are contained in Page Pointer Space



Buffer Manager

The Buffer Manager of the RTL8308/8306 contains a Free Page Pointer FIFO pool to store and provide available free page pointers to all ports. After power up reset, the Buffer Manager will initiate *Descriptor Read* command to get some available free page pointers from Page Pointer Space. When the content of the FIFO is almost empty due to continuous data receptions, the Descriptor Read command will be reinitiated to get more available free page pointers. In the other hand, when the FIFO contents is almost full due to continuous successfully data transmissions, the RTL8308/8306 initiates the *Descriptor Write* command to write the additional available free page pointers back to Page Pointers Space.

Data reception

Each port contains a Receive Data FIFO and a Receive Free Page Pointer FIFO. Initially the Free Page Pointer FIFO is filled up with free page pointers getting from Buffer Manager. Once a packet is coming, the receive data flows into Receive Data FIFO first and then is moved into Packet Buffer by Receive DMA Engine using the free page pointers in Receive Free Page Pointer FIFO via *Get Free Page* command. The RTL8308/8306 always attempts to fill the Free Page Pointer FIFO up with free page pointers.

Data Forwarding

Each port also contains a Transmit Data FIFO, a Transmit Free Page Pointer FIFO and a Transmit Start Address Queue. Once a forwarding condition is met, for cut through mode 384 bytes data are received OK or for store-and-forward mode a packet is received completely, the receiving port will pass the beginning page pointer using Send TX Descriptor command to transmit port and start the Transmit DMA. The transmission port stores the beginning page pointer in Transmit Head Point Queue. The Transmit DMA moves data from Packet Buffer through Transmit Data FIFO and to MII or RMII interface using the free page pointer in the Transmit Free Page Pointer FIFO. Once the packet has been forwarded successfully, the RTL8308/8306 uses Put Free Page command to put related free page pointers back to buffer manager's Free Page Pointer FIFO.

Flow Control

The RTL8308/8306 supports IEEE 802.3x full duplex flow control and half duplex back pressure congestion control. The IEEE 802.3x flow control's ability is auto-negotiated between remote device and the RTL8308/8306 by writing the flow control ability via MDIO to external connected PHY. The RTL8308/8306 adopts a special back pressure design, forwarding one packet successfully after 28 force collisions, to avoid the connected repeater being partitioned.

Loop Detection

The RTL8308/8306 periodically sends out a broadcast 64-byte packet every 3~5 minutes and automatically detect whether if there is a network loop (or bridge loop) existence. The loop LED asserted low to indicate there is a loop exits. The LED goes out by unplugging the both RTL8308/8306's ports of the loop. The Loop frame length is 64 bytes and its format is as below,

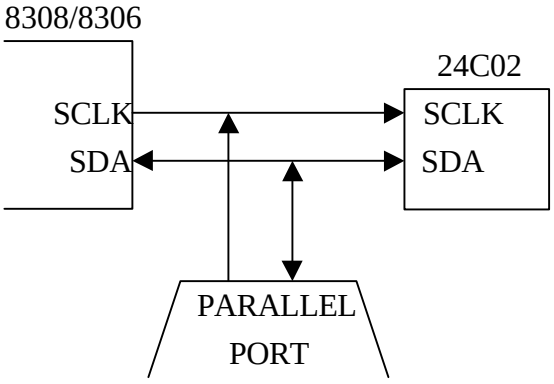
FFFFFF	SID	0040	0000000 ..0000	CRC

Head-Of-Line Blocking

The RTL8308/8306 incorporate a simple mechanism to prevent Head-Of -Line blocking problem. When a packet receiving from receive port A is destined to a congested port B, this packet will be asked to PAUSE for full duplex or be back pressured for half duplex. If a new packet immediately following this packet is coming to the same receive port A, it is destined to loosely traffic port C rather than the congested port B. Then this new packet will be successfully forwarded to port C not affected by port B. The Head-Of-Line Blocking problem usually occurs when interconnected between switch and repeater.

24C02 Interface

The 24C02 interface is a 2-wire serial EEPROM interface providing 2K bits storage space. After power on reset, the RTL8308/8306 uses Random Read and Sequential Read commands to auto-load configuration settings, switch Ethernet ID and so on. After auto-loaded, the 24C02 interface pins SCL and SDA are tri-stated for on-line updating 24C02 contents through a parallel port.



24C02 Device Operation

Clock and Data transitions: The SDA pin is normally pulled high with an external register. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a start or stop condition as defined below.

Start condition: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command.

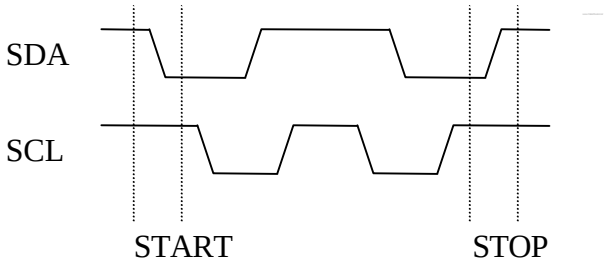
Stop condition: A low-to-high transition of SDA with SCL high is a stop condition.

Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8 bit words. The 24C02 sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

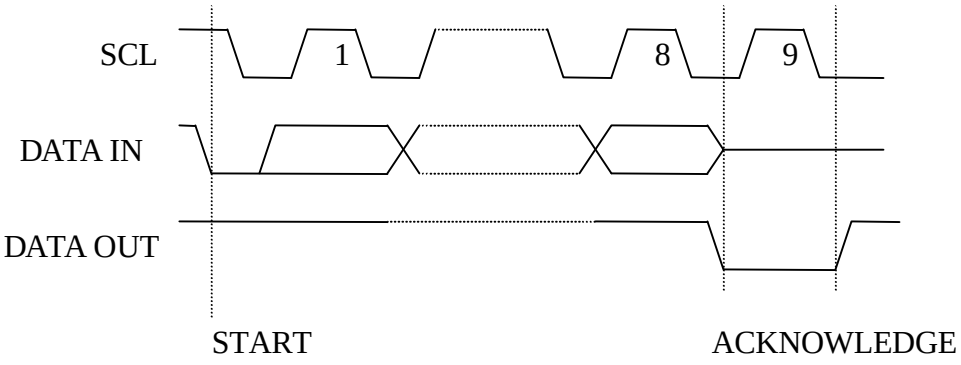
Random Read: A random read requires a "dummy" byte write sequence to load in the data word address.

Sequential Read: For RTL8308/8306, the sequential reads are initiated by a random address read. After the 24C02 receives a data word, it responds with an acknowledge. As long as the 24C02 receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words.

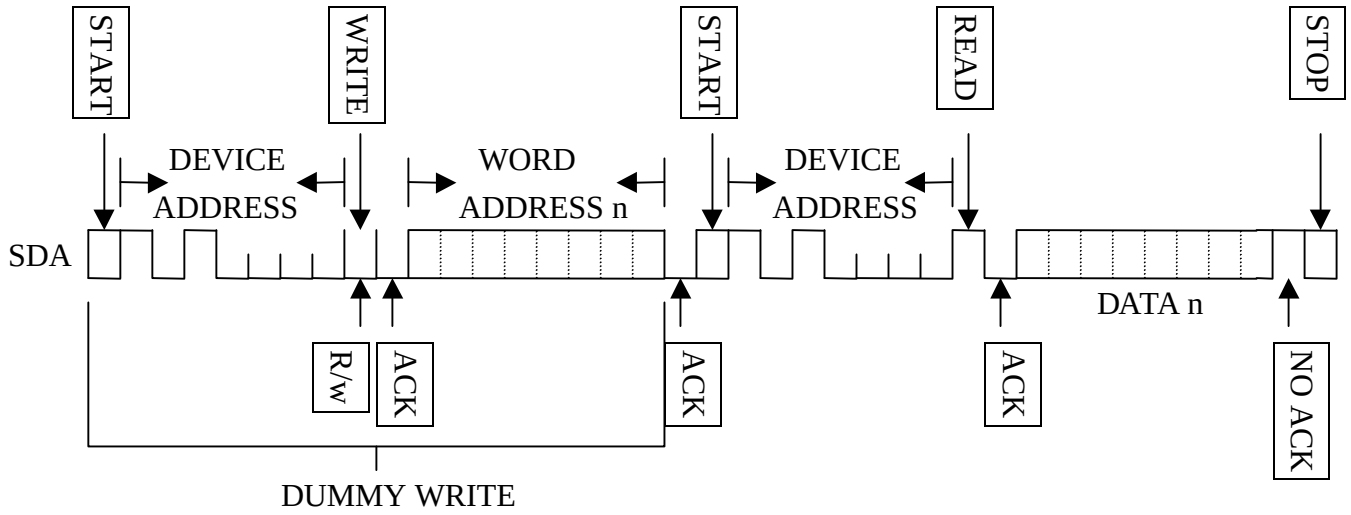
**Start and Stop Definition*



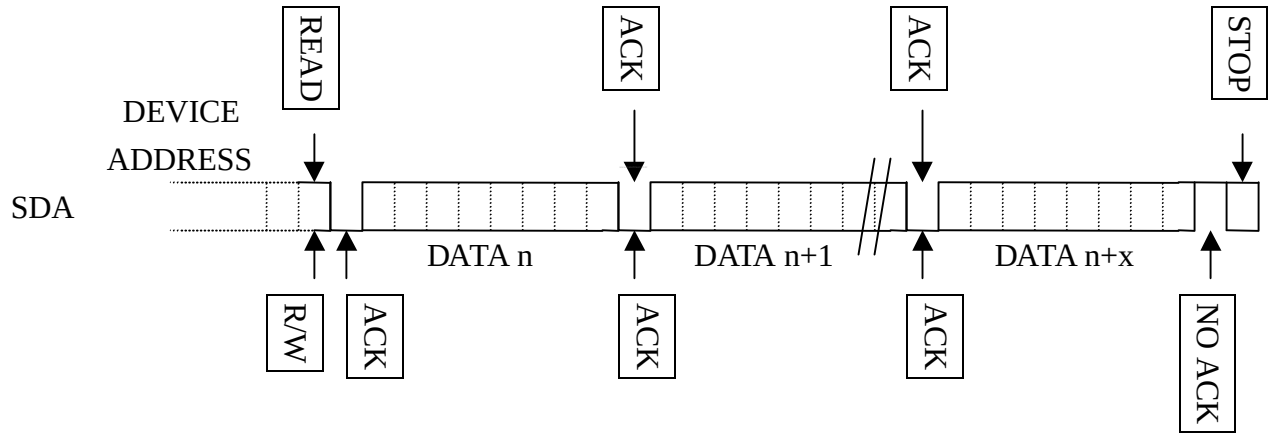
**Output Acknowledge*



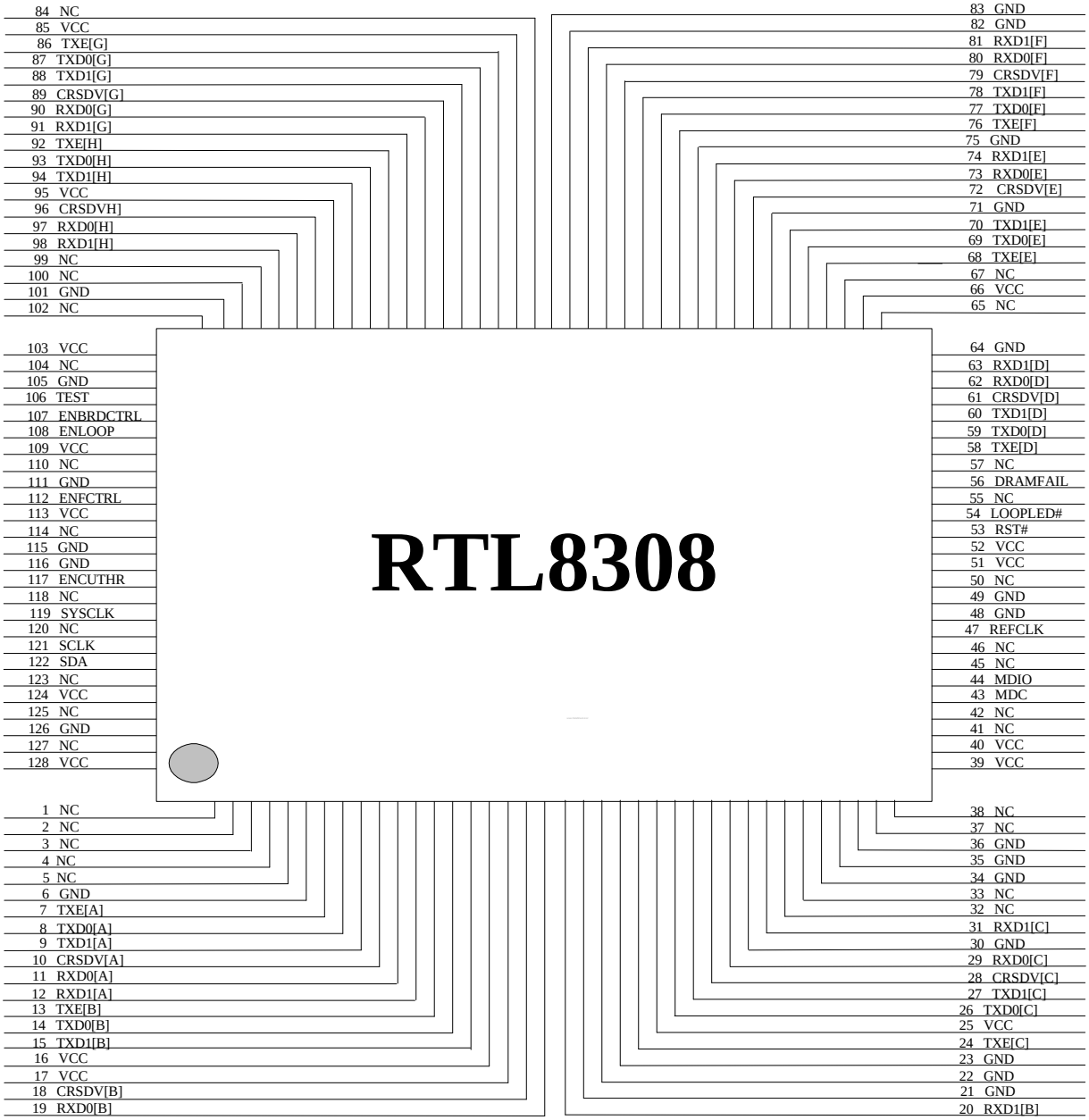
**Random Read*

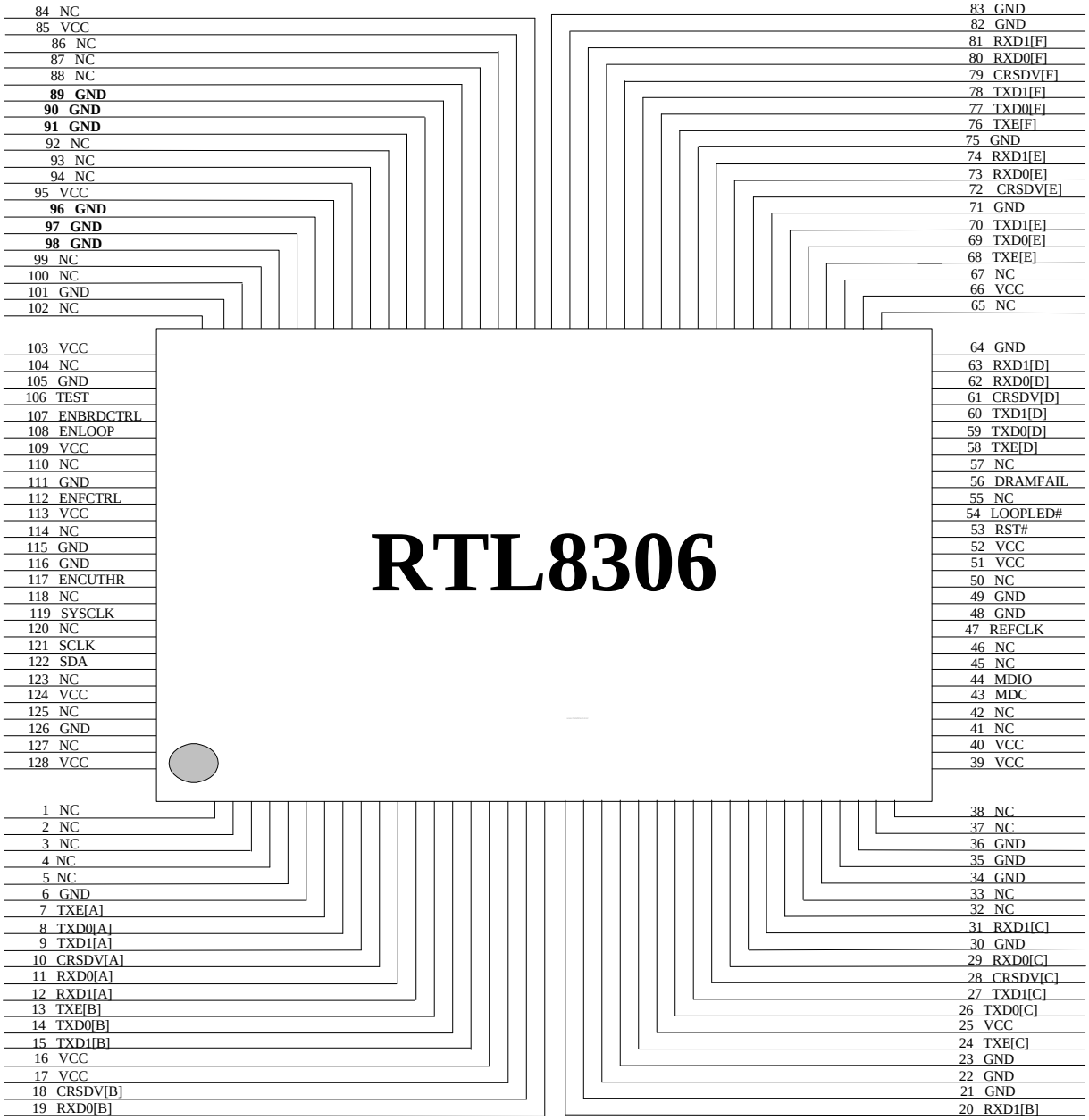


**Sequential Read*



5. Pin Assignment


RTL8308
1 NC
2 NC
3 NC
4 NC
5 NC
6 GND
7 TXE[A]
8 TXD0[A]
9 TXD1[A]
10 CRSDV[A]
11 RXD0[A]
12 RXD1[A]
13 TXE[B]
14 TXD0[B]
15 TXD1[B]
16 VCC
17 VCC
18 CRSDV[B]
19 RXD0[B]
20 RXD1[B]
21 GND
22 GND
23 GND
24 TXE[C]
25 VCC
26 TXD0[C]
27 TXD1[C]
28 CRSDV[C]
29 RXD0[C]
30 GND
31 RXD1[C]
32 NC
33 NC
34 GND
35 GND
36 GND
37 NC
38 NC
39 VCC
40 VCC
41 NC
42 NC
43 MDC
44 MDIO
45 NC
46 NC
47 REFCLK
48 GND
49 GND
50 NC
51 VCC
52 VCC
53 RST#
54 LOOPLED#
55 NC
56 DRAMFAIL
57 NC
58 TXE[D]
59 TXD0[D]
60 TXD1[D]
61 CRSDV[D]
62 RXD0[D]
63 RXD1[D]
64 GND
65 NC
66 VCC
67 NC
68 TXE[E]
69 TXD0[E]
70 TXD1[E]
71 GND
72 CRSDV[E]
73 RXD0[E]
74 RXD1[E]
75 GND
76 TXE[F]
77 TXD0[F]
78 TXD1[F]
79 CRSDV[F]
80 RXD0[F]
81 RXD1[F]
82 GND
83 GND
84 NC
85 VCC
86 TXE[G]
87 TXD0[G]
88 TXD1[G]
89 CRSDV[G]
90 RXD0[G]
91 RXD1[G]
92 TXE[H]
93 TXD0[H]
94 TXD1[H]
95 VCC
96 CRSDVH]
97 RXD0[H]
98 RXD1[H]
99 NC
100 NC
101 GND
102 NC
103 VCC
104 NC
105 GND
106 TEST
107 ENBRDCTRL
108 ENLOOP
109 VCC
110 NC
111 GND
112 ENFCTRL
113 VCC
114 NC
115 GND
116 GND
117 ENCUTHR
118 NC
119 SYSCLK
120 NC
121 SCLK
122 SDA
123 NC
124 VCC
125 NC
126 GND
127 NC
128 VCC


RTL8306
84 NC
85 VCC
86 NC
87 NC
88 NC
89 GND
90 GND
91 GND
92 NC
93 NC
94 NC
95 VCC
96 GND
97 GND
98 GND
99 NC
100 NC
101 GND
102 NC
103 VCC
104 NC
105 GND
106 TEST
107 ENBRDCTRL
108 ENLOOP
109 VCC
110 NC
111 GND
112 ENFCTRL
113 VCC
114 NC
115 GND
116 GND
117 ENCUTHR
118 NC
119 SYSCLK
120 NC
121 SCLK
122 SDA
123 NC
124 VCC
125 NC
126 GND
127 NC
128 VCC
1 NC
2 NC
3 NC
4 NC
5 NC
6 GND
7 TXE[A]
8 TXD0[A]
9 TXD1[A]
10 CRSDV[A]
11 RXD0[A]
12 RXD1[A]
13 TXE[B]
14 TXD0[B]
15 TXD1[B]
16 VCC
17 VCC
18 CRSDV[B]
19 RXD0[B]
83 GND
82 GND
81 RXD1[F]
80 RXD0[F]
79 CRSDV[F]
78 TXD1[F]
77 TXD0[F]
76 TXE[F]
75 GND
74 RXD1[E]
73 RXD0[E]
72 CRSDV[E]
71 GND
70 TXD1[E]
69 TXD0[E]
68 TXE[E]
67 NC
66 VCC
65 NC
64 GND
63 RXD1[D]
62 RXD0[D]
61 CRSDV[D]
60 TXD1[D]
59 TXD0[D]
58 TXE[D]
57 NC
56 DRAMFAIL
55 NC
54 LOOPLED#
53 RST#
52 VCC
51 VCC
50 NC
49 GND
48 GND
47 REFCLK
46 NC
45 NC
44 MDIO
43 MDC
42 NC
41 NC
40 VCC
39 VCC
38 NC
37 NC
36 GND
35 GND
34 GND
33 NC
32 NC
31 RXD1[C]
30 GND
29 RXD0[C]
28 CRSDV[C]
27 TXD1[C]
26 TXD0[C]
25 VCC
24 TXE[C]
23 GND
22 GND
21 GND
20 RXD1[B]

6.Pin Descriptions

- 8308 pin description

RMII Interface			
Symbol	*Type*	*Pin No*	*Description*
TXE[A:H]	O	7,13,24,58, 68,76,86,92	Transmit Enable. The RTL8308 asserts high to indicate that valid data for transmission is presented on the TXD[1:0]
TXD[0:1][A], TXD[0:1][B], TXD[0:1][C], TXD[0:1][D], TXD[0:1][E], TXD[0:1][F], TXD[0:1][G], TXD[0:1][H]	O	8,9, 14,15, 26,27, 59,60, 69,70, 77,78, 87,88, 93,94	Transmit Data [1:0].
CRSDV[A:H]	I	10,18,28,61, 72,79,89,96	CRSDV signals. CRSDV from PHY device is asserted high when media is non-idle.
RXD[0:1][A], RXD[0:1][B], RXD[0:1][C], RXD[0:1][D], RXD[0:1][E], RXD[0:1][F], RXD[0:1][G], RXD[0:1][H]	I	11,12, 19,20, 29,31, 62,63, 73,74, 80,81, 90,91, 97,98	Receive Data [1:0]. The RTL8308/8306 captures the receive data on the rising edge of REFCLK when CRSDV is high.
REFCLK	I	47	Reference Clock input. A 50 MHz signal is used for RMII clock reference.
MDC	O	43	Management Data Clock
MDIO	I/O	44	Management Data Input/Output
Serial EEPROM 24C02 Interface			
Symbol	*Type*	*Pin No*	*Description*
SCLK	O	121	Serial Clock: Internally pulled high
SDA	I/O	122	Serial Data Input/Output: Internally pulled high
System Pins			
Symbol	*Type*	*Pin No*	*Description*
RST#	I	53	Reset: Active low to a known reset state. After power-on reset (low to high), the configuration modes from Mode Pins are determined, the content of serial EEPROM is auto-loaded into and the RTL8308/8306 begins to access the management data of PHY devices.
SYSCLK	I	119	System clock input 50 MHz system clock is used.
Mode Pins (Reset-read)			
Symbol	*Type*	*Pin No*	*Description*
ENLOOP	I	108	Enable loop detection: When pulled high upon reset, the auto loop detection is enabled. When pulled low upon reset, it is disabled.

ENCUTHR	I	117	Enable Cut-through: Pulled high upon reset will select the Cut-through mode. Pulled low upon reset selects the store-and-forward mode.
ENBRDCTRL	I	107	Enable Broadcast storm Control.
ENFCTRL	I	112	Enable Full Duplex Flow Control: Pulled high upon reset will enable the full duplex IEEE802.3x flow control function. The flow control ability will be write to the management register 4 of PHY device one and only one time after power-on reset, for advertising. Pulled low upon reset will disable the flow control function.
LED Pin			
Symbol	*Type*	*Pin No*	*Description*
LOOPLED#	O	54	Loop Detected LED: Low active Asserted low indicates that a network loop is detected.
DRAMFAIL	O	56	DRAM Fail LED: High active Asserted high indicates that the embedded DRAM is failed.
Test Pin			
Symbol	*Type*	*Pin No*	*Description*
TEST	I	106	Test pin : for internal use Must be tied to ground for normal use.
Power Ground Pin			
GND		6,21,22,23,30,34, 35,36,48,49,64,71, 75,82,83,101,105, 115,116,126	
VCC		16,17,25,39,40,51, 52,66,85,95,103, 109,113,124,128	

- 8306 pin description

RMII Interface			
Symbol	*Type*	*Pin No*	*Description*
TXE[A:F]	O	7,13,24,58, 68,76	Transmit Enable. The RTL8306 asserts high to indicate that valid data for transmission is presented on the TXD[1:0]
TXD[0:1][A], TXD[0:1][B], TXD[0:1][C], TXD[0:1][D], TXD[0:1][E], TXD[0:1][F]	O	8,9, 14,15, 26,27, 59,60, 69,70, 77,78	Transmit Data [1:0].
CRSDV[A:F]	I	10,18,28,61, 72,79	CRSDV signals. CRSDV from PHY device is asserted high when media is non-idle.
RXD[0:1][A], RXD[0:1][B], RXD[0:1][C], RXD[0:1][D], RXD[0:1][E], RXD[0:1][F]	I	11,12, 19,20, 29,31, 62,63, 73,74, 80,81	Receive Data [1:0]. The RTL8306 captures the receive data on the rising edge of REFCLK when CRSDV is high.
REFCLK	I	47	Reference Clock input. A 50 MHz signal is used for RMII clock reference.
MDC	O	43	Management Data Clock
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Mode Pins (Reset-read)			
Symbol	*Type*	*Pin No*	*Description*
ENLOOP	I	108	Enable loop detection: When pulled high upon reset, the auto loop detection is enabled. When pulled low upon reset, it is disabled.
ENCUTHR	I	117	Enable Cut-through: Pulled high upon reset will select the Cut-through mode. Pulled low upon reset selects the store-and-forward mode.
ENBRDCTRL	I	107	Enable Broadcast storm Control.

ENFCTRL	I	112	Enable Full Duplex Flow Control: Pulled high upon reset will enable the full duplex IEEE802.3x flow control function. The flow control ability will be write to the management register 4 of PHY device one and only one time after power-on reset, for advertising. Pulled low upon reset will disable the flow control function.
LED Pin			
Symbol	*Type*	*Pin No*	*Description*
LOOPLED#	O	54	Loop Detected LED: Low active Asserted low indicates that a network loop is detected.
DRAMFAIL	O	56	DRAM Fail LED: High active Asserted high indicates that the embedded DRAM is failed.
Test Pin			
Symbol	*Type*	*Pin No*	*Description*
TEST	I	106	Test pin : for internal use Must be tied to ground for normal use.
Power Ground Pin			
GND		6,21,22,23,30,34, 35,36,48,49,64,71, 75,82,83,101,105, 115,116,126, 89,90,91,96,97,98	
VCC		16,17,25,39,40,51, 52,66,85,95,103, 109,113,124,128	

7. Serial EEPROM 24C02 Format

Below is the content of serial EEPROM 24C02. The content includes configuration, Switch Ethernet ID, CRCs for flow control and loop detection.

Bit / Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	AcceptErr	0	0	0
1	0	HashMode	0	0	0	0	0	PHYAD_RV
2-7	Ethernet ID (Physical Address) PAR47~0							
8-11	Pause ON CRC 31~0							
12-15	Pause OFF CRC 31~0							
16-19	Loop Detection CRC 31~0							

HashMode: ~~When 0~~ When 1, address hashing algorithm used for search and learning
~~When 1~~ When 0, address direct mapping algorithm used

AcceptErr: When 0, CRC error packet will be discarded for normal use.
When 1, CRC Error packet can be accepted and forwarded for test.

PHYAD_RV: When 0, port**[A]~[H]** uses PHYAD = 01000b ~ 01111b to access external PHY status.
When 1, port**[H]~[A]** uses PHYAD = 01000b ~ 01111b.

The PHYAD_RV value can be zero or one for RTL8308, but it must be zero for RTL8306.

8. Electrical Characteristics

8.1 Temperature Limit Ratings:

Parameter	Minimum	Maximum	Units
Storage temperature	-55	+125	¢ J
Operating temperature	0	70	¢ J

8.2 DC Characteristics

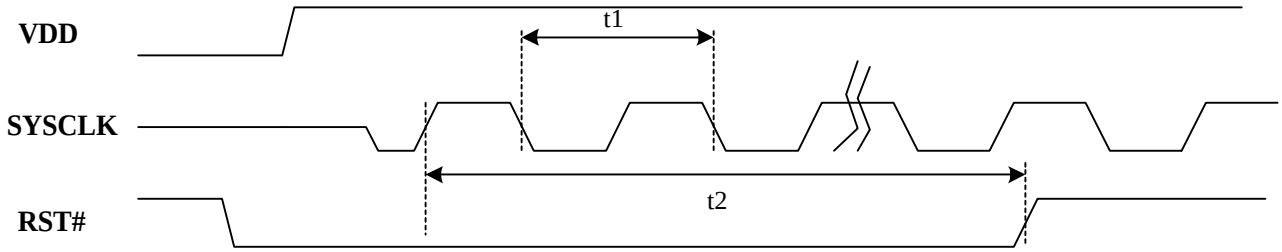
Supply voltage Vcc* = 3.3V +- 5%

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Minimum High Level Output Voltage	I_{OH}= -8mA	0.9 * Vcc		Vcc	V
V_{OL}	Maximum Low Level Output Voltage	I_{OL}= 8mA			0.1 * Vcc	V
V_{IH}	Minimum High Level Input Voltage		0.5 * Vcc		Vcc+0.5	V
V_{IL}	Maximum Low Level Input Voltage		-0.5		0.3 * Vcc	V
I_{IN}	Input Current	V_{IN}=V_{CC} or GND	-1.0		1.0	£ ¤
I_{OZ}	Tri-State Output Leakage Current	V_{OUT}=V_{CC} or GND	-10		10	£ ¤
I_{CC}	Average Operating Supply Current	I_{OUT}=0mA,		**160**	**180**	mA

8.3 AC Characteristics

8.3.1 Reset and Clock Timing

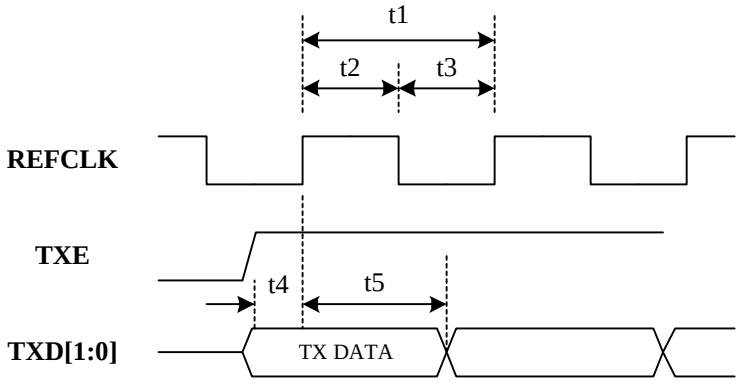
Symbol	Description	Minimum	Typical	Maximum	Units
$f_{clock\ (SYSCK)}$	SYSCLK clock frequency	40	50	66	MHZ
t1	SYSCLK clock period	15	20	25	ns
t2	RST# low pulse duration	1000	-	-	ns



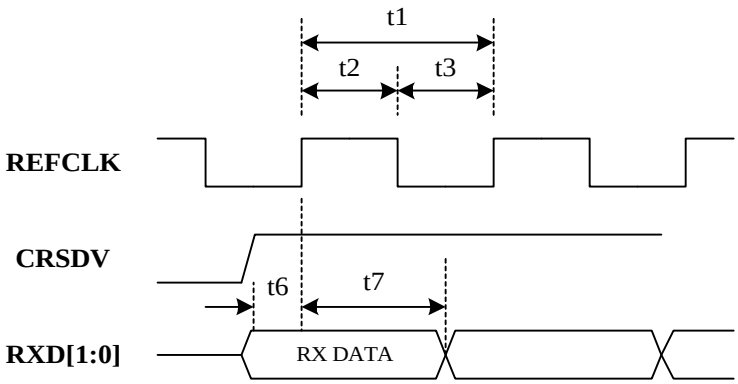
Reset and Clock Timing

8.3.2 RMII Timing

Symbol	Description	Minimum	Typical	Maximum	Units
t1	REFCLK clock period	-	20	-	ns
t2	REFCLK high level width	-	10	-	ns
t3	REFCLK low level width	-	10	-	ns
t4	TXE ,TXD to REFCLK rising setup time	4	-	-	ns
t5	TXE ,TXD to REFCLK rising hold time	2	-	-	ns
t6	CSRDV ,RXD to REFCLK rising setup time	4	-	-	ns
t7	CRSDV ,RXD to REFCLK rising hold time	2	-	-	ns



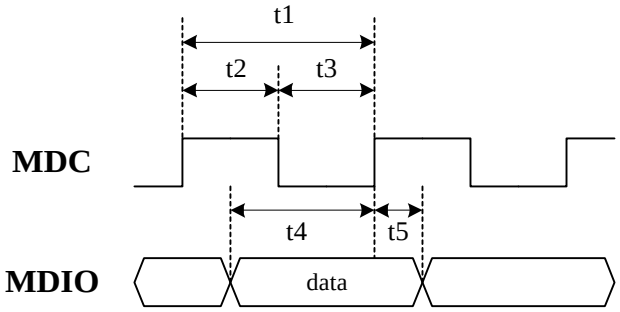
RMII Transmit Timing



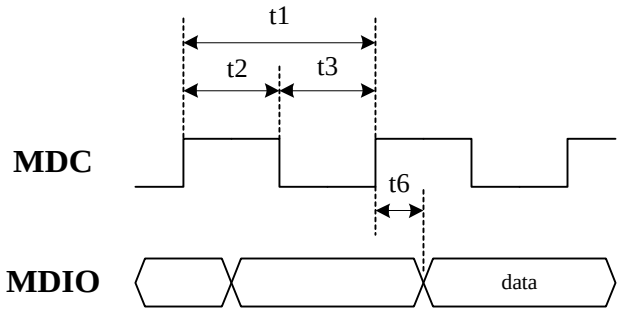
RMII Receive Timing

8.3.3 PHY Management Timing

Symbol	Description	Minimum	Typical	Maximum	Units
t1	MDC clock period	-	SYSCK * 32	-	ns
t2	MDC high level width	-	SYSCK * 16	-	ns
t3	MDC low level width	-	SYSCK * 16	-	ns
t4	MDIO to MDC rising setup time (Write Bits)	10	-	-	ns
t5	MDIO to MDC rising hold time (Write Bits)	10	-	-	ns
t6	MDC to MDIO delay (Read Bits)	-	-	20	ns



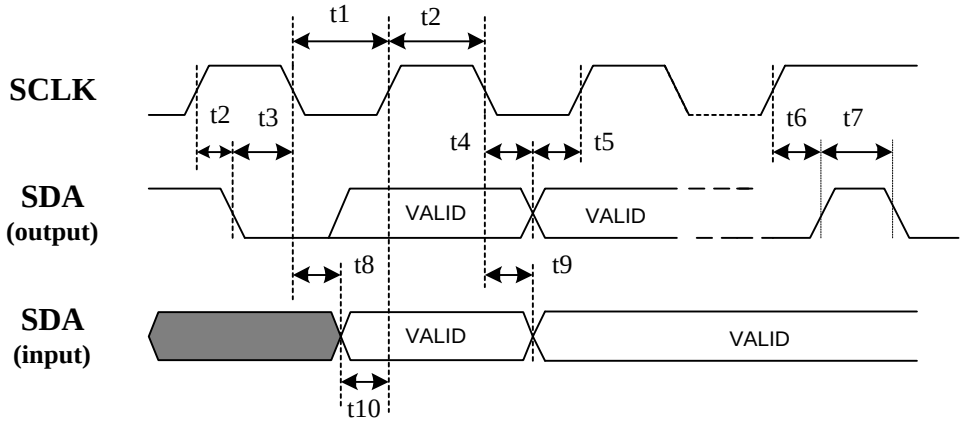
MDIO Write Timing



MDIO Read Timing

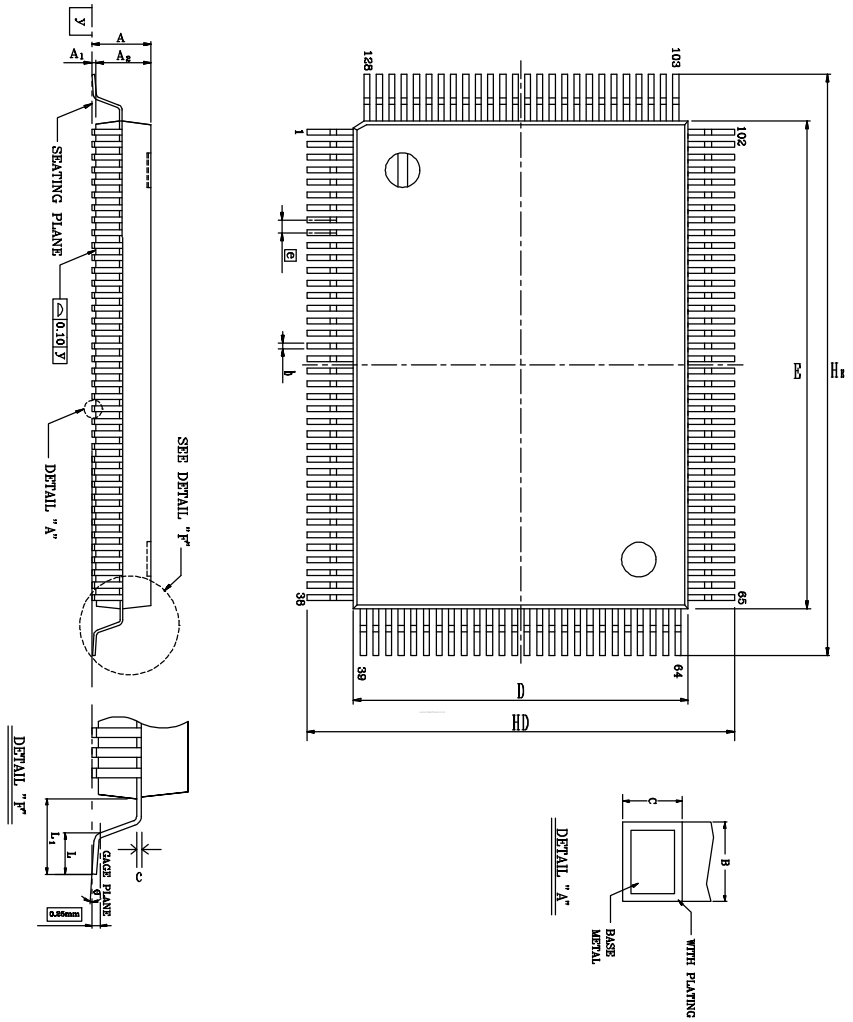
8.3.4 Serial EEPROM 24C02 Timing

Symbol	Description	Minimum	Typical	Maximum	Units
$f_{clock\ (EESCK)}$	Clock frequency , SCLK	-	-	66	kHZ
t1	Clock pulse period	23	-	-	us
t2	Delay time, form SCLK rising to SDA falling	5	-	-	us
t3	Delay time, form SDA falling to SCLK falling	5	-	-	us
t4	Delay time, form SCLK falling to SDA changing	0	-	-	us
t5	Delay time, form SDA valid output to SCLK rising	0	-	-	us
t6	Stop Set-up time	5	-	-	us
t7	Time the bus must is free before a new transmission starting	5	-	-	us
t8	Delay time, form SCLK falling to SDA valid	0	-	-	us
t9	Delay time, form SCLK falling to SDA changing	0	-	-	us
t10	Delay time, from SDA valid input to SCLK rising	10	-	-	us



EEPROM Interface Timing

9. Mechanical Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Type	Max	Min	Type	Max
A	¡ Ð		0.134	¡ Ð	¡ Ð	3.40
A1	0.004	0.010	0.036	0.10	**0.25**	0.91
A2	0.102	0.112	0.122	2.60	**2.85**	3.10
b	0.005	0.009	0.013	0.12	**0.22**	0.32
c	0.002	0.006	0.010	0.05	**0.15**	0.25
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e	0.010	0.020	0.030	0.25	**0.5**	0.75
HD	0.665	0.677	0.689	16.90	**17.20**	17.50
HE	0.902	0.913	0.925	22.90	**23.20**	23.50
L	0.027	0.035	0.043	0.68	**0.88**	1.08
L1	0.053	0.063	0.073	1.35	**1.60**	1.85
y	¡ Ð	¡ Ð	0.004	¡ Ð	¡ Ð	0.10
£ c	0¢	X ¡ Ð	12¢ X	0¢	X ¡ Ð	12¢ X

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar rotrusion/intrusion.
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.

TITLE : **128 QFP** (14x20 mm) PACKAGE OUTLINE -CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL :			
APPROVE		DOC. NO.	530-ASS-P004
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	Q128 - 1
		DATE	Oct. 08 1998
REALTEK SEMI-CONDUCTOR CO., LTD			