RTL8366S/SR

SINGLE-CHIP 5+1-PORT 10/100/1000 MBPS SWITCH CONTROLLER WITH DUAL MAC INTERFACES

DATASHEET

Rev. Pre-1.4
19 Oct. 2007
Track ID:

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL8366S/SR chips.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	**Summary**
Pre-1.0	2007/03/30	Preliminary release.
Pre-1.1	2007/04/16	Enhance function description and correct some features typo.
Pre-1.2	2007/05/11	Remove pins strapping function in LED_P4_2, LED_P3_2, LED_P3_0, LED_P2_2, LED_P0_2, LED_P1_0, and LED_P0_0.
		Change pins name of STESTG0/1/2, STESTL0/1/2, STESTT, STESTH, STESTCKP/N, STESTOP/N, and STESTIP/N to SGND, SVDDL, SVDDT, SVDDH, SDCKP/N, SDTXP/N, and SDRXP/N. Figure 8, Figure 9, Table 2, Table 3, Table 5, and Table 16.
		Add Serdes interface pin description and mode selection in section 6.2 and 9.4.
		Add LED_P4_2/RESERVED pin description for normal operation.
		Add configuration strapping pins description in section 6.6.
		Remove chapter 3 and enhance application example in chapter 4.
		Add 1000Base-X application example circuit in Figure 25.
		Enhance General Purpose Interface description in section 9.3.
		Revise Figure 3, Block Diagram of RTL8366S/SR.
		Revise Applications Block Diagram, Figure 4, Figure 5, Figure 6, and Figure 7.

Pre-1.3	2007/08/03	Change the LED_P4_0/DisBlink description in section 8.20. Use pin floating to disable and pull down to enable power on blinking function.
		Remove the original section 8.12.4.
		Change the description in section 8.12.4, which only insert PVID for untagged or change priority tagged packets to be PVID.
		Correct the configure description in section 6.3. Change the configuration name from SEL_P5MODE[2:0] to SEL_P5MODE[1:0]
Pre-1.4	2007/10/09	Add the Thermal Characteristics in section 11.3
		Add the RGMII/GMII/MII Timing Characteristics in section 11.5.3 and 11.5.4
		Corrected the feature of jumbo frame supporting in section 2
		Corrected the SMI signal description of Figure 1. & Figure 2.
		Corrected “DisBlink” to “EnBlink” in Figure 8, page 22, Figure 9, page 23, Table 2, page 25, Table 3, page 27, Table 11, page 40, Table 13, page 41, and section 8.20, page 61.
		Corrected the default values of Register 0,4, 5, 6,7, 9, 15. in section 10.1, 10.5, 10.6, 10.7, 10.8, 10.10, 10.12.
		Corrected the GMII Pins ”100Mbps” in section 6.3.1, page 30 to ”100Mbps/10Mbps;
		Corrected “DVDDIO1” , “DVDDIO2”to “DVDDIO0”, “DVDDIO1” in section 11.2, page 79.
		Correct the Feature description “One port 1000Base-X Serdes & support UTP/Fiber” to “Port 4 support 1000Base-X Serdes or UTP”
		Combine Table 15 and original Table.12.
		Modified the pin name “SWR_FB”, “En_SWR”, ”VSWN”, “VSWP”, “VPHASE” to “TEST_FB”, “En_TEST”, ”VTESTN”, “VTESTP”, “VPHTEST” in Table 15.
		Appended the Driving Ability to Table 4, page 29,30, Table 5, page 30, Table 6, page 31, 32, Table 7, page 33, Table 8, page 33, 34, Table 9, page 35, 36, Table 10, page 37,38, 39, Table 11, page 40, 41 Table 12, page 41, 42, Table 13, page 42, 43.
		Deleted “SWRVDDH,”, “SWRGND” from Table 41.
		Corrected the EEPROM size from 512 bytes to 2048 bytes in section 2, page 15.
		Corrected the priority queue from 6 queues to 4 queues in section 1, page 13, section 2, page 15, section 8.13, page 58, section 8.13.4, page 60.

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1. General Description

The RTL8366S/SR is a 164/216-pin, ultra low power; high-performance 6-port Gigabit Ethernet switch integrates 5-port Giga-PHY that support 1000Base-T, 100Base-T, and 10Base-T. RTL8366S (LQFP-164) uses the smaller package to minimize PCB size and RTL8366SR (LQFP-216) supports more MAC/PHY interfaces for Router and external CPU application. RTL8366S/SR integrates all the functions of a high-speed switch system—including SRAM for packet buffering, non-blocking switch fabric, and internal register management a single 0.13um CMOS device. Only a 25MHz crystal is required; the EEPROM is optional to configure internal registers.

The 5-th port MAC or PHY, and 6-th port MAC of the RTL8366SR implements dual MII/RGMII (or single GMII for 6-th port MAC) interface for connecting with an external PHY or MAC in specific applications. These interfaces could be connected to external CPU or RISC as 5-port Gigabit Router application.

The embedded packet storage SRAM in the RTL8366S/SR features superior memory management technology to efficiently utilize the memory space. The RTL8366S/SR also integrates a 1K entries address look-up table with a 10-bit 4-way XOR Hashing algorithm for address searching and learning. Auto aging of each entry is provided and the aging time is around 200-400 seconds. 8 Filtering Database are used to provide Independent VLAN Learning and Shared VLAN Learning (IVL/SVL) function.

The RTL8366S/SR supports standard 802.3x flow control frames for full duplex and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources, including the packet buffers and transmitting queues. The RTL8366S/SR supports broadcast/multicast output dropping method, which will forward broadcast/multicast packets to the non-blocked ports only. For the increasing IP multicast application, the RTL8366S/SR supports IPv4 IGMPv1/v2/v3 and IPv6 MLDv1/v2 snooping.

In order to support flexible traffic classification, RTL8366S/SR supports 32-entry ACL rule and multiple actions option. Each port can optional to enable or disable ACL rule check function. ACL rule key can base on packet ingress port, destination/source MAC address, 802.1q VID, 802.1q PRI, EtherType field, destination/source IP address, destination/source port number (TCP and UDP), ICMP, and IGMP. When ACL rule matches, action configuration can choose to Drop/Permit/Redirect/Mirror, change priority value in 802.1q/Q tag, and rate policing. The rate policing mechanism supports 64kbps step up to 1Gbps rate.

In Bridge operation, RTL8366S/SR supports 8 sets (based on Filtering Database) configurable port status: disable, block, learning, and forwarding for Spanning Tree Protocol and Multiple Spanning Tree Protocol. To meet the security and management application, RTL8366S/SR supports IEEE 802.1x Port-based/MAC-based Access Control. For those ports that do not pass the IEEE802.1x authentication, RTL8366S/SR also provides Port-based/MAC-based Guest VLAN function for them to access limited network resource. 1 set Port Mirroring function is configured to reflect the traffic appearing on another

one of switch's port RX, or TX, or both. It also supports many RFC MIBs Counters on each port for easy debug and diagnostic.

To improve real-time or multimedia networking applications, the RTL8366S/SR supports four priority-assignment for each received packet. These are based on (1) Port based priority; (2) 802.1p/Q VLAN tag priority; (3) DSCP field in IPv4/IPv6 header; and (4) ACL-assigned priority. Each output port supports a weighted ratio of four priority queues to fit bandwidth requirements in different applications. Input bandwidth control function helps user to limit per-port traffic utilization. There are 2 leaky buckets for each queue of all ports, one for Average packet rate and the other for Peak packet rate control. Queues scheduling algorithm can use Strict Priority (SP) or Weighted Fair Queue (WFQ) or mixed.

The RTL8366S/SR provides 4K entries VLAN table for 802.1Q Port-based, Tag-based, and Protocol-based VLAN operation to separate logical connectivity from physical connectivity. RTL8366S/SR supports 4 sets Protocol-based VLAN configuration, which can optional select EtherType, LLC, and RFC1042 as search key. Each port may be set to any topology via EEPROM upon reset or EEPROM SMI Slave interface after reset. The RTL8366S/SR also provides options to meet special VLAN application requirements. The first option is the ARP VLAN function, which is used to select to broadcast ARP frames to all VLANs or only forward ARP frames to the original VLAN. The second option is the Leaky VLAN function, which is used to select to send unicast frames to other VLANs or only forward unicast frames to the original VLAN. The VLAN tags can be inserted or removed on a per port basis.

In router applications, the router may want to know which input port of the incoming packet. The RTL8366S/SR supports an option to insert VLAN tag with VID = Port VID (PVID) on each egress port. The RTL8366S/SR also provides an option to admit VLAN tagged packet with a specific PVID only. If this function is enabled, RTL8366S/SR will drop all non-tagged packets and packets with an incorrect PVID.

2. Features

- Single Chip 6 ports gigabit non-blocking switch architecture
  - Embedded 5 ports 10/100/1000Base-T PHY
- Each port supports full duplex 10/100/1000M connectivity (half duplex only supported in 10/100M mode)
- IEEE 802.3x flow control with asymmetric flow control ability
- 832Kbits SRAM for packet buffer
- Supports maximum packet length 16K bytes jumbo frame packet forwarding and 9216 bytes with wire speed
- Supports RealTek Cable Testing (RTCT) Feature
- Extra Interface (5-th port MAC or PHY, and 6-th port MAC) supports (only for RTL8366SR)
  - Media Independent Interface (MII)
  - Gigabit Media Independent Interface (GMII)
  - Reduced Gigabit Media Independent Interface (RGMII)
  - Port 4 support 1000Base-X Serdes or UTP
- Support 32-entry ACL Rules
  - Search keys support Source Port, MAC, TCP, UDP, IPv4, IPv6, ICMP, and IGMP format
  - Actions support mirror, redirect, dropping, priority adjustment, and traffic rate policing
  - Per-port can optional to enable/disable ACL function and set default action when ACL mismatch
- VLAN
  - 802.1Q VLAN supports for 4096 entries
  - Supports Port-based, Tag-based, and Protocol-based VLAN
  - Up to 4 Protocol-based VLAN entries
  - Supports per-port per-VLAN egress VLAN tagging and un-tagging
- Supports SVL and IVL/SVL
  - Supports 1K MAC Address with 4-way hash algorithm
  - Supports 8 entries CAM to avoid learning hash collision
  - Up to 8 Filtering Database
- Supports Spanning Tree port status behavior configuration
  - IEEE 802.1w Rapid Spanning Tree
  - IEEE 802.1s Multiple Spanning Tree with up to 8 Spanning Tree Instances
- Supports IEEE 802.1x Access Control Protocol
  - Port-Based Access Control
  - MAC-Based Access Control
  - Guest VLAN

- Supports Quality of Service (QoS)
  - Input Bandwidth Control from 64Kbps to 1Gbps with 64Kbps step
  - Four Priority Queues per port
  - Per-port per-queue Average and Peak Packet Rate control
  - Scheduling supports Strict Priority (SP) and Weighted Fair Queue (WFQ)
  - IEEE 802.1p/Q and IPv4 DSCP Remarking
  - Priority decision base on Port, 802.1Q VLAN tag PRI, IPv4/IPv6 DSCP, and ACL rule
- Support RFC MIB Counter
  - MIB-II (RFC 1213)
  - Ethernet-Like MIB (RFC 3635)
  - Interface Group MIB (RFC 2863)
  - RMON (RFC 2819)
  - Bridge MIB (RFC 1493)
  - Bridge MIB Extension (RFC 2674)
- Security Filtering
  - Disable learning for each port
  - Disable learning-table aging for each port
  - Drop unknown DA for each port
- Broadcast/Multicast/Unknown DA storm control protects system from attack by hackers
- Supports each port 3 parallel LEDs
- Supports EEPROM SMI Slave interface to access configuration register
- Supports 2048 bytes EEPROM space for configuration
- 25MHz crystal or 3.3V OSC input
- Support 1 interrupt output to external CPU for notification
- Low Power consumption < 500mW/port
- 0.13µm CMOS process
  - RTL83666S: LQFP 164-pin E-PAD package
  - RTL8366SR: LQFP 216-pin E-PAD package

3. Block Diagram

3.1. Block Diagram of RTL8366S/SR

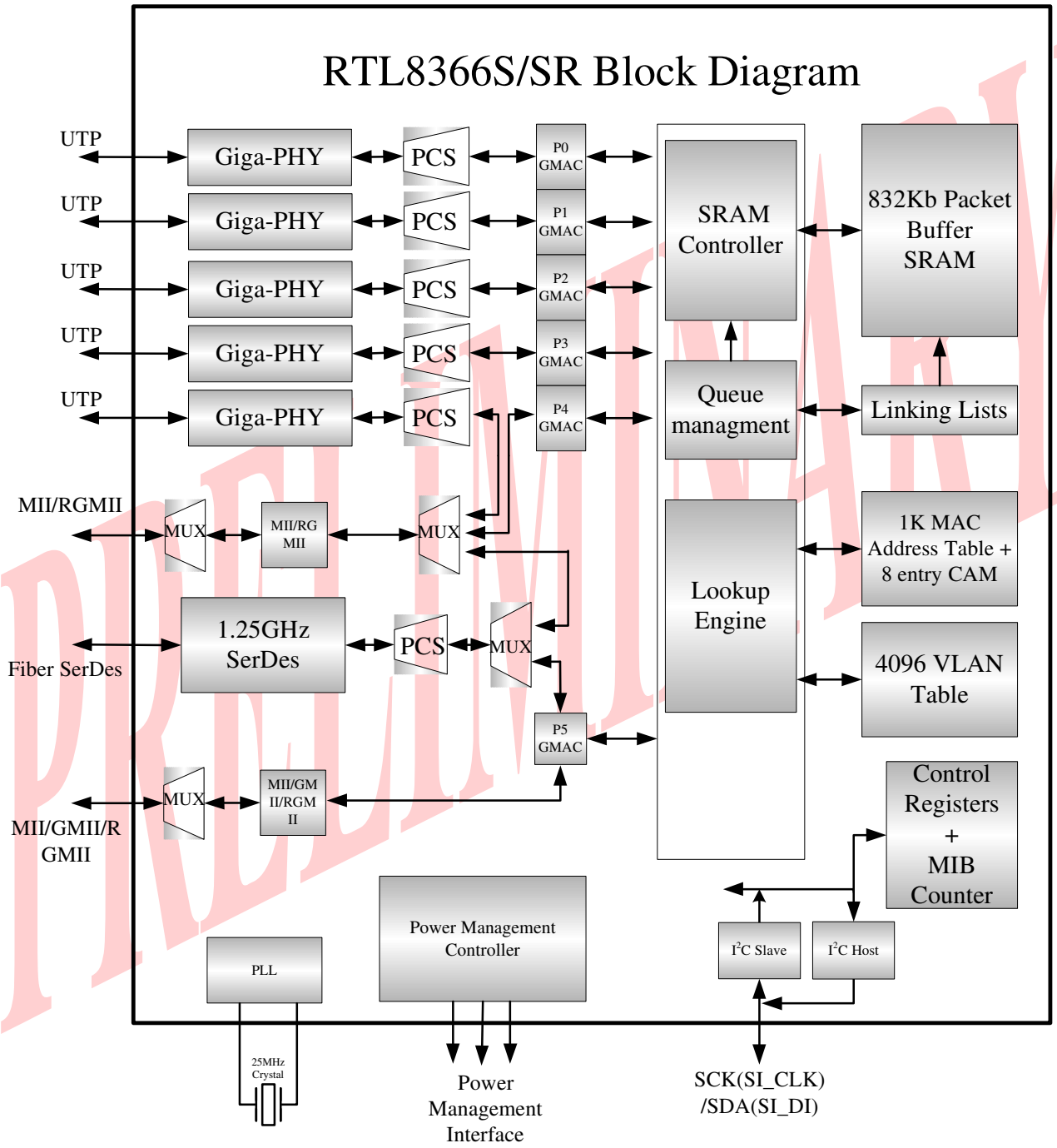


Figure 3. Block Diagram of RTL8366S/SR

4. Applications

4.1. 5 port 1000Base-T Switch

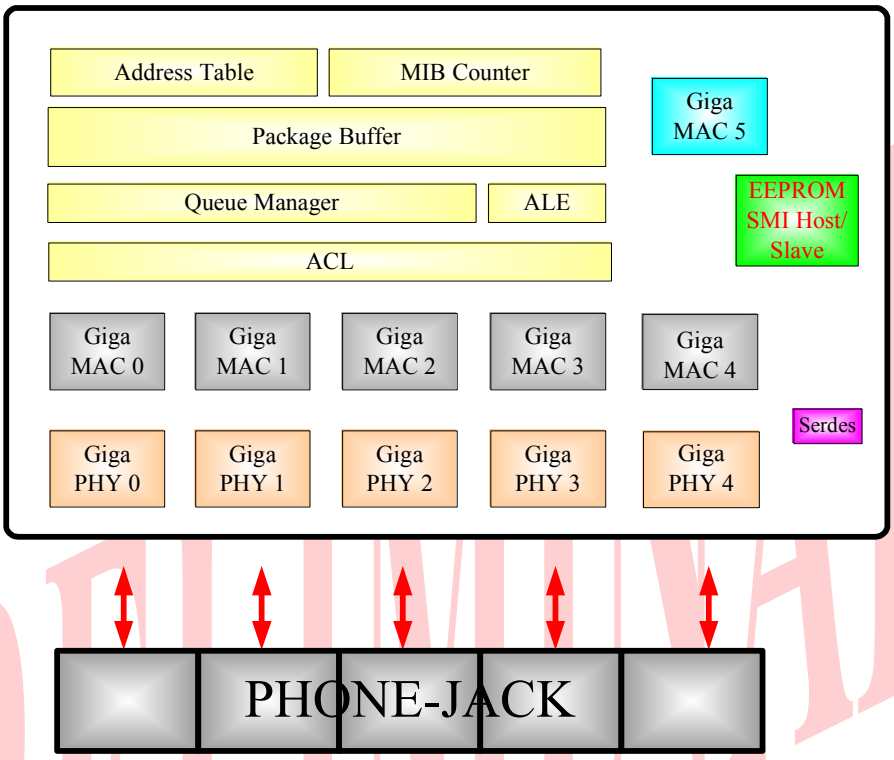


Figure 4. 5-Port 1000Base-T Switch

4.2. 5-Port 1000Base-T Switch, 5th Port Support 1000Base-T/1000Base-X

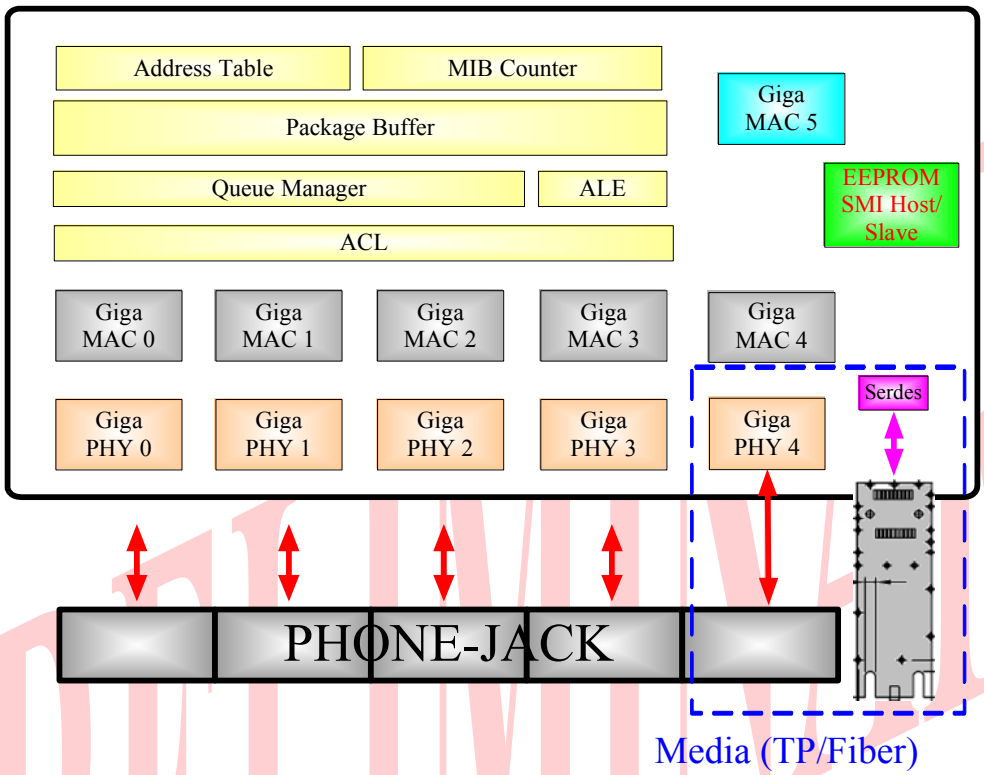


Figure 5. 5-Port 1000Base-T Switch, Port 4 with 1000Base-T/1000Base-X

4.3. 5 port 1000Base-T Router with Dual MII/RGMII

4.3.1. Port 5 MAC and Port 4 PHY in MII/RGMII Mode

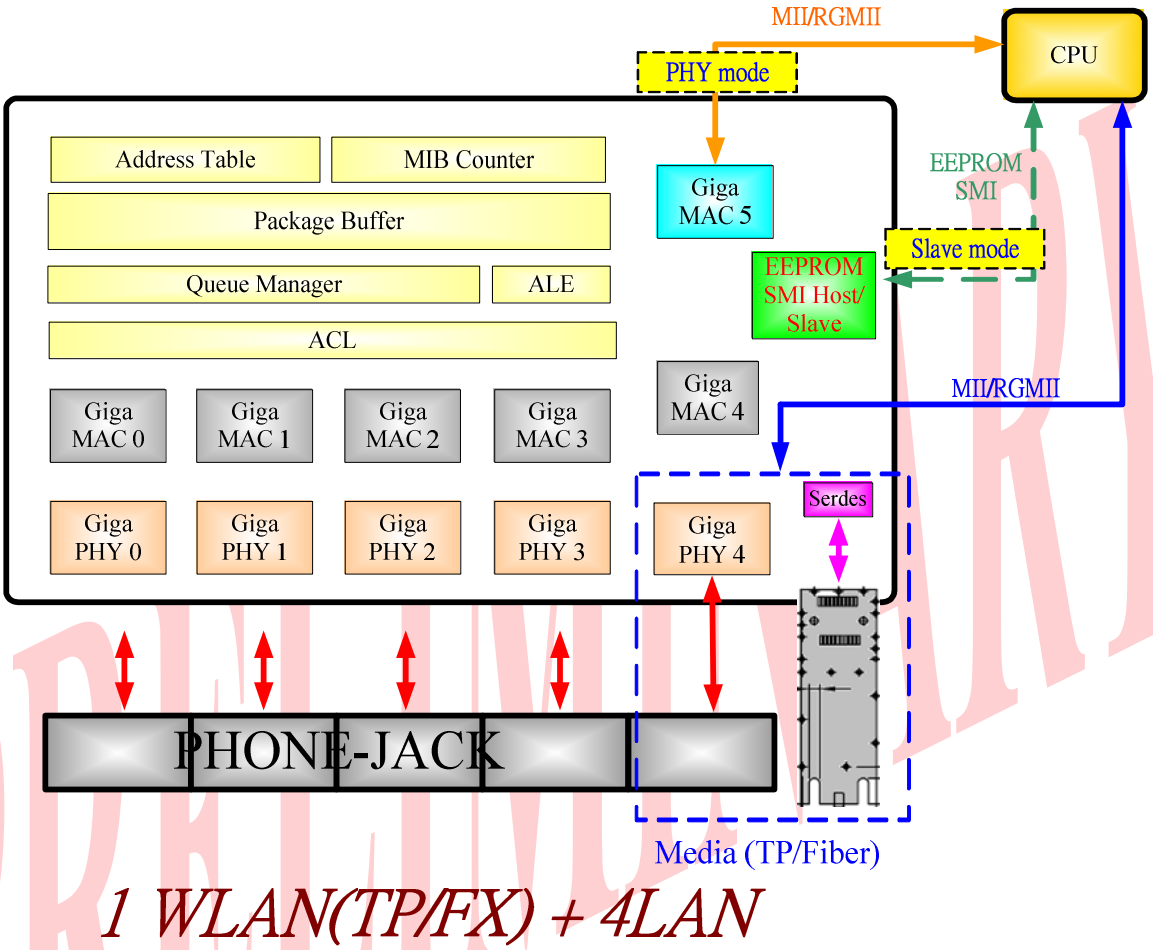


Figure 6. 5-Port 1000Base-T Router with dual MII/RGMII interface

4.4. 5 port 1000Base-T Router with One GMII (One Arm Router)

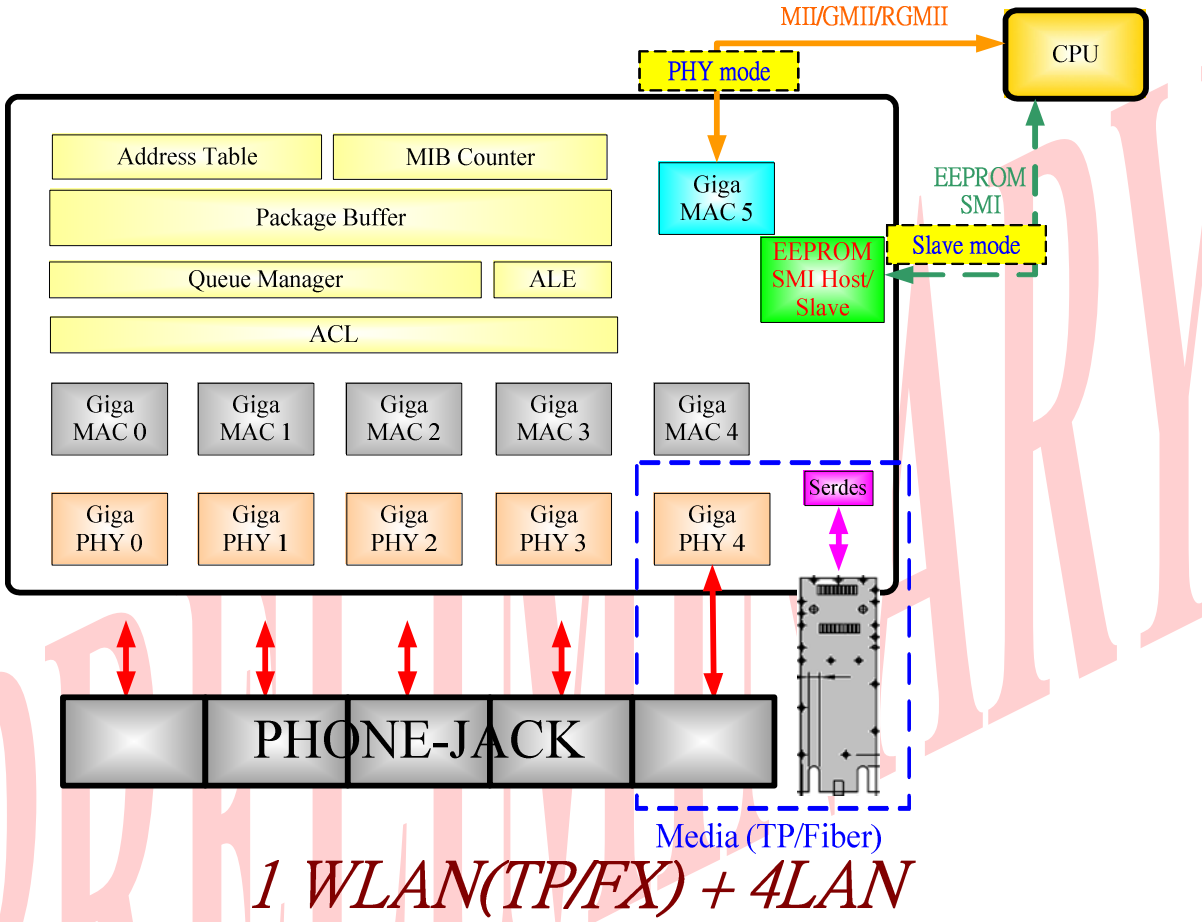


Figure 7. 5-Port 1000Base-T Router with One GMII interface (One Arm Router)

5. Pin Assignments

5.1. RTL8366S Pin Assignments (LQFP164)

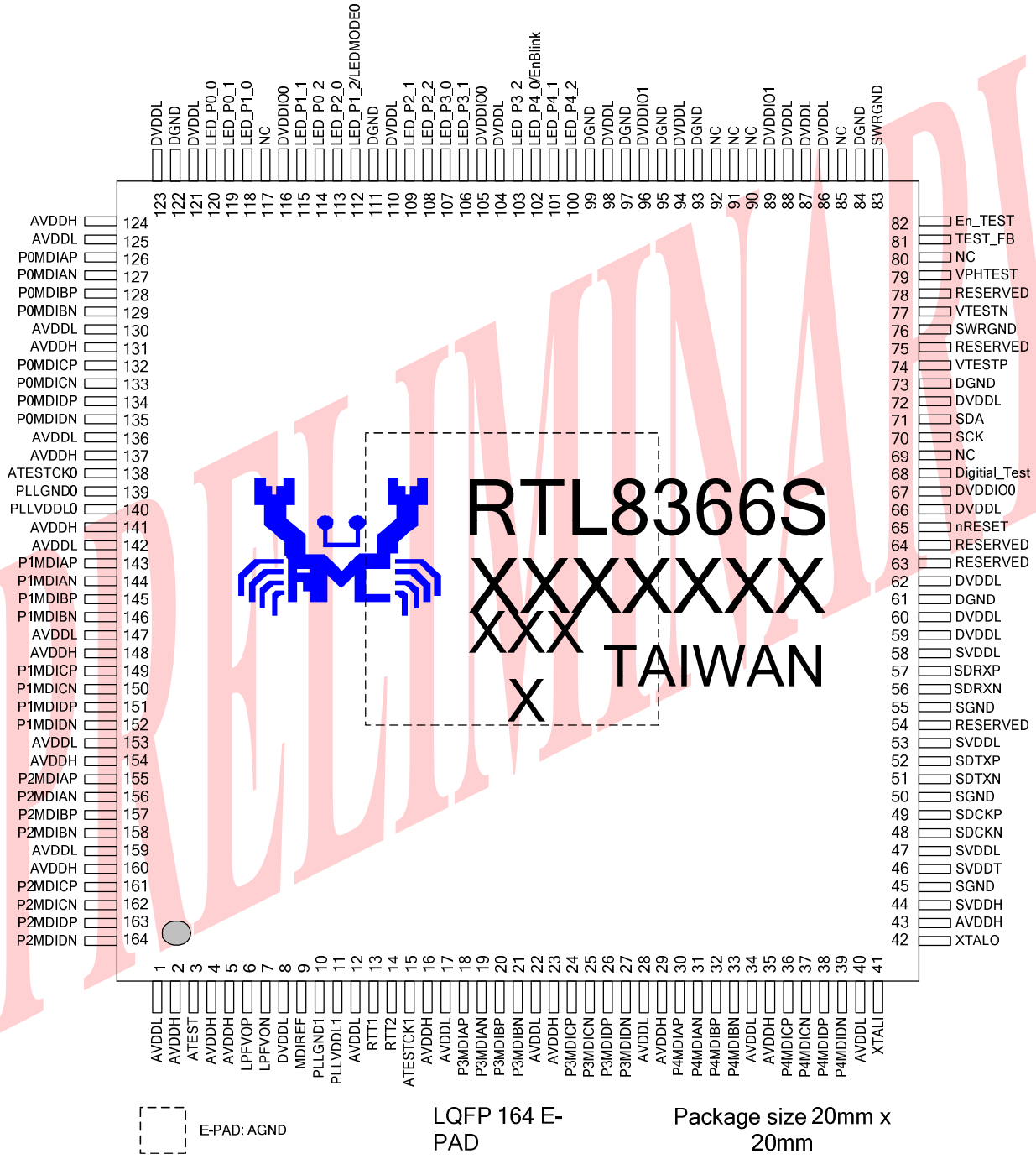


Figure 8. RTL8366S LQFP-164 Pin Assignments

5.2. RTL8366SR Pin Assignments (LQFP216)

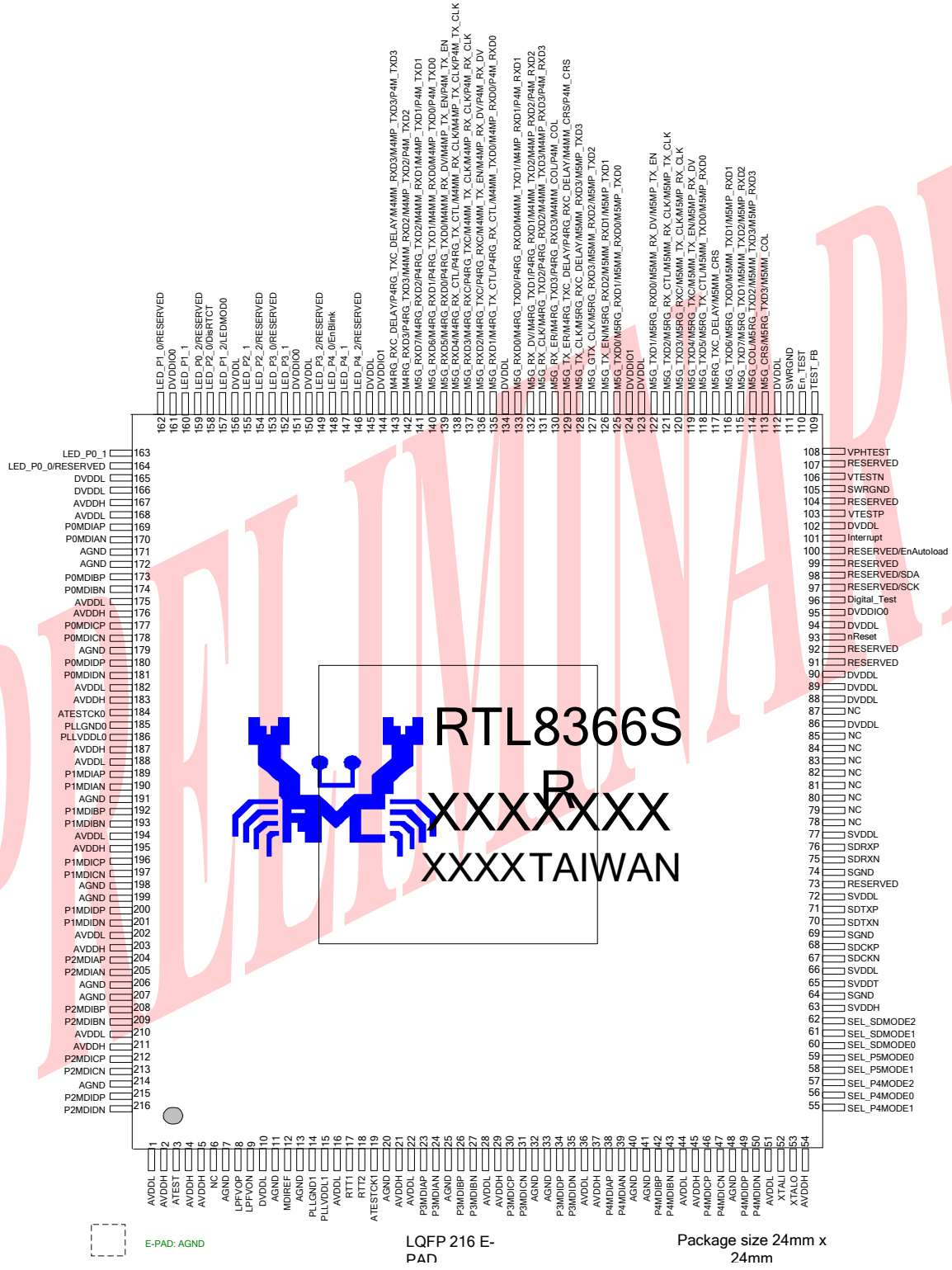


Figure 9. RTL8366SR LQFP-216 Pin Assignments

5.3. *Pin Assignment Table*

5.3.1. Pin Type Conventions

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

Table 1. Pin Types Table

Types	Description
I	Input pin
O	Output pin
I/O	Bi-direction input/output pin
A	Analog pin
AI	Analog input pin
AO	Analog output pin
AI/O	Analog Bi-direction input/output pin
P	Digital power pin
G	Digital ground pin
AP	Analog power pin
AG	Analog ground pin
I_{PD}	Input pin with pull-down resistor
I_{PU}	Input pin with pull-up resistor; (Typical value = 75K Ohm)
O_{OD}	Output pin with open drain
O_{3S}	Output pin with tri-state

5.3.2. RTL8366S (LQFP164) Pin Assignment Table

Table 2. Pin Assignment Table (LQFP 164)

Name	Pin No.	Type	Name	Pin No.	Type
AVDDL	1	AP	SWRGND	83	AG
AVDDH	2	AP	DGND	84	G
ATEST	3	AO	NC	85	
AVDDH	4	AP	DVDDL	86	P
AVDDH	5	AP	DVDDL	87	P
LPFVOP	6	AO	DVDDL	88	P
LPFVON	7	AO	DVDDIO1	89	P
DVDDL	8	P	NC	90	
MDIREF	9	AO	NC	91	
PLLGND1	10	AG	NC	92	
PLLVDDL1	11	AP	DGND	93	G
AVDDL	12	AP	DVDDL	94	P
RTT1	13	AO	DGND	95	G
RTT2	14	AO	DVDDIO1	96	P
ATESTCK1	15	AO	DGND	97	G
AVDDH	16	AP	DVDDL	98	P
AVDDL	17	AP	DGND	99	G
P3MDIAP	18	AI/O	LED_P4_2	100	I/OPU
P3MDIAN	19	AI/O	LED_P4_1	101	I/OPU
P3MDIBP	20	AI/O	LED_P4_0/EnBlink	102	I/OPU
P3MDIBN	21	AI/O	LED_P3_2	103	I/OPU
AVDDL	22	AP	DVDDL	104	P
AVDDH	23	AP	DVDDIO0	105	P
P3MDICP	24	AI/O	LED_P3_1	106	I/OPU
P3MDICN	25	AI/O	LED_P3_0	107	I/OPU
P3MDIDP	26	AI/O	LED_P2_2	108	I/OPU
P3MDIDN	27	AI/O	LED_P2_1	109	I/OPU
AVDDL	28	AP	DVDDL	110	P
AVDDH	29	AP	DGND	111	G
P4MDIAP	30	AI/O	LED_P1_2/LEDMODE0	112	I/OPU
P4MDIAN	31	AI/O	LED_P2_0	113	I/OPU
P4MDIBP	32	AI/O	LED_P0_2	114	I/OPU
P4MDIBN	33	AI/O	LED_P1_1	115	I/OPU
AVDDL	34	AP	DVDDIO0	116	P
AVDDH	35	AP	NC	117	
P4MDICP	36	AI/O	LED_P1_0	118	I/OPU
P4MDICN	37	AI/O	LED_P0_1	119	I/OPU
P4MDIDP	38	AI/O	LED_P0_0	120	I/OPU
P4MDIDN	39	AI/O	DVDDL	121	P
AVDDL	40	AP	DGND	122	G
XTALI	41	AI	DVDDL	123	P
XTALO	42	AO	AVDDH	124	AP
AVDDH	43	AP	AVDDL	125	AP
SVDDH	44	AP	P0MDIAP	126	AI/O
SGND	45	AG	P0MDIAN	127	AI/O
SVDDT	46	AP	P0MDIBP	128	AI/O
SVDDL	47	AP	P0MDIBN	129	AI/O
SDCKN	48	AO	AVDDL	130	AP
SDCKP	49	AO	AVDDH	131	AP
SGND	50	AG	P0MDICP	132	AI/O
SDTXN	51	AO	P0MDICN	133	AI/O
SDTXP	52	AO	P0MDIDP	134	AI/O
SVDDL	53	AP	P0MDIDN	135	AI/O
SCKIN	54	AI	AVDDL	136	AP
SGND	55	AG	AVDDH	137	AP
SDRXN	56	AI	ATESTCK0	138	AO
SDRXP	57	AI	PLLGND0	139	AG
SVDDL	58	AP	PLLVDDL0	140	AP
DVDDL	59	P	AVDDH	141	AP

Name	Pin No.	Type	Name	Pin No.	Type
DVDDL	60	P	AVDDL	142	AP
DGND	61	G	P1MDIAP	143	AI/O
DVDDL	62	P	P1MDIAN	144	AI/O
RESERVED	63	O	P1MDIBP	145	AI/O
RESERVED	64	I/OPU	P1MDIBN	146	AI/O
nRESET	65	IPU	AVDDL	147	AP
DVDDL	66	P	AVDDH	148	AP
DVDDIO0	67	P	P1MDICP	149	AI/O
Digitial_Test	68	IPU	P1MDICN	150	AI/O
NC	69		P1MDIDP	151	AI/O
SCK	70	IPU	P1MDIDN	152	AI/O
SDA	71	I/OPU	AVDDL	153	AP
DVDDL	72	P	AVDDH	154	AP
DGND	73	G	P2MDIAP	155	AI/O
VTESTP	74	AO	P2MDIAN	156	AI/O
RESERVED	75	AP	P2MDIBP	157	AI/O
SWRGND	76	AG	P2MDIBN	158	AI/O
VTESTN	77	AO	AVDDL	159	AP
RESERVED	78	AP	AVDDH	160	AP
VPHTEST	79	AI	P2MDICP	161	AI/O
NC	80		P2MDICN	162	AI/O
TEST_FB	81	AI	P2MDIDP	163	AI/O
En_TEST	82	AIPU	P2MDIDN	164	AI/O

5.3.3. RTL8366SR (LQFP216) Pin Assignment Table

Table 3. Pin Assignment Table (LQFP 216)

Name	Pin No.	Type	Name	Pin No.	Type
AVDDL	1	AP	TEST_FB	109	AI
AVDDH	2	AP	En_TEST	110	AI_{PU}
ATEST	3	AO	SWRGND	111	AG
AVDDH	4	AP	DVDDL	112	P
AVDDH	5	AP	M5G_CRS/ M5RG_TXD3	113	I/O
NC	6		/ M5MM_COL		
AGND	7	AP	M5G_COL	114	I/O
LPFVOP	8	AO	/ M5RG_TXD2		
LPFVON	9	AO	/ M5MM_TXD3 / M5MP_RXD3		
DVDDL	10	P	M5G_TXD7 / M5RG_TXD1	115	O
AGND	11	AG	/ M5MM_TXD2 / M5MP_RXD2		
MDIREF	12	AO	M5G_TXD6	116	O
AGND	13	AG	/ M5RG_TXD0		
PLLGND1	14	AG	/ M5MM_TXD1 / M5MP_RXD1		
PLLVDDL1	15	AP	M5RG_TXC_DELAY / M5MM_CRS	117	I
AVDDL	16	AP	M5G_TXD5	118	O
RTT1	17	AO	/ M5RG_TX_CTL / M5MM_TXD0		
RTT2	18	AO	/ M5MP_RXD0		
ATESTCK1	19	AO	M5G_TXD4/M5RG_TXC	119	O
AGND	20	AG	/ M5MM_TX_EN/M5MP_RX_DV		
AVDDH	21	AP	M5G_TXD3 / M5RG_RXC	120	I/O
AVDDL	22	AP	/ M5MM_TX_CLK / M5MP_RX_CLK		
P3MDIAP	23	AI/O	M5G_TXD2 / M5RG_RX_CTL	121	I/O
P3MDIAN	24	AI/O	/ M5MM_RX_CLK / M5MP_TX_CLK		
AGND	25	AG	M5G_TXD1 / M5RG_RXD0	122	I/O
P3MDIBP	26	AI/O	/ M5MM_RX_DV / M5MP_TX_EN		
P3MDIBN	27	AI/O	DVDDL	123	P
AVDDL	28	AP	DVDDIO1	124	P
AVDDH	29	AP	M5G_TXD0	125	I/O
P3MDICP	30	AI/O	/ M5RG_RXD1 / M5MM_RXD0		
P3MDICN	31	AI/O	/ M5MP_TXD0		
AGND	32	AG	M5G_TX_EN	126	I/O
AGND	33	AG	/ M5RG_RXD2 / M5MM_RXD1		
P3MDIDP	34	AI/O	/ M5MP_TXD1		
P3MDIDN	35	AI/O	M5G_GTX_CLK	127	I/O
AVDDL	36	AP	/ M5RG_RXD3 / M5MM_RXD2		
AVDDH	37	AP	/ M5MP_TXD2		
P4MDIAP	38	AI/O	M5G_TX_CLK	128	I/O_{PU}
P4MDIAN	39	AI/O	/ M5RG_RXC_DELAY / M5MM_RXD3		
AGND	40	AG	/ M5MP_TXD3		
AGND	41	AG	M5G_TX_ER	129	I/O_{PU}
P4MDIBP	42	AI/O	/ M4RG_TXC_DELAY		
P4MDIBN	43	AI/O	/ P4RG_RXC_DELAY / M4MM_CRS		
AVDDL	44	AP	/ P4M_CRS		
AVDDH	45	AP	M5G_RX_ER	130	I/O
P4MDICP	46	AI/O	/ M4RG_TXD3 / P4RG_RXD3		
P4MDICN	47	AI/O	/ M4MM_COL / P4M_COL		
AGND	48	AG	M5G_RX_CLK	131	I/O
P4MDIDP	49	AI/O	/ M4RG_TXD2		
P4MDIDN	50	AI/O	/ P4RG_RXD2 / M4MM_TXD3		
AVDDL	51	AP	/ M4MP_RXD3 / P4M_RXD3		
XTALI	52	AI	M5G_RX_DV	132	I/O
XTALO	53	AO	/ M4RG_TXD1 / P4RG_RXD1		
AVDDH	54	AP	/ M4MM_TXD2 / M4MP_RXD2		
SEL_P4MODE1	55	I_{PU}	/ P4M_RXD2		
SEL_P4MODE0	56	I_{PU}	M5G_RXD0	133	I/O
SEL_P4MODE2	57	I_{PU}	/ M4RG_TXD0		
SEL_P5MODE1	58	I_{PU}	/ P4RG_RXD0 / M4MM_TXD1		
SEL_P5MODE0	59	I_{PU}	/ M4MP_RXD1 / P4M_RXD1		

Name	Pin No.	Type	Name	Pin No.	Type
SEL_SDMODE0	60	I_{PU}	DVDDL	134	P
SEL_SDMODE1	61	I_{PU}	M5G_RXD1	135	I/O
SEL_SDMODE2	62	I_{PU}	/ M4RG_TX_CTL		
SVDDH	63	AP	/ P4RG_RX_CTL / M4MM_TXD0		
SGND	64	AG	/ M4MP_RXD0 / P4M_RXD0		
SVDDT	65	AP	M5G_RXD2 / M4RG_TXC	136	I/O
SVDDL	66	AP	/ P4RG_RXC / M4MM_TX_EN		
SDCKN	67	AO	/ M4MP_RX_DV / P4M_RX_DV		
SDCKP	68	AO	M5G_RXD3 / M4RG_RXC	137	I/O
SGND	69	AG	/ P4RG_TXC / M4MM_TX_CLK		
SDTXN	70	AO	/ M4MP_RX_CLK / P4M_RX_CLK		
SDTXP	71	AO	M5G_RXD4	138	I/O
SVDDL	72	AP	/ M4RG_RX_CTL		
SCKIN	73	AI	/ P4RG_TX_CTL / M4MM_RX_CLK		
SGND	74	AG	/ M4MP_TX_CLK / P4M_TX_CLK		
SDRXN	75	AI	M5G_RXD5 / M4RG_RXD0	139	I
SDRXP	76	AI	/ P4RG_TXD0 / M4MM_RX_DV		
SVDDL	77	AP	/ M4MP_TX_EN / P4M_TX_EN		
NC	78		M5G_RXD6	140	I
NC	79		/ M4RG_RXD1 / P4RG_TXD1		
NC	80		/ M4MM_RXD0 / M4MP_TXD0		
NC	81		/ P4M_TXD0		
NC	82		M5G_RXD7 / M4RG_RXD2	141	I
NC	83		/ P4RG_TXD2 / M4MM_RXD1		
NC	84		/ M4MP_TXD1 / P4M_TXD1		
NC	85		M4RG_RXD3 / P4RG_TXD3	142	I
DVDDL	86	P	/ M4MM_RXD2 / M4MP_TXD2		
NC	87		/ P4M_TXD2		
DVDDL	88	P	M4RG_RXC_DELAY	143	I
DVDDL	89	P	/ P4RG_TXC_DELAY		
DVDDL	90	P	/ M4MM_RXD3 / M4MP_TXD3		
RESERVED	91	O	/P4M_TXD3		
RESERVED	92	I/O_{PU}	DVDDIO1	144	P
nReset	93	I_{PU}	DVDDL	145	P
DVDDL	94	P	LED_P4_2 / RESERVED	146	I/O_{PU}
DVDDIO0	95	P	LED_P4_1	147	I/O_{PU}
Digital_Test	96	I_{PU}	LED_P4_0 / EnBlink	148	I/O_{PU}
RESERVED / SCK	97	I_{PU}	LED_P3_2 / RESERVED	149	I/O_{PU}
RESERVED / SDA	98	I/O_{PU}	DVDDL	150	P
RESERVED	99	O	DVDDIO0	151	P
RESERVED / EnAutoload	100	I	LED_P3_1	152	I/O_{PU}
Interrupt	101	O	LED_P3_0 / RESERVED	153	I/O_{PU}
DVDDL	102	P	LED_P2_2 / RESERVED	154	I/O_{PU}
VTESTP	103	AO	LED_P2_1	155	I/O_{PU}
RESERVED	104	AP	DVDDL	156	P
SWRGND	105	AG	LED_P1_2 / LEDMOD0	157	I/O_{PU}
VTESTN	106	AO	LED_P2_0	158	I/O_{PU}
RESERVED	107	AP	LED_P0_2 / RESERVED	159	I/O_{PU}
VPHTEST	108	AI	LED_P1_1	160	I/O_{PU}
			DVDDIO0	161	P
			LED_P1_0 / RESERVED	162	I/O_{PU}
			LED_P0_1	163	I/O_{PU}
			LED_P0_0 / RESERVED	164	I/O_{PU}
			DVDDL	165	P
			DVDDL	166	P
			AVDDH	167	AP
			AVDDL	168	AP
			P0MDIAP	169	AI/O
			P0MDIAN	170	AI/O
			AGND	171	AG
			AGND	172	AG
			P0MDIBP	173	AI/O
			P0MDIBN	174	AI/O
			AVDDL	175	AP
			AVDDH	176	AP

Name	Pin No.	Type	Name	Pin No.	Type
			P0MDICP	177	AI/O
			P0MDICN	178	AI/O
			AGND	179	AG
			P0MDIDP	180	AI/O
			P0MDIDN	181	AI/O
			AVDDL	182	AP
			AVDDH	183	AP
			ATESTCK0	184	AO
			PLLGND0	185	AG
			PLLVDDL0	186	AP
			AVDDH	187	AP
			AVDDL	188	AP
			P1MDIAP	189	AI/O
			P1MDIAN	190	AI/O
			AGND	191	AG
			P1MDIBP	192	AI/O
			P1MDIBN	193	AI/O
			AVDDL	194	AP
			AVDDH	195	AP
			P1MDICP	196	AI/O
			P1MDICN	197	AI/O
			AGND	198	AG
			AGND	199	AG
			P1MDIDP	200	AI/O
			P1MDIDN	201	AI/O
			AVDDL	202	AP
			AVDDH	203	AP
			P2MDIAP	204	AI/O
			P2MDIAN	205	AI/O
			AGND	206	AG
			AGND	207	AG
			P2MDIBP	208	AI/O
			P2MDIBN	209	AI/O
			AVDDL	210	AP
			AVDDH	211	AP
			P2MDICP	212	AI/O
			P2MDICN	213	AI/O
			AGND	214	AG
			P2MDIDP	215	AI/O
			P2MDIDN	216	AI/O

6. Pin Descriptions

6.1. Media Dependent Interface Pins

Table 4. MDI Pins

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQFP 164	LQFP 216			
P0MDIAP/N	126 127	169 170	AI/O	10	**Port 0 Media Dependent Interface A~D.** For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pair has an internal 100 Ohm termination resistor.
P0MDIBP/N	128 129	173 174			
P0MDICP/N	132 133	177 178			
P0MDIDP/N	134 135	180 181			
P1MDIAP/N	143 144	189 190	AI/O	10	**Port 1 Media Dependent Interface A~D.** For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pair has an internal 100 Ohm termination resistor.
P1MDIBP/N	145 146	192 193			
P1MDICP/N	149 150	196 197			
P1MDIDP/N	151 152	200 201			
P2MDIAP/N	155 156	204 205	AI/O	10	**Port 2 Media Dependent Interface A~D.** For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pair has an internal 100 Ohm termination resistor.
P2MDIBP/N	157 158	208 209			
P2MDICP/N	161 162	212 213			
P2MDIDP/N	163 164	215 216			
P3MDIAP/N	18 19	23 24	AI/O	10	**Port 3 Media Dependent Interface A~D.** For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pair has an internal 100 Ohm termination resistor.
P3MDIBP/N	20 21	26 27			
P3MDICP/N	24 25	30 31			
P3MDIDP/N	26 27	34 35			

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQFP 164	LQFP 216			
P4MDIAP/N	30	38	AI/O	10	**Port 4 Media Dependent Interface A~D.** For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pair has an internal 100 Ohm termination resistor.
	31	39			
P4MDIBP/N	32	42			
	33	43			
P4MDICP/N	36	46			
	37	47			
P4MDIDP/N	38	49			
	39	50			

6.2. Serdes Interface Pins

Serdes Interfaces provides one port Fiber interface. The interface is selected by the pulling up or down of **SEL_SDMODE[1:0]** pins upon power on.

6.2.1. Fiber Serdes Pins

Table 5. Fiber Serdes Pins

Pin Name	Pin No.		Type	Description
	LQFP 164	LQFP 216		
SDRXP/N	57	76	AI	**Fiber Serdes Differential Input:** 1.25GHz serial interfaces to receive data from an External O/E module.
	56	75		
SDTXP/N	52	71	AO	**Fiber Serdes Differential Output:** 1.25GHz serial interfaces to transfer data to an External O/E module.
	51	70		
SDCKP/N	49	68	AO	Reserved for future used.
	48	67		
SCKIN	54	73	AI	25MHz clock Input.

6.3. General Purpose Interfaces (Only for RTL8366SR)

RTL8366SR (LQFP-216) supports General Purpose Interfaces including GMII MAC, GMII PHY, RGMII MAC RGMII PHY, MII MAC, and MII PHY interfaces. The interfaces are selected by the pulling up or down **SEL_P4MODE[2:0]** and **SEL_P5MODE[1:0]** pins upon power on. Interface selection may also be configured by register access after power on.

6.3.1. GMII Pins

When Port 5 MAC is linked at 1Gbps, the interface will be GMII. When Port 5 MAC is linked at 100Mbps/10Mbps, the interface will be MII. 1Gbps Half Duplex is not supported in this configuration.

Table 6. GMII Pins (MAC5 GMII, pins)

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQFP164	LQFP216			
M5G_CRS	N/A	113	I/O	8	**M5G_CRS** Carrier Sense Input when MAC5 GMII interface operation on 10/100 MII half duplex mode. M5G_CRS is only valid in 10/100Mbps MII half duplex mode. It is asserted high when a valid carrier is detected on the media. This pin must be pulled low with 1K Ohm resistor when not used.
M5G_COL	N/A	114	I/O	8	**M5G_COL** Collision Detect Input when MAC5 GMII interface operation on 10/100 MII half duplex mode. M5G_COL is only valid in 10/100Mbps MII half duplex mode. It is asserted high when a collision is detected on the media. This pin must be pulled low with 1K Ohm resistor when not used.
M5G_TXD[7:0]	N/A	115 116 118 119 120 121 122 125	O	8	**M5G_TXD[7:0]** MAC5 GMII Transmit Data Output. Transmits data bus that is sent synchronously at the rising edge of M5G_GTX_CLK. In 10/100Mbps MII mode, only M5G_TXD[3:0] are available and synchronously at the rising edge of M5G_TX_CLK.
M5G_TX_EN	N/A	126	O	8	**M5G_TX_EN** MAC5 GMII Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of M5G_GTX_CLK in GMII mode. Transmit enable that is sent synchronously at the rising edge of M5G_TX_CLK in 10/100Mbps MII mode.
M5G_GTX_CLK	N/A	127	O	8	**M5G_GTX_CLK** MAC5 GMII Transmit Clock Output. 125MHz transmit clock output when GMII is operating at 1Gbps. Used to synchronize M5G_TXD[7:0], M5G_TX_EN, and M5G_TX_ER.

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQFP164	LQFP216			
M5G_TX_CLK	N/A	128	I/O_{PU}	8	**M5G_TX_CLK** 2.5/25MHz Transmit Clock Input when MAC5 GMII interface operation on 10/100 MII mode. 2.5/25MHz clock driven by PHY when operating in 10/100Mbps MII mode. Used to synchronize M5G_TXD[3:0], M5G_TX_EN, and M5G_TX_ER. This pin must be pulled low with 1K Ohm resistor when not used.
M5G_TX_ER	N/A	129	O_{PU}	8	**M5G_TX_ER** MAC5 GMII Transmit Data Error Output. Indicates that the transmit Data is error.
M5G_RX_ER	N/A	130	I		**M5G_RX_ER** MAC5 GMII Receive Data Error. Indicates that the receiving Data is error. The switch filters the receiving packet once the M5G_RX_ER is asserted at the rising edge of M5G_RX_CLK. Valid both in 1000Mbps GMII mode and 10/100Mbps MII MAC mode. This pin must be pulled low with 1K Ohm resistor when not used.
M5G_RX_CLK	N/A	131	I		**M5G_RX_CLK** MAC5 GMII Receive Clock Input. In GMII mode: 125MHz receive clock. Used to synchronize M5G_RXD[7:0], M5G_RX_ER, and M5G_RX_DV. In MII 10/100Mbps mode. M5G_RXC is 2.5/25MHz. Used to synchronize M5G_RXD[3:0], M5G_RX_ER , M5G_RX_DV, M5G_CRS, and M5G_COL. This pin must be pulled low with 1K Ohm resistor when not used.
M5G_RX_DV	N/A	132	I		**M5G_RX_DV** MAC5 GMII Receive Data Valid Input. Receive data valid that is received synchronously at the rising edge of M5G_RX_CLK in both 1Gbps GMII and 10/100Mbps MII MAC mode. This pin must be pulled low with 1K Ohm resistor when not used.
M5G_RXD[7:0]	N/A	141 140 139 138 137 136 135 133	I		**M5G_RXD[7:0]** MAC5 GMII Receive Data Input. Receive data bus that is received synchronously at the rising edge of M5G_RX_CLK. In 10/100Mbps MII mode, only M5G_RXD[3:0] are available. These pins must be pulled low with 1K Ohm resistor when not used.

6.3.2. RGMII Pins

RTL8366SR could support two RGMII interface when GMII interface is disabled.

Table 7. MAC5 RGMII Pins

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQF P164	LQF P216			
M5RG_TXD[3:0]	N/A	113 114 115 116	O	8	**M5RG_TXD[3:0]** MAC5 RGMII Transmit Data output. Transmits data bus that is sent synchronously to M5RG_TXC.
M5RG_TX_CTL	N/A	118	O	8	**M5RG_TX_CTL** MAC RGMII Transmit Control signal output. The M5RG_TX_CTL indicates MAC5 TX_EN at the rising edge of M5RG_TXC and MAC5 TX_ER at the falling edge of M5RG_TXC. At M5RG_TXC falling edge, M5RG_TX_CTL=MAC5 TX_EN (XOR) MAC5 TX_ER.
M5RG_TXC	N/A	119	O	8	**M5RG_TXC** MAC5 RGMII Transmit Clock output. M5RG_TXC is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for M5RG_TXD[3:0] and M5RG_TX_CTL synchronization at M5RG_TXC on both rising and falling edges.
M5RG_RXC	N/A	120	I		**M5RG_RXC** MAC5 RGMII Receive Clock input. M5RG_RXC is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for M5RG_RXD[3:0] and M5RG_RX_CTL synchronization at both M5RG_RXC rising and falling edge. This pin must be pulled low with 1K Ohm resistor when not used.
M5RG_RX_CTL	N/A	121	I		**M5RG_RX_CTL** MAC5 RGMII Receive Control signal input. The M5RG_RX_CTL indicates MAC5 RX_DV at the rising of M5RG_RXC and M5RG_RX_ER at the falling edge of M5RG_RXC. At M5RG_RXC falling edge, M5RG_RX_CTL=MAC5 RX_DV (XOR) MAC5 RX_ER. This pin must be pulled low with 1K Ohm resistor when not used.
M5RG_RXD[3:0]	N/A	127 126 125 122	I		**M5RG_RXD[3:0]** MAC5 RGMII Receive Data input. Receive data bus that is received synchronously to M5RG_RXC. These pins must be pulled low with 1K Ohm resistor when not used.

Table 8. Port 4 RGMII Pins (MAC4 or PHY4 RGMII pins)

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQF P164	LQF P216			
M4RG_TXD[3:0] / P4RG_RXD[3:0]	N/A	130 131 132 133	O	12	**M4RG_TXD[3:0]** MAC4 RGMII Transmit Data output. Transmits data bus that is sent synchronously to M4RG_TXC. **P4RG_RXD[3:0]** PHY4 RGMII Receive Data output. Receive data bus that is sent synchronously to P4RG_RXC.
M4RG_TX_CTL / P4RG_RX_CTL	N/A	135	O	12	**M4RG_TX_CTL** MAC4 RGMII Transmit Control signal output. The M4RG_TX_CTL indicates MAC4 TX_EN at the rising edge of M4RG_TXC and MAC4 TX_ER at the falling edge of M4RG_TXC. At M4RG_TXC falling edge, M4RG_TX_CTL=MAC4 TX_EN (XOR) MAC4 TX_ER. **P4RG_RX_CTL** RGMII Receive Control signal output. The P4RG_RX_CTL indicates PHY4 RX_DV at the rising of P4RG_RXC and P4RG_RX_ER at the falling edge of P4RG_RXC. At P4RG_RXC falling edge, P4RG_RX_CTL=PHY4 RX_DV (XOR) PHY4 RX_ER.
M4RG_TXC / P4RG_RXC	N/A	136	O	12	**M4RG_TXC** MAC4 RGMII Transmit Clock output. M4RG_TXC is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for M4RG_TXD[3:0] and M4RG_TX_CTL synchronization at M4RG_TXC on both rising and falling edges. **P4RG_RXC** PHY4 RGMII Receive Clock output. P4RG_RXC is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for P4RG_RXD[3:0] and P4RG_RX_CTL synchronization at P4RG_RXC on both rising and falling edges.
M4RG_RXC / P4RG_TXC	N/A	137	I		**M4RG_RXC** MAC4 RGMII Receive Clock input. M4RG_RXC is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for M4RG_RXD[3:0] and M4RG_RX_CTL synchronization at both M4RG_RXC rising and falling edge. **PHY4TXC** PHY4 RGMII Transmit Clock input. P4RG_TXC is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for P4RG_TXD[3:0] and P4RG_TX_CTL synchronization at both P4RG_TXC rising and falling edge. This pin must be pulled low with 1K Ohm resistor when not used.

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQF P164	LQF P216			
M4RG_RX_CTL / P4RG_TX_CTL	N/A	138	I		**M4RG_RX_CTL** MAC4 RGMII Receive Control signal input. The M4RG_RX_CTL indicates MAC4 RX_DV at the rising of M4RG_RXC and MAC4 RX_ER at the falling edge of M4RG_RXC. At M4RG_RXC falling edge, M4RG_RX_CTL=MAC4 RX_DV (XOR) MAC4 RX_ER. **P4RG_TX_CTL** PHY4 RGMII Transmit Control signal input. The P4RG_TX_CTL indicates PHY4 TX_EN at the rising edge of P4RG_TXC and PHY4 TX_ER at the falling edge of P4RG_TXC. At P4RG_TXC falling edge, P4RG_TX_CTL=PHY4 TX_EN (XOR) PHY4 TX_ER This pin must be pulled low with 1K Ohm resistor when not used.
M4RG_RXD[3:0] / P4RG_TXD[3:0]	N/A	142 141 140 139	I		**M4RG_RXD[3:0]** MAC 4 RGMII Receive Data input. Receive data bus that is received synchronously to M4RG_RXC. **P4RG_TXD[3:0]** PHY4 RGMII Transmit Data input. Transmits data bus that is received synchronously to P4RG_TXC. These pins must be pulled low with 1K Ohm resistor when not used.

6.3.3. MII Interface Pins

The MII interface only supports when GMII interface is disabled.

Table 9. MAC5 MII Pins (MAC5 MII MAC mode or MAC5 MII PHY mode)

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQF P164	LQF P216			
M5MM_COL	N/A	113	I		**M5MM _COL** MAC5 MII MAC mode Collision Detect Input when operation on 10/100 MII half duplex mode. This pin must be pulled low with 1K Ohm resistor when not used.

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQFP164	LQFP216			
M5MM_CRS	N/A	117	I		**M5MM_CRS** MAC5 MII MAC mode Carrier Sense Input when operation on 10/100 MII half duplex mode. This pin must be pulled low with 1K Ohm resistor when not used.
M5MM_TXD[3:0] / M5MP_RXD[3:0]	N/A	114 115 116 118	O	8	**M5MM_TXD[3:0]** MAC5 MII MAC Mode Transmit Data Output. Transmits data bus that is sent synchronously at the rising edge of M5MM_TX_CLK. **M5MP_RXD[3:0]** MAC5 MII PHY Mode Receive Data Output. Receive data bus that is sent synchronously at the rising edge of M5MP_RX_CLK.
M5MM_TX_EN / M5MP_RX_DV	N/A	119	O	8	**M4MM_TX_EN** MAC5 MII MAC Mode Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of M5MM_TX_CLK. **M5MP_RX_DV** MAC5 MII PHY Mode Receive Data Valid Output. Receive Data Valid that is sent synchronously at the rising edge of M5MP_RX_CLK.
M5MM_TX_CLK / M5MP_RX_CLK	N/A	120	I/O	8	**M5MM_TX_CLK** MAC5 MII MAC Mode Transmit Clock Input. In MII 100Mbps, M5MM_TX_CLK is 25MHz clock Input. In MII 10Mbps, M5MM_TX_CLK is 2.5MHz clock Input. Used to synchronize M5MM_TXD[3:0], M5MM_TX_EN, and M5MM_TX_ER. **M5MP_RX_CLK** MAC5 MII PHY Mode Receive Clock Output. In MII 100Mbps, M5MP_RX_CLK is 25MHz clock Output. In MII 10Mbps, M5MP_RX_CLK is 2.5MHz clock Output. Used to synchronize M5MP_RXD[3:0], M5MP_RX_DV, M5MP_RX_ER, M5MP_CRS, and M5MP_COL. This pin must be pulled low with 1K Ohm resistor when not used.

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQFP164	LQFP216			
M5MM_RX_CLK / M5MP_TX_CLK	N/A	121	I/O	8	**M5MM_RX_CLK** MAC5 MII MAC Mode Receive Clock Input. In MII 100Mbps, M5MM_RX_CLK is 25MHz clock Input. In MII 10Mbps, M5MM_RX_CLK is 2.5MHz clock Input. Used to synchronize M5MM_RXD[3:0], M5MM_RX_DV, M5MM_TX_ER , M5MP_CRS, and M5MP_COL. **M5MP_TX_CLK** MAC5 MII PHY Mode Transmit Clock Output. In MII 100Mbps, M5MP_TX_CLK is 25MHz clock Output. In MII 10Mbps, M5MP_TX_CLK is 2.5MHz clock Output. Used to synchronize M5MP_TXD[3:0], M5MP_RX_EN, and M5MP_TX_ER. This pin must be pulled low with 1K Ohm resistor when not used.
M5MM_ RX_DV / M5MP_ TX_EN	N/A	122	I		**M5MM_RX_DV** MAC5 MII MAC Mode Receive Data Valid Input. Receive Data Valid that is received synchronously at the rising edge of M5MM_RX_CLK. **M5MP_TX_EN** MAC5 MII PHY Mode Transmit Data Enable Input. Transmit Data Enable that is received synchronously at the rising edge of M5MP_TX_CLK. This pin must be pulled low with 1K Ohm resistor when not used.
M5MM_RXD[3:0] / M5MP_TXD[3:0]	N/A	128 127 126 125	I		**M5MM_RXD[3:0]** MAC5 MII MAC Mode Receive Data Input. Receive data that is received synchronously at the rising edge of M5MM_RX_CLK. **M5MP_TXD[3:0]** MAC5 MII PHY Mode Transmit Data Input. Transmits data that is received synchronously at the rising edge of M5MP_TX_CLK. These pins must be pulled low with 1K Ohm resistor when not used.

Table 10. Port 4 MII Pins (MAC4 MII MAC mode, MAC4 MII PHY mode, or PHY4 MII pins)

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQFP164	LQFP216			
M4MM _CRS / P4M _CRS	N/A	129	I / O	8	**M4MM_CRS** MAC4 MII MAC mode Carrier Sense Input when operation on 10/100 MII half duplex mode. **P4M_CRS** PHY4 MII Carrier Sense Output. P4M_CRS is only valid in half duplex mode. It is asserted high when a valid carrier is detected on the media. This pin must be pulled low with 1K Ohm resistor when not used.
M4MM _COL / P4M _COL	N/A	130	I / O	8	**M4MM _COL** MAC4 MII MAC mode Collision Detect Input when operation on 10/100 MII half duplex mode. **P4M _COL** PHY4 MII Collision Detect Output. P4M_COL is only valid in half duplex mode. It is asserted high when a collision is detected on the media. This pin must be pulled low with 1K Ohm resistor when not used.
M4MM_TXD[3:0] / M4MP_RXD[3:0] / P4M_RXD[3:0]	N/A	131 132 133 135	O	8	**M4MM_TXD[3:0]** MAC4 MII MAC Mode Transmit Data Output. Transmits data bus that is sent synchronously at the rising edge of M4MM_TX_CLK. **M4MP_RXD[3:0]** MAC4 MII PHY Mode Receive Data Output. Receive data bus that is sent synchronously at the rising edge of M4MP_RX_CLK. **P4M_RXD[3:0]** PHY4 MII Receive Data Output. Receive data bus that is sent synchronously at the rising edge of P4M_RX_CLK.

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQFP164	LQFP216			
M4MM_TX_EN / M4MP_RX_DV / P4M_RX_DV	N/A	136	O	8	**M4MM_TX_EN** MAC4 MII MAC Mode Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of M4MM_TX_CLK. **M4MP_RX_DV** MAC4 MII PHY Mode Receive Data Valid Output. Receive Data Valid that is sent synchronously at the rising edge of M4MP_RX_CLK. **P4M_RX_DV** PHY4 MII Receive Data Valid Output. Receive Data Valid that is sent synchronously at the rising edge of P4M_RX_CLK.
M4MM_TX_CLK / M4MP_RX_CLK / P4M_RX_CLK	N/A	137	I/O	8	**M4MM_TX_CLK** MAC4 MII MAC Mode Transmit Clock Input. In MII 100Mbps, M4MM_TX_CLK is 25MHz clock Input. In MII 10Mbps, M4MM_TX_CLK is 2.5MHz clock Input. Used to synchronize M4MM_TXD[3:0], M4MM_TX_EN, and M4MM_TX_ER. **M4MP_RX_CLK** MAC4 MII PHY Mode Receive Clock Output. In MII 100Mbps, M4MP_RX_CLK is 25MHz clock Output. In MII 10Mbps, M4MP_RX_CLK is 2.5MHz clock Output. Used to synchronize M4MP_RXD[3:0], M4MP_RX_DV, M4MP_RX_ER, M4MP_CRS, and M4MP_COL. **P4M_RX_CLK** PHY4 MII Mode Receive Clock Output. In MII 100Mbps, P4M_RX_CLK is 25MHz clock Output. In MII 10Mbps, P4M_RX_CLK is 2.5MHz clock Output. Used to synchronize P4M_RXD[3:0], P4M_RX_DV, P4M_RX_ER, P4M_CRS, and P4M_COL. This pin must be pulled low with 1K Ohm resistor when not used.

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQF P164	LQF P216			
M4MM_RX_CLK / M4MP_TX_CLK / P4M_TX_CLK	N/A	138	I/O	8	**M4MM_RX_CLK** MAC4 MII MAC Mode Receive Clock Input. In MII 100Mbps, M4MM_RX_CLK is 25MHz clock Input. In MII 10Mbps, M4MM_RX_CLK is 2.5MHz clock Input. Used to synchronize M4MM_RXD[3:0], M4MM_RX_DV, M4MM_TX_ER , M4MP_CRS, and M4MP_COL. **M4MP_TX_CLK** MAC4 MII PHY Mode Transmit Clock Output. In MII 100Mbps, M4MP_TX_CLK is 25MHz clock Output. In MII 10Mbps, M4MP_TX_CLK is 2.5MHz clock Output. Used to synchronize M4MP_TXD[3:0], M4MP_RX_EN, and M4MP_TX_ER. **P4M_TX_CLK** PHY4 MII Mode Transmit Clock Output. In MII 100Mbps, P4M_TX_CLK is 25MHz clock Output. In MII 10Mbps, P4M_TX_CLK is 2.5MHz clock Output. Used to synchronize P4M_TXD[3:0], P4M_TX_EN, and P4M_TX_ER. This pin must be pulled low with 1K Ohm resistor when not used.
M4MM_ RX_DV / M4MP_ TX_EN / P4M_ TX_EN	N/A	139	I		**M4MM_RX_DV** MAC4 MII MAC Mode Receive Data Valid Input. Receive Data Valid that is received synchronously at the rising edge of M4MM_RX_CLK. **M4MP_TX_EN** MAC4 MII PHY Mode Transmit Data Enable Input. Transmit Data Enable that is received synchronously at the rising edge of M4MP_TX_CLK. **P4M_TX_EN** PHY4 MII Transmit Data Enable Input. Transmit Data Enable that is received synchronously at the rising edge of P4M_TX_CLK. This pin must be pulled low with 1K Ohm resistor when not used.

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQF P164	LQF P216			
M4MM_RXD[3:0] / M4MP_TXD[3:0] / P4M_TXD[3:0]	N/A	143 142 141 140	I		**M4MM_RXD[3:0]** MAC4 MII MAC Mode Receive Data Input. Receive data that is received synchronously at the rising edge of M4MM_RX_CLK. **M4MP_TXD[3:0]** MAC4 MII PHY Mode Transmit Data Input. Transmits data that is received synchronously at the rising edge of M4MP_TX_CLK. **P4M_TXD[3:0]** PHY4 MII Transmit Data Input. Transmits data that is received synchronously at the rising edge of P4M_TX_CLK. These pins must be pulled low with 1K Ohm resistor when not used.

6.4. LED Pins

Table 11. LED Pins

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQF P164	LQF P216			
LED_P4_2 / RESERVED	100	146	I/O_{PU}	8	Port 4 LED_2 output signal. *Note: this pin must be pulled low for normal operation and the LED output polarity will change from low active to high active. Please see section 8.20 for more detail.*
LED_P4_1	101	147	I/O_{PU}	8	Port 4 LED_1 output signal.
LED_P4_0 / EnBlink	102	148	I/O_{PU}	8	Port 4 LED_0 output signal. *Note: when EnBlink is pulled low, LED output polarity will change from low active to high active. Please see section 8.20 for more detail.*
LED_P3_2 / RESERVED	103	149	I/O_{PU}	8	Port 3 LED_2 output signal.
LED_P3_1	106	152	I/O_{PU}	8	Port 3 LED_1 output signal.
LED_P3_0 / RESERVED	107	153	I/O_{PU}	8	Port 3 LED_0 output signal.
LED_P2_2 / RESERVED	108	154	I/O_{PU}	8	Port 2 LED_2 output signal.

Pin Name	Pin No.		Type	Drive (mA)	Description
	LQF P164	LQF P216			
LED_P2_1	109	155	I/O_{PU}	8	Port 2 LED_1 output signal.
LED_P1_2 / LEDMOD0	112	157	I/O_{PU}	8	Port 1 LED_2 output signal. *Note: when LEDMOD0 is pulled low, LED output polarity will change from low active to high active. Please see section 8.20 for more detail.*
LED_P2_0 / EnRTCT	113	158	I/O_{PU}	8	Port 2 LED_0 output signal. *Note: when EnRTCT is pulled low, LED output polarity will change from low active to high active. Please see section 8.20 for more detail.*
LED_P0_2 / RESERVED	114	159	I/O_{PU}	8	Port 0 LED_2 output signal.
LED_P1_1	115	160	I/O_{PU}	8	Port 1 LED_1 output signal.
LED_P1_0 / RESERVED	118	162	I/O_{PU}	8	Port 1 LED_0 output signal.
LED_P0_1	119	163	I/O_{PU}	8	Port 0 LED_1 output signal.
LED_P0_0 / RESERVED	120	164	I/O_{PU}	8	Port 0 LED_0 output signal.

6.5. Miscellaneous Pins

Table 12. Miscellaneous Pins

Pin Name	Pin No.		Type	Description
	LQF P164	LQF P216		
RESERVED	63	91	O	Reserved for future used, must let floating.
RESERVED	64	92	I/O_{PU}	Reserved for future used, must let floating.
SCK / RESERVED	70	97	I_{PU}	Clock of EEPROM SMI. EEPROM interface when
SDA / RESERVED	71	98	I/O_{PU}	Data of EEPROM SMI. EEPROM interface when
RESERVED	N/A	99	O_{PU}	Reserved for future used, must let floating.
RESERVED / EnAutoload	N/A	100	I_{PU}	Reserved for future used, must let floating.

Pin Name	Pin No.		Type	Description
	LQFP164	LQFP216		
Interrupt	N/A	101	O	Interrupt output for external CPU.
XTALI	41	52	AI	25MHz crystal clock input and feedback pin.
XTALO	42	53	AO	25MHz crystal clock output pin.
MDIREF	9	12	AO	Reference resistor. A 2.49K Ohm (1%) resistor must be connected between MDIREF and GND.
nRESET	65	93	I_{PU}	System pin reset input. Low active use to reset RTL8366S/SR.

6.6. Configuration Strapping Pins

Table 13. Configuration Strapping Pins (For RTL8366S and RTL8366SR)

Pin Name	Pin No.		Type	Description
	LQFP 164	LQFP 216		
LED_P4_2 / RESERVED	102	148	I/O_{PU}	Internal used configuration. This pin must be pulled low via external resister for normal operation. *Note: this pin must be pulled low for normal operation and the LED output polarity will change from low active to high active. Please see section 8.20 for more detail.*
LED_P4_0 / EnBlink	102	148	I/O_{PU}	Power On LED Blinking configuration. Pull up: enable power on LED blinking (default). Pull down: disable power on LED blinking. *Note: when EnBlink is pulled low, LED output polarity will change from low active to high active. Please see section 8.20 for more detail.*
LED_P1_2 / LEDMOD0	112	157	I/O_{PU}	LED Mode configuration. Pull up: select LED mode 1. Pull down: select LED mode 0. *Note: when LEDMOD0 is pulled low, LED output polarity will change from low active to high active. Please see section 8.20 for more detail.*

Pin Name	Pin No.		Type	Description
	LQFP 164	LQFP 216		
LED_P2_0 / EnRTCT	113	158	I/O_{PU}	Enable RealTek Cable Tester after power on configuration. Pull up: enable power on RTCT function. Pull down: disable power on RTCT function. *Note: when EnRTCT is pulled low, LED output polarity will change from low active to high active. Please see section 8.20 for more detail.*
RESERVED / EnAutoload	N/A	100	I_{PU}	Enable EEPROM auto-load after power on configuration. Pull up: enable power on auto-load function. Pull down: disable power on auto-load function.

Table 14. Configuration Strapping Pins (Only for RTL8366SR)

Pin Name	Pin No.		Type	Description
	LQFP 164	LQF P216		
SEL_P4MODE[2:0]	N/A	57 55 56	I_{PU}	Detail description please refers to section 9.3.
SEL_P5MODE[1:0]	N/A	58 59	I_{PU}	Detail description please refers to section 9.3.
SEL_SDMODE[2:0]	N/A	62 61 60	I_{PU}	Detail description please refers to section 9.4. *Note: these pins must be pulled low for normal 5-Port Gigabit Switch operation.*
M4RG_TXC_DELAY / P4RG_RXC_DELAY	N/A	129	I_{PU}	M4RG_TXC_DELAY, MAC4 RGMII TXC delay configuration. Use to enable TXC delay 2nsec to TXD[3:0] when Port 4 MAC or PHY in RGMII mode. Pull up: enable TXC delay 2nsec to TXD[3:0] Pull down: disable TXC delay to TXD[3:0]
M4RG_RXC_DELAY / P4RG_TXC_DELAY	N/A	143	I_{PU}	M4RG_RXC_DELAY, MAC4 RGMII RXC delay configuration. Use to enable RXC delay 4nsec to RXD[3:0] when Port 4 MAC or PHY in RGMII mode. Pull up: enable RXC delay 4nsec to RXD[3:0] Pull down: disable RXC delay to RXD[3:0]

Pin Name	Pin No.		Type	Description
	LQFP 164	LQF P216		
M5RG_TXC_DELAY	N/A	117	I_{PU}	M5RG_TXC_DELAY, MAC5 RGMII TXC delay configuration. Use to enable TXC delay 2nsec to TXD[3:0] when Port 5 MAC in RGMII mode. Pull up: enable TXC delay 2nsec to TXD[3:0] Pull down: disable TXC delay to TXD[3:0]
M5RG_RXC_DELAY	N/A	128	I_{PU}	M5RG_RXC_DELAY, MAC5 RGMII RXC delay configuration. Use to enable RXC delay 2nsec to RXD[3:0] when Port 5 MAC in RGMII mode. Pull up: enable RXC delay 2nsec to RXD[3:0] Pull down: disable RXC delay to RXD[3:0]

6.7. Testing Pins

Table 15. Testing Pins

Pin Name	Pin No.		Type	Description
	LQF P164	LQF P216		
ATEST	3	3	AO	Reserve for internal used, must let floating.
LPFVOP	6	8	AO	Reserve for internal used, must let floating.
LPFVON	7	9	AO	Reserve for internal used, must let floating.
RTT1	13	17	AO	Reserve for internal used, must let floating.
RTT2	14	18	AO	Reserve for internal used, must let floating.
ATESTCK0	138	184	AO	Reserve for internal used, must let floating.
ATESTCK1	15	19	AO	Reserve for internal used, must let floating.
Digital_Test	68	96	I_{PU}	Reserve for internal used, must let floating.
VTESTP	74	103	AO	Reserve for internal used, must let floating.
VTESTN	77	106	AO	Reserve for internal used, must let floating.
VPHTEST	79	108	AI	Reserve for internal used, must let floating.
TEST_FB	81	109	AI	Reserve for internal used, must let floating.
En_TEST	82	110	AI_{PU}	Reserve for internal used, must be pulled down with 1K Ohm resistor for normal application.

6.8. Power and GND Pins

Table 16. Power and GND Pins

Pin Name	Pin No.		Type	Description
	LQFP164	LQFP216		
RESERVED	75, 78	104, 107	AP	Reserved for future used, must let floating.

Pin Name	Pin No.		Type	Description
	LQFP164	LQFP216		
SWRGND	76, 83	105, 111	AG	Reserved for future used, must connect to GND.
DVDDIO0	67, 105, 116	95, 151, 161	P	Digital I/O High Voltage Power for SMI, LED, nRESET.
DVDDIO1	89, 96	124, 144	P	Digital I/O High Voltage Power for General Purpose Interfaces.
DVDDL	8, 59, 60, 62, 66, 72, 86, 87, 88, 94, 98, 104, 110, 121, 123	10, 86, 88, 89, 90, 94, 102, 112, 123, 134, 145, 150, 156, 165, 166	P	Digital Low Voltage Power.
SVDDH	44	63	AP	Serdes High Voltage Power.
SVDDT	46	65	AP	Serdes Low Voltage Power.
SVDDL	47, 53, 58	66, 72, 77	AP	Serdes Low Voltage Power.
AVDDH	2, 4, 5, 16, 23, 29,35, 43, 124, 131, 137, 141, 148, 154, 160	2, 4, 5, 21, 29, 37, 45, 54, 167, 176, 183, 187, 195, 203, 211	AP	Analog High Voltage Power.
AVDDL	1, 12, 17, 22, 28, 34, 40, 125, 130, 136, 142, 147, 153, 159	1, 16, 22, 28, 36, 44, 51, 168, 175, 182, 188, 194, 202, 210	AP	Analog Low Voltage Power.
PLLVDDL0	140	186	AP	PLL0 Low Voltage Power.
PLLVDDL1	11	15	AP	PLL1 Low Voltage Power.
AGND	E-PAD	7, 11, 13, 20, 25, 32, 33, 40, 41, 48, 171, 172, 179, 191, 198, 199, 206, 207, 214	AG	Analog GND.
PLLGND0	139	14	AG	PLL0 GND.
PLLGND1	10	185	AG	PLL1 GND.
SGND	45, 50, 55	64, 69, 74	AG	Serdes GND.
DGND	E-PAD, 61, 73, 84, 93, 95, 97, 99, 111, 122	E-PAD	G	Digital GND.

7. Physical Layer Function Description

7.1. MDI Interface

The RTL8366S/SR embedded 5 Gigabit Ethernet PHY in one chip. Each port uses a single common MDI interface to support 1000Base-T, 100Base-Tx, and 10Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

7.2. 1000Base-T Transmit Function

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through D/A converter.

7.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. Afterwards, the received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. Then, the 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

7.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven into the network media in the form of MLT-3 signaling. The MLT-3 multi-level

signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

7.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

7.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

7.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

7.8. Auto-Negotiation for UTP

The RTL8366S/SR obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8366S/SR advertises full capabilities (1000Full, 100Full, 100Half, 10Full, 10Half) together with flow control ability.

7.9. Crossover Detection and Auto Correction

The RTL8366S/SR automatically determines whether or not it needs to crossover between pairs as shown in the Table 17 so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, the RTL8366S/SR automatically switch its pin pairs when

necessary to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The pin mapping in MDI and MDI Crossover mode is given below.

Table 17. Media Dependent Interface Pin Mapping

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	Unused	Unused	D	Unused	Unused
D	D	Unused	Unused	C	Unused	Unused

7.10. Polarity Correction

The RTL8366S/SR automatically corrects polarity errors on the receiver pairs in the 1000Base-T and 10Base-T modes. In 100Base-Tx mode, the polarity does not matter.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the de-scrambler is locked the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link up. The polarity becomes unlock when link is down.

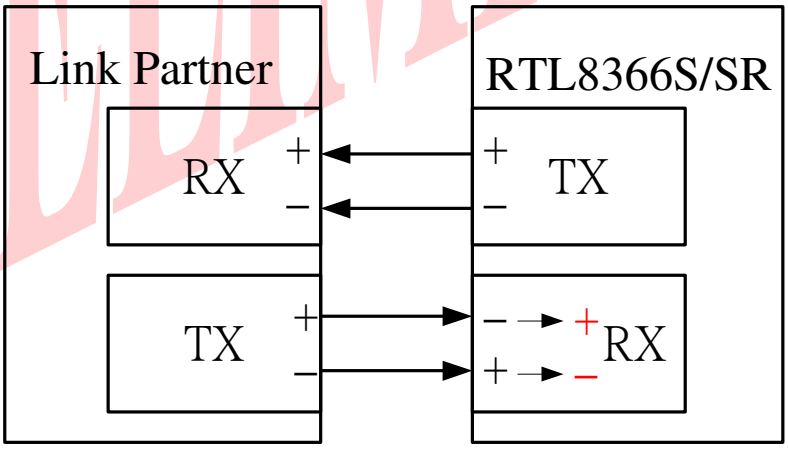


Figure 10. Conceptual Example of Polarity Correction

8. Switch Function Description

8.1. Reset

8.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse will be generated and the RTL8366S/SR will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the nRESET signal.
- Auto load the configuration from EEPROM if EEPROM is detected.
- Complete the embedded SRAM BIST process.
- Initialize the packet buffer descriptor allocation.
- Initialize the internal registers and prepare them to be accessed by the external CPU.

8.1.2. Software Reset

The RTL8366S/SR supports two software resets; a chip reset and a soft reset.

8.1.2.1 CHIP_RESET

When CHIP_RESET is set to 0b1 (write and self clear), the chip will take the following steps:

1. Download configuration from strap pin and EEPROM.
2. Start embedded SRAM BIST (Built-In Self Test).
3. Clear all the Lookup and VLAN tables.
4. Reset all registers to default values.
5. Restart the auto-negotiation process.

8.1.2.2 SOFT_RESET

When set SOFT_RESET is set to 0b1 (write and self clear), the chip will take the following steps:

6. Clear the FIFO and re-start packet buffer link list.
7. Restart the auto-negotiation process.

8.2. 802.3x Full Duplex Flow Control

The RTL8366S/SR supports IEEE 802.3x flow control in 10/100/1000M modes. Flow control can be decided in two ways:

- When Auto-Negotiation is enabled, flow control depends on the result of NWay.
- When Auto-Negotiation is disabled, flow control depends on PORT_ABILITYn[7:6] (n: 0 - 4).

The RTL8366S/SR supports asymmetrical flow control in 1Gbps mode. The Auto-Negotiation module checks the flow control ability of the PHY MII register 4, 9 and those of its link partner to resolve the flow control mode. The following shows the flow control resolution truth table.

Table 18. Flow Control Resolution Truth Table

Local Device		Link Partner		Local Device Resolution	Local Partner Resolution
PAUSE	**ASM_DIR**	**PAUSE**	**ASM_DIR**		
0	0	Irrelevant	Irrelevant	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	0	Irrelevant	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	1	Enable PAUSE Transmit Disable PAUSE Receive	Enable PAUSE Receive Disable PAUSE Transmit
1	0	0	Irrelevant	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	Irrelevant	1	Irrelevant	Enable PAUSE Transmit and Receive	Enable PAUSE Transmit and Receive
1	1	0	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	1	0	1	Enable PAUSE Receive Disable PAUSE Transmit	Enable PAUSE Transmit Disable PAUSE Receive

8.3. Half Duplex Flow Control

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called “truncated binary exponential backoff”. At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slot time (512 bit times). The number of slot times to delay before the n^{th} retransmission attempt is chosen as a uniformly distributed random integer ‘r’ in the range:

$$0 \leqq r < 2^k$$

where:

k =min (n, backoffLimit). The backoffLimit for the RLT8366S/SR is 9.

The half duplex back-off algorithm in the RTL8366S/SR does not have the maximum retry count limitation of 16 (as defined in IEEE 802.3). This means packets in the switch will not be dropped if the back-off retry count is over 16.

8.3.1. Back Pressure Mode

In BACK-PRESSURE mode, the RTL8366S/SR sends a 4-byte jam pattern (data=0xAA) to collide with incoming packets when congestion control is activated. The Jam pattern collides at the fourth byte counted from the preamble. Receive one packet after 48 consecutive jam collisions (data collisions are not included in the 48).

8.3.2. Defer Mode

DEFER mode asserts the TXEN signal for 2K bytes in order to force the link partner to back-off. The IPG between two asserted TXEN is 56 bits. When congestion control is activated on the ingress port, the RTL8366S/SR will send a 4-byte jam pattern at the first incoming packet. The link partner will back-off and wait to re-try. The RTL8366S/SR will start the DEFER signal 56 bits after the link partner starts to back-off.

8.4. Search and Learning

When a packet is received, the RTL8366S/SR uses the destination MAC address and Filtering Database Index (FID) to search the 1K-entry look-up table. 48-bits MAC address and 3-bits FID use hash algorithm, as the following equation, to calculate 8 bits index value. The RTL8366S/SR uses this 8-bits index to compare the packet MAC address with 4-entry data (MAC address) in look-up table, as shown in Table 19. This is the “Address Search”. If the destination MAC address is not found, the switch will broadcast the packet according to VLAN configuration.

Index[7] = $MAC_7 \oplus MAC_{15} \oplus MAC_{23} \oplus MAC_{31} \oplus MAC_{39} \oplus MAC_{47} \oplus FID_1$

Index[6] = $MAC_6 \oplus MAC_{14} \oplus MAC_{22} \oplus MAC_{30} \oplus MAC_{38} \oplus MAC_{46} \oplus FID_0$

Index[5] = $MAC_5 \oplus MAC_{13} \oplus MAC_{21} \oplus MAC_{29} \oplus MAC_{37} \oplus MAC_{45} \oplus FID_2$

Index[4] = $MAC_4 \oplus MAC_{12} \oplus MAC_{20} \oplus MAC_{28} \oplus MAC_{36} \oplus MAC_{44} \oplus FID_1$

Index[3] = $MAC_3 \oplus MAC_{11} \oplus MAC_{19} \oplus MAC_{27} \oplus MAC_{35} \oplus MAC_{43} \oplus FID_0$

Index[2] = $MAC_2 \oplus MAC_{10} \oplus MAC_{18} \oplus MAC_{26} \oplus MAC_{34} \oplus MAC_{42} \oplus FID_2$

Index[1] = $MAC_1 \oplus MAC_9 \oplus MAC_{17} \oplus MAC_{25} \oplus MAC_{33} \oplus MAC_{41} \oplus FID_1$

Index[0] = $MAC_0 \oplus MAC_8 \oplus MAC_{16} \oplus MAC_{24} \oplus MAC_{32} \oplus MAC_{40} \oplus FID_0$

Table 19. L2 Table 4-Way Hash Index Method

Index	Entry 0	Entry 1	Entry 2	Entry 3
0x00	MAC Addr 0	MAC Addr 1	MAC Addr 2	MAC Addr 3
0x01	MAC Addr 4	MAC Addr 5	MAC Addr 6	MAC Addr 7
0x02	MAC Addr 8	MAC Addr 9	MAC Addr 10	MAC Addr 11
…				
0xFE	MAC Addr 1016	MAC Addr 1017	MAC Addr 1018	MAC Addr 1019
0xFF	MAC Addr 1020	MAC Addr 1021	MAC Addr 1022	MAC Addr 1023

The RTL8366S/SR then uses the source MAC address and FID of the incoming packet to hash into 8-bits index. ASIC compares the source MAC address with 4-entry data (MAC address) in this index. The RTL8366S/SR will update the entry with new information, if one of the 4-entry matches. But, if no one match and the 4-entry are not all occupied by other MAC addresses. The RTL8366S/SR will record the source MAC address and ingress port number into one empty entry. This process is called “Learning”.

The RTL8366S/SR supports 8-entry Content Address Memory (CAM) to avoid look-up table hash collision. When all 4-entry in the look-up table index are occupied, the source MAC address can be learned into one of the 8-entry CAM. If both look-up table and CAM are full, the source MAC address will not be learned in the RTL8366S/SR.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if it’s time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8366S/SR is between 200 and 400 seconds (typical is 300 seconds).

8.5. SVL and IVL/SVL

The RTL8366S/SR supports 8 groups FID for L2 search and learning. In default operation, all VLAN entries belong to the same FID. This is called Share VLAN Learning (SVL). If all VLAN entries are

configured into 8 different FIDs, then the same source MAC address with different FID can be learned into different look-up table entry. This is called Independent and Share VLAN Learning (IVL/SVL.)

8.6. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length <64 bytes), and oversize packets (length >maximum length) will be discarded by the RTL8366S/SR. The maximum packet length may be set to 1522, 1536, 1552, or 12K bytes.

8.7. IEEE 802.3 Reserved Group Addresses Filtering Control

The RTL8366S/SR supports the ability to drop/forward 802.1D specified reserved group MAC addresses: 01-80-C2-00-00-04 to 01-80-C2-00-00-0F. The default setting enables forwarding of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause) and 01-80-c2-00-00-02 (802.3ad LACP) will always be filtered. MAC address 01-80-C2-00-00-03 is always forwarded. This function is controlled by RMA_EN[8:0] registers. Table 20 shows the Reserved Multicast Address (RMA) configuration mode from 01-80-C2-00-00-00 to 01-80-C2-00-00-2F.

Table 20. Reserved Multicast Address Configuration Table

Assignment	Value	RMA_EN bit
Bridge Group Address	01-80-C2-00-00-00	Bit 0 0b0: Normal process 0b1: Trap to CPU
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE operation	01-80-C2-00-00-01	Bit 1
IEEE Std 802.3ad Slow Protocols-Multicast address	01-80-C2-00-00-02	Bit 2
IEEE Std 802.1X PAE address	01-80-C2-00-00-03	Bit 3
All LANs Bridge Management Group Address	01-80-C2-00-00-10	Bit 4
GMRP Address	01-80-C2-00-00-20	Bit 5
GVRP address	01-80-C2-00-00-21	Bit 6
Undefined 802.1 bridge address	01-80-C2-00-00-04 | 01-80-C2-00-00-0F	Bit 7
Undefined GARP address	01-80-C2-00-00-22 | 01-80-C2-00-00-2F	Bit 8

8.8. Broadcast/Multicast/Unknown DA Storm Control

The RTL8366S/SR can enable or disable per-port broadcast/multicast/unknown DA storm control by setting BC_STORM_EN/MC_STORM_EN/UNDA_STORM_EN registers, default are disabled. After receiving 32/64/128/255 broadcast/multicast/unknown DA packets by the enabled port within a reference period, all the other broadcast/multicast/unknown DA packets will be dropped. The reference period has 4 duration options by register configuration.

8.9. Port Security Function

The RTL8366S/SR supports 3 kinds of security function to prevent malicious attack.

- Per-port enable/disable SA auto-learning for the ingress packet.
- Per-port enable/disable look-up table aging update function for the ingress packet.
- Per-port enable/disable drop all unknown DA packets.

8.10. MIB Counter

RTL8366S/SR supports a set of counters, to support management function.

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

8.11. Port Mirroring

The RTL8366S/SR supports one set of port mirroring functions for all ports. The TX, or RX, or both TX/RX packets of the source port can be monitored from a mirror port.

8.12. VLAN Function

The RTL8366S/SR supports 4K VLAN groups. These can be configured as port-based VLANs, IEEE 802.1Q tag-based VLANs, and Protocol-based VLAN. Two ingress filtering and egress filtering options provide flexible VLAN configuration:

Ingress filtering option 1: The Acceptable Frame Type of the Ingress Process can be set to 'Admit All' or 'Admit All Tagged'.

Ingress filtering option 2: 'Admit' or 'Discard' frames associated with a VLAN for which that port is not in the member set.

Egress filtering option 1: 'Forward' or 'Discard' ARP broadcast frames between different VLAN domain.

Egress filtering option 2: 'Forward' or 'Discard' Leaky VLAN frames between different VLAN domain.

Egress filtering option 3: 'Forward' or 'Discard' multicast VLAN frames between different VLAN domain.

VLAN tag can be inserted or removed at the output port. The RTL8366S/SR will insert a Port VID (PVID) for untagged frames or remove the tag from tagged frames. The RTL8366S/SR also supports a special insert VLAN tag function to separate traffic from WAN and LAN sides in Router and Gateway applications.

In router applications, the router may want to know which input port this packet came from. The RTL8366S/SR supports Port VID (PVID) for each port and can insert a PVID in the VLAN tag on egress. Using this function, VID information carried in the VLAN tag will be changed to PVID. The RTL8366S/SR also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, it will drop non-tagged packets and packets with an incorrect PVID.

8.12.1. Port-based VLAN

If the VLAN function is enabled by setting register DisVLAN=0b0, the default VLAN membership configuration by internal register is port 4 overlapped with all the other ports to form four individual VLANs. This default configuration of the VLAN function could be modified via an attached serial EEPROM or EEPROM SMI Slave interface. The 4K-entry VLAN Table designed into the RTL8366S/SR provide full flexibility for users to configure the input ports to associate with different VLAN groups. Each input port can join more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members.

8.12.2. IEEE802.1Q Tag-based VLAN

The RTL8366S/SR supports 4K VLAN entries to perform 802.1Q tag-based VLAN mapping. In 802.1Q VLAN mapping, the RTL8366S/SR uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. RTL8366S/SR compares the explicit identifier in the VLAN tag with the 4K VLAN Table to determine the VLAN association of this packet, and then forwards this packet to the member set of this VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When '802.1Q tag aware VLAN' is enabled, the RTL8366S/SR performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If '802.1Q tag aware VLAN' is disabled, the RTL8366S/SR performs only port-based VLAN mapping both on non-tagged and tagged frames. The processing flow when '802.1Q tag aware VLAN' is enabled is illustrated below.

Two VLAN ingress filtering functions are supported by the RTL8366S/SR in registers. One is the 'VLAN tag admit control, which provides the ability to receive VLAN-tagged frames only. Untagged or priority tagged (VID=0) frames will be dropped. The other is 'VLAN member set ingress filtering', which will drop frames if the ingress port is not in the member set.

There are also four optional egress filtering functions. 'Unicast leaky VLAN' and 'ARP leaky VLAN' are supported by the RTL8366S/SR via register access.

8.12.3. Protocol-based VLAN

The RTL8366S/SR support 4 groups Protocol-based VLAN configuration. The packet format can be RFC 1042, LLC, and Ethernet, as shown in Figure 11. There are 4 tables configuration to assign the frame type and corresponding field value. Take IP packet configuration as an example, user can configure the frame type to be "Ethernet" and value to be "0x0800". Each table will index to one of the entry in 4K-entry VLAN table. Packet stream match the protocol type and value will follow the VLAN member configuration of the indexed entry to forward the packets.

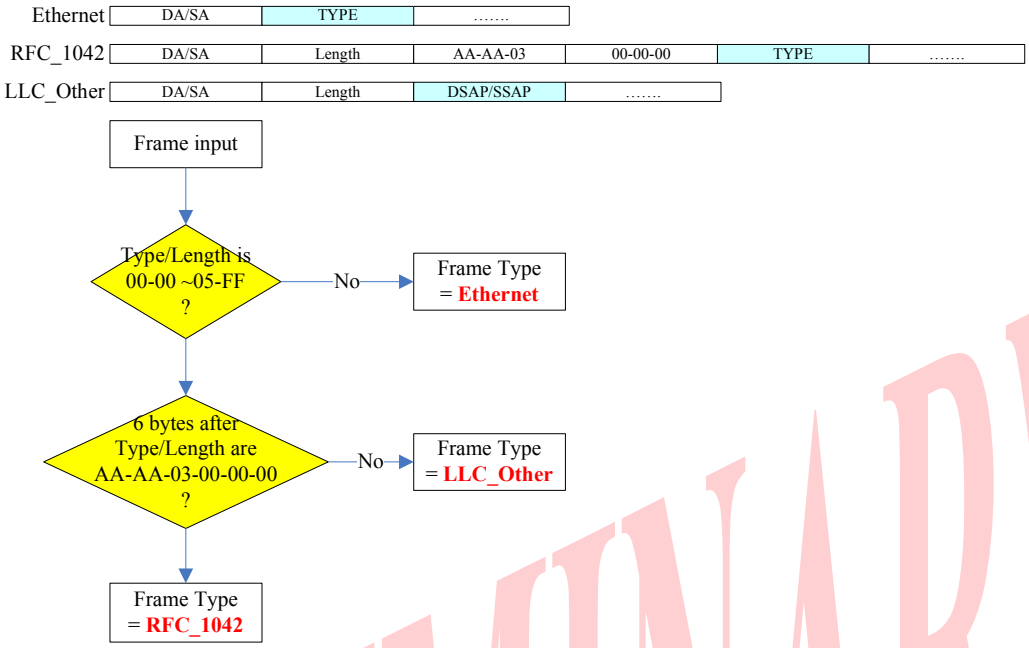


Figure 11. Protocol-based VLAN Frame Format and Flow Chart

8.12.4. Port VID

In a router application, the router may want to know which input port this packet came from. The RTL8366S/SR supports Port VID (PVID) for each port to insert a PVID in the VLAN tag for untagged or priority tagged packets on egress port. When 802.1Q tag aware VLAN is enabled, VLAN tag admit control is enabled, and non-PVID Discard is enabled at the same time; packets with an incorrect PVID and non-tagged packets will be dropped.

8.13. QoS Function

RTL8366S/SR could support 4 priority queues and the input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1p/Q Tag-based priority, IPv4/IPv6 DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in RTL8366S/SR, the packet's priority will be assigned base on priority selection table.

Each queue has 2 leaky buckets, one for Average Packet Rate and one for Peak Packet Rate. Per-queue in each output port can select as Strict Priority (SP) or Weighted Fair Queue (WFQ) for packet scheduling algorithm.

8.13.1. Input Bandwidth Control

Input bandwidth control is to limit the input bandwidth, when input traffic is more than RX bandwidth parameter, this port will send out a 'pause ON' frame or drop the input packet depending on flow control status. Per-port can configure input bandwidth control rate from 64Kbps to 1Gbps in 64Kbps step.

8.13.2. Priority Assignment

Priority assignment specifies the priority of a received packet according to different rules. The RTL8366S/SR can recognize the QoS priority information of incoming packets to give a different egress service priority. The RTL8366S/SR identifies the priority of packets based on several types of QoS priority information:

- Port-based priority
- 802.1p/Q-based priority
- IPv4/IPv6 DSCP-based priority
- ACL-based priority

8.13.3. Priority Queue Scheduling

RTL8366S/SR supports MAX^2-MIN packet scheduling algorithm. The packet scheduling has three steps:

8. Type I leaky bucket, which specifies the average packet rate of one queue;
9. Type II leaky bucket, which specifies the peak packet rate of one queue;
10. "Weighted Fair Queue (WFQ)", which decides which queue is selected in one slot time to guarantee the minimal packet rate of one queue.

In addition, each queue of each port can select Strict Priority or WFQ packet scheduling according to packet scheduling mode. Figure 12 shows RTL8366S/SR packet scheduling block diagram.

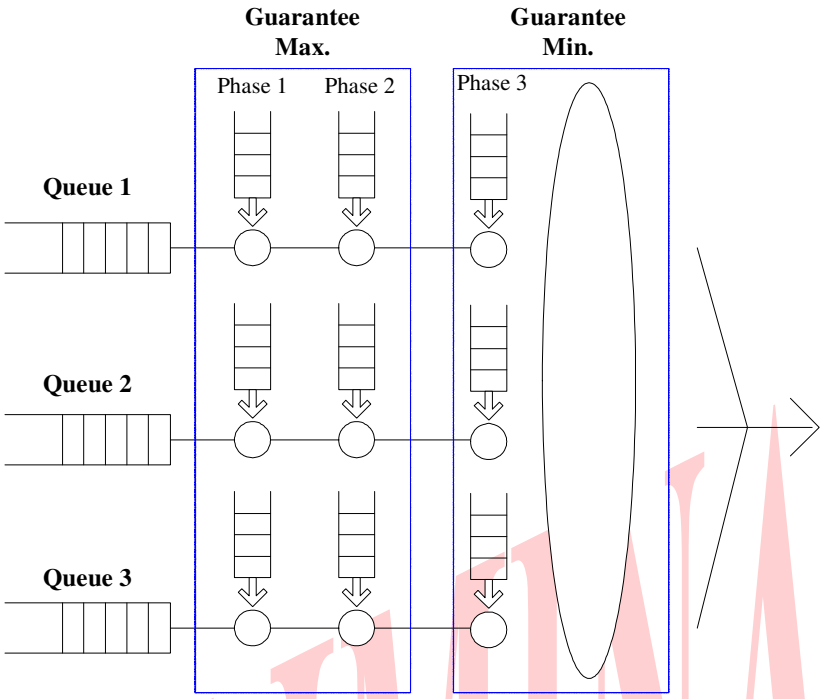


Figure 12. RTL8366SR MAX^2-MIN Scheduling Block Diagram

8.13.4. 802.1p/Q and DSCP Remarking

The RTL8366S/SR also supports 802.1p/Q and IP DSCP remarking function. When packets egress from one of the 4 queues, the packet's 802.1p/Q priority and IP DSCP can optional be remarked as configured value. Each output queue has 3-bits 802.1p/Q and 6-bits IP DSCP value configuration register for whole system.

8.14. ACL Function

RTL8366S/SR supports 32-entry ACL rules. When a packet is received, its source port, Source MAC address, Destination Address, Protocol, source IP address, destination IP address, source port number, destination port number (TCP or UDP packet), and EtherType code (non IP packet) are recorded and compared to application ACL entry.

If a received packet matched multiple entries, the entry with the least address is valid. If the entry is valid, the action bit and priority bit will be applied. If action bit is "Drop", the packet will be dropped. If action bit is "CPU", the packet will be trapped to CPU instead of forwarding to non CPU port except it has been determined Drop by other rules (other than ACL rule). If action bit is "Permit", ACL rule will take no effect to other rules. If action bit is "Mirror", the packet will be forwarded to mirror port and L2 lookup result destination port. The mirror port indicates the port, which is configured in port mirror

mechanism. The priority bit will take effect only if action bit are “CPU”, “Permit”, and “Mirror”. Priority bit is used to determine the packet queue ID according to priority assignment mechanism.

8.15. IGMP&MLD Snooping Function

RTL8366S/SR supports IGMP v1/v2/v3 and MLD v1/v2 snooping. RTL8366S/SR can trap all IGMP and MLD packets to CPU port. CPU processes these packets, gets the information of the IP multicast groups for all ports, and writes proper multicast entry to lookup table through EEPROM SMI.

The typical application of RTL8366S/SR IGMP and MLD snooping function is shown in following figure:

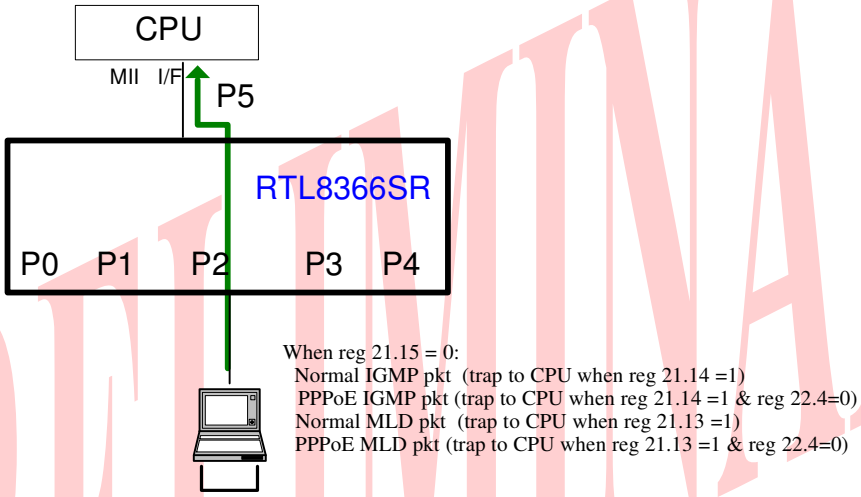


Figure 13. IGMP&MLD Application example

8.16. 802.1x Function

RTL8366S/SR supports IEEE 802.1x Port-based/MAC-based Access Control about security.

- Port-based access control for each port.
- Authorized Port-based Access Control for each port.
- Port-based Access Control Direction for each port.
- MAC-based access control for each port.
- MAC-based Access Control Direction.
- Optional Unauthorized behavior.

8.16.1. Port-based Access Control

When hosts connect with a switch, the switch will ask the PC host for authenticating .The switch will transmit the information sent by the host to Authentication Server for authenticating.

8.16.2. MAC-based Access Control

MAC-based Access Control provide multi-authentication for logical port, every logical port represents a source MAC address. There are some logical ports for a physical port according to MAC-based Access Control. When a logical port is authenticated, the relevant source MAC address can access the network. Whether the source MAC address that is not authenticated or provided for 802.1x function will be dropped or trapped to CPU.

8.17. Guest VLAN

When the RTL8366S/SR enables Port-based or MAC-based 802.1x function and the connected PC doesn't support 802.1x function or pass authentication procedure. The RTL8366S/SR will drop all packets from this port or packets with unauthorized MAC address.

The RTL8366S/SR also supports one set Guest VLAN to allow the unauthorized ports or packets to be forwarded to a limited VLAN domain. User can configure one VLAN ID and member set for these unauthorized packets.

8.18. 802.1D Function

RTL8366S/SR supports 8 sets (based on FID) and four stares of each port for CPU implement 802.1D (STP) and 802.1s (MSTP) function:

- **Disable state:** the port will not receive/sent packet and not do learning**.**
- **Blocking state:** the port will only receive BPDU packet of spanning tree protocol, but not sent any packet and not do learning.
- **Learning state:** the port will receive any packet including spanning tree BPDU, and do learning at the same time, but only sent BPDU packet**.**
- **Forwarding state:** the port will receive/send any packet and does learning.

RTL8366S/SR also supports per port transmission/reception enable/disable function, user can control per port state by register access.

8.19. RTCT

The RTL8366S/SR physical layer transceivers use DSP technology to implement RealTek Cable Tester (RTCT) feature. The RTCT function could be used to detect short, open, or impedance mismatch in each differential pairs with cable length information. RTL8366S/SR also provide LEDs to indicator test status and result.

8.20. LED Indicator

The RTL8366S/SR supports parallel LEDs for each port. Each port has three LED indicator pins. Each pin may have different indicator meanings set by pins LEDMODE[1:0]. Refer to the pin descriptions for details. Upon reset, the RTL8366S/SR supports chip diagnostics and LED functions by blinking all LEDs once. This function can be disabled by asserting EnBlink to 0b0 (pull down). LED_BLINK_RATE[2:0] determines the LED blinking period for activity and collision.

There are 3 LED pins have configuration strapping function, LED_P4_2/RESERVED, LED_P4_0/EnBlink, and LED_P1_2/LEDMODE0. All of these 3 pins are pulled up with internal resister. For LED_P4_2/RESERVED, user must use external resister to pull down for normal operation. For LED_P4_0/EnBlink, user can optional floating or pull down to disable or enable power on LED blinking. For LED_P1_2/LEDMODE0, user can option floating or pull down to select LED mode. If these pins pull down, the LED signals will output high active to turn on LED. Else, the LED signal will output low active to turn on LED. The reference circuit please refers to Figure 14 and Figure 15. The typical values for pull-down resistors are 10KΩ.

The LED_P***n***_0, LED_P***n***_1, and LED_P***n***_2 pins are dual function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is floating or pull high upon reset, the pin output is active low after reset. Otherwise, if the pin input is pulled down upon reset, the pin output is active high after reset.

The LED_P***n***_0 or LED_P***n***_2 can combine with LED_P***n***_1 as Bi-color LED. And LED_P***n***_1 should operation at the same polarity as another Bi-color LED pin. For example, LED_P0_1 should keep floating upon reset if LED_P0_1 combine with LED_P0_2 as a Bi-color LED and LED_P0_2 input is floating upon reset. These two LED pins output is active low after reset at this configuration. By the way, LED_P0_1 should pull down upon reset if LED_P0_1 combine with LED_P0_2 as a Bi-color LED and LED_P0_2 input is pull down upon reset. These two LED pins output are active high after reset at this configuration.

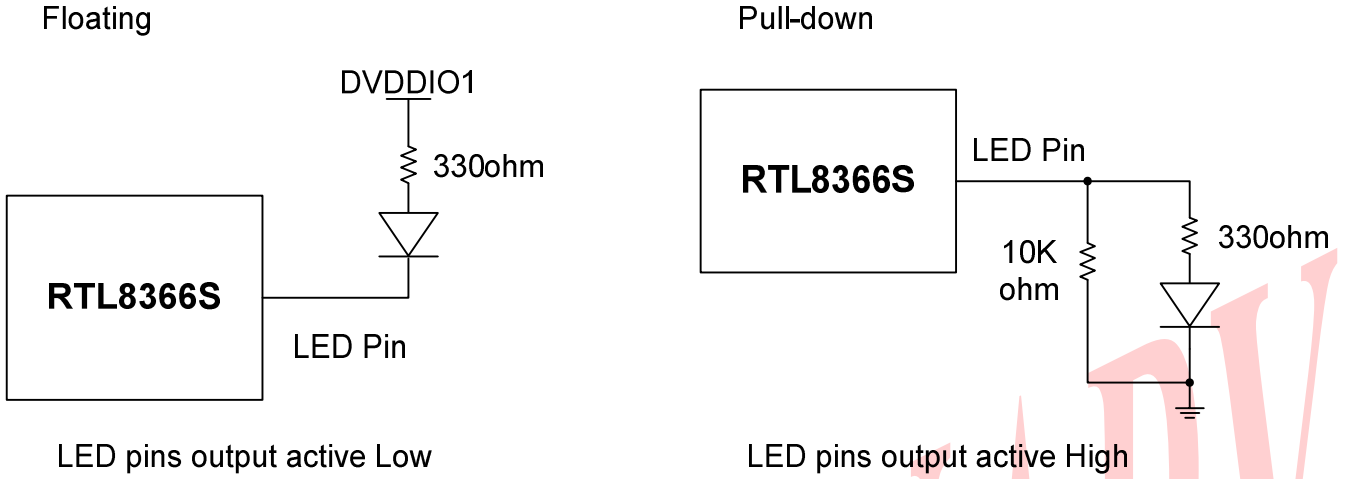


Figure 14. Floating and Pull-Down of single color LED Pins

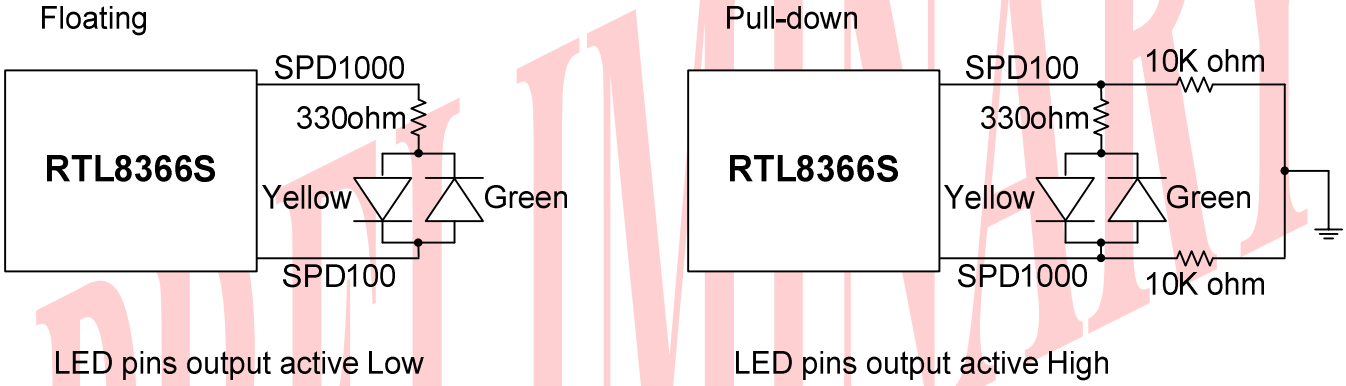


Figure 15. Floating and Pull-Down of Bi-color LED Pins

8.21. Interrupt for External CPU

The RTL8366S/SR provides one Interrupt output pin to notify external CPU for status alarm. Interrupt pin output polarity can be configured by register access. Per-port has link-up and link-down interrupt flags with mask in configuration registers. When enable port link-up or link-down interrupt mask, the RTL8366S/SR will raise the interrupt signal to alarm external CPU. CPU can read the interrupt flag to find out which port has link-up or link down status change.

9. Interface Descriptions

9.1. EEPROM SMI Host to EEPROM

The EEPROM interface of the RTL8366S/SR uses the serial bus EEPROM Serial Management Interface (SMI). The 8K-bit 24C08 EEPROM is read via the EEPROM SMI protocol. When the RTL8366S/SR is powered up, the RTL8366S/SR drives SCK and SDA to read the registers from the EEPROM.

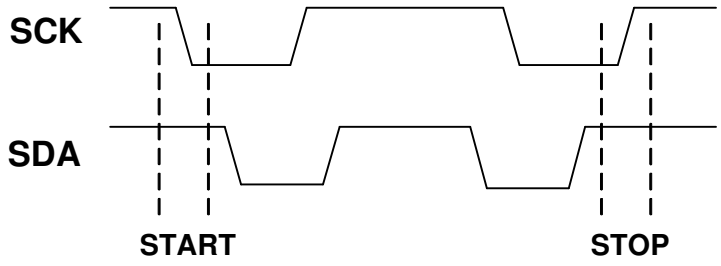


Figure 16. SMI Start and Stop Command

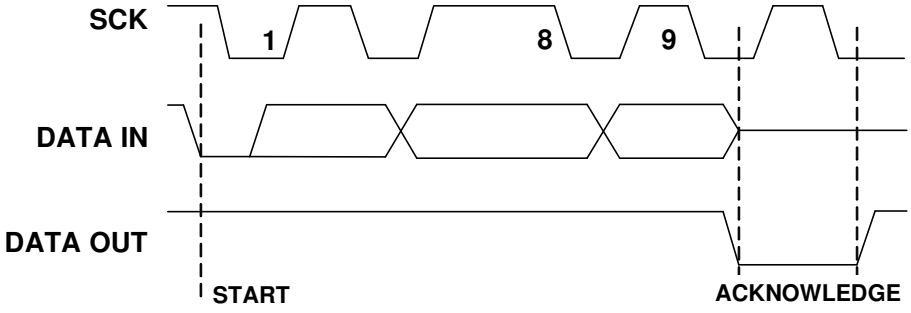


Figure 17. EEPROM SMI Host to EEPROM

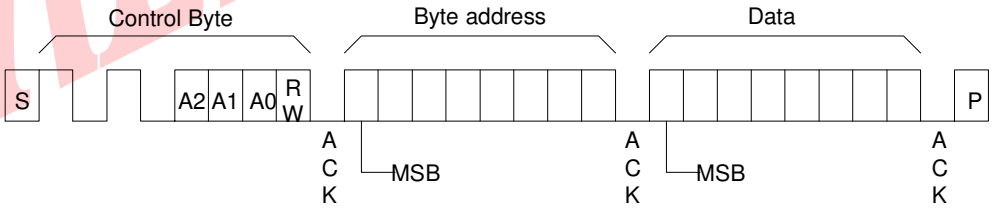


Figure 18. EEPROM SMI Host Mode Frame

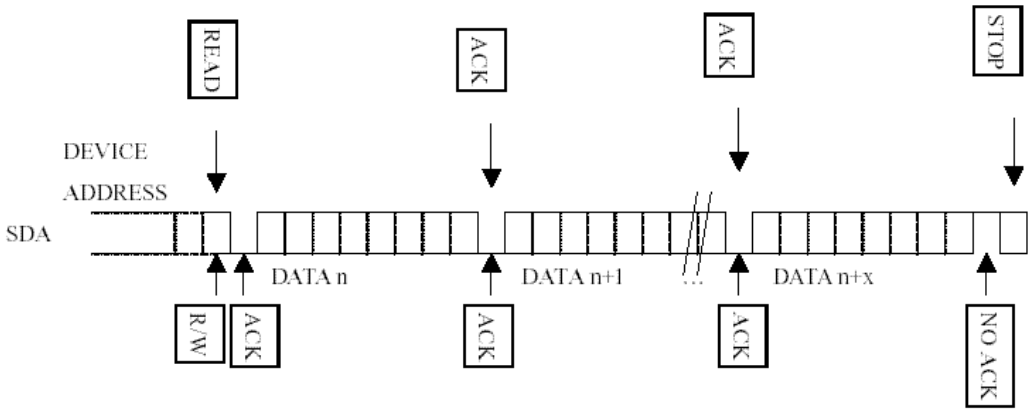


Figure 19. EEPROM SMI Sequential Read

9.2. EEPROM SMI Slave for External CPU

When EEPROM auto-load is complete, the RTL8366S/SR registers can be accessed via SCK and SDA via an external CPU. The device address of the RTL8366S/SR is 0x4. For the start and end of a write/read command, SCK needs one extra clock before/after the start/stop signals.

Regiter write through EEPROM SMI Slave interface

Address: 16'h0318

Data: 16'h1918

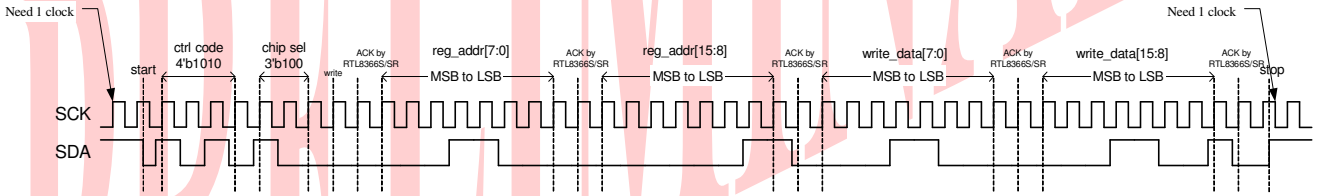


Figure 20. EEPROM SMI Write Command for Slave Mode

Regiter read through EEPROM SMI Slave interface

Address: 16'h0318

Data: 16'h1918

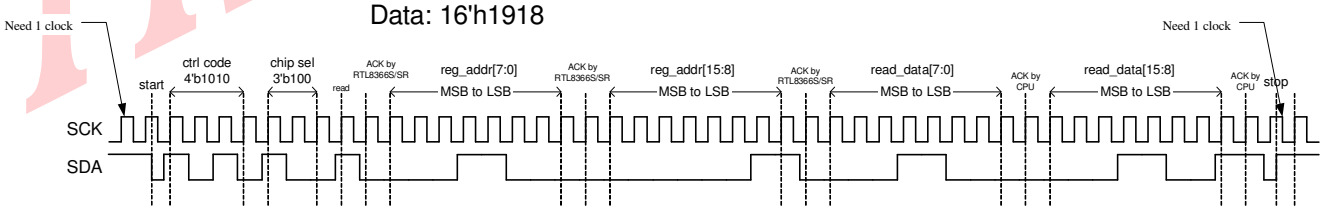


Figure 21. EEPROM SMI Read Command for Slave Mode

9.3. General Purpose Interface (Only for RTL8366SR)

In Gateway or WLAN-11n Router application, RTL8366SR supports dual RGMII interface, one for Port 5 MAC and the other is for Port 4 PHY (as shown in Figure 6). But, in one arm router application, which CPU only has one MII/GMII/RGMII interface, RTL8366SR also supports Port 5 MAC to configure as GMII interface (as shown in Figure 7). When Port 5 MAC is configured as GMII interface, Port 4 MAC or PHY can't be selected as any MII/GMII/RGMII interface. The following table shows the configuration mode for Port 5 MAC and Port 4 PHY.

- SerDes, Port 4, Port 5 MAC Interface Selection Table:

Table 21. SerDes, Port4&Port 5 MAC Mode Selection

Mode	Interface	Mode Selection		Description
0	**SerDes**	SEL_SDMODE[2:0]	0b001	Port 4 PHY or Fiber by register configuration
	Port 4 MAC or PHY	SEL_P4MODE[2:0]	0b010	Port 4 PHY with MII (PHY mode)
	Port 5 MAC	SEL_P5MODE[2:0]	0b010	Port 5 MAC with RGMII
1	**SerDes**	SEL_SDMODE[2:0]	0b001	Port 4 PHY or Fiber by register configuration
	Port 4 MAC or PHY	SEL_P4MODE[2:0]	0b000	Port 4 MAC
	Port 5 MAC	SEL_P5MODE[2:0]	0b001	Port 5 MAC with RGMII
2	**SerDes**	SEL_SDMODE[2:0]	0b001	Port 4 PHY or Fiber by register configuration
	Port 4 MAC or PHY	SEL_P4MODE[2:0]	0b000	Port 4 MAC
	Port 5 MAC	SEL_P5MODE[2:0]	0b001	Port 5 MAC with GMII
3	**SerDes**	SEL_SDMODE[2:0]	0b001	Port 4 PHY or Fiber by register configuration
	Port 4 MAC or PHY	SEL_P4MODE[2:0]	0b011	Port 4 PHY with MII (PHY mode)
	Port 5 MAC	SEL_P5MODE[2:0]	0b011	Port 5 MAC with MII (PHY mode)
4	**SerDes**	SEL_SDMODE[2:0]	the others	Reserved for future used
	Port 4 MAC or PHY	SEL_P4MODE[2:0]	the others	Reserved for future used
	Port 5 MAC	SEL_P5MODE[2:0]	the others	Reserved for future used

9.3.1. Port 5 MAC GMII Mode Interface (1Gbps)

Only Port 5 MAC can support GMII mode for one arm router application. When RTL8366SR configured in this mode, switch doesn't support Port 4 PHY MII/RGMII mode.

Table 22 shows the pin numbers and names in RTL8366SR (LQFP-216) and Figure 22 shows the signal diagram for Port 5 MAC in GMII interface.

Table 22. Port 5 MAC GMII Mode Pins

Pin No.	Port 5 MAC GMII
113	M5G_CRS
114	M5G_COL
115, 116, 118, 119	M5G_TXD[7:4]
120, 121, 122, 125	M5G_TXD[3:0]
126	M5G_TX_EN
127	M5G_GTX_CLK (125MHZ)
128	M5G_TX_CLK (25/2.5 MHz)
129	M5G_TX_ER
130	M5G_RX_ER
131	M5G_RX_CLK (125/25/2.5 MHz)
132	M5G_RX_DV
133, 135, 136, 137	M5G_RXD[0:3]
138, 139, 140, 141	M5G_RXD[4:7]

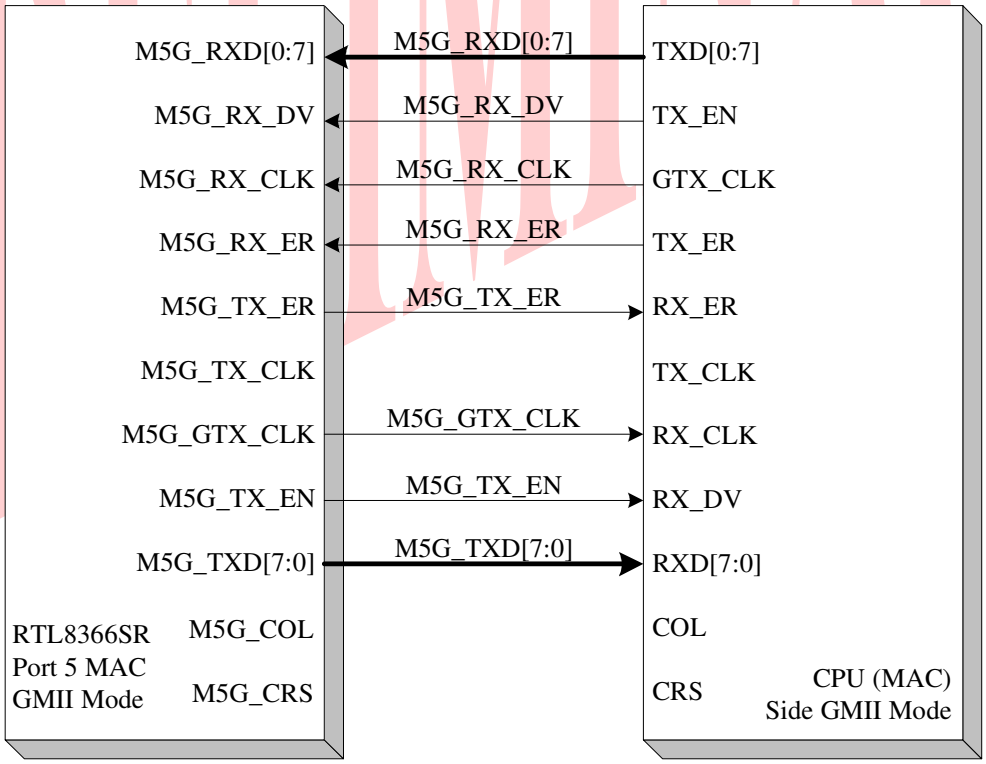


Figure 22. Signal Diagram of MAC GMII Mode Interface (1Gbps)

9.3.2. Port 5 MAC and Port 4 PHY RGMII Mode (1Gbps)

Port 5 MAC and Port 4 MAC of RTL8366SR supports RGMII interfaces to external CPU. The pin numbers and names are shown in Table 23 and Table 24. Figure 23 shows the signal diagram for Port 5 MAC or Port 4 PHY in RGMII interfaces.

Table 23. MAC5 RGMII Pins

Type	Port 5 MAC RGMII
113, 114, 115, 116	M5RG_TXD[3:0]
118	M5RG_TX_CTL
119	M5RG_TXC
120	M5RG_RXC
121	M5RG_RX_CTL
122, 125, 126, 127	M5RG_RXD[0:3]
117	M5RG_TXC_DELAY
128	M5RG_RXC_DELAY

Table 24. Port 4 MAC or PHY RGMII Pins

Type	Port 4 MAC RGMII	Port 4 PHY RGMII
130, 131, 132, 133	M4RG_TXD[3:0]	P4RG_RXD[3:0]
135	M4RG_TX_CTL	P4RG_RX_CTL
136	M4RG_TXC	P4RG_RXC
137	M4RG_RXC	P4RG_TXC
138	M4RG_RX_CTL	P4RG_TX_CTL
139, 140, 141, 142	M4RG_RXD[0:3]	P4RG_TXD[0:3]
129	M4RG_TXC_DELAY	P4RG_RXC_DELAY
143	M4RG_RXC_DELAY	P4RG_TXC_DELAY

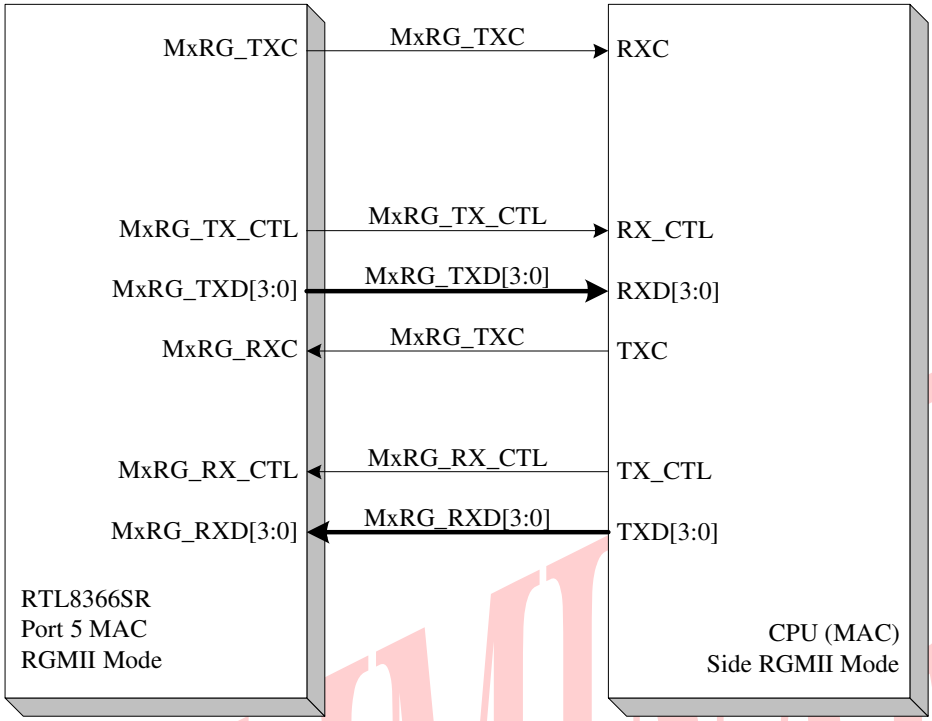


Figure 23. Signal Diagram of RGMII Mode Interface

9.3.3. Port 5 MAC and Port 4 PHY MII MAC/PHY Mode Interface (100Mbps)

Both Port 5 MAC and Port 4 MAC of RTL8366SR support MII MAC/PHY mode interfaces to external CPU. The pin numbers and names are shown in Table 25 and Table 26. Figure 24 shows the signal diagram for Port 5 MAC or Port 4 PHY in MII PHY mode interface.

Table 25. Port 5 MAC MII Pins

Type	Port 5 MAC MII PHY Mode
113	N/A
117	N/A
114, 115, 116, 118	M5MP_RXD[3:0]
119	M5MP_RX_DV
120	M5MP_RX_CLK
121	M5MP_TX_CLK
122	M5MP_TX_EN
125, 126, 127, 128	M5MP_TXD[3:0]

Table 26. Port 4 MII Pins

Type	Port 4 MAC MII MAC Mode	Port 4 PHY MII
129	M4MM_CRS	P4M_CRS
130	M4MM_COL	P4M_COL
131, 132, 133, 135	M4MM_TXD[3:0]	P4M_RXD[3:0]
136	M4MM_TX_EN	P4M_RX_DV
137	M4MM_TX_CLK	P4M_RX_CLK
138	M4MM_RX_CLK	P4M_TX_CLK
139	M4MM_RX_DV	P4M_TX_EN
140, 141, 142, 143	M4MM_RXD[0:3]	P4M_TXD[0:3]

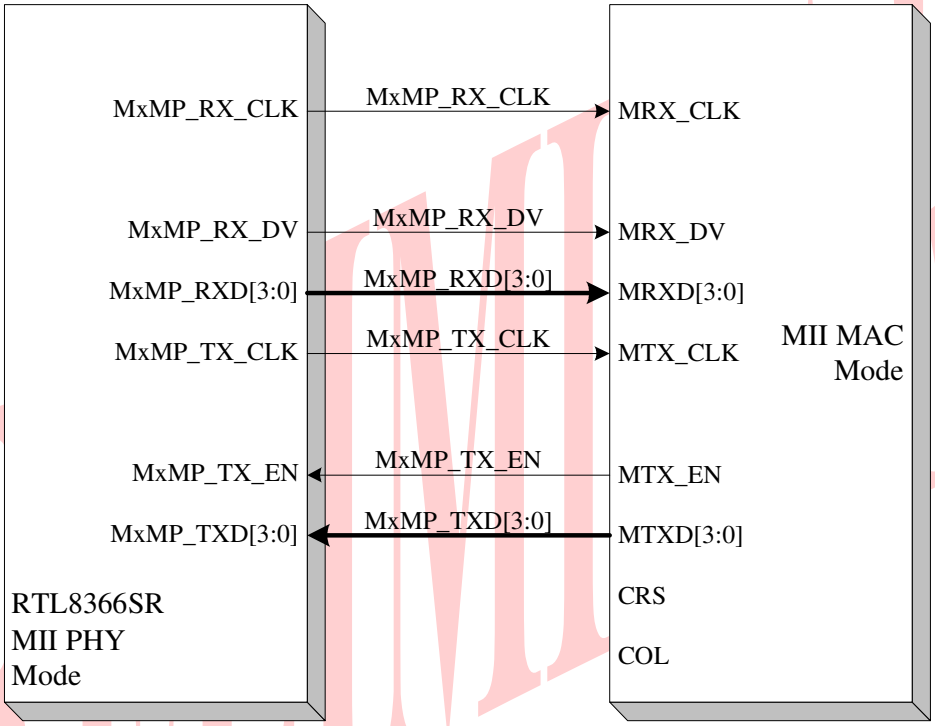


Figure 24. Signal Diagram of MII PHY Mode Interface (100Mbps)

9.4. Serdes Interface

RTL8366S and RTL8366SR support one Serdes interface for 1000Base-X application. Serdes interface can be enabled/disabled by pin strapping SEL_SDMODE[2:0]. These pins are pulled up with internal resisters, so user must connect these pins to GND via 1K-ohm resister for normal 5-Port Gigabit switch operation. Table 27 shows the configuration for Serdes interface. When SEL_SDMODE[2:0] = 0b001, Port 4 MAC (5-th Port) will support Copper and Serdes by configuration to switch the traffic toward the higher priority interface. Application diagram is shown in Figure 5. When Serdes is selected in this mode,

Port 4 MAC can't be selected as RGMII/MII PHY interface in RTL8366SR. 1000Base-X application example circuit for RTL8366S/SR is shown in Figure 25.

Table 27. Serdes Interface Mode Selection

SEL_SDMODE[2:0]	Application
0b000	Disable Serdes interface 5-Port 1000Base-TX Gigabit Switch.
0b001	5-th Port Copper or Fiber by configuration. 4-Port 1000Base-TX with 1-Port Copper or Fiber Configuration.
0b010 – 0b111 (default)	Reserved for future used.

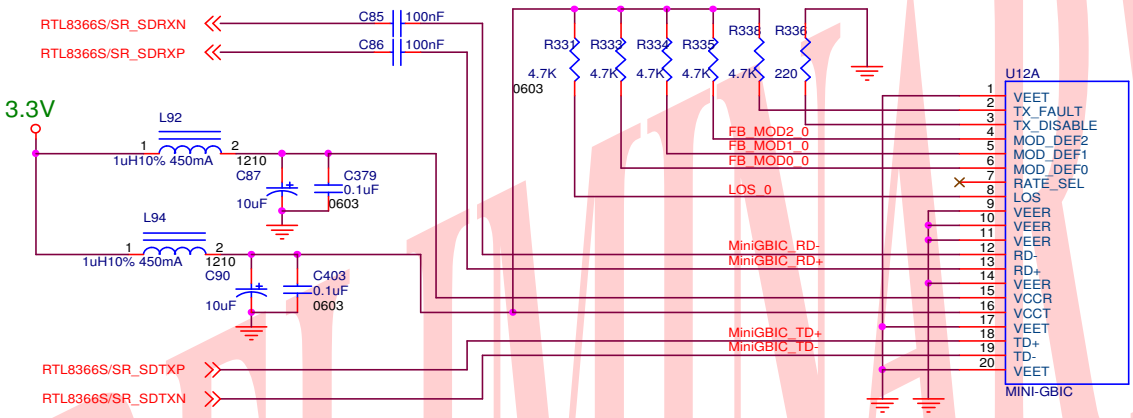


Figure 25. 1000Base-X Application Circuit for Mini-GBIC

10. Register Descriptions

10.1. Page 0: PCS Register (PHY 0~4)

Table 28. Register Descriptions

Name	Page	Register	Register Description	Default
PHY 0~4 Register	0	0	Control Register	0x1140
		1	Status Register	0x7949
		2	PHY Identifier 1	0x001C
		3	PHY Identifier 2	0xC960
		4	Auto-Negotiation Advertisement Register	0x0DE1
		5	Auto-Negotiation Link Partner Ability Register	0x0000
		6	Auto-Negotiation Expansion Register	0x0004
		7	Auto-Negotiation Page Transmit Register	0x2001
		8	Auto-Negotiation Link Partner Next Page Register	0x0000
		9	1000Base-T Control Register	0x0F00
		10	1000Base-T Status Register	0x0000
		11	Reserved	0x0000
		12	Reserved	0x0006
		13	Reserved	0xF880
		14	Reserved	0x0000
		15	Extended Status	0x3000
		16	ASIC Control Register	0x0060
		17	ASIC Control Register	0x4040
		18	ASIC Control Register	0x0000
		19	ASIC Control Register	0x0000
		20	ASIC Control Register	0x1060
		21	ASIC Control Register	0x0000
		22	ASIC Control Register	0x0000
		23	ASIC Control Register	0x2108
		24	ASIC Control Register	0x2740
		25	ASIC Control Register	0x8E00
		26	ASIC Control Register	0x0040
		27	ASIC Control Register	0x4013
		28	ASIC Control Register	0x8409
		29	ASIC Control Register	0x0000
		30	ASIC Control Register	0x0123
		31	ASIC Control Register	0x0000

10.1.1. Register 0: Control

Table 29. Register 0: Control

Reg.bit	Name	Mode	Description	Default
0.15	Reset	RW/SC	1=PHY reset. 0=Normal operation. This bit is self-clearing.	0
0.14	Loopback (Digital loopback)	RW	1: Enable loopback. This will loopback TXD to RXD and ignore all activity on the cable media 0: Normal operation This function is usable only when this PHY is operated in 10Base-T full duplex, 100Base-TX full duplex, or 1000Base-T full duplex.	0
0.13	Speed Selection[0]	RW	[0.6,0.13] Speed Selection[1:0] 11=Reserved 10=1000 Mbps 01=100 Mbps 00=10 Mbps When NWay is enabled, this bit reflects the result of auto-negotiation (Read only). When NWay is disabled, this bit can be set through SMI. (Read/Write).	0
0.12	Auto Negotiation Enable	RW	1: Enable auto-negotiation process 0: Disable auto-negotiation process This bit can be set through SMI (Read/Write).	1
0.11	Power Down	RW	1: Power down. All functions will be disabled except SMI function 0: Normal operation	0
0.10	Isolate	RW	1: Electrically isolates the PHY from GMII. PHY is still able to respond to MDC/MDIO 0: Normal operation	0
0.9	Restart Auto Negotiation	RW/SC	1: Restart Auto-Negotiation process 0: Normal operation	0
0.8	Duplex Mode	RW	1: Full duplex operation 0: Half duplex operation When NWay is enabled (Reg0.12=1), this bit reflects the result of auto-negotiation (Read only). When NWay is disabled (Reg0.12=0, force mode of UTP or 1000Base-X), this bit can be set through SMI (Read/Write).	1
0.7	Collision Test	RO	1 = Collision test enabled. 0 = Normal operation. When set, this bit will cause the COL signal to be asserted in response to the assertion of TXEN within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the de-assertion of TXEN.	0
0.6	Speed Selection[1]	RW	See bit 13	1
0.[5:0]	Reserved	RO	Reserved	000000

10.1.2. Register 1: Status

Table 30. Register 1: Status

Reg.bit	Name	Mode	Description	Default
1.15	100Base-T4	RO	0= No 100Base-T4 capability. RTL8366S/SR doesn't support 100Base-T4 mode and bit should always be 0.	0
1.14	100Base-TX-FD	RO	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
1.13	100Base-TX-HD	RO	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1
1.12	10Base-T-FD	RO	1: 10Base-T full duplex capable 0: Not 10Base-TX full duplex capable	1
1.11	10Base-T-HD	RO	1: 10Base-T half duplex capable 0: Not 10Base-TX half duplex capable	1
1.10	100Base-T2-FD	RO	0= No 100Base-T2 full duplex capability. RTL8366S/SR doesn't support 100Base-T2 mode and this bit should always be 0.	0
1.9	100Base-T2-HD	RO	0= No 100Base-T2 half duplex capability. RTL8366S/SR doesn't support 100Base-T2 mode and this bit should always be 0.	0
1.8	Extended Status	RO	1=Extended status information in Register 15 The RTL8366S/SR always support Extended Status Register.	1
1.7	Reserved	RO	Reserved	0
1.6	MF Preamble Suppression	RO	The RTL8366S/SR will accept management frames with preamble suppressed.	1
1.5	Auto-negotiate Complete	RO	1: Auto-negotiation process completed. 0: Auto-negotiation process not completed	0
1.4	Remote Fault	RO/LH	1=Remote fault indication from link partner has been detected. 0=No remote fault indication detected. This bit will remain set until it is cleared by reading register 1 via management interface.	0
1.3	Auto-Negotiation Ability	RO	1=Auto-negotiation capable. (permanently =1) 0=Without Auto-negotiation capability.	1
1.2	Link Status	RO/LL	1=Link has never failed since previous read. 0=Link has failed since previous read. If link fails, this bit will be set to 0 until bit is read.	0
1.1	Jabber Detect	RO/LH	1=Jabber detected. 0=No Jabber detected. Jabber is supported only in 10Base-T mode.	0
1.0	Extended Capability	RO	1=Extended register capable. (permanently =1) 0=Not extended register capable.	1

10.1.3. Register 2: PHY Identifier 1

The PHY Identifier Registers #1 and #2 together form a unique identifier for the PHY section of this device. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management.

Table 31. Register 2: PHY Identifier 1

Reg.bit	Name	Mode	Description	Default
2.[15:0]	OUI	RO	Composed of the 3rd to 18th bits of the Organizationally Unique Identifier (OUI), respectively	0x001C

10.1.4. Register 3: PHY Identifier 2

Table 32. Register 3: PHY Identifier 2

Reg.bit	Name	Mode	Description	Default
3.[15:10]	OUI	RO	Assigned to the 19th through 24th bits of the OUI	110010
3.[9:4]	Model Number	RO	Manufacturer's model number (16: Indicates RTL8366	010110
3.[3:0]	Revision Number	RO	Manufacturer's revision number (00: Indicates S	0000

10.1.5. Register 4: Auto-Negotiation Advertisement

This register contains the advertisement abilities of this device as they will be transmitted to its Link Partner during Auto-negotiation.

Note: Each time the link ability of the RTL8366S/SR is reconfigured, the auto-negotiation process should be executed to allow the configuration to take effect.

Table 33. Register 4: Auto-Negotiation Advertisement

Reg.bit	Name	Mode	Description	Default
4.15	Next Page	RO	1= Additional next pages exchange desired. 0= No additional next pages exchange desired.	0
4.14	Acknowledge	RO	Permanently=0	0
4.13	Remote Fault	RW	1: Advertises that the RTL8366S/SR has detected a remote fault 0: No remote fault detected	0
4.12	Reserved	RO	Reserved	0
4.11	Asymmetric Pause	RW	1: Advertises that the RTL8366S/SR has asymmetric flow control capability. 0=Without asymmetric flow control capability.	1
4.10	Pause	RW	1=Advertises that the RTL8366S/SR has flow control capability. 0=Without flow control capability.	1
4.9	100Base-T4	RO	1 = 100Base-T4 capable. 0 = Not 100Base-T4 capable. (Permanently =0)	0
4.8	100Base-TX-FD	RW	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
4.7	100Base-TX	RW	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1

4.6	10Base-T-FD	RW	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	1
4.5	10Base-T	RW	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	1
4.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	00001

The setting of Register 4 has no effect unless auto-negotiation is restarted or link down.

If 1000BASE-T is advertised, then the required next pages are automatically transmitted.

10.1.6. Register 5: Auto-Negotiation Link Partner Ability

This register contains the advertised abilities of the Link Partner as received during Auto-negotiation. The content changes after the successful Auto-negotiation.

Table 34. Register 5: Auto-Negotiation Link Partner Ability

Reg.bit	Name	Mode	Description	Default
5.15	Next Page	RO	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
5.14	Acknowledge	RO	1: Link Partner acknowledges reception of Fast Link Pulse (FLP) words 0: Not acknowledged by Link Partner	0
5.13	Remote Fault	RO	1: Remote Fault indicated by Link Partner 0: No remote fault indicated by Link Partner	0
5.12	Reserved	RO	Technology Ability Field Received code word bit 12	0
5.11	Asymmetric Pause		1=Asymmetric Flow control supported by Link Partner. 0=No Asymmetric flow control supported by Link Partner. When auto-negotiation is enabled, this bit reflects Link Partner ability. (Read only)	0
5.10	Pause	RO	1=Flow control supported by Link Partner. 0=No flow control supported by Link Partner. When auto-negotiation is enabled, this bit reflects Link Partner ability. (Read only)	0
5.9	100Base-T4	RO	1: 100Base-T4 supported by Link Partner 0: 100Base-T4 not supported by Link Partner	0
5.8	100Base-TX-FD	RO	1: 100Base-TX full duplex supported by Link Partner 0: 100Base-TX full duplex not supported by Link Partner	0
5.7	100Base-TX	RO	1: 100Base-TX half duplex supported by Link Partner 0: 100Base-TX half duplex not supported by Link Partner	0
5.6	10Base-T-FD	RO	1: 10Base-TX full duplex supported by Link Partner 0: 10Base-TX full duplex not supported by Link Partner	0
5.5	10Base-T	RO	1: 10Base-TX half duplex supported by Link Partner 0: 10Base-TX half duplex not supported by Link Partner	0
5.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	00000

10.1.7. Register 6: Auto-Negotiation Expansion

Table 35. Register 6: Auto-Negotiation Expansion

Reg.bit	Name	Mode	Description	Default
6.[15:5]	Reserved	RO	Ignore on read	0
6.4	Parallel Detection Fault	RO /LH	1=A fault has been detected via the Parallel Detection function. 0=No fault has been detected via the Parallel Detection function.	0
6.3	Link Partner Next Page Ability	RO	1= Link Partner is Next Page able. 0= Link Partner is not Next Page able.	0
6.2	Local Next Page Ability	RO	1= RTL8366S/SR is Next Page able. (permanently =0)	1
6.1	Page Received	RO /LH	1= A New Page has been received. 0= A New Page has not been received.	0
6.0	Link Partner Auto-Negotiation Ability	RO	If Auto-Negotiation is enabled, this bit means: 1= Link Partner is Auto-Negotiation able. 0= Link Partner is not Auto-Negotiation able.	0

10.1.8. Register 7: Auto-Negotiation Page Transmit Register

Table 36. Register 7: Auto-Negotiation Page Transmit Register

Reg.bit	Name	Mode	Description	Default
7.15	Next Page	RW	1=Another next page desired 0=No other next page to send	0
7.14	Reserved	RO	1=A fault has been detected via the Parallel Detection function. 0=No fault has been detected via the Parallel Detection function.	0
7.13	Message Page	RW	1=Message page	1
7.12	Acknowledge 2	RW	1=local device has the ability to comply with the message received. 0= local device has no ability to comply with the message received.	0
7.11	Toggle	RO	Toggle bit	0
7.[10:0]	Message/Unformatted Field	RW	Content of message/unformatted page	1

10.1.9. Register 8: Auto-Negotiation Link Partner Next Page Register

Table 37. Register 8: Auto-Negotiation Link Partner Next Page Register

Reg.bit	Name	Mode	Description	Default
8.15	Next Page	RO	Received link code word bit 15.	0
8.14	Acknowledge	RO	Received link code word bit 14.	0
8.13	Message Page	RO	Received link code word bit 13.	0
8.12	Acknowledge 2	RO	Received link code word bit 12.	0
8.11	Toggle	RO	Received link code word bit 11.	0
8.[10:0]	Message/Unformatted Field	RO	Received link code word bit 10:0.	0

10.1.10. Register 9: 1000Base-T Control Register

Table 38. Register 9: 1000Base-T Control Register

Reg.bit	Name	Mode	Description	Default
9.[15:13]	Test Mode	RW	Test mode select: 000=Normal mode. 001=Test mode 1 – Transmit waveform test. 010=Test mode 2 – Transmit jitter test in MASTER mode. 011=Test mode 3 – Transmit jitter test in SLAVE mode. 100=Test mode 4 – Transmitter distortion test. 101,110,111=Reserved	000
9.12	MASTER/SLAVE Manual Configuration Enable	RW	1=Enable MASTER/SLAVE manual configuration. 0=Disable MASTER/SLAVE manual configuration.	0
9.11	MASTER/SLAVE Configuration Value	RW	1=Configure PHY as MASTER during MASTER/SLAVE negotiation, only when 9.12 is set to logical one. 0= Configure PHY as SLAVE during MASTER/SLAVE negotiation, only when 9.12 is set to logical one.	1
9.10	Port Type	RW	1=Multi-port device 0=Single-port device	1
9.9	1000BASE-T Full Duplex	RW	1=Advertise PHY is 1000BASE-T full duplex capable. 0= Advertise PHY is not 1000BASE-T full duplex capable.	1
9.8	1000BASE-T Half Duplex	RW	1=Advertise PHY is 1000BASE-T half duplex capable. 0= Advertise PHY is not 1000BASE-T half duplex capable.	0
9.[7:0]	Reserved	RW	Reserved	0

10.1.11. Register 10: 1000Base-T Status Register

Table 39. Register 10: 1000Base-T Status Register

Reg.bit	Name	Mode	Description	Default
10.15	MASTER/SLAVE Configuration Fault	RO/LH/SC	1=MASTER/SLAVE configuration fault detected. 0=no MASTER/SLAVE configuration fault detected.	0
10.14	MASTER/SLAVE Configuration Resolution	RO	1=Local PHY configuration resolved to MASTER0=Local PHY configuration resolved to SLAVE	0
10.13	Local Receiver Status	RO	1=Local receiver OK. 0=Local receiver not OK.	0
10.12	Remote Receiver Status	RO	1=Remote receiver OK. 0= Remote receiver not OK.	0
10.11	Link Partner 1000BASE-T Full Duplex	RO	1=Link partner is capable of 1000BASE-T full duplex 0=Link partner is not capable of 1000BASE-T full duplex	0
10.10	1000BASE-T Half Duplex	RO	1=Link partner is capable of 1000BASE-T half duplex 0=Link partner is not capable of 1000BASE-T half duplex	0
10.[9:8]	Reserved	RO	Reserved	0
10.[7:0]	Idle Error Count	RO/SC	Idle error counter. The counter stops automatically when it reaches 0xFF.	0

10.1.12. Register 15: Extended Status

Table 40. Register 15: Extended Status

Reg.bit	Name	Mode	Description	Default
15.15	1000BASE-X Full Duplex	RO	1=1000BASE-X full duplex capable. 0=Not 1000BASE-X full duplex capable.	0
15.14	1000BASE-X Half Duplex	RO	1=1000BASE-X half duplex capable. 0=Not 1000BASE-X half duplex capable.	0
15.13	1000BASE-T Full Duplex	RO	1=1000BASE-T full duplex capable. 0=Not 1000BASE-T full duplex capable.	1
15.12	1000BASE-T Half Duplex	RO	1=1000BASE-T half duplex capable. 0=Not 1000BASE-T half duplex capable	1
15.[11:0]	Reserved	RO	Reserved	0

11. Electrical Characteristics

11.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 41. Absolute Maximum Ratings

Parameter	Min	Max	Units
Maximum junction temperatures (Tj)		+125	°C
Storage Temperature	-10	+125	°C
DVDDIO, AVDDH, and SVDDH Supply Referenced to DGND, AGND and SGND	GND-0.3	+3.63	V
DVDDL, AVDDL, SVDDL, and PLLVDDL Supply Referenced to DGND, AGND, SGND, and PLLGND	GND-0.3	+1.32	V
SVDDT Supply Reference to SGND	GND-0.3	+1.65	V
Digital Input Voltage	GND-0.3	VDDIO+0.3	V

11.2. Recommended Operating Range

Table 42. Operating Range

Parameter		Min	Typical	Max	Units
Ambient Operating Temperature (Ta)		0	-	70	°C
DVDDIO0, AVDDH and SVDDH Supply Voltage Range		3.135	3.3	3.465	V
DVDDIO1 Supply Voltage Range	3.3V	3.135	3.3	3.465	V
	2.5V	2.375	2.5	2.626	
	1.5V	1.425	1.5	1.575	
DVDDL, AVDDL, SVDDL, PLLVDDL Supply Voltage Range		1.0	1.05	1.26	V
SVDDT Supply Voltage Range	1.5V (Internal Regulator)	1.425	1.5	1.575	V
	1.05V	1.0	1.05V	1.26	

11.3. Thermal Characteristics

11.3.1. LQFP 216

11.3.1.1 Assembly Description

Table 43. Assembly Description

Package	Type	E-Pad LQFP216
	Dimension (L x W)	24 x 24 mm
	Thickness	1.4 mm
PCB	PCB Dimension (L x W)	101.6 x 114.3 mm^2
	PCB Thickness	1.6 mm
	Number of Cu Layer-PCB	2 layers (2S) -Top layer: 20% coverage of Cu, -Bottom layer: 75% coverage of Cu 4 layers (2S2P) -1st layer: 20% coverage of Cu -2nd layer: 80% coverage of Cu -3rd layer: 80% coverage of Cu -4th layer: 75% coverage of Cu

11.3.1.2 Material Property

Table 44. Material Property

Item		**Material**	**Thermal Conductivity K (W/m-k)**
Package	Die	Si	147
	Silver Paste	1033BF	1.5
	Lead Frame	CDA7025	168
	Mold Compound	7372	0.92
PCB		Cu	400
		FR4	0.2

11.3.1.3 Simulation Conditions

Table 45. Simulation Conditions

Input Power	3 W
Test Board (PCB)	2L(2S)/4L (2S2P)
Control Condition	Air Flow = 0, 1, 2, 3 m/s

11.3.1.4 Results Summaries

Table 46. Thermal Performance of E-Pad LQFP216 on 4L/2L PCB under Still Air Convention

	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}
4L PCB	17.3	8.1	5.4	1.8	9.8
2L PCB	42.4	11.7	7.4	2.6	25.7

θ_{JA}:Junction to ambient thermal resistance,

θ_{JB}: Junction to board thermal resistance,

θ_{JC}: Junction to case thermal resistance

Ψ_{JT}: Junction to top center of package thermal characterization

Ψ_{JB}: Junction to bottom surface center of PCB thermal characterization

Table 47. Thermal Performance of E-Pad LQFP216 on 4L PCB under Forced Convection

	Air Flow (m/s)	0	1	2	3
4L PCB	θ JA	17.3	14.4	13.4	12.6
	Ψ JT	1.8	2	2.3	2.6
	Ψ JB	9.8	9.4	9.3	9.2
2L PCB	θ JA	42.4	34.3	31.4	28.9
	Ψ JT	2.6	3.4	4.3	4.8
	Ψ JB	25.7	24.6	24.4	24.1

11.3.2. LQFP 164

11.3.2.1 Assembly Description

Table 48. Assembly Description

Package	Type	E-Pad LQFP164
	Dimension (L x W)	20 x 20 mm
	Thickness	1.4 mm
PCB	PCB Dimension (L x W)	85 x 100 mm
	PCB Thickness	1.6 mm
	Number of Cu Layer-PCB	2-Layer: All top layer Cu coverage is 25% except for package gnd plane & 5 blocks shown in Page 7 All bottom layer Cu coverage is 75%, except for Power Jack & Phone Jack Blocks 4-Layer: All top layer Cu coverage is 20% except for package gnd plane & 5 blocks shown in Page 7 Middle Cu Coverage: 80% All bottom layer Cu coverage is 75%, except for Power Jack & Phone Jack Blocks

11.3.2.2 Material Property

Table 49. Material Property

Item		Material	Thermal Conductivity K (W/m-k)
Package	Die	Si	147
	Silver Paste	1033BF	2.5
	Lead Frame	CDA7025	168
	Mold Compound	7372	0.88
PCB		Cu	400
		FR4	0.2

11.3.2.3 Simulation Conditions

Table 50. Simulation Conditions

Input Power	2.7 W
Test Board (PCB)	2L (2S) / 4L (2S2P)
Control Condition	Air Flow = 0, 1, 2, 3 m/s

11.3.2.4 Results Summaries

Table 51. Thermal Performance of E-Pad LQFP164 on 4L/2L PCB under Still Air Convention

	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}
4L PCB	14.1	3.1	5.5	1.7	6.0
2L PCB	18.8	3.4	6.5	2.2	9.6

θ_{JA}:Junction to ambient thermal resistance,

θ_{JB} : Junction to board thermal resistance,

θ_{JC}: Junction to case thermal resistance

Ψ_{JT}**:** Junction to top center of package thermal characterization

Ψ_{JB}: Junction to bottom surface center of PCB thermal characterization

Table 52. Thermal Performance of E-Pad LQFP164 on 4L/2L PCB under Forced Convection

	Air Flow (m/s)	0	1	2	3
4L PCB	θ_{JA}	14.1	10.9	10.0	9.5
	Ψ_{JT}	1.7	1.9	2.3	2.8
	Ψ_{JB}	6.0	5.9	5.9	5.8
2L PCB	θ_{JA}	18.8	15.2	14.1	13.4
	Ψ_{JT}	2.2	2.5	2.9	3.5
	Ψ_{JB}	9.6	9.2	9.1	9.0

11.4. DC Characteristics

Table 53. DC Characteristics

Parameter	SYM	Condition	Min	Typical	Max	Units
Power Supply Current for DVDDIO1 (for General Purpose interface)	$I_{DVDDIO1}$			65		mA
Power Supply Current for SVDDH (for SerDes interface)	I_{SVDDH}			38		mA
Power Supply Current for SVDDL (for SerDes interface)	I_{SVDDL}			58		mA
System Idle						
Power Supply Current for DVDDIO0	$I_{DVDDIO0}$			5		mA
Power Supply Current for AVDDH	I_{AVDDH}			380		mA
Power Supply Current for DVDDL	I_{DVDDL}			149		mA
Power Supply Current for AVDDL (include PLLVDDL)	I_{AVDDL}			190		mA
Total Power Consumption for all Ports	PS			1626.5		mW
1000M Active						
Power Supply Current for DVDDIO0	$I_{DVDDIO0}$			42		mA
Power Supply Current for AVDDH	I_{AVDDH}			284		mA
Power Supply Current for DVDDL	I_{DVDDL}			997		mA
Power Supply Current for AVDDL (include PLLVDDL)	I_{AVDDL}			519		mA
Total Power Consumption for all Ports	PS			2667.6		mW
100M Active						
Power Supply Current for DVDDIO0	$I_{DVDDIO0}$			43		mA
Power Supply Current for AVDDH	I_{AVDDH}			203		mA
Power Supply Current for DVDDL	I_{DVDDL}			271		mA
Power Supply Current for AVDDL (include PLLVDDL)	I_{AVDDL}			184		mA
Total Power Consumption for all Ports	PS			1289.6		mW
10M Active						
Power Supply Current for DVDDIO0	$I_{DVDDIO0}$			24		mA

Parameter	SYM	Condition	Min	Typical	Max	Units
Power Supply Current for AVDDH	I_{AVDDH}			550		mA
Power Supply Current for DVDDL	I_{DVDDL}			150		mA
Power Supply Current for AVDDL (include PLLVDDL)	I_{AVDDL}			71		mA
Total Power Consumption for all Ports	PS			2126.3		mW
VDDIO = 3.3V						
TTL Input High Voltage	V_{ih}		2.0			V
TTL Input Low Voltage	V_{il}				0.8	V
Output High Voltage	V_{oh}		2.7			V
Output Low Voltage	V_{ol}				0.6	V
VDDIO = 1.5V						
TTL Input High Voltage	V_{ih}		1.0			V
TTL Input Low Voltage	V_{il}				0.5	V
Output High Voltage	V_{oh}		1.1			V
Output Low Voltage	V_{ol}				0.4	V

11.5. AC Characteristics

11.5.1. EEPROM SMI Host Mode Timing Characteristics

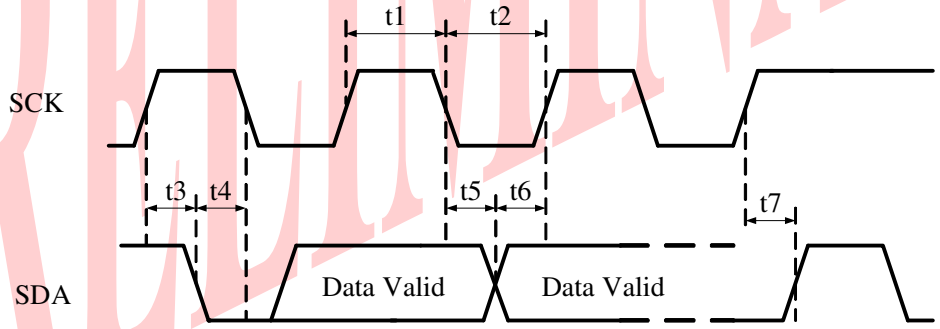


Figure 26. EEPROM SMI Host Mode Timing Characteristics

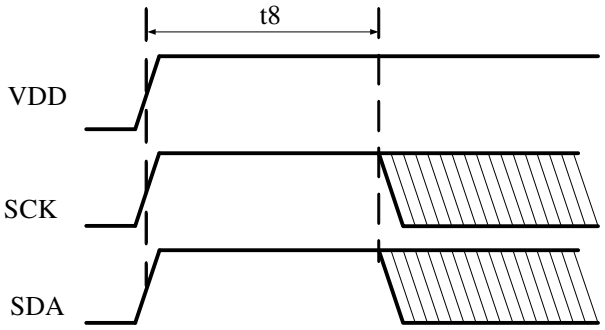


Figure 27. SCK/SDA Power on Timing

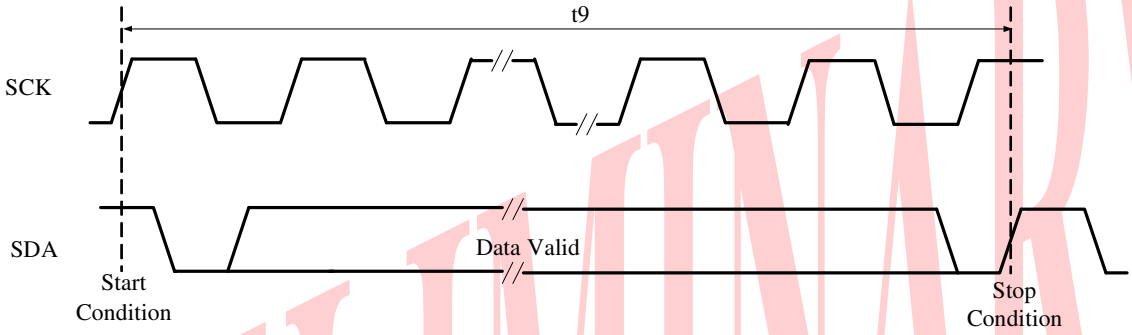


Figure 28. EEPROM Auto-Load Timing

Table 54. EEPROM SMI Host Mode Timing Characteristics

Symbol	Description	I/O	Min	Typical	Max	Units
t1	SCK high time	O	-	840	-	ns
t2	SCK low time	O	-	840	-	ns
t3	START condition setup time	O	-	840	-	ns
t4	START condition hold time	O	-	840	-	ns
t5	Data hold time	O	-	860	-	ns
t6	Data setup time	O	-	840	-	ns
t7	STOP condition setup time	O	-	860	-	ns
t8	SCK/SDA active from power on	O	-	100	-	ms
t9	EEPROM Auto-Load time	O	-	32	-	ms

11.5.2. EEPROM SMI Slave Mode Timing Characteristics

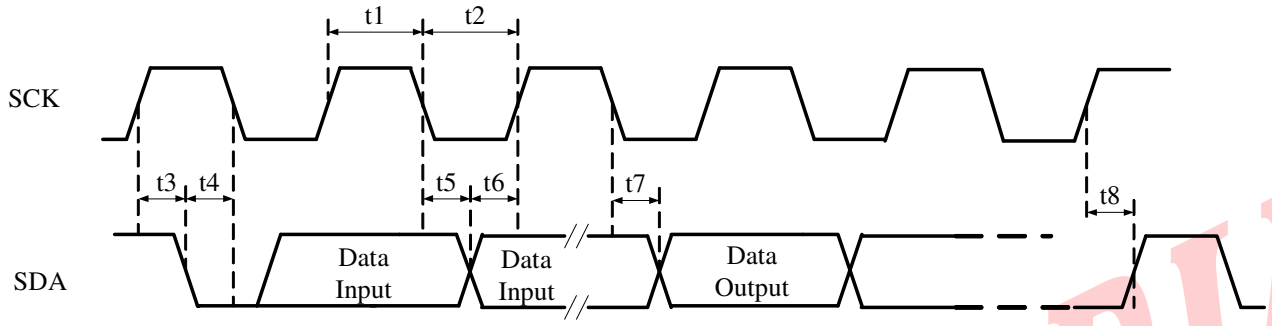


Figure 29. EEPROM SMI Slave Mode Timing Characteristics

Table 55. EEPROM SMI Slave Mode Timing Characteristics

Symbol	Description	I/O	Min	Typical	Max	Units
t1	SCK high time	I	4.0	-	-	µs
t2	SCK low time	I	4.0	-	-	µs
t3	START condition setup time	I	4.0	-	-	µs
t4	START condition hold time	I	4.0	-	-	µs
t5	Data hold time	I	5.0	-	-	µs
t6	Data setup time	I	250	-	-	ns
t7	Clock to data output delay	O	-	9	-	ns
t8	STOP condition setup time	I	4.0	-	-	µs

11.5.3. GMII/MII Timing Characteristics

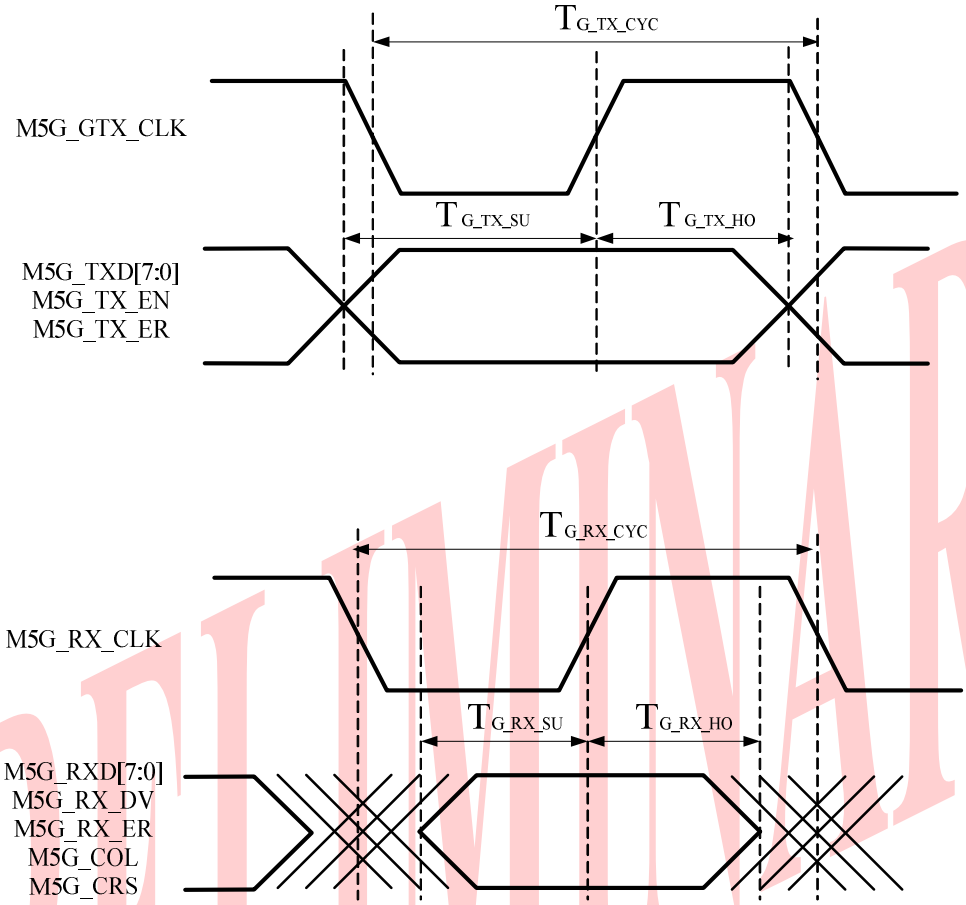
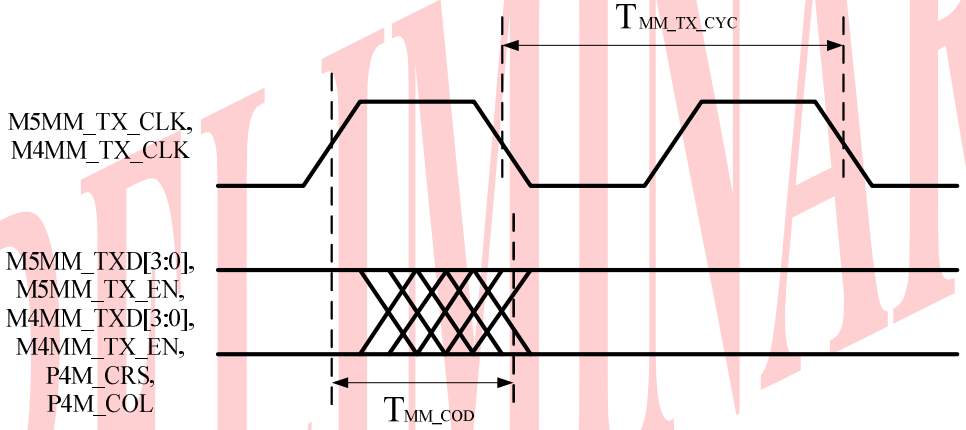


Figure 30. GMII Timing Characteristics

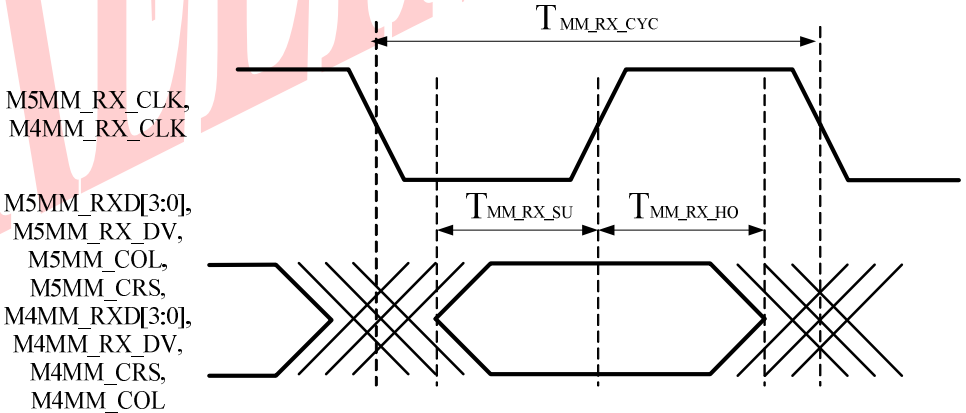
Table 56. GMII Timing Characteristics

Parameter	SYM	Description/Condition	I/O	Min	Typical	Max	Units
1000Base-T M5G_GTX_CLK Output Cycle Timing	$T_{G\_TX\_CYC}$	125MHz clock output.	O	7.5	8.0	8.5	ns
1000Base-T M5G_RX_CLK Input Cycle Time	$T_{G\_RX\_CYC}$	125MHz clock input.	I	7.5	8.0	-	ns
1000Base-T M5G_TXD[7:0], M5G_TX_ER, and M5G_TX_EN, Output Setup Time	$T_{G\_TX\_SU}$		O	2.5	5.8	-	ns

Parameter	SYM	Description/Condition	I/O	Min	Typical	Max	Units
1000Base-T M5G_TXD[7:0], M5G_TX_ER, and M5G_TX_EN, Output Hold Time	$T_{G\_TX\_HO}$		O	0.5	1.5	-	ns
1000Base-T M5G_RXD[7:0], M5G_RX_DV, M5G_RX_ER, M5G_CRS , and M5G_COL Input Setup Time	$T_{G\_RX\_SU}$		I	2	-	-	ns
1000Base-T M5G_RXD[7:0], M5G_RX_DV, M5G_RX_ER, M5G_CRS , and M5G_COL Input Hold Time	$T_{G\_RX\_HO}$		I	0	-	-	ns



MII MAC mode Clock to Data Output Delay Timing

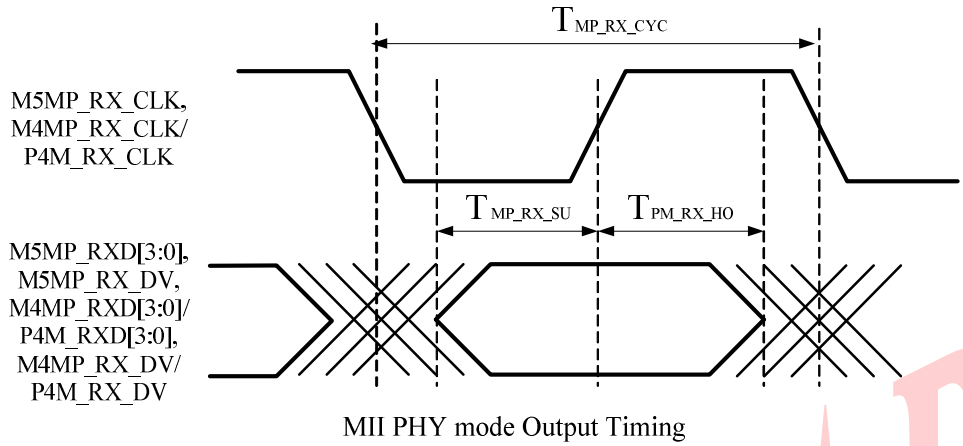


MII MAC mode Iuput Timing

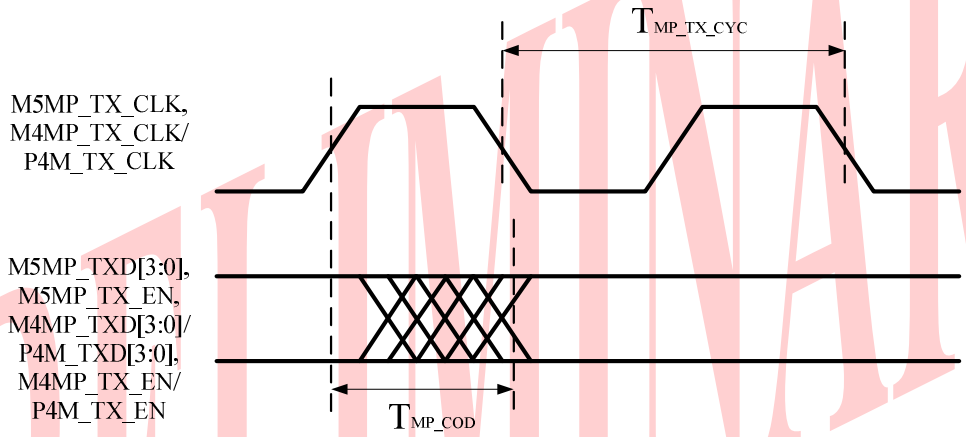
Figure 31. MII MAC mode Timing Characteristics

Table 57. MII MAC mode Timing Characteristics

Parameter	SYM	Description/Condition	I/O	Min	Typical	Max	Units
100Base-T M5MM_TX_CLK, M4MM_TX_CLK, M5MM_RX_CLK, and M4MM_RX_CLK Input Cycle Time	1 / $T_{MM\_TX\_CYC}$ 1 / $T_{MM\_RX\_CYC}$	25MHz clock input.	I	25-100 ppm	25	25+100 ppm	MHz
10Base-T M5MM_TX_CLK, M4MM_TX_CLK, M5MM_RX_CLK, and M4MM_RX_CLK Input Cycle Time	$T_{MM\_TX\_CYC}$ $T_{MM\_RX\_CYC}$	2.5MHz clock input.	I	2.5-100 ppm	2.5	2.5+100 ppm	MHz
M5MM_TX_CLK, M4MM_TX_CLK to M5MM_TXD[3:0], M5MM_TX_EN, M4MM_TXD[3:0], M4MM_TX_EN, P4M_CRS, P4M_COL Output delay Time	T_{MM_COD}		O	0	6	25	ns
M5MM_RXD[3:0], M5MM_RX_DV, M5MM_COL, M5MM_CRS, M4MM_RXD[3:0], M4MM_RX_DV, M4MM_CRS, M4MM_COL Input Setup Time	$T_{MM\_RX\_SU}$		I	10	-	-	ns
M5MM_RXD[3:0], M5MM_RX_DV, M5MM_COL, M5MM_CRS, M4MM_RXD[3:0], M4MM_RX_DV, M4MM_CRS, M4MM_COL Input Hold Time	$T_{MM\_RX\_HO}$		I	10	-	-	ns



MII PHY mode Output Timing



MII PHY mode Clock Output to Data Input Delay Timing

Figure 32. MII PHY mode Timing Characteristics

Table 58. MII PHY mode Timing Characteristics

Parameter	SYM	Description/Condition	I/O	Min	Typical	Max	Units
100M M5MP_RX_CLK, M4MP_RX_CLK/P4M_RX_CLK, M5MP_TX_CLK, and M4MP_TX_CLK/P4M_TX_CLK Output Cycle Time	1 / $T_{MP\_RX\_CYC}$ 1 / $T_{MP\_TX\_CYC}$	25MHz clock Output.	O	25-100 ppm	25	25+100 ppm	MHz
10M M5MP_RX_CLK, M4MP_RX_CLK/P4M_RX_CLK, M5MP_TX_CLK, and M4MP_TX_CLK/P4M_TX_CLK Output Cycle Time	1 / $T_{MP\_RX\_CYC}$ 1 / $T_{MP\_TX\_CYC}$	2.5MHz clock Output.	O	2.5-100 ppm	2.5	2.5+100 ppm	MHz

Parameter	SYM	Description/Condition	I/O	Min	Typical	Max	Units
100M M5MP_RXD[3:0], M5MP_RX_DV, M4MP_RXD[3:0]/P4M_RXD[3:0], and M4MP_RX_DV/P4M_RX_DV to M5MP_RX_CLK and M4MP_RX_CLK/P4M_RX_CLK Output Setup Time	$T_{MP\_RX\_SU}$		O	10	18	-	ns
100M M5MP_RXD[3:0], M5MP_RX_DV, M4MP_RXD[3:0]/P4M_RXD[3:0], and M4MP_RX_DV/P4M_RX_DV to M5MP_RX_CLK and M4MP_RX_CLK/P4M_RX_CLK Output Hold Time	$T_{MP\_RX\_HO}$		O	10	21.6	-	ns
100M M5MP_TX_CLK, M4MP_TX_CLK/P4M_TX_CLK clock output to M5MP_TXD[3:0], M5MP_TX_EN, M4MP_TXD[3:0]/P4M_TXD[3:0], M4MP_TX_EN/P4M_TX_EN input delay Time	T_{MP_COD}		I	0	-	25	ns

11.5.4. RGMII Timing Characteristics

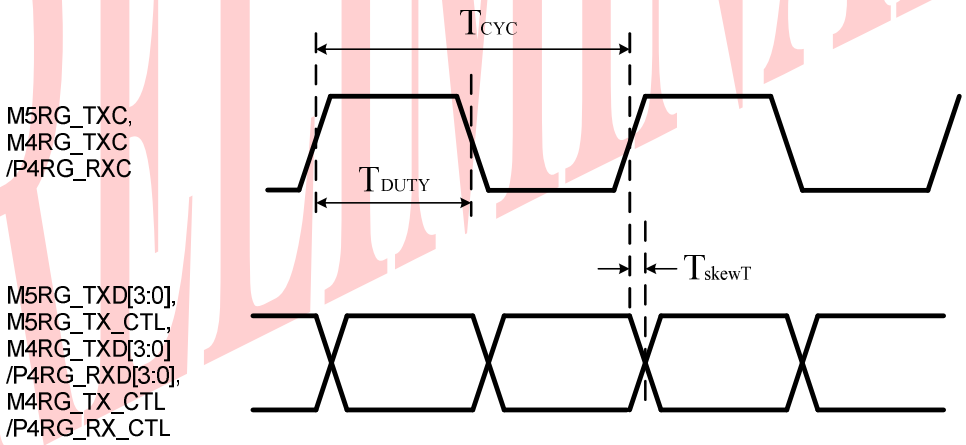


Figure 33. RGMII Output Timing Characteristics (M5RG_TXC_DELAY=0 or M4RG_TXC_DELAY/P4RG_RXC_DELAY=0)

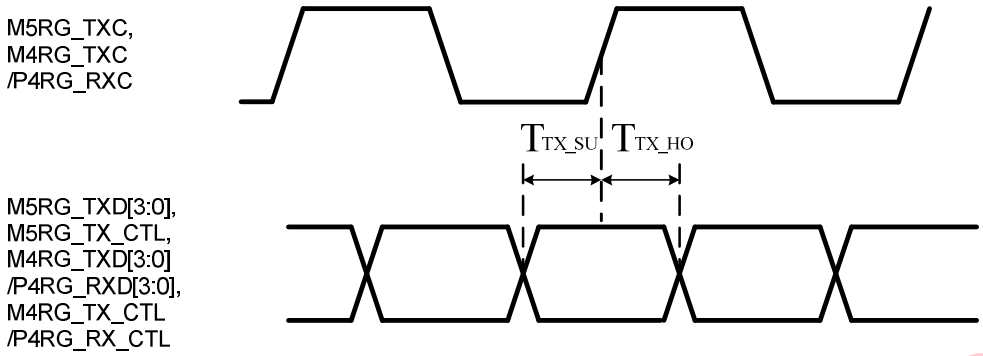


Figure 34. RGMII Output Timing Characteristics (M5RG_TXC_DELAY=1 or M4RG_TXC_DELAY /P4RG_RXC_DELAY=1)

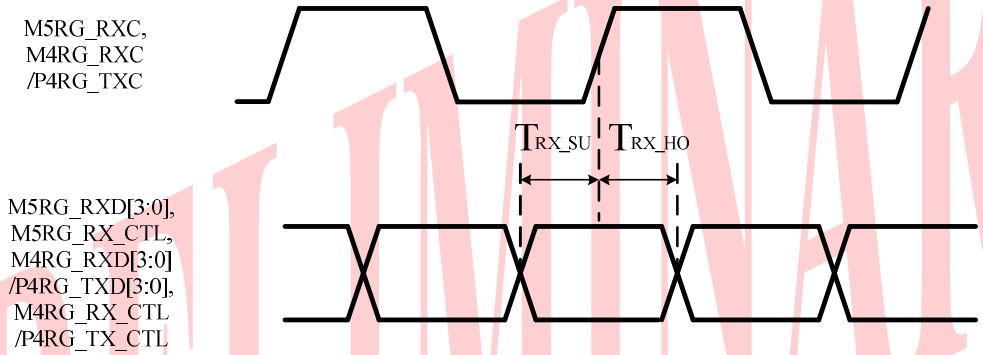


Figure 35. RGMII Input Timing Characteristics (M5RG_RXC_DELAY=0 or M4RG_RXC_DELAY /P4RG_TXC_DELAY=0)

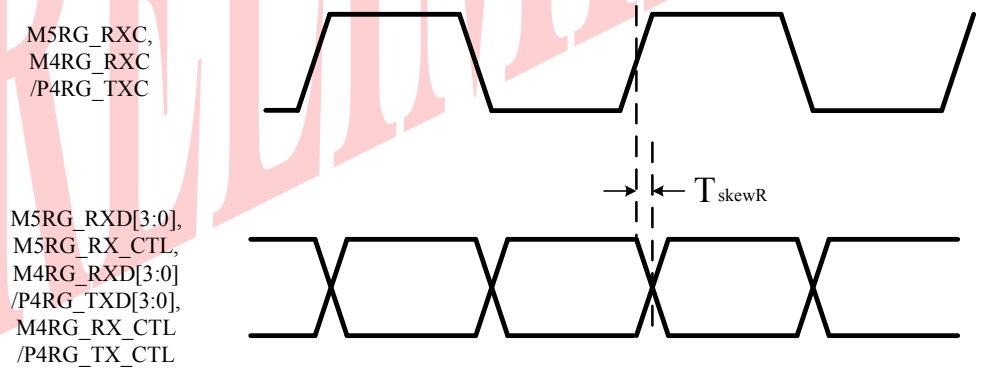


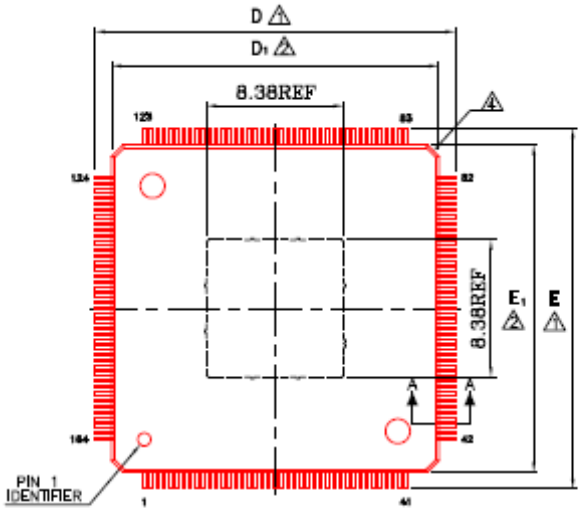
Figure 36. RGMII Input Timing Characteristics (M5RG_RXC_DELAY=1 or M4RG_RXC_DELAY /P4RG_TXC_DELAY=1)

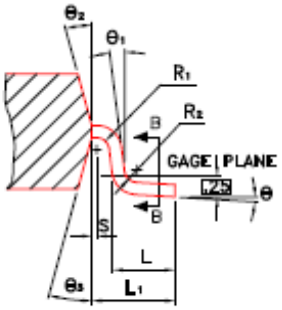
Table 59. RGMII Timing Characteristics

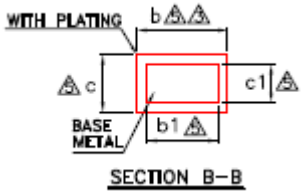
Parameter	SYM	Description/Condition	I/O	Min	Typical	Max	Units
1000M M5RG_TXC, M4RG_TXC/P4RG_RXC Output Cycle Time	T_{TX_CYC}	125MHz clock output. Refer to Figure 33.	O	7.2	8	8.8	ns
100M M5RG_TXC, M4RG_TXC/P4RG_RXC Output Cycle Time	T_{TX_CYC}	25MHz clock output. Refer to Figure 33.	O	36	40	44	ns
10M M5RG_TXC, M4RG_TXC /P4RG_RXC Output Cycle Time	T_{TX_CYC}	2.5MHz clock output. Refer to Figure 33.	O	360	400	440	ns
M5RG_TXD[3:0], M5RG_TX_CTL , M4RG_TXD[3:0]/P4RG_RXD[3:0] , M4RG_TX_CTL/P4RG_RX_CTL to M5RG_TXC, M4RG_TXC /P4RG_RXC Output Skew	T_{skewT}	Disable Output Clock delay (M5RG_TXC_DELAY=0 or M4RG_TXC_DELAY/P4RG_ RXC_DELAY=0). Refer to Figure 33.	O	-500	440	500	ps
M5RG_TXD[3:0], M5RG_TX_CTL, M4RG_TXD[3:0]/P4RG_RXD[3:0] , M4RG_TX_CTL/P4RG_RX_CTL to M5RG_TXC, M4RG_TXC/P4RG_RXC Output Setup Time	T_{TX_SU}	Enable Output Clock delay (M5RG_TXC_DELAY=1 or M4RG_TXC_DELAY/P4RG_ RXC_DELAY=1). Refer to Figure 34.	O	1.2	1.6	-	ns
M5RG_TXD[3:0], M5RG_TX_CTL, M4RG_TXD[3:0]/P4RG_RXD[3:0] , M4RG_TX_CTL, P4RG_RX_CTL to M5RG_TXC, M4RG_TXC /P4RG_RXC Output Hold Time	T_{TX_HO}	Enable Output Clock delay (M5RG_TXC_DELAY=1 or M4RG_TXC_DELAY/P4RG_ RXC_DELAY=1). Refer to Figure 34.	O	1.2	2.2	-	ns
M5RG_RXD[3:0], M5RG_RX_CTL, M4RG_RXD[3:0]/P4RG_TXD[3:0] , M4RG_RX_CTL/P4RG_TX_CTL to M5RG_RXC, M4RG_RXC/P4RG_TXC Input Setup Time	T_{RX_SU}	Disable Input Clock delay (M5RG_RXC_DELAY=0 or M4RG_RXC_DELAY/P4RG_ TXC_DELAY=0). Refer to Figure 35.	I	1.0	-	-	ns
M5RG_RXD[3:0], M5RG_RX_CTL, M4RG_RXD[3:0]/P4RG_TXD[3:0] , M4RG_RX_CTL /P4RG_TX_CTL to M5RG_RXC, M4RG_RXC/P4RG_TXC Input Hold Time	T_{RX_HO}	Disable Input Clock delay (M5RG_RXC_DELAY=0 or M4RG_RXC_DELAY/P4RG_T XC_DELAY=0). Refer to Figure 35.	I	1.0	-	-	ns
M5RG_RXD[3:0], M5RG_RX_CTL, M4RG_RXD[3:0]/P4RG_TXD[3:0] , M4RG_RX_CTL/P4RG_TX_CTL to M5RG_RXC, M4RG_RXC/P4RG_TXC Input Skew	T_{skewR}	Enable Input Clock delay. (M5RG_RXC_DELAY=1 or M4RG_RXC_DELAY/P4RG_ TXC_DELAY=1). Refer to Figure 36.	I	0	-	1.8	ns

12. Mechanical Dimensions

12.1. LQ164EPAD





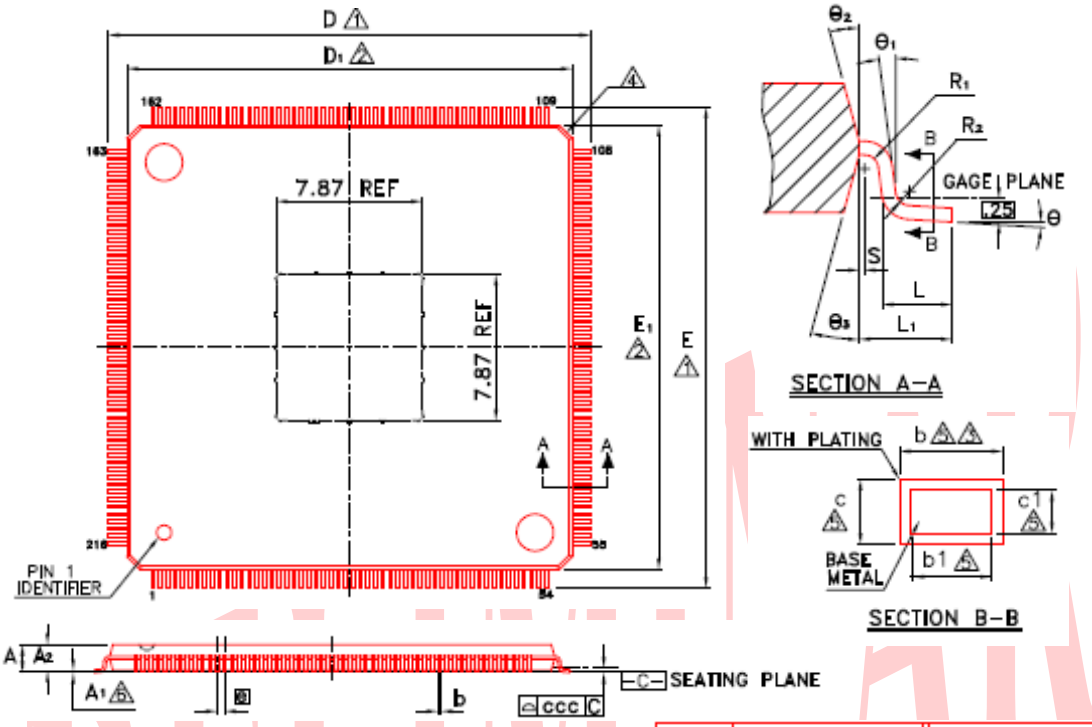


NOTE :

1. TO BE DETERMINED AT SEATING PLANE C .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026
9. SPECIAL CHARACTERISTICS C CLASS: ccc

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.60	---	---	0.063
A1	0.05	---	0.15	0.002	---	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	---	0.20	0.004	---	0.008
c1	0.09	0.12	0.16	0.004	0.005	0.006
D	21.60	22.00	22.40	0.850	0.866	0.882
D1	---	20.00	---	---	0.787	---
E	21.60	22.00	22.40	0.850	0.866	0.882
E1	---	20.00	---	---	0.787	---
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	---	1.00	---	---	0.039	---
R1	0.08	---	---	0.003	---	---
R2	0.08	---	---	0.003	---	---
S	0.20	---	---	0.008	---	---
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	---	---	0°	---	---
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

12.2. LQ216EPAD



NOTE :

1. TO BE DETERMINED AT SEATING PLANE C .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 .
9. SPECIAL CHARACTERISTICS C CLASS: ccc

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	0.14	0.20	0.004	0.006	0.008
c1	0.09	0.12	0.16	0.004	0.005	0.006
D	25.85	26.00	26.15	1.018	1.024	1.030
D1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E1	23.90	24.00	24.10	0.941	0.945	0.949
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	—	0.003	—	—
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

13. Ordering Information

Table 60. Ordering Information

Part Number	Package	Status
RTL8366S-GR	LQ164-EPAD	
RTL8366SR-GR	LQ216-EPAD	

Note:
1. RTL8366S-GR is for 5-Port Gigabit Switch application.
2. RTL8366SR-GR is for 5-Port Gigabit Router application.

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