



RTL8710AF

SINGLE-CHIP 802.11b/g/n 1T1R WLAN SoC

Release DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

| Revision | Release Date | Summary |
|----------|--------------|---|
| 0.0 | 2015/12/01 | First release. |
| 1.0 | 2016/1/7 | Correct timer source clock |
| 1.01 | 2016/2/16 | Correct pin function group table |
| 1.02 | 2016/5/13 | 1. Correct pin assignment figure 2. Correct pin function group table 3. Correct power on trap table |

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1. General Description

Realtek RTL8710AF is a highly integrated single-chip low power 802.11n Wireless LAN (WLAN) network controller. It combines an ARM-CM3 MCU, WLAN MAC, a 1T1R capable WLAN baseband, and RF in a single chip. It also provides a bunch of configurable GPIOs which are configured as digital peripherals for different applications and control usage.

RTL8710AF integrates internal memories for complete WIFI protocol functions. The embedded memory configuration also provides simple application developments.

2. Features

General

- Package QFN48 (6x6mm²)
- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Complete 802.11n solution for 2.4GHz band
- 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth
- 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating in 802.11n mode

Standards Supported

- 802.11b/g/n compatible WLAN
- 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services

- WIFI WPS support
- WIFI Direct support
- Light Weight TCP/IP protocol

WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism

WLAN PHY Features

- 802.11n OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz bandwidth transmission

- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 64QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC

Peripheral Interfaces

- 2 high speed UART interface with baud rate up to 4MHz, and only one of them has flow control
- 1 log UART with standard baud rate support
- 1 I²C interface
- 1 SPI supported with baud rate up to 10.4MHz (master).
- Maximum 17 GPIO pins

3. Block Diagram

3.1. Functional Block Diagram

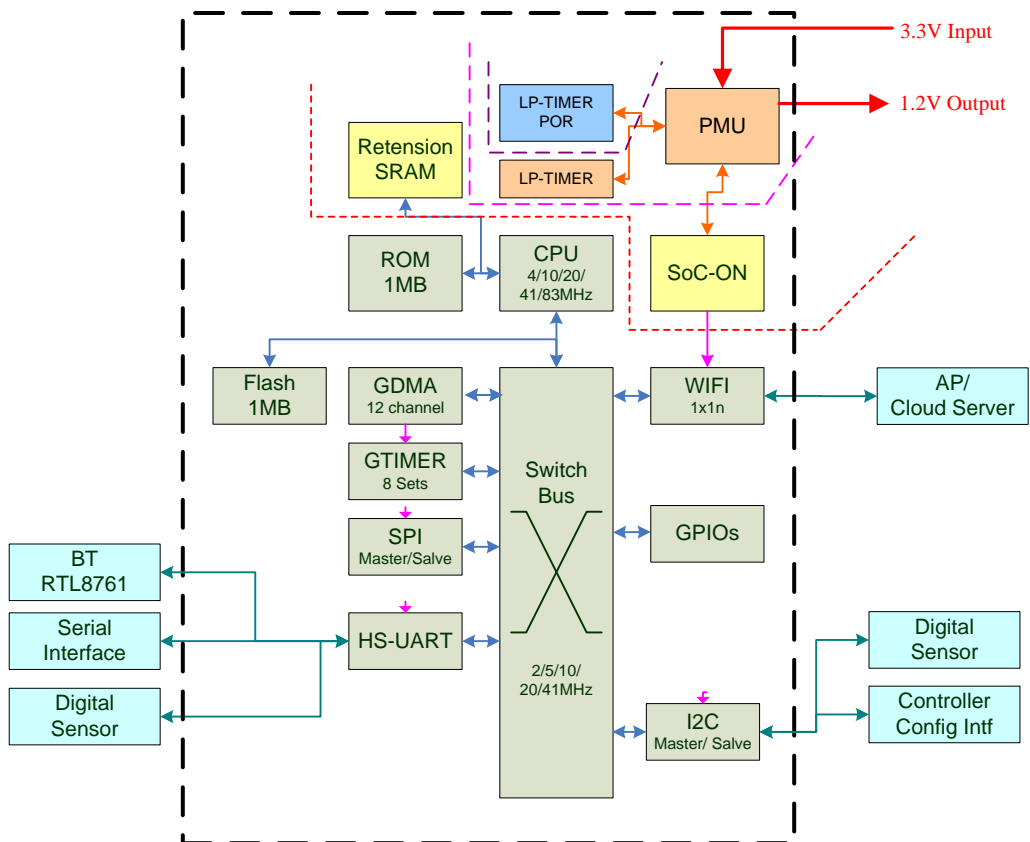


Figure 1. Block Diagram

3.2. WIFI Application Diagram

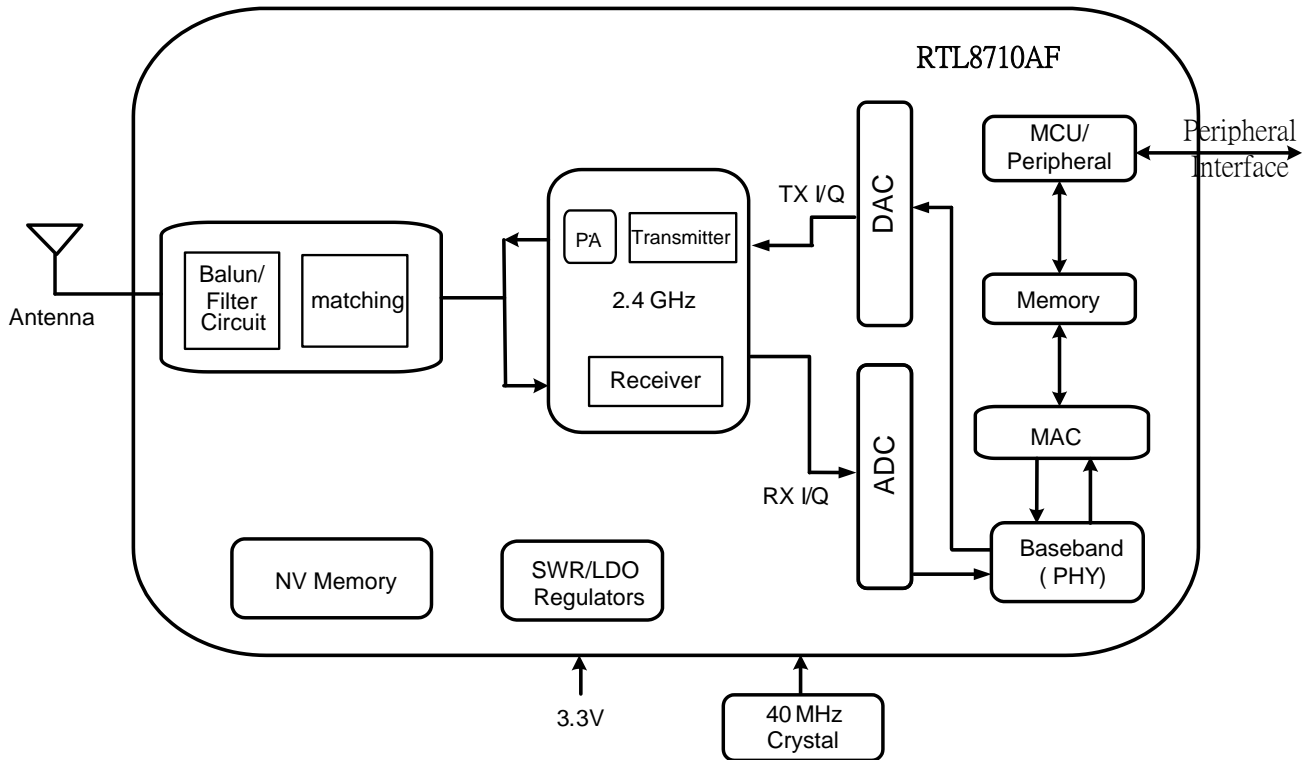


Figure 2. Single-Band 11n (1x1) Solution

3.3. Power Supply Application Diagram

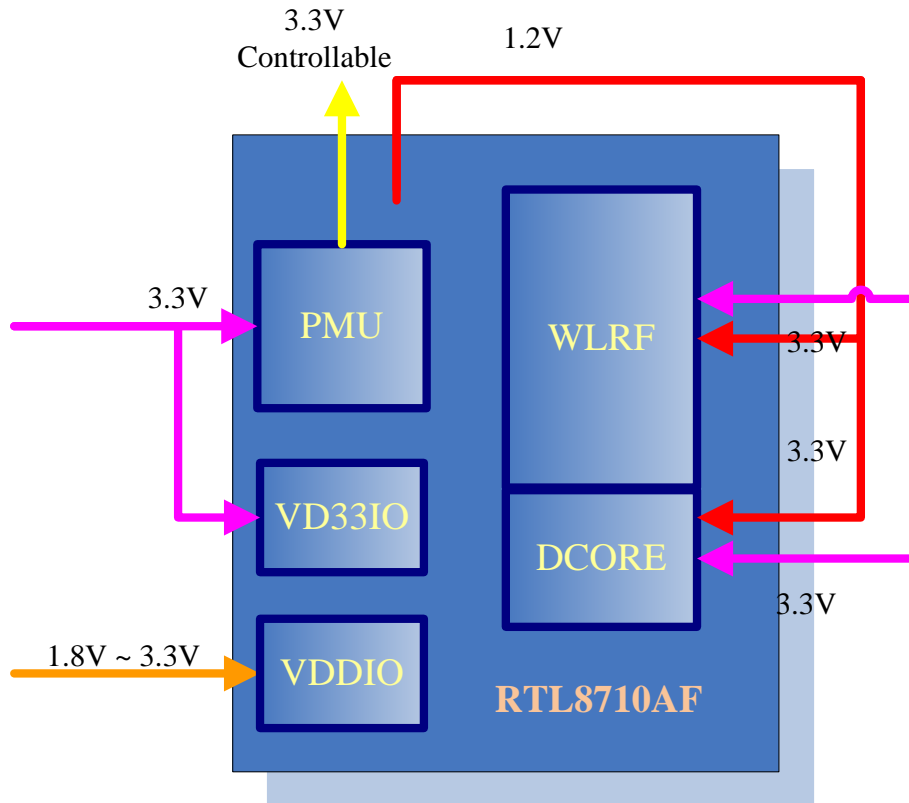


Figure 3. Power Supply Architecture

The integrated Power Management Unit (PMU) provides the following features:

- 1.2V power bulk or LDO selectable.
- 3.3V power source integrated power cut controlled by FW.

4. Memory Mapping

4.1. Programming Space

| Name | Mode | Physical | Size | IP Function |
|------|------|-------------|-------|---|
| Code | | 0x0000_0000 | 1MB | Instruction Memory (ROM) |
| | | 0x000F_FFFF | | |
| | | 0x1000_0000 | 448KB | Inter SRAM: BD SRAM and Buffer SRAM share total 448KB physical sram |
| | | 0x1006_FFFF | | |
| | | 0x1FFF_0000 | 64KB | TCM (Tightly-Coupled Memory) SRAM |
| | | 0x1FFF_FFFF | | |

4.2. IO Space

| Name | Mode | Physical | Size | IP Function |
|------------|------|-------------|------|----------------------|
| Peripheral | | 0x4000_0000 | 4KB | SYS Control (SYSON) |
| | | 0x4000_0FFF | | |
| | | 0x4000_1000 | 2KB | GPIO Control |
| | | 0x4000_17FF | | |
| | | 0x4000_1800 | RSVD | |
| | | 0x4000_1FFF | | |
| | | 0x4000_2000 | 4KB | Timer Control |
| | | 0x4000_2FFF | | |
| | | 0x4000_3000 | 1KB | UART for Log |
| | | 0x4000_33FF | | |
| | | 0x4000_3400 | 1KB | RSVD |
| | | 0x4000_37FF | | |
| | | 0x4000_3800 | 1KB | I2C_3 Control |
| | | 0x4000_3BFF | | |
| | | 0x4000_3C00 | RSVD | |
| | | 0x4000_4FFF | | |
| | | 0x4000_5000 | 4KB | RSVD |
| | | 0x4000_5FFF | | |
| | | 0x4000_6000 | 4KB | SPI flash controller |
| | | 0x4000_6FFF | | |
| | | 0x4000_7000 | RSVD | |
| | | 0x4000_FFFF | | |
| | | 0x4001_0000 | 4KB | RSVD |
| | | 0x4001_0FFF | | |
| | | 0x4001_1000 | 4KB | RSVD |
| | | 0x4001_1FFF | | |

| Name | Mode | Physical | Size | IP Function |
|-------------|------|-------------|------|----------------|
| Peripheral | | 0x4004_0000 | 1KB | UART_0 Control |
| | | 0x4004_03FF | | |
| | | 0x4004_0400 | 1KB | RSVD |
| | | 0x4004_07FF | | |
| | | 0x4004_0800 | 1KB | RSVD |
| | | 0x4004_0BFF | | |
| | | 0x4004_0C00 | | RSVD |
| | | 0x4004_1FFF | | |
| | | 0x4004_2000 | 1KB | SPI_0 Control |
| | | 0x4004_23FF | | |
| | | 0x4004_2400 | 1KB | RSVD |
| | | 0x4004_27FF | | |
| | | 0x4004_2800 | 1KB | RSVD |
| | | 0x4004_2BFF | | |
| | | 0x4004_2C00 | | RSVD |
| | | 0x4004_3FFF | | |
| | | 0x4004_4000 | 1KB | RSVD |
| | | 0x4004_43FF | | |
| | | 0x4004_4400 | 1KB | RSVD |
| | | 0x4004_47FF | | |
| 0x4004_4800 | | RSVD | | |
| 0x4004_FFFF | | | | |

| Name | Mode | Physical | Size | IP Function |
|------------|------|-------------|------|--------------------|
| Peripheral | | 0x4005_0000 | 16KB | RSVD |
| | | 0x4005_3FFF | | |
| | | 0x4005_4000 | | RSVD |
| | | 0x4005_7FFF | | |
| | | 0x4005_8000 | 16KB | RSVD |
| | | 0x4005_BFFF | | |
| | | 0x4005_C000 | | RSVD |
| | | 0x4005_FFFF | | |
| | | 0x4006_0000 | 2KB | GDMA0 |
| | | 0x4006_07FF | | |
| | | 0x4006_0800 | 2KB | RSVD for other DMA |
| | | 0x4006_0FFF | | |
| | | 0x4006_1000 | 2KB | GDMA1 |
| | | 0x4006_17FF | | |
| | | 0x4006_1800 | | RSVD for other DMA |
| | | 0x4006_1FFF | | |

| Name | Mode | Physical | Size | IP Function |
|-------------|-------|-------------|-------|-------------------------------------|
| Peripheral | | 0x4006_2000 | 1KB | RSVD |
| | | 0x4006_23FF | | |
| | | 0x4006_2400 | 3KB | RSVD |
| | | 0x4006_2FFF | | |
| | | 0x4006_3000 | 1KB | RSVD |
| | | 0x4006_33FF | | |
| | | 0x4006_3400 | 3KB | RSVD |
| | | 0x4006_3FFF | | |
| | | 0x4006_4000 | 1KB | RSVD |
| | | 0x4006_43FF | | |
| | | 0x4006_4400 | | RSVD |
| | | 0x4006_4FFF | | |
| | | 0x4006_5000 | 1KB | RSVD |
| | | 0x4006_53FF | | |
| | | 0x4007_0000 | 16KB | Security Engine |
| | | 0x4007_3FFF | | |
| | | 0x4007_4000 | 48KB | RSVD |
| | | 0x4007_FFFF | | |
| | | 0x4008_0000 | 256KB | WIFI REG & TX/RX FIFO direct map |
| | | 0x400B_FFFF | | |
| 0x400C_0000 | 256KB | RSVD | | |
| 0x400F_FFFF | | | | |
| 0x403F_FFFF | 1MB | RSVD | | |

4.3. Extension Memory Space

| Name | Mode | Physical | Size | IP Function |
|-------|------|-------------|------|-----------------------|
| Flash | | 0x9800_0000 | 1MB | External flash memory |
| | | 0x9810_0000 | | |

5. Pin Assignments

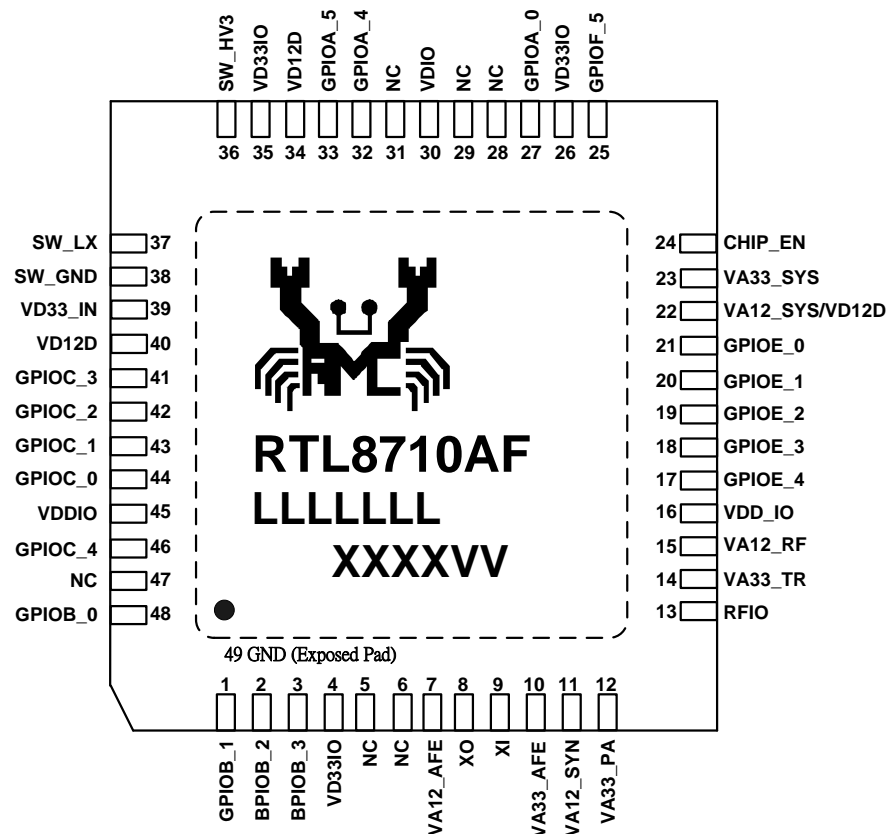


Figure 4. Pin Assignments

5.1. Package Identification

The version is shown in the location marked 'VV' in Figure 4, e.g., A0=Version A0

6. Pin Descriptions

The following signal type codes are used in the tables:

| | | | |
|------|---|--------|---------------------|
| I: | Input | O: | Output |
| T/S: | Tri-State bi-directional input/output pin | S/T/S: | Sustained Tri-State |
| O/D: | Open Drain | P: | Power pin |

6.1. Power On Trap Pin

Table 1. Power On Trap Pins

| Symbol | Type | Pin No | Description |
|-----------------|------|--------|---|
| NORMAL_MODE_SEL | I | 2 | Shared with GPIOB_2 1: Normal operation mode 0: Enter into test/debug mode |
| BOOT_SCENARIO | I | 48 | Shared with GPIOB_0 0: booting from flash 1: booting from internal memory |
| EEPROM_SEL | I | 25 | Shared with GPIOF_5 0: Internal NV memory select 1: reserved for internal testing use |
| ICFG0 | I | 44 | Shared with GPIOC_0 When NORMAL_MODE_SEL is "0", then ICFG0 is test mode BIT0. |

| Symbol | Type | Pin No | Description |
|--------|------|--------|---|
| ICFG1 | I | 43 | Shared with GPIOC_1 When NORMAL_MODE_SEL is "0", then ICFG1 is test mode BIT1. |
| ICFG2 | I | 42 | Shared with GPIOC_2 When NORMAL_MODE_SEL is "0", then ICFG2 is test mode BIT2. |
| ICFG3 | I | 41 | Shared with GPIOC_3 When NORMAL_MODE_SEL is "0", then ICFG3 is test mode BIT3. |

6.2. RF Pins

Table 2. RF Pins

| Symbol | Type | Pin No | Description |
|--------|------|--------|--------------|
| RF_IO | IO | 13 | WL RF signal |

6.3. Power Pins

Table 3. Power Pins

| Symbol | Type | Pin No | Description |
|--------|------|----------------|--|
| SW_LX | P | 37 | Switching Regulator Output |
| SW_HV3 | P | 36 | Switching Regulator Input Or Linear Regulator input from 3.3V to 1.2V |
| VA33 | P | 10, 12, 14, 23 | 3.3V for Analog Circuit |
| VD33IO | P | 4, 26, 35, 39 | VDD3.3V for Digital IO or digital blocks |

| Symbol | Type | Pin No | Description |
|--------|------|---------------|--------------------------------|
| VDD_IO | P | 16, 45 | GPIOE and GPIOC group IO power |
| VDIO | P | 30 | GPIOA group IO power |
| VD12D | P | 34, 40 | VDD 1.2V Digital Circuit |
| VA12 | P | 7, 11, 15, 22 | 1.2V for analog blocks |
| SW_GND | P | 38 | Switching Regulator Ground |

6.4. Clock Pins

Table 4. Clock Pins

| Symbol | Type | Pin No | Description |
|--------|------|--------|---|
| XI | I | 9 | 40MHz OSC Input Input of 40MHz Crystal Clock Reference |
| XO | O | 8 | Output of 40MHz Crystal Clock Reference |

6.5. Digital IO Pins

Please refer to section 6 Pin Function Table for more detailed information.

| Symbol | Type | Pin No | Description |
|---------------|-------------|---------------|---|
| GPIOB_0 | IO | 48 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOB_1 | IO | 1 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOB_2 | IO | 2 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOB_3 | IO | 3 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOE_0 | IO | 21 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOE_1 | IO | 20 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOE_2 | IO | 19 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOE_3 | IO | 18 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOE_4 | IO | 17 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOA_0 | IO | 27 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOA_4 | IO | 32 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOA_5 | IO | 33 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOC_0 | IO | 44 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOC_1 | IO | 43 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOC_2 | IO | 42 | GPIO pin. The MUX function can be referred to Pin Function Table. |

| Symbol | Type | Pin No | Description |
|---------|------|--------|---|
| GPIOC_3 | IO | 41 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOC_4 | IO | 46 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| CHIP_EN | I | 24 | Enable chip. 1: enable chip; 0: shutdown chip |

7. Pin Function Table

7.1. Pin Configurable Function Group Summary Table

Table 5. Pin Function Group Table

| PIN name | JTAG | UART Group | I2C Group | SPI Group | WL_LED | WKDT | GPIO INT | Default State | SCHMT |
|----------|-----------|--------------|-----------|-----------|---------|--------|----------|---------------|-------|
| GPIOA_0 | | UART2_IN | | | | | GPIO_INT | PH | O |
| GPIOA_4 | | UART2_OUT | | | | | | PH | |
| GPIOA_5 | | | | | | D_SBY0 | | PH | |
| GPIOB_0 | | UART_LOG_OUT | | | | | | HI | |
| GPIOB_1 | | UART_LOG_IN | | | WL_LED0 | D_SLP0 | | PH | |
| GPIOB_2 | | | I2C3_SCL | | | | | HI | O |
| GPIOB_3 | | | I2C3_SDA | | | | GPIO_INT | PH | |
| GPIOC_0 | | UART0_IN | | SPI0_CS0 | | | | HI | |
| GPIOC_1 | | UART0_CTS | | SPI0_CLK | | | GPIO_INT | HI | O |
| GPIOC_2 | | UART0_RTS | | SPI0_MOSI | | | | HI | |
| GPIOC_3 | | UART0_OUT | | SPI0_MISO | | | GPIO_INT | HI | O |
| GPIOC_4 | | | | SPI0_CS1 | | | GPIO_INT | HI | |
| GPIOE_0 | JTAG_TRST | | | | | | | PH | O |
| GPIOE_1 | JTAG_TDI | | | | | | | PH | O |
| GPIOE_2 | JTAG_TDO | | | | | | | PH | O |
| GPIOE_3 | JTAG_TMS | | | | | | | PH | O |
| GPIOE_4 | JTAG_CLK | | | | | | | PH | O |

NOTE1: PH = Pull-High, HI = High-impedance

NOTE2: Others' pull control can be done by register setting.

8. Functional Description

8.1. Power Management Control Unit

8.1.1. Features

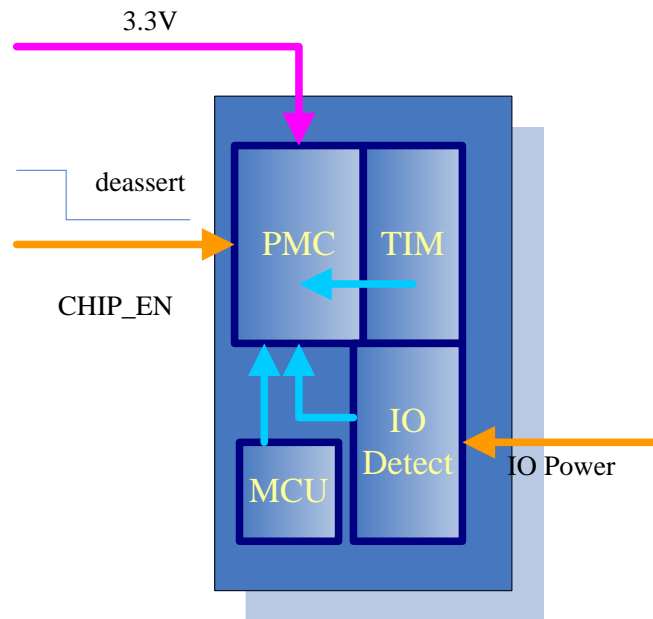
The PMU provides the following functions:

- Bulk/LDO to output 1.2V
- 2 very Low power clock source with less accuracy: 1K and 500K
- 1 low power 32.768KHz clock source with moderate accuracy
- Wakeup system detector to resume from low power state

8.1.2. Power Mode Description

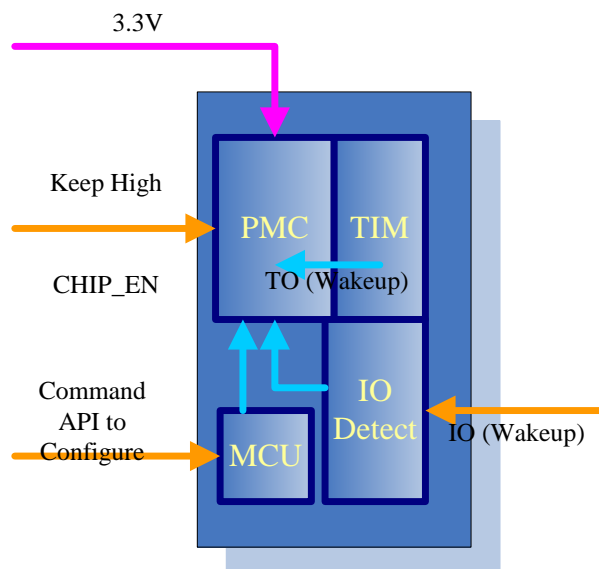
8.1.2.1 Shutdown Mode

CHIP_EN deasserts to shutdown whole chip without external power cut components required.



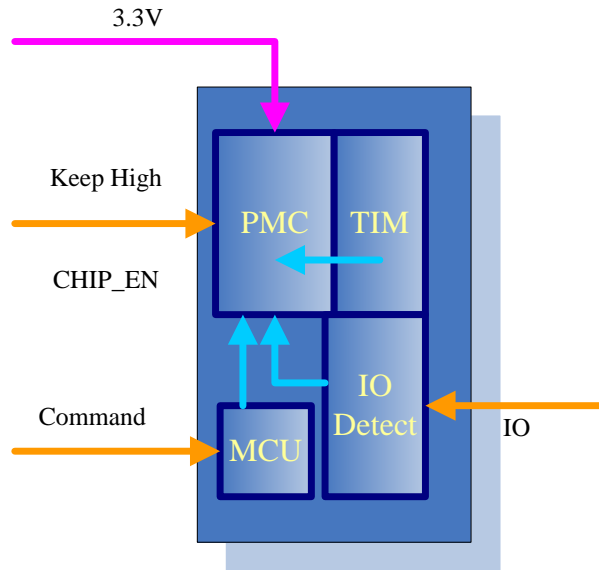
8.1.2.2 Deep Sleep Mode

CHIP_EN keeps high. Enter into Deep Sleep mode by API. The trigger timer period can be configured or GPIOB_0 can be used as external trigger event. The DLSP trigger timer can be configured with the range 1 ~ 3600 sec.



8.1.2.3 Deep Standby Mode

CHIP_EN keeps high. Entering into Deep Sleep mode by API. The trigger timer period can be configured or all GPIO group can be used as external trigger event.



8.2. Memory System

8.2.1. Memory Architecture

RTL8710AF integrates ROM, internal SRAM, extended NOR flash to provide applications with a variety of memory requirements.

8.2.2. Internal ROM

RTL8710AF integrates 1MB ROM to provide high access speed, low leakage memory. The ROM memory clock speed is up to 83MHz. The ROM lib provides the following functions:

- Boot Code and MCU initialization
- Default UART driver
- Non-flash booting functions and drivers
- Peripheral libs
- Security function libs

8.2.3. Internal SRAM

448KB SRAM is integrated to provide instruction, data, and buffer usage. The maximum clock speed is up to 83.3MHz.

Additional 64KB fast access data memory (TCM) is provided for FW data section. The range is 0x1FFF-0000 ~ 0x1FFF-FFFF.

8.2.4. SPI NOR Flash

Features

- Targeted SPI flash frequency: Up to 41.6MHz (when CPU clock is 83.3MHz)
- In addition to a programmed I/O interface, also supports a memory-mapped I/O interface for read operation
- Supports Read and Fast Read in memory-mapped I/O mode

Supported NOR Flash List

Table 6. Flash Bus DC Parameters

| Vendor | Part Number | Density | Voltage | IO |
|--------|-----------------|---------|---------|-------|
| MXIC | MXIC_MX25L8006E | 8M Bits | 3.3V | 1I/2O |

Electrical Specifications

Table 7. Flash Bus DC Parameters

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units | Notes |
|-----------------|----------------------------------|----------------------------|------|------|------|-------|-------|
| V _{IH} | Input-High Voltage | LVTTL | 2.0 | - | - | V | 1 |
| V _{IL} | Input-Low Voltage | LVTTL | - | - | 0.8 | V | 2 |
| V _{OH} | Output-High Voltage | - | 2.4 | - | - | V | 3 |
| V _{OL} | Output-Low Voltage | - | - | - | 0.4 | V | 3 |
| I _{IL} | Input-Leakage Current | V _{IN} =3.3V or 0 | -10 | ±1 | 10 | μA | - |
| I _{OZ} | Tri-State Output-Leakage Current | - | -10 | ±1 | 10 | μA | - |
| R _{PU} | Input Pull-Up Resistance | - | - | 75 | - | KΩ | 4 |
| R _{PD} | Input Pull-Down Resistance | - | - | 75 | - | KΩ | 4 |

Note 1: V_{IH} overshoot: V_{IH} (MAX)=V_{DDH} + 2V for a pulse width ≤ 3ns.

Note 2: V_{IL} undershoot: V_{IL} (MIN)=-2V for a pulse width ≤ 3ns.

Note 3: The output current buffer is 8mA for the flash address and data bus; and is 8mA for Flash control signals.

Note 4: These values are typical values checked in the manufacturing process and are not tested.

8.3. General Purpose DMA Contrller

8.3.1. Features of GDMA

- Dual port DMA with totally 12 channels
- Configurable endian
- Support memory-memory, memory-peripheral, peripheral-memory, and peripheral-peripheral DMA transfer
- Support block level flow control
- Support address auto-reload, link-listed mode
- Support scatter-gather mode

8.4. General Purpose Timer

8.4.1. Features of GTimer

- 8 Gtimer supported
- Source clock is 32.768KHz
- Support Counter mode and timer mode

8.5. GPIO Functions

8.5.1. Features of GPIO

- GPO and GPI function
- Support interrupt detection with configurable polarity per GPIO
- Internal weak pull up and pull low per GPIO
- Multiplexed with other specific digital functions

8.6. UART Interface Characteristics

8.6.1. Features of UART

- Support 2 HS-UART (max baud rate 4MHz, DMA mode and only one of them has flow control) and 1 Log UART (IO mode)
- UART (RS232 Standard) Serial Data Format

- Transmit and Receive Data FIFO
- Programmable Asynchronous Clock Support
- Auto Flow Control
- Programmable Receive Data FIFO Trigger Level
- DMA data moving support to save CPU loading

8.6.2. High Speed UART Specification

The RTL8710AF UART interface with flow control is a standard 4-wire interface with RX, TX, CTS, and RTS. The default baud rate is 115.2k baud. In order to support high and low speed baud rate, the RTL8710AF provides multiple UART clocks.

Table 8. UART Baud Rate Specifications

| Desired Baud Rate | Actual Baud Rate | Error (%) | Desired Baud Rate | Actual Baud Rate | Error (%) |
|-------------------|------------------|-----------|-------------------|------------------|-----------|
| 300 | 300 | 0.00% | 38400 | 38462 | 0.16% |
| 600 | 600 | 0.00% | 56000 | 55970 | -0.05% |
| 900 | 900 | 0.00% | 57600 | 57692 | 0.16% |
| 1200 | 1200 | 0.00% | 76800 | 76531 | -0.35% |
| 1800 | 1800 | 0.00% | 115200 | 115385 | 0.16% |
| 2400 | 2400 | 0.00% | 128000 | 127119 | -0.69% |
| 3600 | 3601 | 0.03% | 153600 | 153061 | -0.35% |
| 4800 | 4798 | -0.04% | 230400 | 229167 | -0.54% |
| 7200 | 7198 | -0.03% | 460800 | 458333 | -0.54% |
| 9600 | 9603 | 0.03% | 500000 | 500000 | 0.00% |
| 14400 | 14395 | -0.03% | 921600 | 916667 | -0.54% |
| 19200 | 19182 | -0.09% | 1000000 | 1000000 | 0.00% |
| 28800 | 28846 | 0.16% | 1382400 | 1375000 | -0.54% |

| Desired Baud Rate | Actual Baud Rate | Error (%) |
|-------------------|------------------|-----------|
| 1444444 | 1437500 | -0.48% |
| 1500000 | 1500000 | 0.00% |
| 1843200 | 1833333 | -0.54% |
| 2000000 | 2000000 | 0.00% |
| 2100000 | 2083333 | -0.79% |
| 2764800 | 2777778 | 0.47% |

| Desired Baud Rate | Actual Baud Rate | Error (%) |
|-------------------|------------------|-----------|
| 3000000 | 3000000 | 0.00% |
| 3250000 | 3250000 | 0.00% |
| 3692300 | 3703704 | 0.31% |
| 3750000 | 3750000 | 0.00% |
| 4000000 | 4000000 | 0.00% |

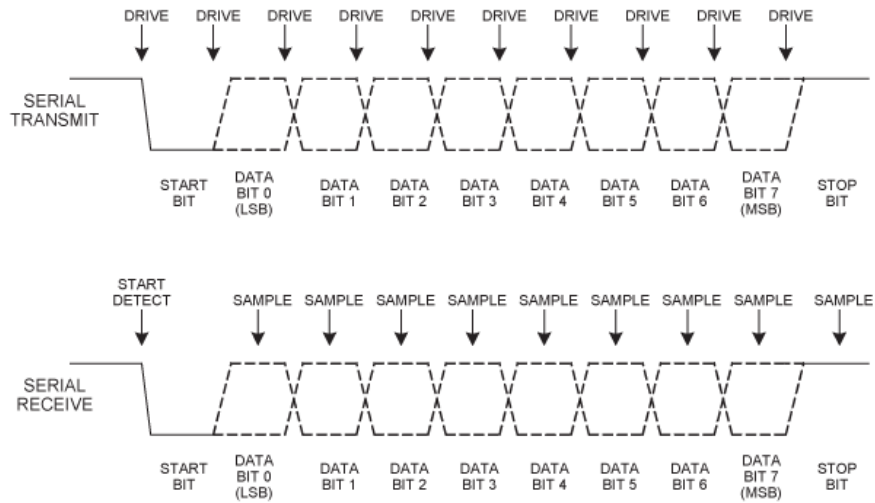


Figure 5. UART Interface Waveform

8.6.3. UART Interface Signal Levels

The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8710AF UART interface via the IO power.

8.7. SPI Interface

8.7.1. Features of SPI

- Support 1 SPI port
- Support Master/Slave mode
- Support DMA to offload CPU bandwidth
- 1 high speed SPI (Master/Slave)

- Support baud rate up to 10.4MHz (Master mode)
- Support baud rate up to 2.6MHz (Slave mode Rx only)
- Support baud rate up to 2MHz (Slave mode TRx)
- Programmable clock bit-rate
- Programmable clock polarity and phase
- Multiple Serial Interface Operations support
 - Motorola - SPI
 - Texas Instruments - SSI
 - National Semiconductor - Microwire

8.8. I2C Interface

8.8.1. Features of I2C

- Support 1 I2C port
- Three speeds:
 - Standard mode (0 to 100 Kb/s)
 - Fast mode (<400 Kb/s)
 - High-speed mode (<3.4 Mb/s) (with appropriate bus loading)
- Master or Slave I2C operation
- 7- or 10-bit addressing
- Transmit and receive buffers
- TX and RX DMA support (I2C 0 and 1 only)

8.9. Security Engine

8.9.1. Features

- Provide low SW computing and high performance encryption
- Supported authentication algorithms:
 - MD5
 - SHA-1
 - SHA-2 (SHA-224 / SHA-256)
 - HMAC-MD5
 - HMAC-SHA1
 - HMAC-SHA2
-
- Supported Encryption / Decryption mechanisms:
 - DES (CBC / ECB)
 - 3DES (CBC / ECB)
 - AES-128 (CBC / ECB / CTR)
 - AES-192 (CBC / ECB / CTR)
 - AES-256 (CBC / ECB / CTR)

9. Electrical Characteristics

9.1. Temperature Limit Ratings

Table 9. Temperature Limit Ratings

| Parameter | Minimum | Maximum | Units |
|-------------------------------|---------|---------|-------|
| Storage Temperature | -55 | +125 | °C |
| Ambient Operating Temperature | -20 | +85 | °C |
| Junction Temperature | 0 | +125 | °C |

9.2. Temperature Characteristics

Table 10. Thermal Properties

| Power (w) | PCB (layer) | Theta ja (C/W) | Theta jc (C/W) | Psi jt (C/W) |
|-----------|-------------|----------------|----------------|--------------|
| 1 | 2 | 38.7 | 12.4 | 0.35 |
| 1 | 4 | 28.1 | 11.1 | 0.24 |

9.3. Power Supply DC Characteristics

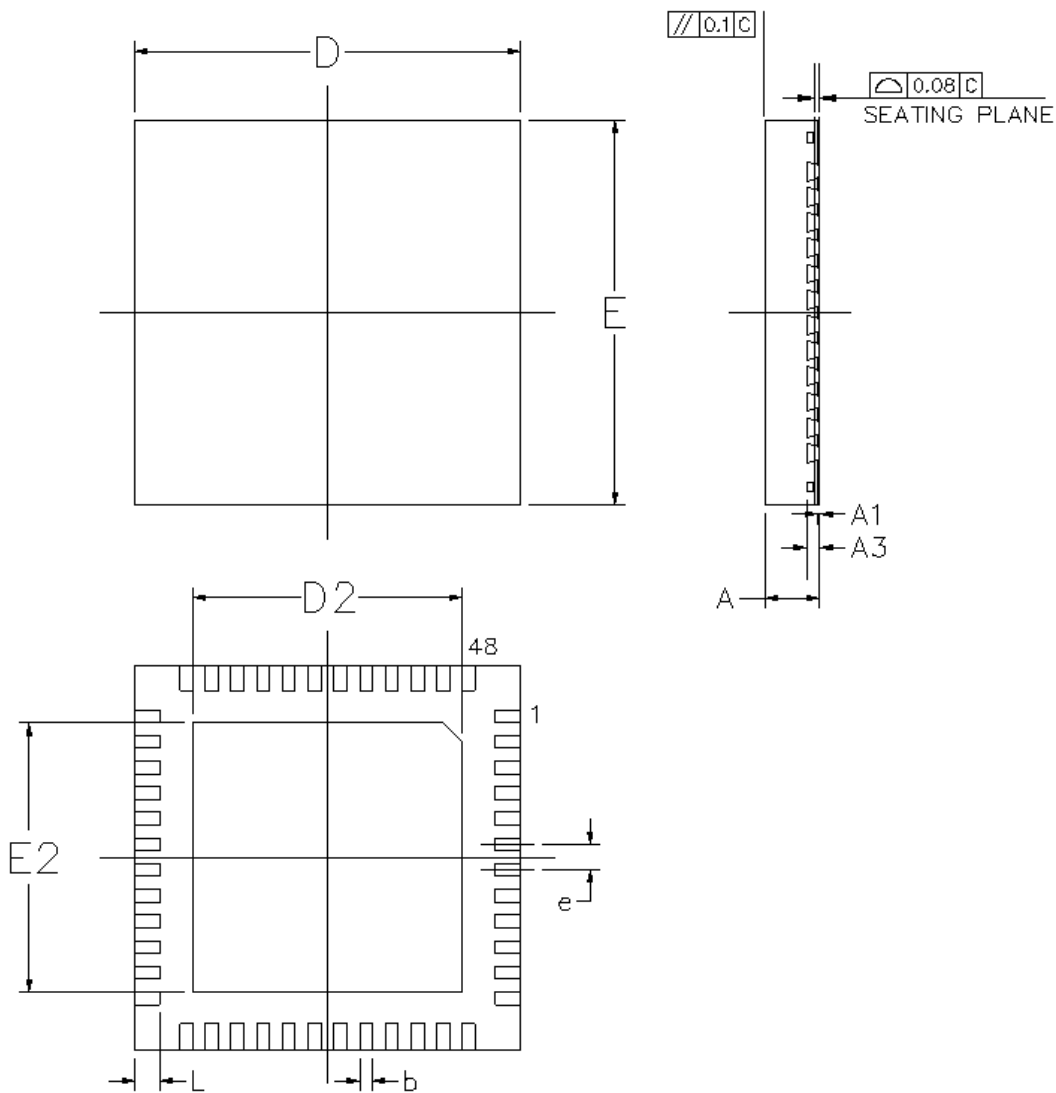
Table 11. Power Supply DC Characteristics

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|----------------------|---------------------------|---------|---------|---------|-------|
| VA33, VD33IO, SW_HV3 | 3.3V Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| VDD_IO | Digital IO Supply Voltage | 1.62 | 1.8~3.3 | 3.6 | V |

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|-----------------------------------|---|---------|---------|---------|-------|
| VA12_AFE, VA12_SYN, VA12_RF | 1.2V Core Supply Voltage | 1.08 | 1.2 | 1.32 | V |
| IDD33 | 3.3V Rating Current (with internal regulator and integrated CMOS PA) | - | - | 450 | mA |
| IDD_IO | IO Rating Current (including VDD_IO) | | | 200 | mA |
| IDD_IO_33 | 3.3V IO Rating Current | | | 50 | mA |

9.4. Mechanical Dimensions

9.4.1. Package Specification



9.4.2. Mechanical Dimensions Notes

| Symbol | Dimension in mm | | | Dimension in inch | | |
|----------------|-----------------|------|------|-------------------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.75 | 0.85 | 1.00 | 0.030 | 0.034 | 0.039 |
| A ₁ | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A ₃ | 0.20 REF | | | 0.008 REF | | |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D/E | 6.00BSC | | | 0.236BSC | | |
| D2/E2 | 4.15 | 4.4 | 4.65 | 0.163 | 0.173 | 0.183 |
| e | 0.40BSC | | | 0.016BSC | | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |

Notes :

1. CONTROLLING DIMENSION : MILLIMETER(mm).
2. REFERENCE DOCUMENTL : JEDEC MO-220.

9.5. Digital IO Pin DC Characteristics

9.5.1. Electrical Specifications

Table 12. Typical Digital IO DC Parameters (3.3V Case)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|-----------------|----------------------------|------------|------|------|------|-------|
| V _{IH} | Input-High Voltage | LVTTL | 2.0 | - | - | V |
| V _{IL} | Input-Low Voltage | LVTTL | - | - | 0.8 | V |
| V _{OH} | Output-High Voltage | LVTTL | 2.4 | - | - | V |
| V _{OL} | Output-Low Voltage | LVTTL | - | - | 0.4 | V |
| V _{T+} | Schmitt-trigger High Level | | 1.78 | 1.87 | 1.97 | V |
| V _{T-} | Schmitt-trigger Low Level | | 1.36 | 1.45 | 1.56 | V |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------|-----------------------|--------------------|------|---------|------|---------|
| I_{IL} | Input-Leakage Current | $V_{IN}=3.3V$ or 0 | -10 | ± 1 | 10 | μA |

Table 13. Typical Digital IO DC Parameters (1.8V Case)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------|----------------------------|--------------------|----------------------|---------|----------------------|---------|
| V_{IH} | Input-High Voltage | CMOS | $0.65 \times V_{CC}$ | - | - | V |
| V_{IL} | Input-Low Voltage | CMOS | - | - | $0.35 \times V_{CC}$ | V |
| V_{OH} | Output-High Voltage | CMOS | $V_{CC}-0.45$ | - | - | V |
| V_{OL} | Output-Low Voltage | CMOS | - | - | 0.45 | V |
| V_{T+} | Schmitt-trigger High Level | | 1.02 | 1.09 | 1.14 | V |
| V_{T-} | Schmitt-trigger Low Level | | 0.67 | 0.73 | 0.8 | V |
| I_{IL} | Input-Leakage Current | $V_{IN}=1.8V$ or 0 | -10 | ± 1 | 10 | μA |

10. Ordering Information

Table 14. Ordering Information

| Part Number | Package | Status |
|------------------|---------|--------|
| RTL8710AF-VB1-CG | QFN48 | MP |
| | | |