



REALTEK

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RTL8761ATT-CG

BLUETOOTH 2.1/3.0/4.0/4.1/4.2 CONTROLLER, UART INTERFACE

DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 1.0

05 January 2018

Track ID: JATR-8275-15



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USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

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- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2018/01/05	First release.

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1. General Description

The Realtek RTL8761ATT is a highly integrated single-chip Bluetooth 2.1/3.0/4.0/4.1/4.2 controller with a UART interface. It combines a BT Protocol Stack (LM, LL, L2CAP, GATT, RFCOMM, SPP, and LE), BT Baseband, modem, and BT RF in a single chip.

The RTL8761ATT Bluetooth controller complies with Bluetooth core specification v4.0/v4.1/v4.2, and supports dual mode (BR/EDR + AMP + Low Energy Controllers). It is compatible with previous versions, including v2.1 + EDR and v3.0 + HS. For BR/EDR, it allows one active link in either slave mode or master mode. For Low Energy, it supports multiple states and allows one active links in slave mode. A BR/EDR link and an LE link can be active at the same time.

2. Features

General

- 32-pin QFN
- Bluetooth single chip

Host Interface

- Complies with HS-UART with configurable baud rate for Bluetooth

Bluetooth Controller

- Compatible with Bluetooth v2.1 and v3.0 Systems
- Supports Bluetooth 4.2 Low Energy (BLE)
- HS-UART interface for Bluetooth data transmission compliant with H4 specification
- Integrated MCU to execute Bluetooth protocol stack
- Supports all packet types in basic rate and enhanced data rate
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff mode)
- Enhanced BT/Wi-Fi Coexistence Control to improve transmission quality in different profiles
- Bluetooth 4.2 Dual Mode support: Simultaneous LE and BR/EDR
- Supports multiple Low Energy states

Profile

- Supports SPP Profile
- Supports GATT Profile

Bluetooth Transceiver

- Fast AGC control to improve receiving dynamic range
- Supports Slave AFH mode to improve transmission quality
- Integrated internal Class 1, Class 2, and Class 3 PA
- Supports Power Control
- Bluetooth Low Energy Support
- Integrated 32K oscillator for power management

Peripheral Interfaces

- Configurable LED pin

3. Pin Assignments

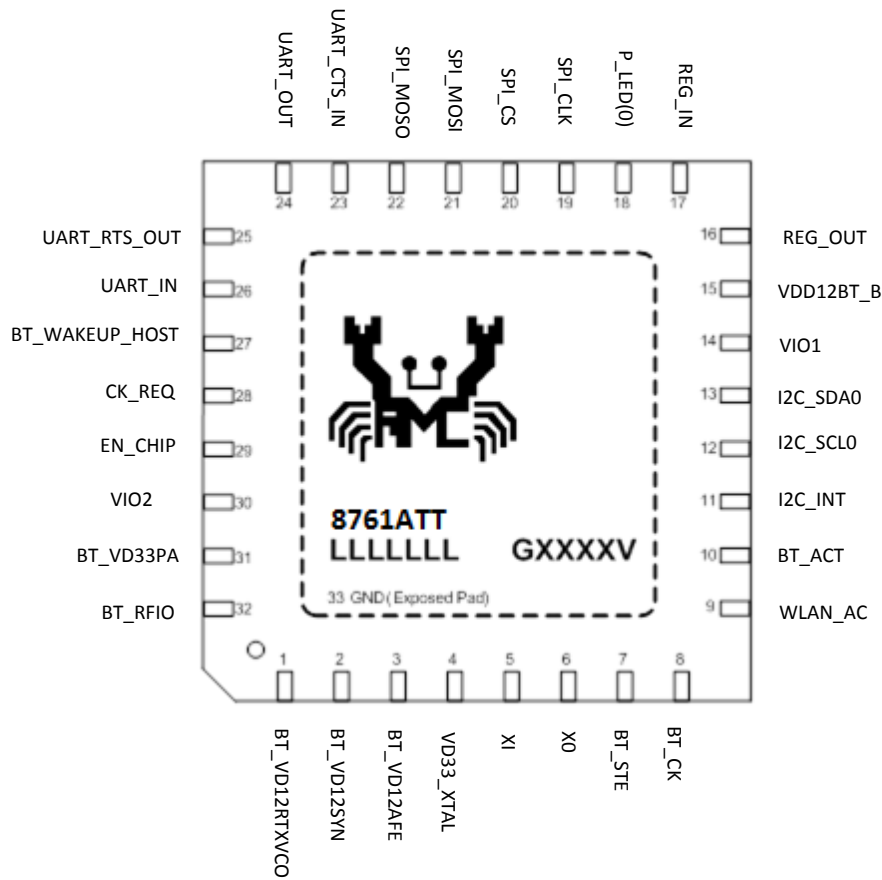


Figure 1. Pin Assignments

3.1. Package Identification

Green package is indicated by the 'G' in GXXXXV (Figure 1).

3.2. Block Diagram

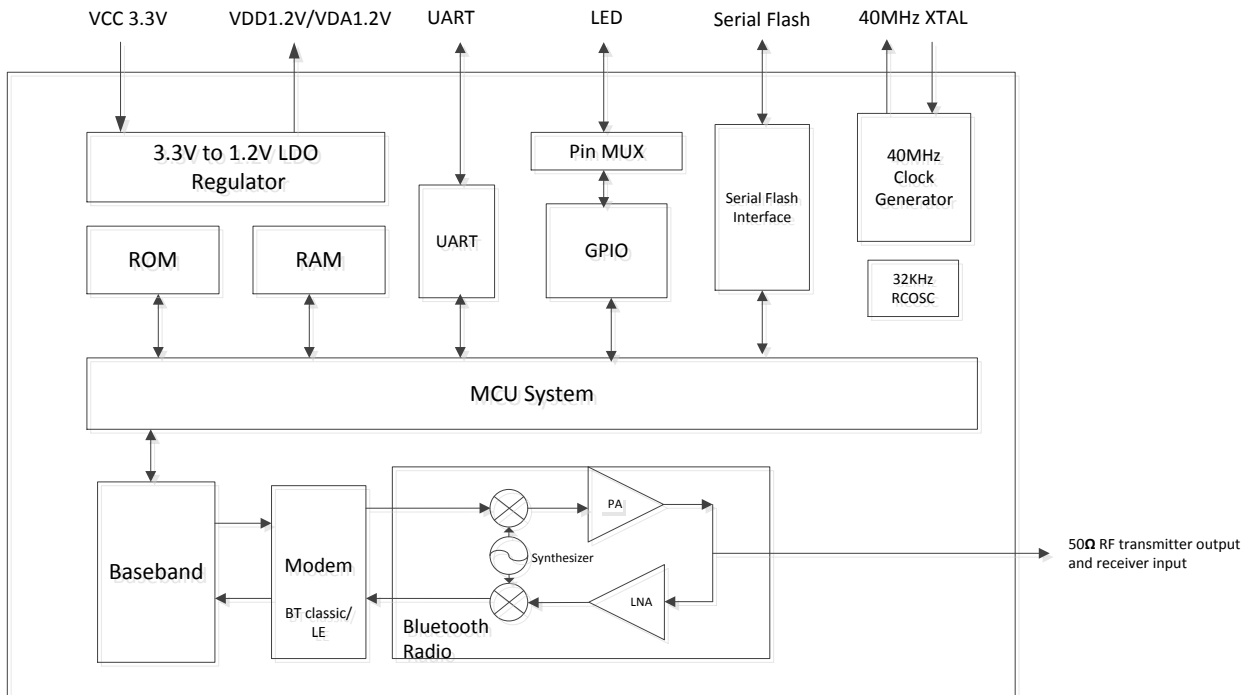


Figure 2. Block Diagram of RTL8761ATT

3.3. Power Architectonics

3.3.1. Regulators Architectonics

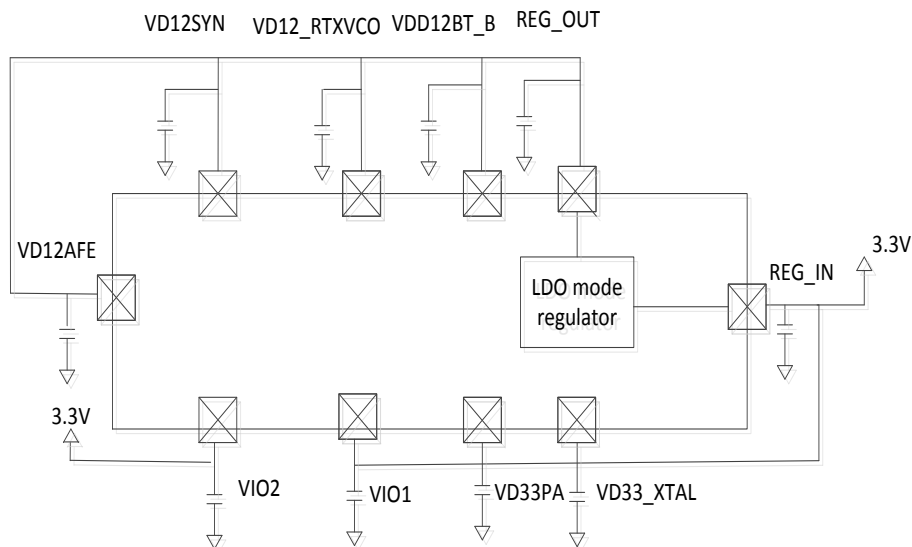


Figure 3. Regulators Architectonics of RTL8761ATT

3.3.2. Power On Sequence

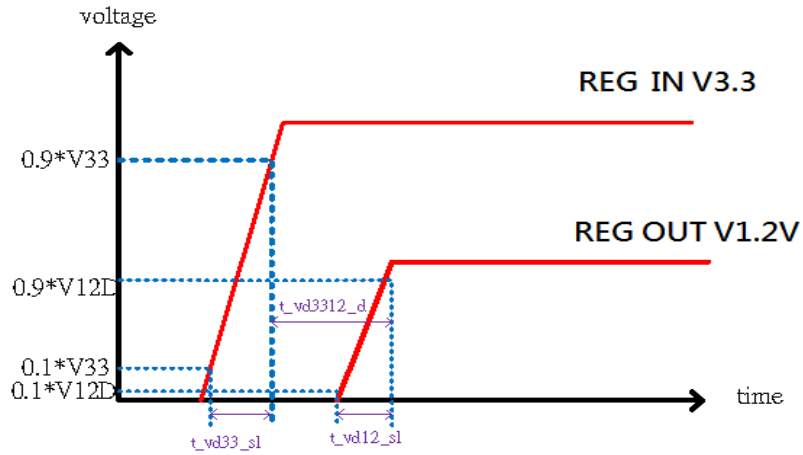


Figure 4. LDO Power Sequence of RTL8761ATT

Table 1. LDO Power Sequence of RTL8761ATT

Parameter	Min.	Typ.	Max.	Unit
t_vd33_sl	1	-	-	ms
t_vd12_sl	1	-	-	ms
vd3312	3	-	-	ms

3.3.3. EN_CHIP Control

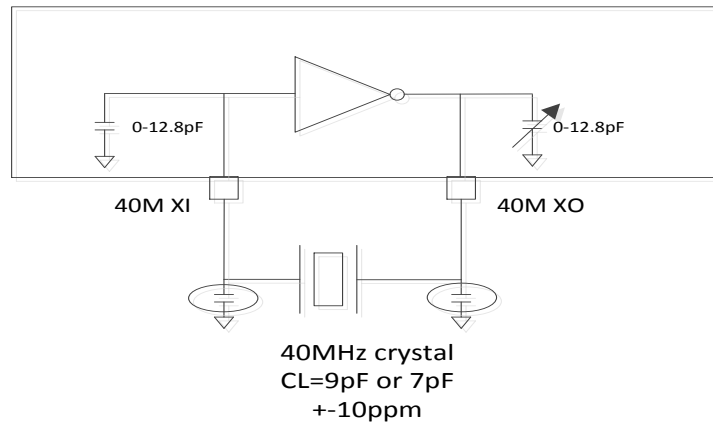
EN_CHIP # pin is active low to trigger reset behavior and the drive low should be longer than 100ms (>100ms) to avoid unconditional rest noise from the PCB board.



Figure 5. EN_CHIP Single control

3.4. Clock Tree

The RTL8761ATT has a 40MHz oscillator circuit: 40MHz is for system main clock in active mode while 32.768-kHz is for low power clock in sleep mode.



(* Refer to section 5.6 Crystal Oscillator 40MHz, page 16.

Figure 6. Clock Tree

4. Pin Descriptions

The following signal type codes are used in the tables:

I: Input	O: Output
PI: Power Input	PO: Power Output

4.1. Power-On Trap Pins

Table 2. Power-On Trap Pins

Symbol	Type	Pin No	Power Domain	Description
BT_STE	I	7	VIO1	0: Normal operation mode 1: Enter into EEPROM mode
WLAN_ACT	I	9	VIO1	0: Normal operation mode 1: Enter into TEST mode
BT_ACT	I	10	VIO1	0 : Normal operation mode 1: Realtek Debug Mode
BT_WAKE_HOST	I	27	VIO1	0 : Normal operation mode 1 : Realtek Debug Mode

4.2. RF Interface Pin

Table 3. RF Interface Pin

Symbol	Type	Pin No	Description
BT_RFIO	IO	32	RF Path

4.3. LED Interface Pin

Table 4. LED Interface Pin

Symbol	Type	Pin No	Description
P_LED(0)	O	18	LED Pin (Active Low) / Debug Log Pin

Note: The LED pin can also function as a debug log pin.

4.4. Power Management Handshake Interface Pins

Table 5. Power Management Handshake Interface Pins

Symbol	Type	Pin No	Power Domain	Description
BT_WAKE_HOST	O	27	VIO2	BT wakeup host signal
CLK_REQ	O	28	VIO2	Clock request signal
EN_CHIP	I	29	VIO2	BT wakeup host signal

4.5. Clock and Other Pins

Table 6. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	5	Crystal Clock Reference Input
XO	O	6	Crystal Clock Reference Output

4.6. Power Pins

Table 7. Power Pins

Symbol	Type	Pin No	Description
VD12RTXVCO	PI	1	VDD1.2V for VCO RTX
VD12SYN	PI	2	VDD1.2V for synthesizer
VD12AFE	PI	3	VDD1.2V for AFE
VD33_XTAL	PI	4	VDD 3.3V for XTAL
VIO1	PI	14	VDD 3.3V for IO
VDD12BT_B	PI	15	VDD 1.2V for digital
REG_OUT	PO	16	Regulator Output
REG_IN	PI	17	Regulator Input
VIO2	PI	30	IO supply
VD33PA	PI	31	VDD 3.3V for Bluetooth

4.7. PTA Pins

Table 8. PTA Pins

Symbol	Type	Pin No	Power Domain	Description
BT_STE	O	7	VIO1	State signal
BT_CK	O	8	VIO1	Clock signal
WLAN_ACT	I	9	VIO1	WLAN active signal
BT_ACT	O	10	VIO1	BT active signal
I2C_INT	O	11	VIO1	I2C interrupt signal / GPIO
I2C_SCL0	I	12	VIO1	I2C clock signal /GPIO
I2c_SDA0	IO	13	VIO1	I2C data signal/GPIO

Note: I2C_INT, I2C_SCL0, and I2C_SDA can also operate as GPIO pins.

4.8. Interface

Table 9. Interface Pins

Symbol	Type	Pin No	Power Domain	Description
SPI_CLK	O	19	VIO1	Serial flash clock output
SPI_CS	I/O	20	VIO1	Serial flash chip select, low active
SPI_MOSI	I/O	21	VIO1	Serial flash data output for 1-bit mode, connect to SI pin of external FLASH memory
SPI_MOSO	I/O	22	VIO1	Serial flash data input for 1-bit mode, connect to SO pin of external FLASH memory.
UART_CTS_IN	I	23	VIO2	UART Interface CTS input for HW flow control
UART_OUT	O	24	VIO2	UART Interface Output
UART_RTS_OUT	O	25	VIO2	UART Interface RTS input for HW flow control
UART_IN	I	26	VIO2	UART Interface Input

5. Electrical and Thermal Characteristics

5.1. Temperature Limit Ratings

Table 10. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

5.2. Power Supply DC Characteristics

Table 11. Power Supply DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VD33_XATL, VIO1, SWR_IN, BT_VDD33PA	3.3V Supply Voltage	3.0	3.3	3.6	V
BT_VD12SYN, VDD12BT_B, BT_VD12VCO/RTX	1.2V Supply Voltage	1.10	1.2	1.32	V
VIO2	IO Supply Voltage	1.8	3.3	3.6	V

5.3. 3.3V Digital IO Pin DC Characteristics

Table 12. 3.3V Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V _{IH}	Input high voltage	0.9*VIO	-	VIO+0.4	V
V _{IL}	Input low voltage	-0.4	-	0.4	V
V _{OH} (VIO=1.8V)	Output high voltage	VIO-0.2	-	-	V
V _{OL} (VIO=1.8V)	Output low voltage	-	-	0.2	V
V _{OH} (VIO=3.3V)	Output high voltage	VIO-0.4	-	-	V
V _{OL} (VIO=3.3V)	Output low voltage	-	-	0.4	V

Note: This VIO is the voltage of the IO input. The representative is VIO1 or VIO2.

5.4. UART Interface Characteristics

The RTL8761ATT UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. The interface supports the Bluetooth 2.0 UART HCI H4 specifications. The default baud rate is 115.2 k baud. In order to support high and low speed baud rate, the RTL8761ATT provides multiple UART clocks.

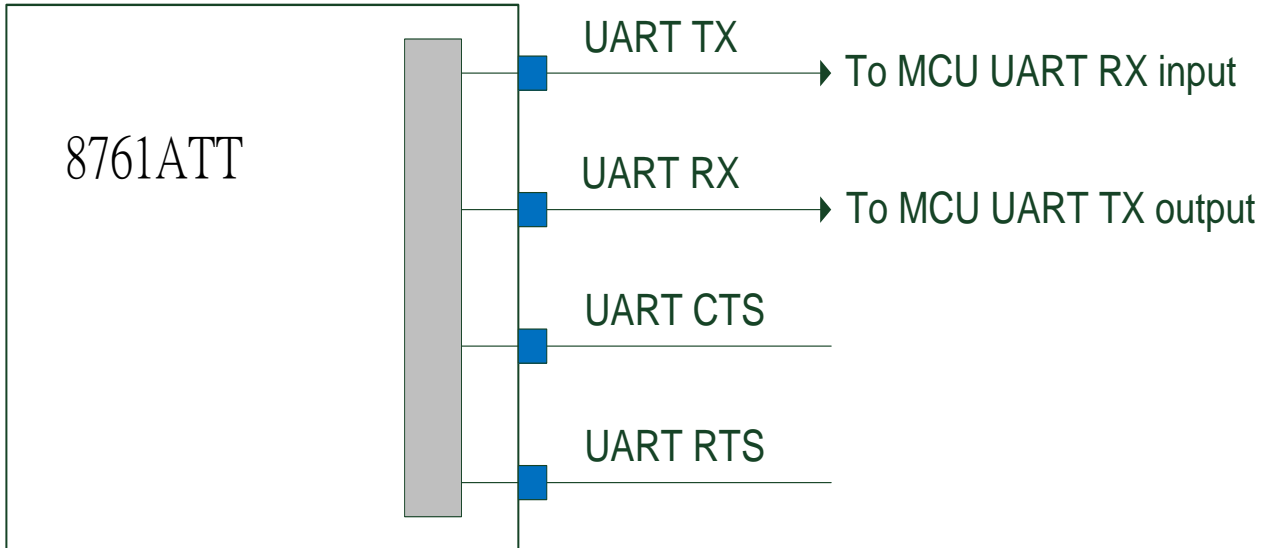


Figure 7. UART Interface Block Diagram

The UART Interface waveform show as:

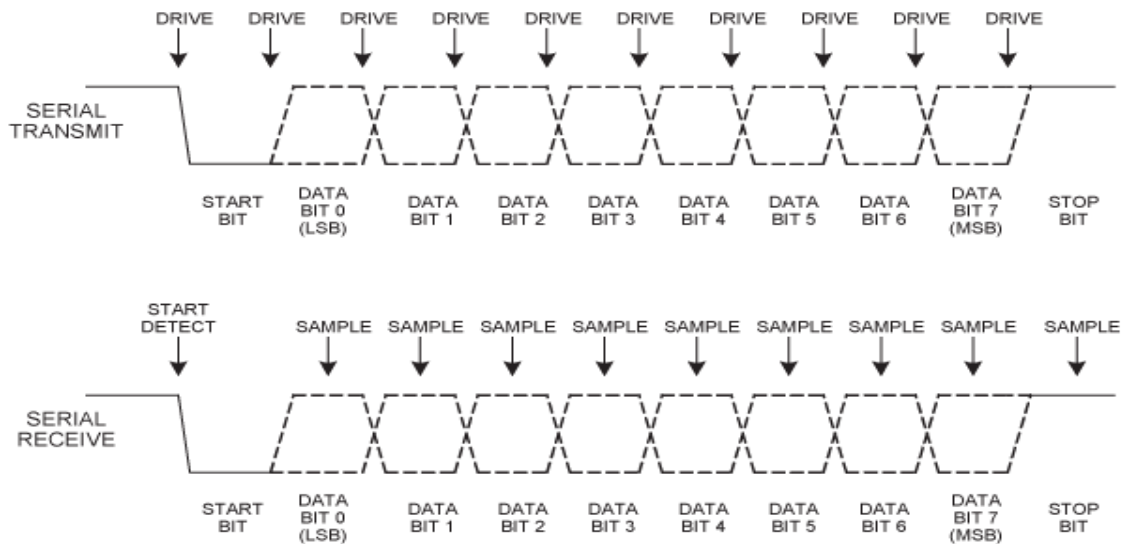


Figure 8. UART Interface Waveform

Table 12. UART Interface Power-On Timing Parameters

Desired Baud Rate	Actual Baud Rate	Error (%)
300	300	0.00%
600	600	0.00%
900	900	0.00%
1200	1200	0.00%
1800	1800	0.00%
2400	2400	0.00%
3600	3601	0.03%
4800	4798	-0.04%
7200	7198	-0.03%
9600	9603	0.03%
14400	14395	-0.03%
19200	19182	-0.09%
28800	28846	0.16%
38400	38462	0.16%
56000	55970	-0.05%
57600	57692	0.16%
76800	76531	-0.35%
115200	115385	0.16%
128000	127119	-0.69%

Desired Baud Rate	Actual Baud Rate	Error (%)
153600	153061	-0.35%
230400	229167	-0.54%
460800	458333	-0.54%
500000	500000	0.00%
921600	916667	-0.54%
1000000	1000000	0.00%
1382400	1375000	-0.54%
1444444	1437500	-0.48%
1500000	1500000	0.00%
1843200	1833333	-0.54%
2000000	2000000	0.00%
2100000	2083333	-0.79%
2764800	2777778	0.47%
3000000	3000000	0.00%
3250000	3250000	0.00%
3692300	3703704	0.31%
3750000	3750000	0.00%
4000000	4000000	0.00%

5.4.1. UART Interface Signal Levels

The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8761ATT UART interface.

The 3.3V, 2.8V, and 1.8V DC characteristics of typical signal levels are shown in section 5.3 3.3V Digital IO Pin DC Characteristics, page 10.

5.4.2. UART Interface Power-On Sequence

The UART interface power-on sequence differs depending on whether or not host flow control is supported.

UART Hardware Flow Control Not Supported

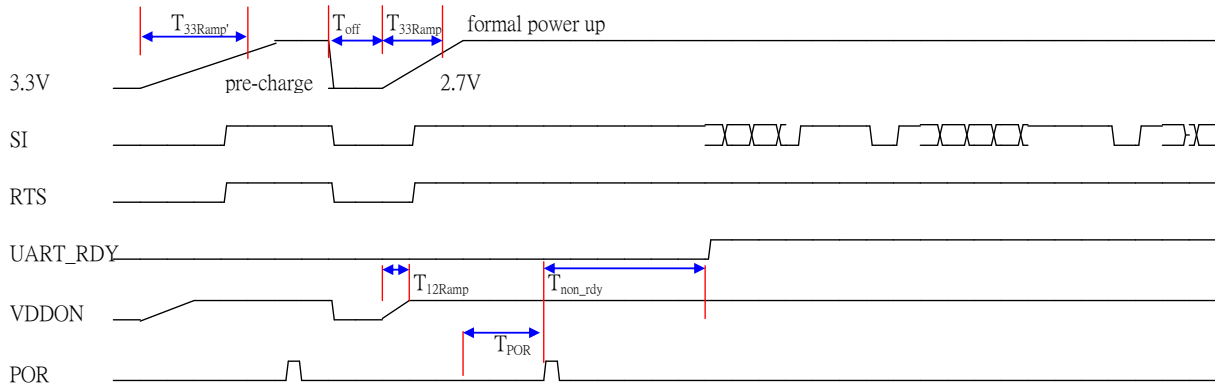


Figure 9. UART Power-On Sequence without Hardware Flow Control

UART Hardware Flow Control Supported

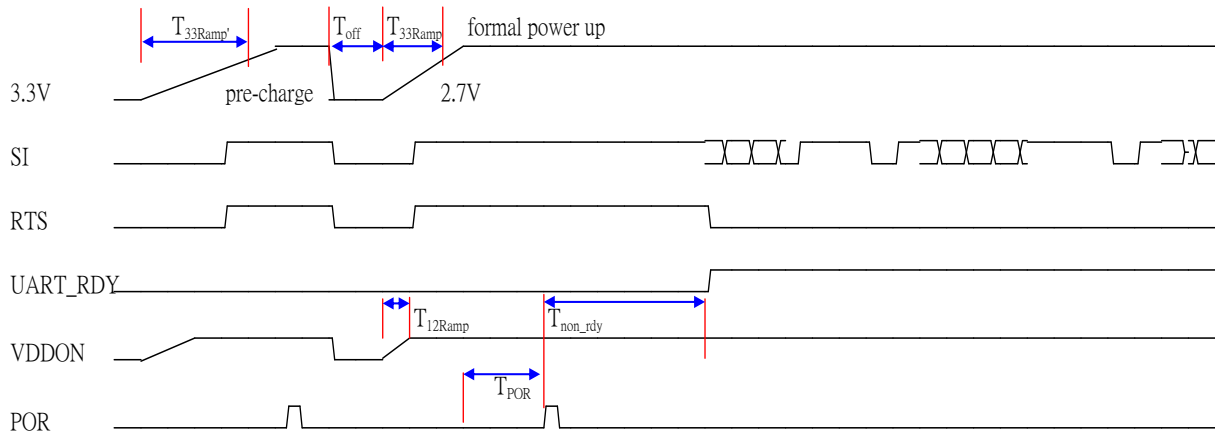


Figure 10. UART Power On Sequence with Hardware Flow Control

Table 13. UART Interface Power-On Sequence

Symbol	Description
T_{33ramp}	3.3V Power Pre-Charge Ramp Up Duration Before Formal Power Up. We recommend that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power on sequence. This procedure can eliminate host card detection issues when power ramp up duration is too long, or when a system warm reboot fails.
T_{off}	The duration 3.3V is cut off before formal power up.
T_{33ramp}	The 3.3V main power ramp up duration.
T_{12ramp}	The internal 1.2V ramp up duration.
T_{POR}	The duration from when the power-on reset releases and the power management unit executes power on tasks. A power on reset will detect both 3.3V and 1.2V power ramp up after a predetermined duration.
T_{non_rdy}	UART Not Ready Duration. In this state, the RTL8761ATT will not respond to any commands.

We recommend that the card detection procedures are divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.

During the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V power is cut off and is turned on after the T_{off} period. The ramp up time is specified in the T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the Bluetooth block. The Bluetooth firmware then initializes all circuits, including the UART. In addition to waiting the T_{non_rdy} time, if the host supports UART hardware flow control it can detect RTS signals and follow the formal UART flow control handshake.

Table 14. UART Interface Power On Timing Parameters

Symbol	Min	Typical	Max	Unit
T_{33ramp}	-	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{por}	2	2	8	ms
T_{non_rdy}	1	2	10	ms

5.5. RF Radio

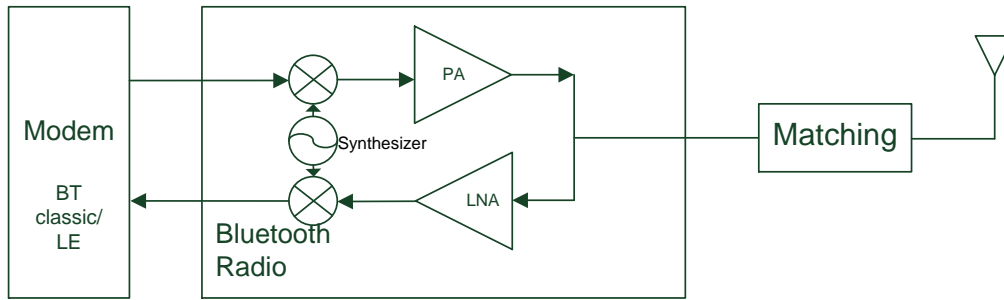


Figure 11. RF Radio Block Diagram

Transceiver:

This is a fully integrated all parts of radio transceiver and compliant with Bluetooth SIG test specification. It is designed for low power consumption and excellent transmit and receive performance in the ISM band.

Transmit Part:

Transmit mixer: The Transmit mixer translates the baseband input signal to form the RF signal. It is designed to provide good stability and modulation characteristics.

Power Amplifier: The power amplifier integrated in the chip can provide up to +3 dBm in the ISM band.

Receive Part:

Low Noise Amplifier: Amplifies the low energy RF signal to the desired level without significantly increasing the noise power. It is designed to maintain with good linearity in high input power environments.

Receive mixer: The Receiver mixer receives an input RF signal and outputs an IF signal. The IF signal is then passed along the IF path to the demodulator.

Synthesizer: This is a control loop that compares the crystal and VCO between their phases. If the VCO frequency shifts, then the phase difference produces an error signal for the control loop.

Reference:

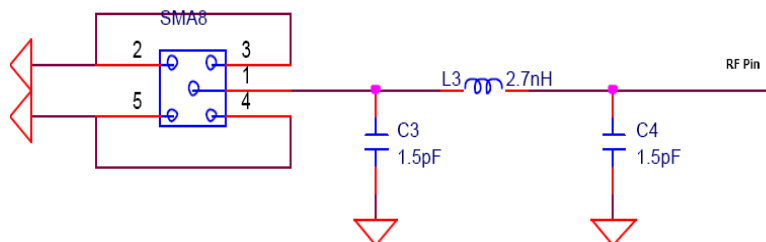


Figure 12. RF Radio Reference circuit

5.6. Crystal Oscillator 40MHz

The PCB connection between the 40MHz XTAL and 8761ATT is shown in Figure 13. The 40MHz XTAL specification is shown in Table 15. The external capacitor is selected via the following equation:

$$CL = \frac{(C1 + Cxi)(C2 + Cxo)}{(C1 + Cxi + C2 + Cxo)} + Cstray$$

Where CL is the load capacitance of the 40MHz XTAL.

Cxi and Cxo are internal trimming capacitors. A typical value for Cxi/Cxo in the 8761ATT is 6.4pF. The tuning range of Cxi/Cxo is 0pF~12.8pF.

Cstray is parasitic capacitance from package and PCB routing effects. In a standard case the capacitance is from 2~5pF, but the actual value of Cstray is strongly dependent on PCB layout and the package size of the XTAL. For example, when CL=12pF crystal is selected, C1 is equal to C2 and Cxi is equal to Cxo, and Cstray is estimated as 4pF.

C1+Cx1=16pF; in a typical setting Cxi is 6.4pF, and C1, C2 is 16-6.4~10pF. For precise frequency accuracy, fine-tuning Cxi/Cxo is recommended during the mass production procedure.

Table 15. 40MHz Crystal Specification Suggestions

Parameter	Min.	Typ.	Max.
Frequency (MHz)	-	40	-
Frequency tolerance (ppm)	-	-	±10
Frequency stability (ppm) over operating temperature	-	-	±10
Load capacitance (pF)	-	12	-
Drive Level (μW)	-	-	300
Equivalent Series Resistance (Ohm)	-	-	40
Insulation Resistance (MOhm)	500	-	-

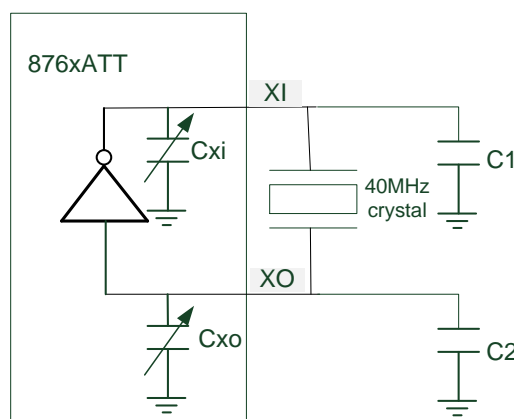


Figure 13. Crystal Oscillator 40MHz

5.7. Serial FLASH Memory Interface

The RTL8761ATT does not support internal FLASH memory, but supports a serial interface to connect to external serial FLASH memory for parameter and data storage purposes. The RTL8761ATT supports 1-bit and 2-bit mode,

The figure below shows the connectivity of the serial FLASH memory of the RTL8761ATT.

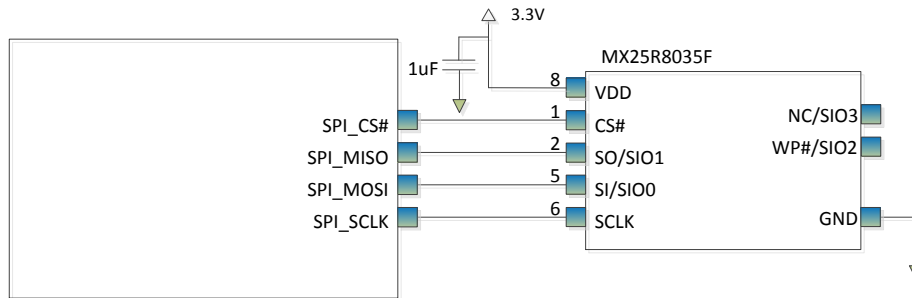


Figure 14. Serial FLASH Memory Interface

Note: For best serial FLASH memory performance, we suggest to use our Qualified Vendor List (QVL).

5.8. LED

The RTL8761ATT supports dynamic GPIO assignment to drive the LED for status indication. It allows the flexibility to assign the GPIO at the best pin out location to ease PCB routing complication.

The LED indication method could be selected in the UI tool and programmed into FLASH memory in the mass production process.

The LED can still be active in deep sleep mode, without need for MCU control.

Table 16. LED Specification Suggestions

Parameter	Min.	Typ.	Max.	Unit
Driving capacity	-	-	12	mA
GPIO V _{OH}	1.8	-	3.6	V
GPIO V _{OL}	-	0.2	-	-

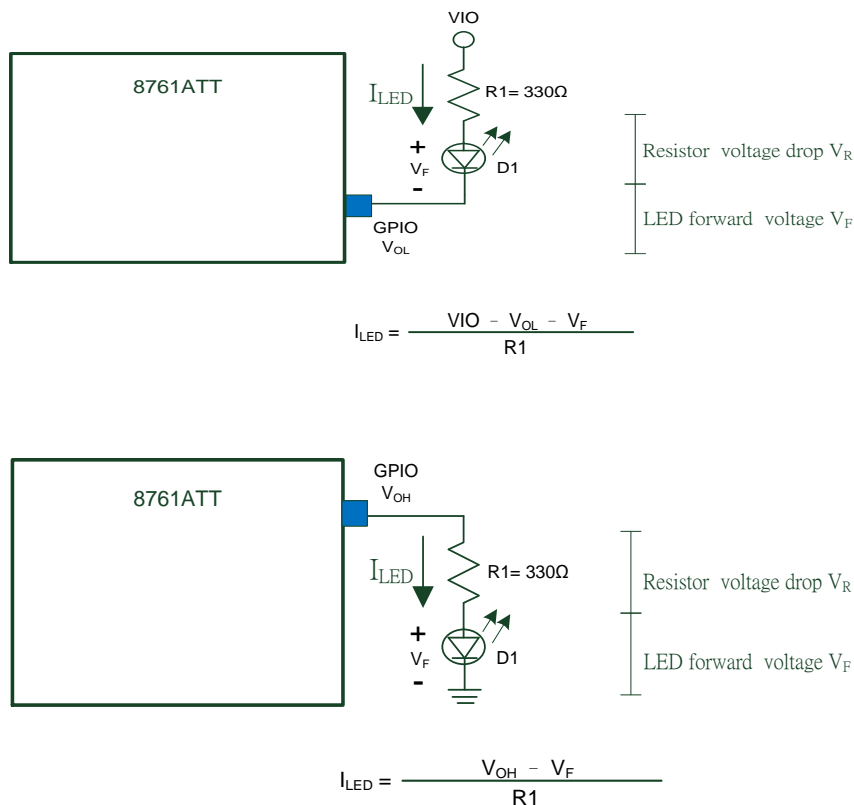


Figure 15. LED References

This VIO is the voltage of the IO input.

Where V_F is defined in the LED specification; V_{OL} is defined as the GPIO drive low level, typically 0.2V.

V_{OH} depends on the VIO output level; if VIO=1.8V, V_{OH}=1.8V; if VIO=3.3V, V_{OH}=3.3V.

R1=330Ω for LED drive with 4mA with VIO=3.3V.

R1 can be adjusted according to the LED brightness needed.

6. Mechanical Dimensions

6.1. Layout Land Pattern

Layout Land Pattern

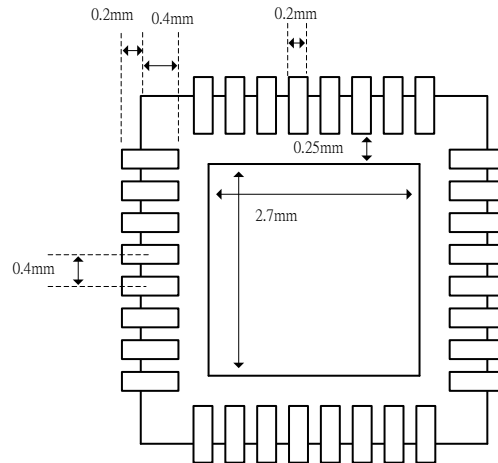


Figure 16. Layout Land Pattern

Suggested stencil open for SMT soldering on EP pad
(exposed pad under the chip)

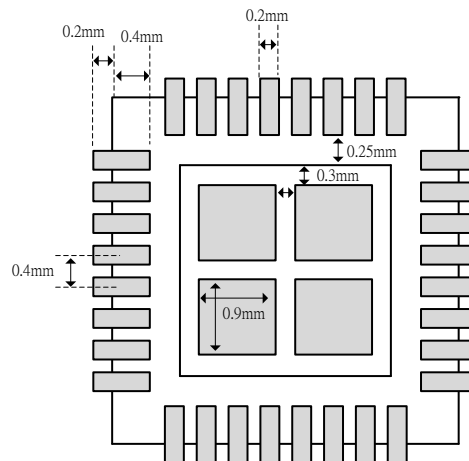


Figure 17. Suggested Stencil Open for SMT Soldering on EP Pad

6.2. Package Dimension QFN32

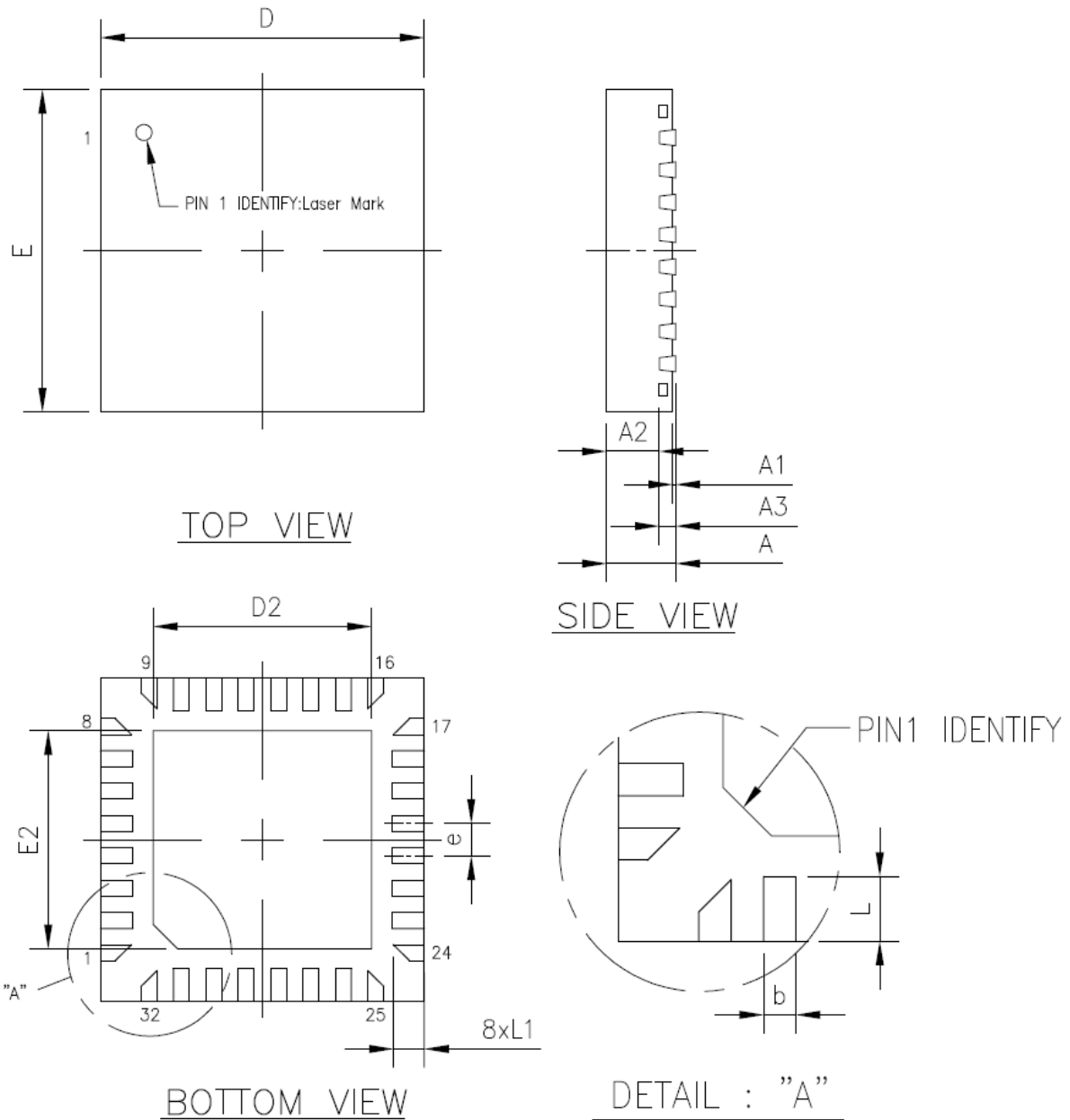


Figure 18. QFN32 Package Dimensions

6.3. Mechanical Dimensions Notes

Table 17. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	—	0.65	0.70	—	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.080	0.010
D/E	4.00 BSC			0.157 BSC		
D2/E2	2.45	2.70	2.95	0.096	0.106	0.116
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	0.282	0.382	0.482	0.011	0.015	0.019

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).

Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

6.4. Storage Condition

Table 18. Storage Condition

	MIN.	TYP.	MAX.
Storage Temperature	-	-	30°C
Storage Humidity	-	-	60%

7. Ordering Information

Part Number	Package	Status
RTL8761ATT	QFN-32, 'Green' Package	Mass Production

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