RTL8761ATV-CG

BLUETOOTH 2.1/3.0/4.0 CONTROLLER, UART INTERFACE

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2014/07/15	First release.

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1. General Description

The Realtek RTL8761ATV-CG is a highly integrated single-chip Bluetooth 2.1/3.0/4.0 controller with a UART interface. It combines a BT Protocol Stack (LM, LL, and LE), BT Baseband, modem, and BT RF in a single chip.

The RTL8761ATV Bluetooth controller complies with Bluetooth core specification v4.0, and supports dual mode (BR/EDR + AMP + Low Energy Controllers). It is compatible with previous versions, including v2.1 + EDR and v3.0 + HS. For BR/EDR, it supports scatternet topology and allows active links in slave mode and master mode. For Low Energy, it supports multiple states and allows active links in master mode. The links in BR/EDR and LE can be active simultaneously.

2. Features

General

- 32-pin QFN
- Bluetooth single chip

Host Interface

- Complies with HS-UART with configurable baud rate for Bluetooth

Bluetooth Controller

- Compatible with Bluetooth v2.1 and v3.0 Systems
- Supports Bluetooth 4.0 Low Energy(BLE)
- HS-UART interface for Bluetooth data transmission compliant with H4 and H5 specification
- PCM interface for audio data transmission via Bluetooth controller
- Integrated MCU to execute Bluetooth protocol stack
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/eSCO link
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff/Sniff Sub-rating/Hold/Park)
- Enhanced BT/Wi-Fi Coexistence Control to improve transmission quality in different profiles
- Bluetooth 4.0 Dual Mode support: Simultaneous LE and BR/EDR
- Supports multiple Low Energy states

Bluetooth Transceiver

- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Integrated internal Class 1, Class 2, and Class 3 PA
- Bluetooth 3.0+HS compliant
- Supports Power Control/Enhanced Power Control
- Bluetooth Low Energy Support
- Integrated 32K oscillator for power management

Peripheral Interfaces

- Configurable LED pin

3. Pin Assignments

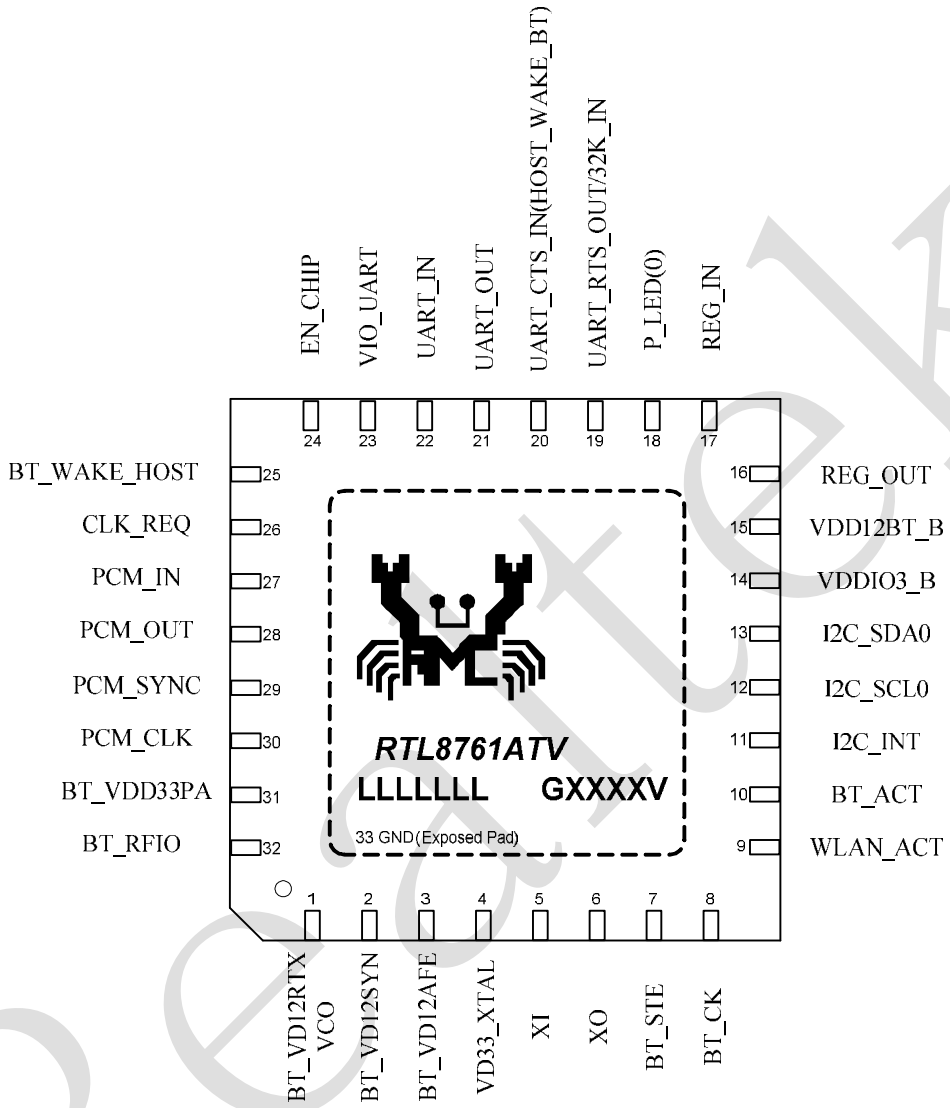


Figure 1. Pin Assignments

3.1. Package Identification

Green package is indicated by the 'G' in GXXXXV (Figure 1).

4. Pin Descriptions

The following signal type codes are used in the tables:

I: Input O: Output

P: Power

4.1. Power-On Trap Pins

Table 1. Power-On Trap Pins

Symbol	Type	Pin No	Description
BT_STE	I	7	0: Normal operation mode 1: Enter into EEPROM mode
WLAN_ACT	I	9	0: Normal operation mode 1: Enter into TEST mode
BT_ACT	-	10	0: TBD 1: TBD
BT_WAKE_HOST	I	25	0: TBD 1: TBD
PCM_OUT	I	28	0: TBD 1: TBD

4.2. RF Interface

Table 2. RF Interface

Symbol	Type	Pin No	Description
BT_RFIO	IO	32	RF Path

4.3. LED Interface

Table 3. LED Interface

Symbol	Type	Pin No	Description
P_LED(0)	O	18	LED Pin (Active Low)

4.4. Power Management Handshake Interface

Table 4. Power Management Handshake Interface

Symbol	Type	Pin No	Description
BT_WAKE_HOST	O	25	BT wakeup host signal.
CLK_REQ	O	26	Clock request signal
HOST_WAKE_BT	I	20	Host wakeup BT signal.
EN_CHIP	I	24	Enable BT signal

4.5. Clock and Other Pins

Table 5. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	5	Input of Crystal Clock Reference
XO	O	6	Output of Crystal Clock Reference

4.6. Power Pins

Table 6. Power Pins

Symbol	Type	Pin No	Description
REG_OUT	P	16	Regulator Output
REG_IN	P	17	Regulator Input
BT_VD33PA	P	31	VDD 3.3V for Bluetooth
VD33_XTAL	P	4	VDD 3.3V for XTAL
BT_VD12SYN	P	2	VDD1.2V for synthesizer
VDDIO3_B	P	14	VDD 3.3V for IO
VDD12BT_B	P	15	VDD 1.2V for digital
BT_VD12AFE	P	3	VDD1.2V for AFE
VIO_UART	P	23	IO supply
BT_VD12RTXVCO	P	1	VDD1.2V for VCO RTX

4.7. PTA

Table 7. PTA Pins

Symbol	Type	Pin No	Description
BT_STE	O	7	State signal
BT_CK	O	8	Clock signal
WLAN_ACT	I	9	WLAN active signal
BT_ACT	O	10	BT active signal
I2C_INT	O	11	I2C interrupt signal
I2C_SCL0	I	12	I2C clock signal
I2c_SDA0	IO	13	I2C data signal

5. Electrical and Thermal Characteristics

5.1. Temperature Limit Ratings

Table 8. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

5.2. Power Supply DC Characteristics

Table 9. Power Supply DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VD33_XATL, VDDIO3B, SWR_IN, VIO_UART, BT_VDD33PA	3.3V Supply Voltage	3.0	3.3	3.6	V
BT_VD12SYN, VDD12BT_B, BT_VD12VCO/RTX	1.2V Supply Voltage	1.10	1.2	1.32	V

5.3. Digital IO Pin DC Characteristics

Table 10. 3.3V IO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	-	0	0.9	V
V_{OH}	Output high voltage	2.97	-	3.3	V
V_{OL}	Output low voltage	0	-	0.33	V

5.4. UART Interface Characteristics

The RTL8761ATV UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. The interface supports the Bluetooth 2.0 UART HCI H4 and H5 specifications. The default baud rate is 115.2 kbaud. In order to support high and low speed baud rate, the RTL8761ATV provides multiple UART clocks.

Table 11. UART Interface Power-On Timing Parameters

Desired Baud Rate	Actual Baud Rate	Error (%)
300	300	0.00%
600	600	0.00%
900	900	0.00%
1200	1200	0.00%
1800	1800	0.00%
2400	2400	0.00%
3600	3601	0.03%
4800	4798	-0.04%
7200	7198	-0.03%
9600	9603	0.03%
14400	14395	-0.03%
19200	19182	-0.09%
28800	28846	0.16%
38400	38462	0.16%
56000	55970	-0.05%
57600	57692	0.16%
76800	76531	-0.35%
115200	115385	0.16%
128000	127119	-0.69%

Desired Baud Rate	Actual Baud Rate	Error (%)
153600	153061	-0.35%
230400	229167	-0.54%
460800	458333	-0.54%
500000	500000	0.00%
921600	916667	-0.54%
1000000	1000000	0.00%
1382400	1375000	-0.54%
1444444	1437500	-0.48%
1500000	1500000	0.00%
1843200	1833333	-0.54%
2000000	2000000	0.00%
2100000	2083333	-0.79%
2764800	2777778	0.47%
3000000	3000000	0.00%
3250000	3250000	0.00%
3692300	3703704	0.31%
3750000	3750000	0.00%
4000000	4000000	0.00%

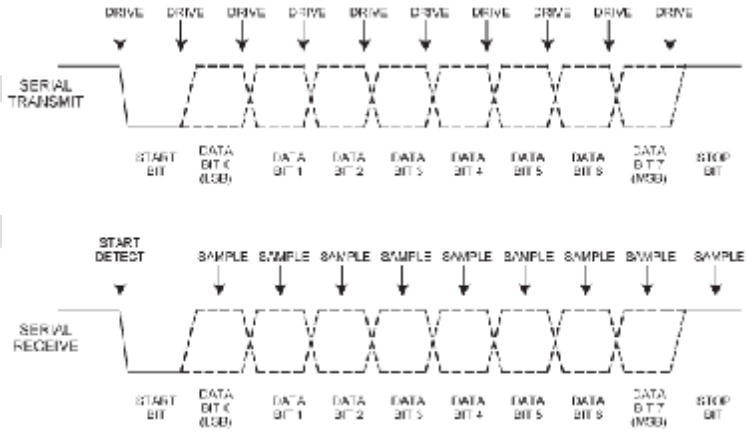


Figure 2. UART Interface Waveform

5.4.1. UART Interface Power-On Sequence

The UART interface power-on sequence differs depending on whether or not host flow control is supported.

UART Hardware Flow Control Not Supported

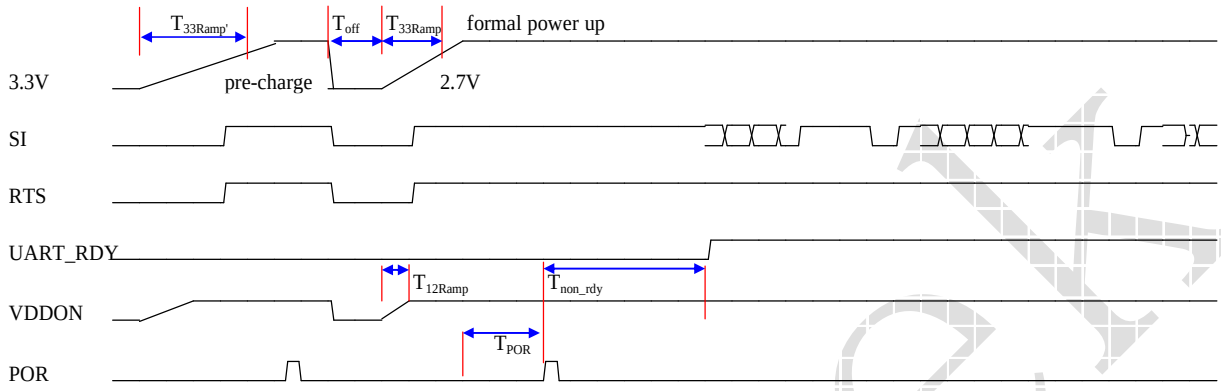


Figure 3. UART Power-On Sequence without Hardware Flow Control

UART Hardware Flow Control Supported

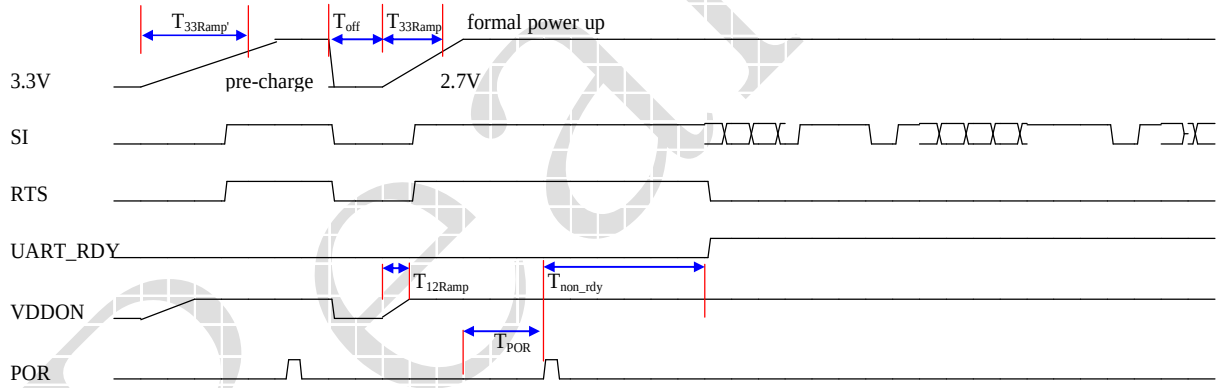


Figure 4. UART Power On Sequence with Hardware Flow Control

Table 12. UART Interface Power-On Sequence

Symbol	Description
T_{33ramp}	3.3V Power Pre-Charge Ramp Up Duration Before Formal Power Up. We recommend that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power on sequence. This procedure can eliminate host card detection issues when power ramp up duration is too long, or when a system warm reboot fails.
T_{off}	The duration 3.3V is cut off before formal power up.
T_{33ramp}	The 3.3V main power ramp up duration.
T_{12ramp}	The internal 1.2V ramp up duration.

Symbol	Description
T_{POR}	The duration from when the power-on reset releases and the power management unit executes power on tasks. A power on reset will detect both 3.3V and 1.2V power ramp up after a predetermined duration.
T_{non_rdy}	UART Not Ready Duration. In this state, the RTL8761ATV will not respond to any commands.

We recommend that the card detection procedures are divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.

During the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V power is cut off and is turned on after the T_{off} period. The ramp up time is specified in the T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the Bluetooth block. The Bluetooth firmware then initializes all circuits, included the UART. In addition to waiting the T_{non_rdy} time, if the host supports UART hardware flow control it can detect RTS signals and follow the formal UART flow control handshake.

Table 13. UART Interface Power On Timing Parameters

	Min	Typical	Max	Unit
T_{33ramp}	-	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{por}	2	2	8	ms
$T_{non\text{-}rdy}$	1	2	10	ms

5.5. PCM Interface Characteristics

The RTL8761ATV supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit A-law/μ-law, and 13/16-bit linear PCM formats
- Supports sign-extension and zero-padding for 8-bit and 13-bit samples
- Supports padding of Audio Gain to 13-bit samples
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports SCO/ESCO link

5.5.1. PCM Format

FrameSync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. A Long FrameSync indicates the start of ADC_Data at the rising edge of FrameSync (Figure 5), and a Short FrameSync indicates the start of ADC_Data at the falling edge of FrameSync (Figure 6).

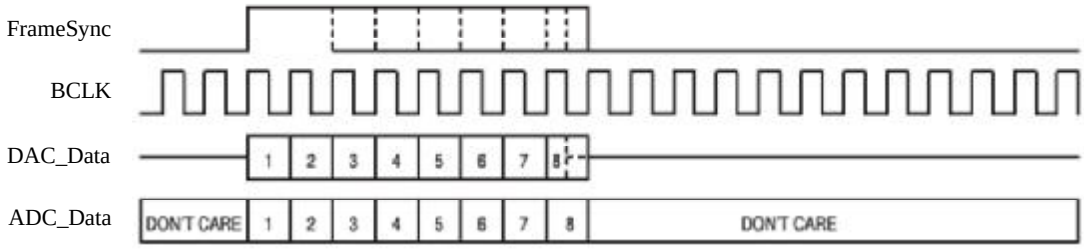


Figure 5. Long FrameSync

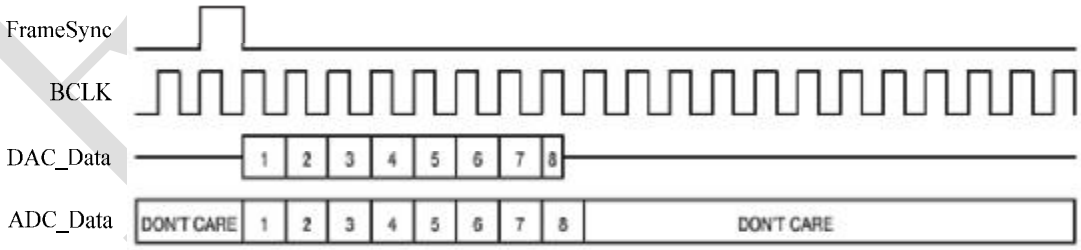


Figure 6. Short FrameSync

5.5.2. Sign Extension and Zero Padding for 8-Bit and 13-Bit Samples

For 16-bit linear PCM output, 3 or 8 unused bits may be sign extended/zero padded.

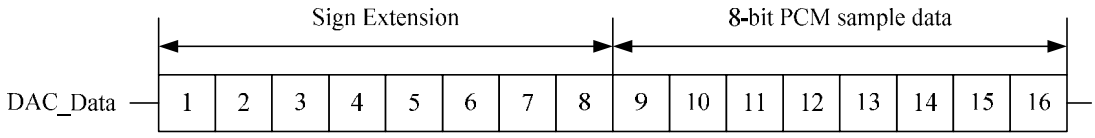


Figure 7. 16-Bit Output Data with 8-Bit PCM Sample Data and Sign Extension

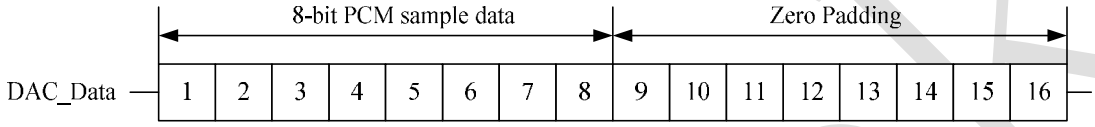


Figure 8. 16-Bit Output Data with 8-Bit PCM Sample Data and Zero Padding

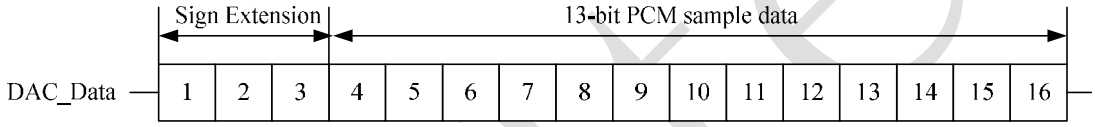


Figure 9. 16-Bit Output Data with 13-Bit PCM Sample Data and Sign Extension

For 16-bit linear PCM output, 3-bit programmable audio gain value can be padded to 13-bit sample data.

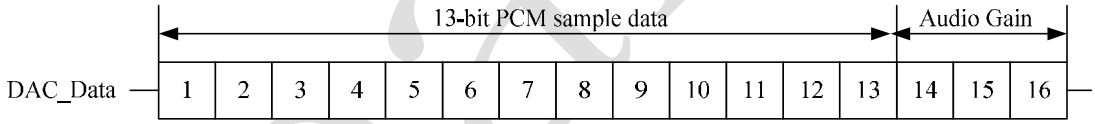


Figure 10. 16-Bit Output Data with 13-Bit PCM Sample Data and Audio Gain

5.5.3. PCM Interface Timing

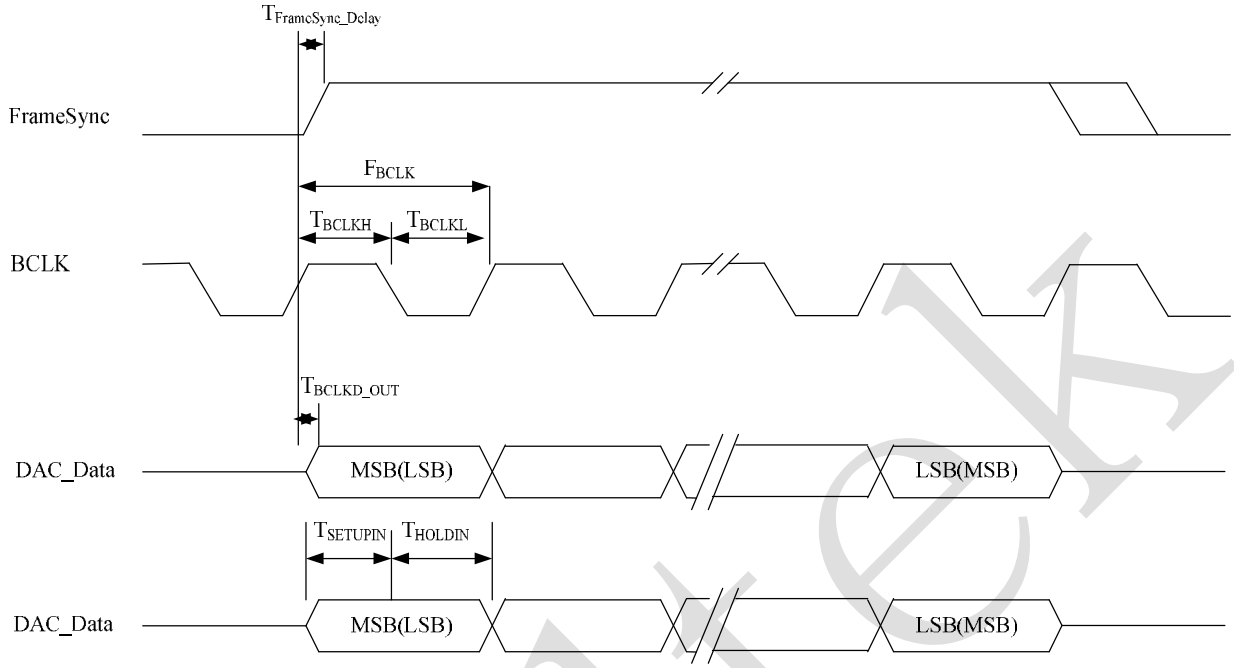


Figure 11. PCM Interface (Long FrameSync)

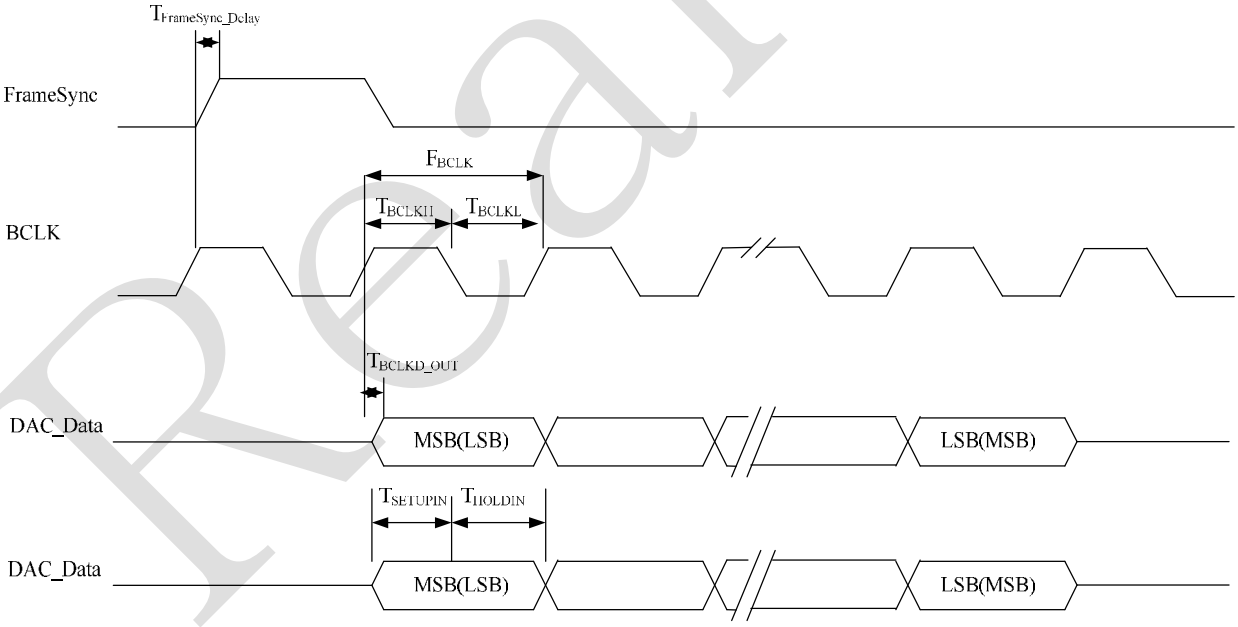


Figure 12. PCM Interface (Short FrameSync)

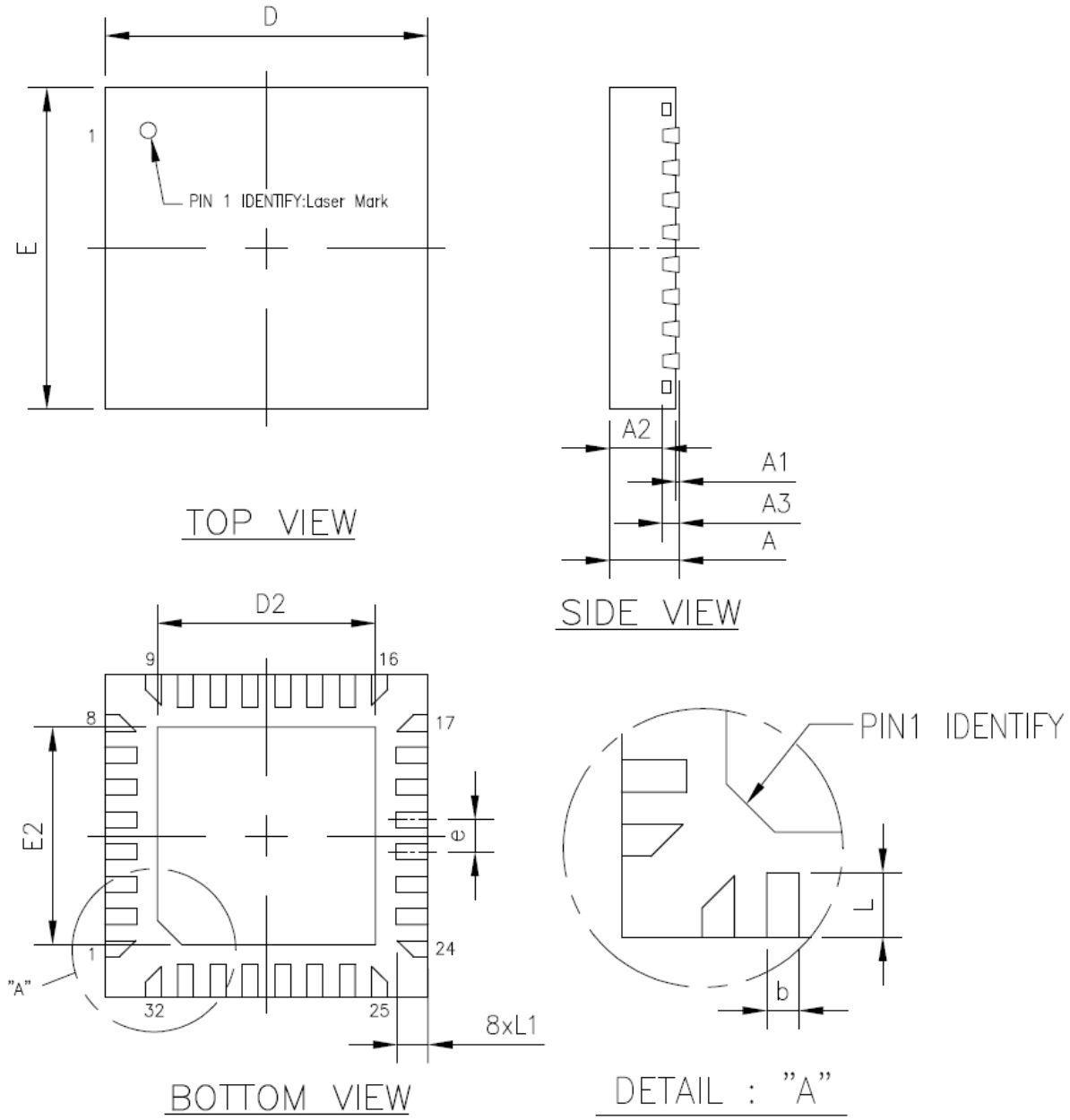
Table 14. PCM Interface Clock Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
F_{BCLK}	Frequency of BCLK (Master)	64	-	512	kHz
$F_{FrameSync}$	Frequency of Frame Sync (Master)	-	8	-	kHz
F_{BCLK}	Frequency of BCLK (Slave)	64	-	512	kHz
$F_{FrameSync}$	Frequency of Frame Sync (Slave)	-	8	-	kHz
D	Data Size	8	8	16	bits
N	Number of Slots Per Frame	1	1	1	Slots

Table 15. PCM Interface Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{BCLKH}	High Period of BCLK	980	-	-	ns
T_{BCLKL}	Low Period of BCLK	970	-	-	ns
$T_{FrameSync\_Delay}$	Delay Time from BCLK High to Frame Sync High	-	-	75	ns
T_{BCLKD_OUT}	Delay Time from BCLK High to Valid DAC_Data	-	-	125	ns
$T_{SETUPIN}$	Set-up Time for ADC_Data Valid to BCLK Low	10	-	-	ns
T_{HOLDIN}	Hold Time for BCLK Low to ADC_Data Invalid	125	-	-	ns

6. Mechanical Dimensions



6.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	—	0.65	0.70	—	0.026	0.028
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.080	0.010
D/E		4.00 BSC			0.157 BSC	
D2/E2	2.45	2.70	2.95	0.096	0.106	0.116
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	0.282	0.382	0.482	0.011	0.015	0.019

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

7. Ordering Information

Table 16. Ordering Information

Part Number	Package	Status
RTL8761ATV-CG	QFN-32, 'Green' Package	Mass Production

Note: See page 3 for package identification.

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