RTL8801B

2-PORT 100/200/400MBPS CABLE TRANSCEIVER/ARBITER CHIP

DATASHEET

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USING THIS DOCUMENT

This document is intended for use by the software engineer when programming for Realtek RTL8801B controller chips. Information pertaining to the hardware design of products using these chips is contained in a separate document.

Though every effort has been made to assure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2002/05/30	First release.
1.1	2003/02/12	Modify block diagram and general description.
2.0	2003/03/22	Modify pin descriptions.
3.0	2003/06/03	Modify application information.
3.4	2003/08/05	Cosmetic changes to document layout.

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1. General Description

The RTL8801B provides a two-port physical layer (PHY) function in a cable-based IEEE 1394-1995 and IEEE P1394a network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission.

1. Data bits to be transmitted through the cable ports are received from the Link On 2/4/8 data lines (D0-D8), and are latched internally in the RTL8801B in synchronization with the 49.152MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304, 196.608, or 393.216Mbps as an outbound data-strobe information stream. During transmission, the encoded data is transmitted on the twisted pair B (TPB) cable pair(s), and the encoded strobe information is transmitted on the twisted pair A (TPA) cable pair(s).
2. During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the received clock signal and the serial data bits. The serial data bits are split into two nibbles, or four by two bits, and parallel transmitted (repeated) out of the other active (connected) cable ports.
3. Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The output of these comparators is used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of the common-mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage for the presence of a remotely supplied twisted-pair bias voltage. The presence or absence of this common-mode voltage is used as an indication of cable connection status. The cable connection status signal is internally debounced in the RTL8801B on a cable disconnect-to-connect. The debounced cable connection status signal initiates a bus reset. On a cable disconnect-to-connect, a debounce delay is incorporated. There is no delay on a cable disconnect.

2. Features

- Fully supports provisions of IEEE 1394-1995 for High-Performance Serial Bus and the P1394a draft 2.0 standard
- Provides three fully compliant cable ports at 100/200/400Mbps. Can be implemented with one or two ports available
- Fully compliant with Open HCI requirements
- Full P1394a additional function support
- Supports optional 1394 Annex J electrical isolation barrier at PHY-link interface
- Supports power-down feature to conserve energy in battery-powered applications
- Cable power presence monitoring
- Separate cable bias (TPBIAS) and driver termination voltage supply for each port
- Encode and decode functions included for data-strobe bit level encoding
- Supports Link Pulse Status as a part of the PHY-link interface
- Incoming data resynchronized to local clock
- Single 24.576 MHz crystal provides transmit/receive data at 100/200/400Mbps and Link Layer Controller clock at 49.152 MHz.
- Node power-class information signaling for system power management
- Adaptive equalizer
- Easily configured as a repeater
- Single 3.3V power supply
- 48-pin LQFP package

3. Block Diagram

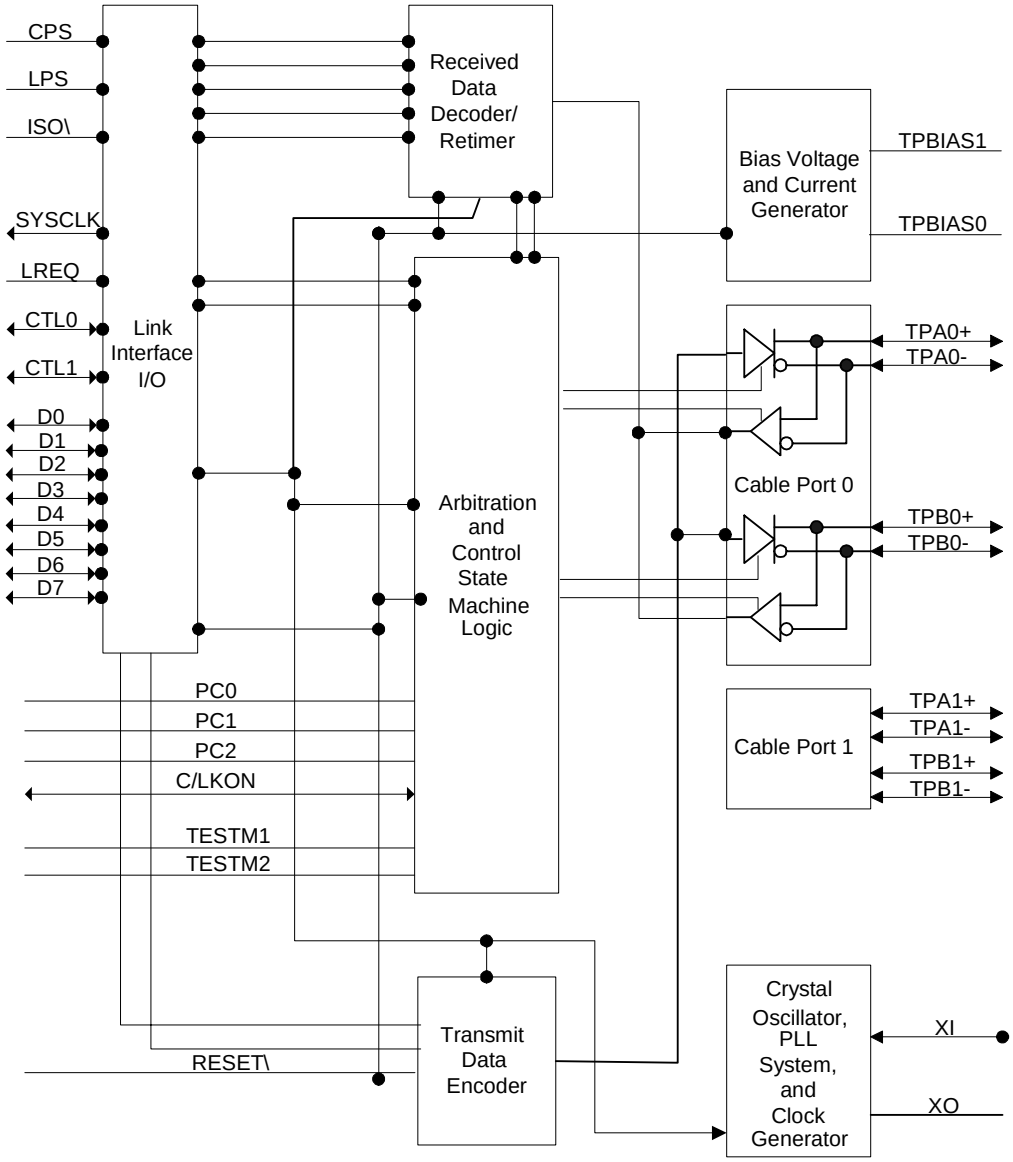


Figure 1. Block Diagram

4. Pin Assignments

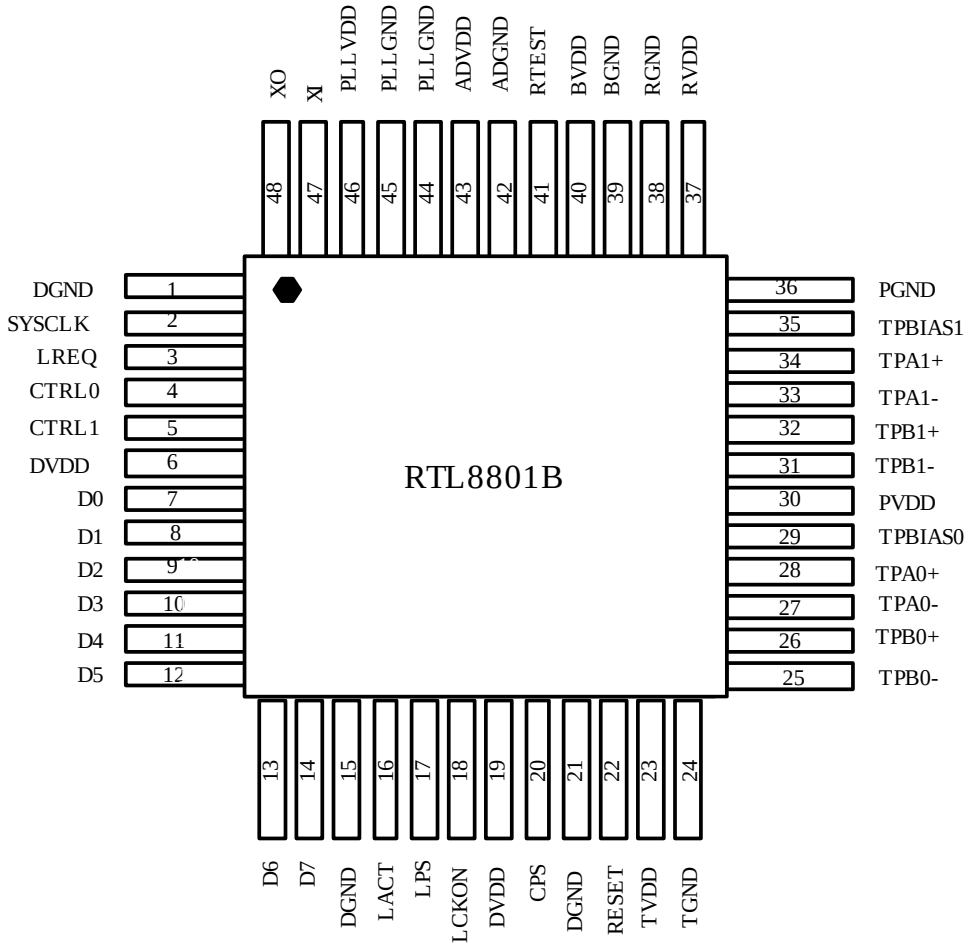


Figure 2. Pin Assignments

5. Pin Descriptions

Table 1. Pin Descriptions

Symbol	Type	Pin(s) No.	Description
C/LKON	I/O	18	Input. Bus manager capable. When set as input, C/LKON specifies in the Self-ID packet that the node is bus manager capable. Output: Link On. When set as output, C/LKON indicates the reception of a link-on packet by asserting a 6.114MHz square wave signal.
CPS	I	20	Cable Power Status. CPS is normally connected to the cable power through a 400-Kohm resistor. This circuit driver an internal comparator that detects the presence of cable power.
LPS	I	17	Link Power Status. LPS monitors the Link power status and is connected to either the VDD supplying the Link, or to a pulsed output that is active when the Link is powered.
LREQ	I	3	Link Request. LREQ is an input from the Link that requests the PHY to perform some service.
LACT	I	16	Link Active. Indicates whether the PHY is linked or not.
CTL0 CTL1	I/O	4, 5	Control I/O. The CTLn pins are bi-directional communication control signals between the PHY and LLC.
D0-D7	I/O	7, 8, 9, 10, 11, 12, 13, 14	Data I/O. The D terminals are bi-directional and pass data between the PHY and LLC.
SYSCLK	O	2	System Clock. SYSCLK provides a 49.152 MHZ clock signal, which is synchronized with the data transfers to the LLC.
TPA0+ TPA0-	I/O	27, 28	Port0, Cable Pair A. TPA0 is the port A connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept matched (and as short as possible) to the external load resistors and to the cable connector.
TPA1+ TPA1-	I/O	33, 34	Port1, Cable Pair A. TPA1 is the port A connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept matched (and as short as possible) to the external load resistors and to the cable connector.
TPB0+ TPB0-	I/O	25, 26	Port0, Cable Pair B. TPB0 is the port B connection to the twisted-pair cable .Board traces from each pair of positive and negative differential signal pins should be kept matched (and as short as possible) to the external load resistors and to the cable connector.
TPB1+ TPB1-	O	31, 32	Port1, Cable Pair B. TPB1 is the port B connection to the twisted-pair cable .Board traces from each pair of positive and negative differential signal pins should be kept matched (and as short as possible) to the external load resistors and to the cable connector.

Symbol	Type	Pin(s) No.	Description
TPBIAS0 TPBIAS1	O	29, 35	Portn, Twisted Pair Bias. Provides the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers and for sending a valid cable connection signal to the remote nodes.
XI XO	-	47, 48	Crystal Oscillator Input and Output.
PLLGND	-	44, 45	PLL Circuit Ground. The pin should be tied to the low impedance ground plane.
PLLVDD	-	46	PLL Circuit Power. PLLVDD supplies power to the PLL circuit.
BVDD	-	40	Digital Power.
PGND	-	36	Port Circuit Ground.
PVDD	-	30	Port Circuit Power.
RGND	-	38	Digital Ground.
RVDD	-	37	Digital Power.
TVDD	-	23	Digital Power.
BTSET	I	41	Bang Gap Voltage Setting. Internal reference voltage is applied to a resistor connected between this pin and ground to set the operating current and the cable driver output current. A resistor with a value of 4.02K ohm +/- 1% should be used to meet the IEEE1394-1995 standard requirements for output voltage limits.
AVDD	-	43	Analog Circuit Power.
AGND	-	42	Analog Circuit Ground.
DVDD	-	19	Digital Power.
DGND	-	1, 21	Digital Ground.
BGND		39	Digital Ground.
DVDD	-	6	Digital Power.
DGND	-	15	Digital Ground.
RESET	I	22	Reset Pin.
TGND		24	Digital Ground.

6. Register Descriptions

Definitions and usage for each of the registers listed below are provided on this and the following pages.

6.1. PHY Register Map for the Cable Environment

Table 2. PHY Register Map for the Cable Environment

Address	0	1	2	3	4	5	6	7
0000b	Physical_ID						R	PS
0001b	RHB	IBR	Gap_count					
0010b	Extended(7)			Reserved	Total_ports			
0011b	Max_speed			Reserved	Delay			
0100b	Link_active	Contender	Jitter			Pwr_class		
0101b	Resume_int	ISBR	Loop	Pwr_fail	Timeout	Port_event	Enab_accel	Enab_multi
0110b	Reserved							
0111b	Page_select			Reserved	Port_select			
1000b	Register0 (page_select)							
1111b	Register7 (page_select)							

6.2. PHY Register Fields for the Cable Environment

Table 3. PHY Register Fields for the Cable Environment

Item	Size	Type	Power Reset Value	Description
Physical_ID	6	R	-	The address of this node is determined during self-identification. A value of 63 indicates a miss-configured bus and the link will not transmit any packets.
R	1	R	-	When set to 1, indicates that this node is the root.
PS	1	R	-	Cable Power Status.
RHB	1	RW	0	Root Hold-off Bit. When set to 1, instructs the PHY to attempt to become the root during the next tree identify process.
IBR	1	RW	0	Initiate Bus Reset. When set to 1, instructs the PHY to initiate a bus reset immediately (without arbitration). This bit causes assertion of the reset state for 166µs and is self-clearing.
Gap_count	6	RW	3F	Used to configure the arbitration timer setting in order to optimize gap times according to the topology of the bus. IEEE 1394-1995 4.3.6
Extended	3	R	7	This field has a constant value of seven, which indicates the extended PHY register map.
Total_ports	5	R	3	The number of ports implemented by this PHY.
Max_speed	3	R	010	Indicates the maximum speed this PHY supports. 000: 98.304Mbps 001: 98.304, 196.608Mbps 010: 98.304, 196.608, 393.216Mbps All other values are reserved for future definition.
Delay	4	R	0	Worse case repeater delay, expressed as 144+ (delay*20) ns.

Item	Size	Type	Power Reset Value	Description
Link_active	1	RW	1	Link enabled. Default value of 1 subsequent to a power reset. Otherwise cleared or set by software to control the value of the L bit transmitted in the self-ID packet. The transmitted L bit shall be the logical AND of this bit and the LPS signal.
Contender	1	RW	Pin C/LKON	Contender. Cleared or set by software to control the value of the C bit transmitted in the self-ID packet.
Pwr_class	3	RW	Pin PC0-PC2	Power Class. Controls the value of the pwr field transmitted in the self-ID packet. 000: Node does not need power and does not repeat power. 001: Node is self-powered and provides a minimum of 15W to the bus. 010: Node is self-powered and provides a minimum of 30W to the bus. 011: Node is self-powered and provides a minimum of 45W to the bus. 100: Node may be powered from the bus and is using up to 1W. 101: Node is powered from the bus and is using up to 1W. An additional 2W is required to enable the link and higher layers. 110: Node is powered from the bus and is using up to 1W. An additional 5W is required to enable the link and higher layers. 111: Node is powered from the bus and is using up to 1W. An additional 9W is required to enable the link and higher layers.
Jitter	3	R	0	The difference between the fastest and slowest repeater data delay, expressed as (jitter+1)*20ns.
Resume_int	1	RW	0	Resume Interrupt Enable. When set to 1, the PHY will set port_event to 1 if resume operations commences for any port.
ISBR	1	RW	0	Initiate Short (Arbitrated) Bus Reset. A write of 1 to this bit instructs the PHY to arbitrate and issue a short bus reset. This bit is self-clearing.
Loop	1	RW	0	Loop Detect. A write of 1 to this bit clears it to zero.
Pwr_fail	1	RW	0	Cable Power Failure Detect. Set to 1 when the PS bit changes from 1 to zero. A write of 1 to this bit clears it to zero.
Timeout	1	RW	0	Arbitration State Machine Timeout. A write of 1 to this bit clears it to zero.
Port_event	1	RW	0	Port Event Detect. The PHY sets this bit to 1 if *Connected*, *Bias*, *Disabled*, or *Fault* status change for a port whose Int_enable bit is 1. The PHY also sets this bit to 1 if resume operations commence for any port and Resume_int is 1. A write of 1 to this bit clears it to zero.
Enab_accel	1	RW	0	Enable Arbitration Acceleration. When set to 1, the PHY will use the enhancements specification in P1394a.
Enab_multi	1	RW	0	Enable Multi-Speed Packet Concatenation. When set to 1, the Link will signal the speed of all packets to the PHY.

Item	Size	Type	Power Reset Value	Description
Page_select	3	RW	000	Selects which of eight possible PHY register pages are accessible through the window at PHY register addresses 1000b through 1111b, inclusive.
Port_select	4	RW	0000	If the page selected by Page_select presents per port information, this field selects which port's registers are accessible through the window at PHY register addresses 1000b through 1111b, inclusive.

6.3. PHY Register Page0: Port Status Page

The port Status page is used to access configuration and status information for each of the PHY's ports. The port is selected by writing zero to Page_select and the desired port number to Port_select in the PHY register at address 0111.

Table 4. PHY Register Page0: Port Status Page

	0	1	2	3	4	5	6	7
1000b	AStat		BStat		Child	Connected	Bias	Disabled
1001b	Negotiated_speed			Int_enable	Fault			
1010b								
1011b								
1100b								
1101b								
1110b								
1111b								

6.4. PHY Register Port Status Page Fields

Table 5. PHY Register Port Status Page Fields

Item	Size	Type	Power Reset Value	Description
Astat	2	R	-	TPA Line State for the Port. 00: Invalid 01: 1 10: 0 11: z
Bstat	2	R	-	Same encoding as Astat.
Child	1	R	-	If equal to 1, the port is a child, otherwise it is a parent. The meaning of this bit is undefined from the time a bus reset is detected until the PHY transitions to state T1: Child Handshake during the tree identify process (see 4.4.2.2 in IEEE Std 1394-1995).
Connected	1	R	0	If equal to 1, the port is connected, otherwise it is disconnected. The value reported by this bit is filtered by hysteresis logic to reduce multiple status changes caused by contact scrape when a connector is inserted or removed.
Bias	1	R	-	If equal to 1, bias voltage is detected (possible connection). The value reported by this bit is filtered by hysteresis logic to reduce multiple status changes caused by contact scrape when a connector is inserted or removed.

Item	Size	Type	Power Reset Value	Description
Disabled	1	RW	0	When set to 1, the port is disabled. The value of this bit subsequent to a power reset is implementation-dependent, but should be a strappable option.
Negotiated_ speed	3	R	-	Indicates the maximum speed negotiated between this PHY port and its immediately connected port; the encoding is: 000: 98.304Mbps 001: 196.608Mbps 010: 393.216Mbps
Int_Enable	1	RW	0	Enable Port Event Interrupts. When set to 1, the PHY will set Port_event to 1 if there is any change in the Connected, Bias, Disabled, or Fault (for this port) state.
Fault	1	RW	0	Set to 1 if an error is detected during a suspend or resume operation. A write of 1 to this bit clears it to zero.

6.5. PHY Register Page 1: Vendor Identification Page

The Vendor Identification page is used to identify the PHY's vendor and compliance level. The page is selected by writing 1 to Page_select in the PHY register at address 0111.

Table 6. PHY Register Page 1: Vendor Identification Page

	0	1	2	3	4	5	6	7
1000b	Compliance_level							
1001b	Reserved							
1010b	Vendor_ID							
1011b								
1100b								
1101b	Product_ID							
1110b								
1111b								

6.6. PHY Register Vendor Identification Page Fields

Table 7. PHY Register Vendor Identification Page Fields

Item	Size	Type	Description	Default
Compliance_ level	8	R	Standard to which the PHY implementation complies: 0: Not specified 1: IEEE P1394a All other values reserved.	1
Vendor_ID	24	R	The company ID or Organizationally Unique Identifier (OUI) of the manufacturer of the PHY. The most significant byte of Vendor_ID appears at PHY register location 1010 and the least significant at 1100.	00 e0 4c
Product_ID	24	R	The meaning of this number is determined by the company or organization that has been granted Vendor_ID. The most significant byte of Product_ID appears at PHY register location 1101 and the least significant at 1111.	00

7. Functional Description

The main controller of the cable PHY is the block labeled ‘Arbitration and Control State Machine Logic’ (see Figure 1, page 3), which responds to arbitration requests from the link layer and changes in the state of attached ports. It provides management and timing signals for transmitting, receiving, and repeating packets. It also provides for bus reset and configuration. The cable environment supports the immediate, fair, isochronous, and cycle_master arbitration classes, where the cycle_master class is only available in the root node.

Cable arbitration has two parts: a three-phase initialization process (bus reset, tree identify, and self-identify), and a normal operation phase. Each of these phases is described using a state machine. The state machine and the list of actions and conditions are the normative part of the IEEE standard.

The ‘Received Data Decoder/Retimer’ block decodes the data-strobe signal and retimes the received data to a local fixed-frequency clock provided by the local clock. Since the clocks of receiving and transmitting nodes can be up to 100 ppm different from the nominal, the data resynch function has to be able to compensate for a difference of 200 ppm over the maximum packet length of 84.31µs (1024 byte isochronous packet at 98.304Mbps). Data reception for the cable environment physical layer has three major functions: decoding the data-strobe signal to recover a clock, synchronizing the data to a local clock for use by the link layer, and repeating the synchronized data out to all other connected ports.

The ‘Transmit Data Encoder’ block provides a common interface to the link layer for both packet data and arbitration signals (gaps and bus reset indicators). Data transmission is a straightforward function: the data bits are sent to the attached peer PHY along with the appropriately encoded strobe signal using timing provided by the PHY transmit clock. If a connected port cannot accept data at the requested speed, then no data is sent (leaving the drivers in the ‘01’ data prefix condition).

The ‘Link Interface I/O’ block provides a scalable, cost-effective method to connect one serial bus link chip to one serial bus PHY chip. The width of the data bus scales with the highest speed both chips can support, using two pins per 100Mbps. The clock rate of the signals at this interface remains constant, independent of speed, to support galvanic isolation for implementations where it is desirable.

The PHY has control over the bidirectional pins. The link only drives these pins when control is transferred to it by the PHY. The link performs all unsolicited activity through a dedicated request pin. Possible actions that may occur on the interface are categorized as transmit, receive, status, and request.

8. Characteristics

8.1. Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply Voltage	-0.3	4	V
Storage Temp.	-65	150	°C

8.2. Operating Range

Table 9. Operating Range

Symbol	Conditions	Min.	Max.	Units
Vcc	Supply voltage	3.0	3.6	V
TA	Operating Temperature	0	70	°C

8.3. Power Dissipation

Max = 900 mW

8.4. Timing Waveforms

Dn, CTLn, LREQ Input Setup and Hold Times Waveforms

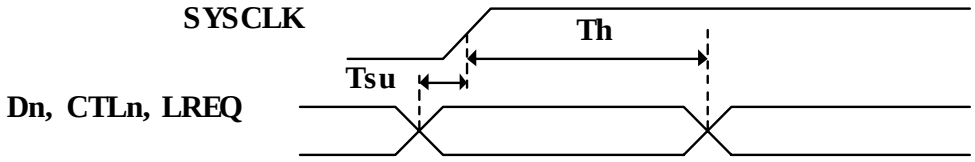


Figure 3. Timing Waveforms

Table 10. Digital Timing Characteristics

Symbol	Parameter	Min.	Units
Tsu	Setup time, Dn, CTLn, LREQ to Sysclk	5	ns
Th	Hold time, Dn, CTLn, LREQ before Sysclk	2	ns

9. Application Information

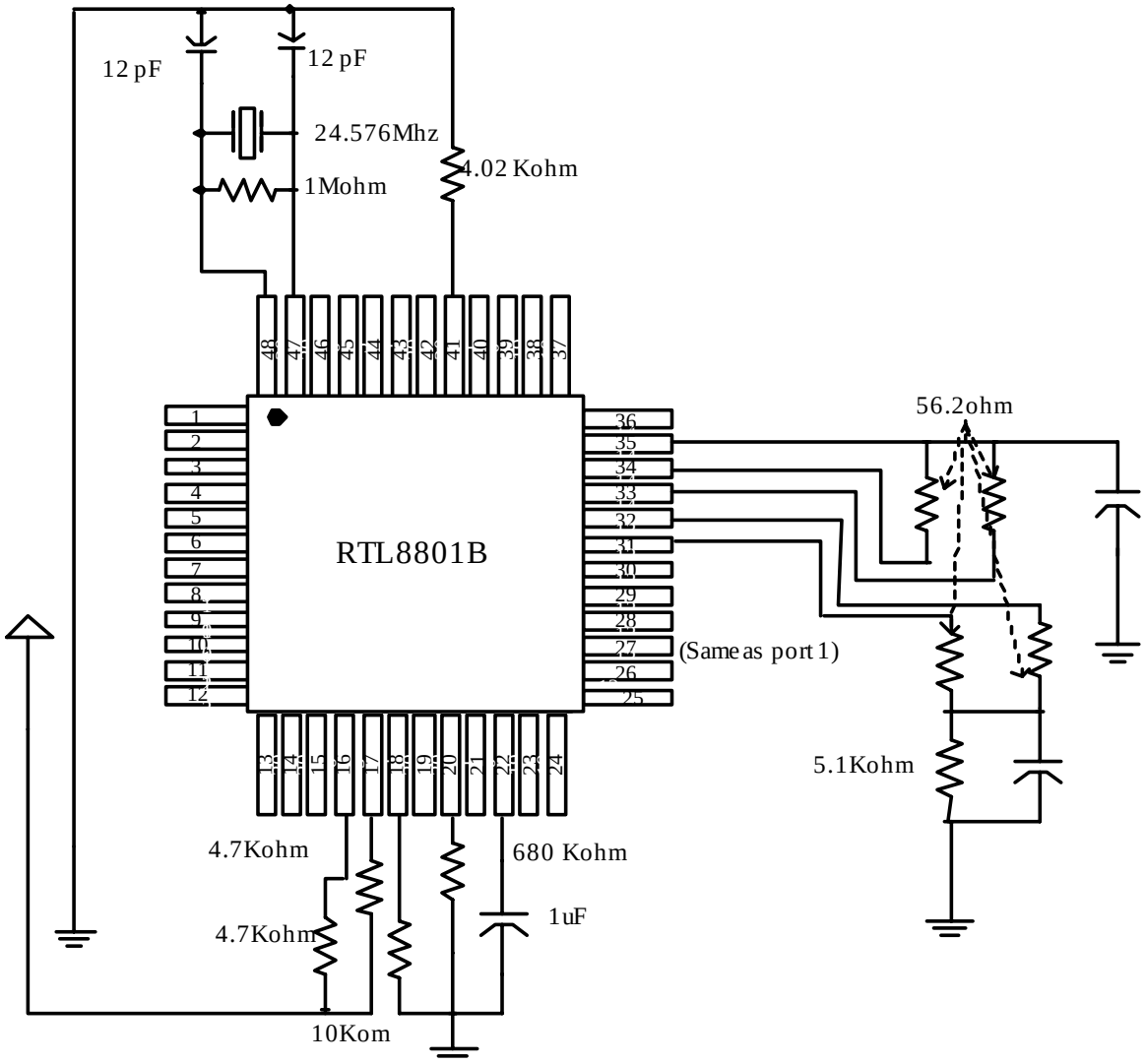
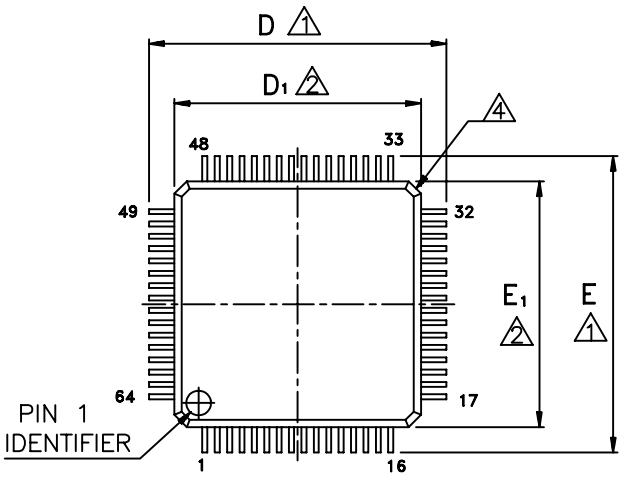
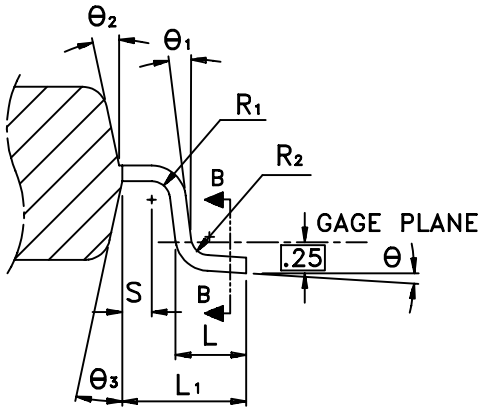


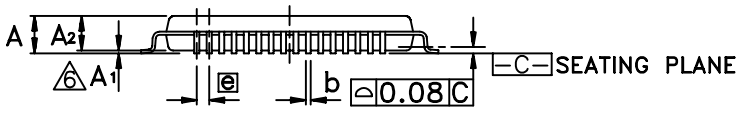
Figure 4. Application Information

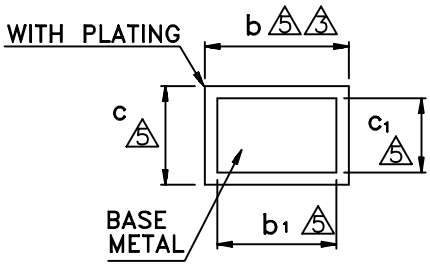
10. Mechanical Dimensions





SECTION A–A





SECTION B–B

See the Mechanical Dimensions notes on the next page.

10.1. Mechanical Dimensions Notes

A	-	-	0.067	-	-	1.70
A1	0.000	0.004	0.008	0.00	**0.1**	0.20
A2	0.051	0.055	0.059	1.30	**1.40**	1.50
b	0.006	0.009	0.011	0.15	**0.22**	0.29
b1	0.006	0.008	0.010	0.15	**0.20**	0.25
c	0.004	-	0.008	0.09	-	0.20
c1	0.004	-	0.006	0.09	-	0.16
D	0.472 BSC			12.00 BSC		
D1	0.394 BSC			10.00 BSC		
E	0.472 BSC			12.00 BSC		
E1	0.394 BSC			10.00 BSC		
e	0.020 BSC			0.50 BSC		
L	0.016	0.024	0.031	0.40	0.60	0.80
L1	0.039 REF			1.00 REF		
θ	0°	3.5°	9°	0°	3.5°	9°
θ1	0°	-	-	0°	-	-
θ2	12° TYP			12° TYP		
θ3	12° TYP			12° TYP		

Notes:

1.To be determined at seating plane -c-

2.Dimensions D_1 and E_1 do not include mold protrusion. D_1 and E_1 are maximum plastic body size dimensions including mold mismatch

3.Dimension b does not include dambar protrusion.
Dambar can not be located on the lower radius of the foot.

4.Exact shape of each corner is optional.

5.These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

6. A_1 is defined as the distance from the seating plane to the lowest point of the package body.

7.Controlling dimension : millimeter.

8. Reference document : JEDEC MS-026 , BBC

TITLE : 64LD LQFP (10x10x1.4mm) PACKAGE OUTLINE DRAWING , FOOTPRINT 2.0mm			
LEADFRAME MATERIAL:			
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