RTL8821CS

SINGLE-CHIP 802.111/b/g/n/ac 1T1R WLAN with Integrated Bluetooth 2.1/4.2 CONTROLLER WITH SDIO INTERFACE

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2016/01/05	Preliminary release.
0.2	2016/6/20	Modify general description and features

Notice:

This Data Sheet is the preliminary release for the product specification reference. The specification will be adjusted by the actual product specification and function in the mass production without further notice.

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1. General Description

The Realtek RTL8821CS is a highly integrated single-chip that support 1-stream 802.11ac solutions with Multi-user MIMO (Multiple-Input, Multiple-Output) STA mode with integrated Bluetooth 2.1/4.2 controller, SDIO (SDIO 1.1/2.0/3.0) interface, and HS-UART mixed interface. It combines a WLAN MAC, a 1T1R capable WLAN baseband, and RF in s single chip. The RTL8821CS provides a complete solution for a high-performance integrated wireless and Bluetooth device.

The RTL8821CS baseband implements Multi-user Multiple Input, Multiple Output (MU MIMO) Orthogonal Frequency Division Multiplexing (OFDM) STA mode with one transmit and one receive path (1T1R). Features include one spatial stream transmission, short Guard Interval (GI) of 400ns, spatial spreading, and support for variant channel bandwidth. Moreover, RTL8821CS provides one spatial stream space-time block code (STBC), Transmit Beamforming (TxBF) and Low Density Parity Check (LDPC) to extend the range of transmission. As the recipient, the RTL8821CS also supports explicit sounding packet feedback that helps senders with beamforming capability.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b, 802.11g and 802.11a data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability are available, and CCK provides support for legacy data rates, with long or short preamble. The high speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation of the individual subcarriers, and rate compatible coding rate of 1/2, 2/3, 3/4, and 5/6, provide up to 433.3Mbps for IEEE 802.11ac MIMO OFDM.

The RTL8821CS builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference.

Receive vector diversity for multi-stream application is implemented for efficient utilization of the MIMO channel. Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end.

The RTL8821CS supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control functions to obtain better performance in the analog portions of the transceiver.

The RTL8821CS MAC supports 802.11e for multimedia applications, 802.11i and WAPI (Wireless Authentication Privacy Infrastructure) for security, and 802.11n/802.11ac for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol

efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, U-APSD, and MIMO power saving reduce the power wasted during idle time, and compensate for the extra power required to transmit MIMO OFDM. The RTL8821CS provides simple legacy, 20MHz/40MHz/80MHz co-existence mechanisms to ensure backward and network compatibility.

The RTL8821CS Bluetooth controller complies with Bluetooth core specification v4.2, and supports dual mode (BR/EDR + Low Energy Controllers). It is compatible with previous versions, including v2.1 + EDR. For BR/EDR, it supports scatternet topology and allows active links in slave mode, and active links in master mode. For Low Energy, it supports multiple states and allows active links in master mode. The links in BR/EDR and LE can be active simultaneously.

2. Features

General

- TFBGA 5.2x5.2mm package
- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/b/g/n/ac compatible WLAN
- Support 802.11ac 1x1,Wave-2 compliant with MU-MIMO STA mode
- Complete 802.11n MIMO solution for 2.4GHz and 5Ghz band
- Maximum PHY data rate up to 86.7Mbps using 20MHz bandwidth, 200Mbps using 40MHz bandwidth, and 433.3Mbps using 80MHz bandwidth.
- Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates
- Backward compatible with 802.11a/n devices while operating at 802.11ac data rates.

Host Interface

- Complies with SDIO 1.1/2.0/3.0 for WLAN with clock rate up to 100MHz (SDR50 and DDR50)
- G-SPI interface for configurable endian for WLAN
- Complies with HS-UART with configurable baud rate for Bluetooth

Standards Supported

- IEEE 802.11a/b/g/n/ac compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- IEEE 802.11h DFS, TPC, Spectrum Measurement
- IEEE 802.11k Radio Resource Measurement
- WAPI (Wireless Authentication Privacy Infrastructure) certified.
- Cisco Compatible Extensions (CCX) for WLAN devices

MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate Block Acknowledgement (BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- MIMO power saving mechanism
- Channel management and co-existence

- Multiple BSSID feature allows the RTL8821CS to assume multiple MAC identities when used as a wireless bridge
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- WiFi Direct supports wireless peer to peer applications
- WiFi NAN (Neighborhood Area Network) support
- WiFi FTM (Fine Time Measurement) supported
- WiFi TDLS (Tunneled Direct Link Setup) Supported
-

Other Features

- Supports Wake-On-WLAN via Magic Packet and Wake-up frame
- Transmit Beamforming
- CCA on secondary through RTS/CTS handshake.
- Support TCP/UDP/IP checksum offload

Peripheral Interfaces

- Up to 15 General Purpose Input/Output pins
- Three configurable LED pins (mux with GPIO pins)
- Generates 40MHz clock for peripheral chip.
- Single external power source 3.3V only

PHY Features

- IEEE 802.11ac OFDM
- IEEE 802.11n OFDM
- One Transmit and One Receive path
- 5MHz / 10MHz / 20MHz / 40MHz / 80MHz bandwidth transmission
- Support 2.4Ghz and 5Ghz band channels
- Short Guard Interval (400ns)
- Sounding packet.
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g, 150Mbps in 802.11n and 433Mbps in 802.11ac.
- Switch diversity used for DSSS/CCK
- Support STBC receiving
- Support LDPC transmitting
- Hardware antenna diversity
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC
- Build-in both 2.4GHz and 5GHz PA
- Build-in both 2.4GHz and 5GHz LNA

Bluetooth Controller

- Compatible with Bluetooth v2.1+EDR
- Support Bluetooth 4.2 features
- HS-UART interface for Bluetooth data transmission compliant with H4 and H5 specification
- PCM interface for audio data transmission via Bluetooth controller
- Integrated MCU to execute Bluetooth protocol stack
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/eSCO link (allows one link for PCM interface and three links for HS-UART)
- Supports piconets in a scatternet
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff/Sniff Sub-rating)
- Enhanced BT/WLAN Coexistence Control to improve transmission quality in different profiles
- Bluetooth 4.0 Dual Mode support: Simultaneous LE and BR/EDR
- Supports multiple Low Energy states

Bluetooth Transceiver

- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Integrated internal Class 1, Class 2, and Class 3 PA
- Supports Enhanced Power Control
- Supports Bluetooth Low Energy
- Integrated 32K oscillator for power management

Peripheral Interfaces

- General Purpose Input/Output (8 pins)
- 4-wire EEPROM control interface (93C46)
- Three configurable LED pins
- Flexible CRYSTAL frequency selection(52, 48, 40, 38.4, 27, 26, 25, 24, 20, 19.2, 17.664, 16, 14.318, 13 and 12MHz)
- Support CRYSTAL or external clock input

3. Application Diagrams

3.1. 11ac Dual-Band 1x1 RF Application with Antenna Diversity

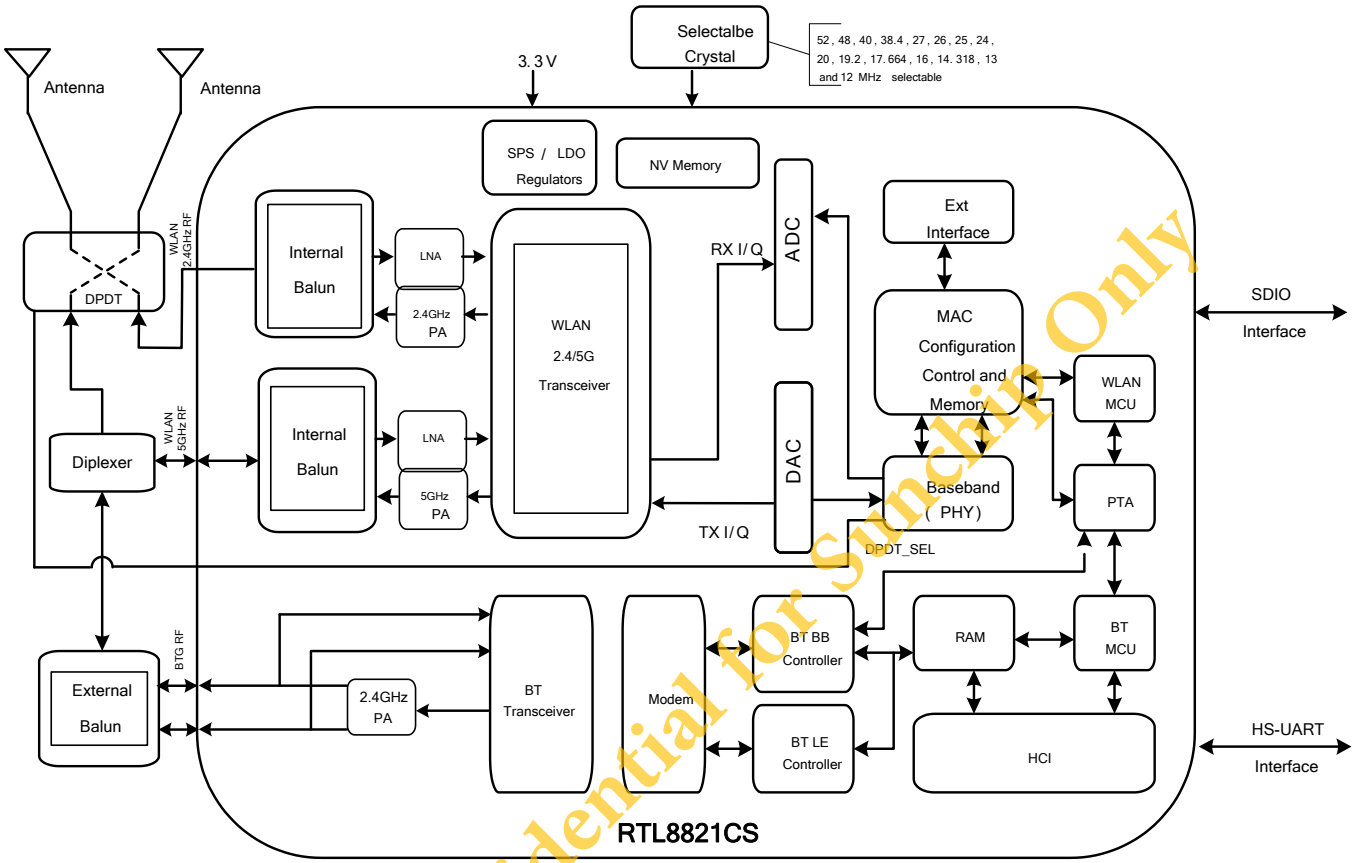


Figure 1. Dual-Band MIMO 1x1 Solution(11ac 1x1 MAC/BB/RF + PA) and Integrated Bluetooth Controller Solution with Antenna Diversity --- RTL8821CS

3.2. 11ac Dual-Band 1x1 RF Application with Single Antenna

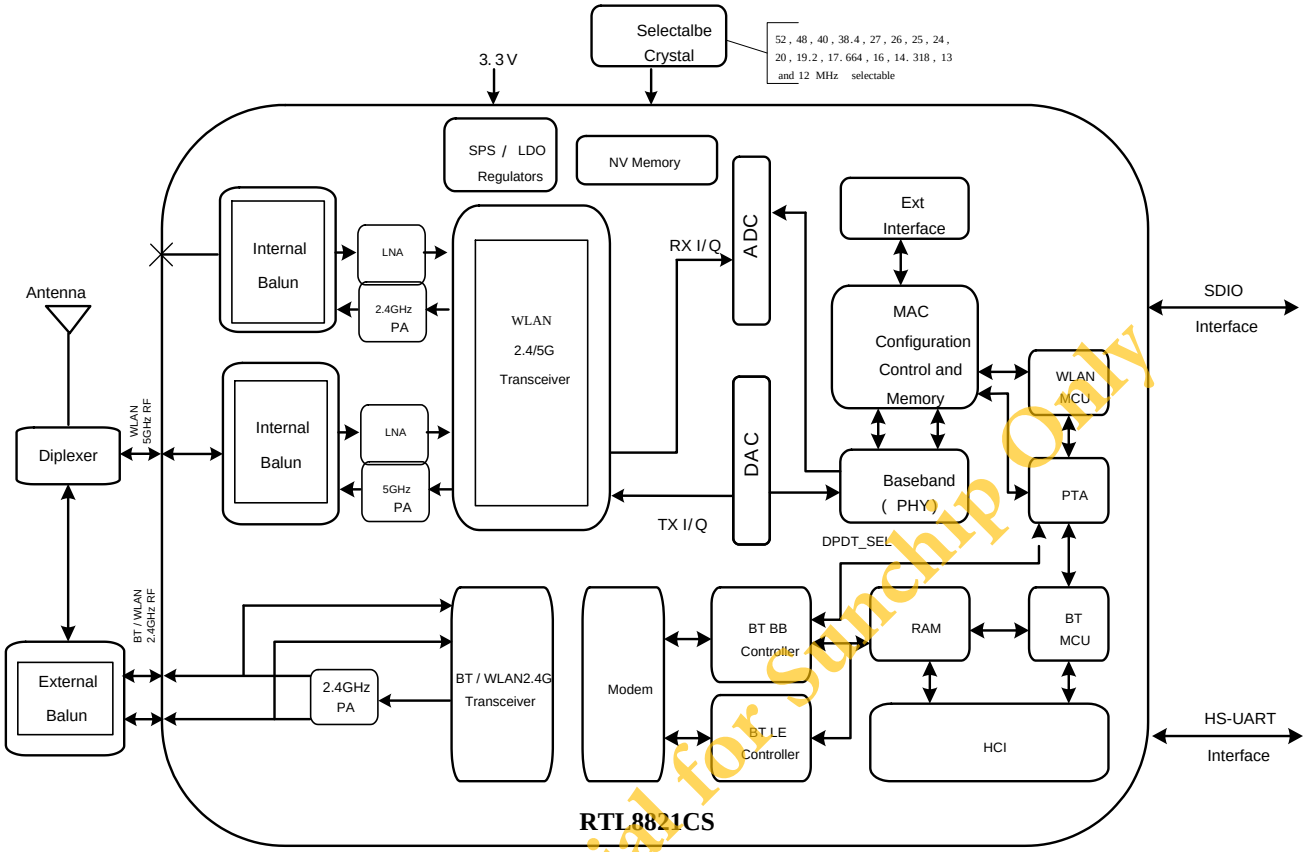


Figure 2. Dual-Band MIMO 1x1 Solution(11ac 1x1 MAC/BB/RF + PA) and Integrated Bluetooth Controller Solution with Single Antenna --- RTL8821CS

4. TFPGA Ball Assignments

Figure 3. TFBGA Ball Assignments

4.1. Package Identification

Green package is indicated by a 'G' in the location marked 'T' in

Figure 3.

Mark Item	Body (mm^2)	LOGO FONT / LOGO SIZE	2.7 x 2.2 mm^2	Mark Example	備註 Remark
T54	5x5~ 5.2x5.2				1. Pin 1 dot diameter 0.4mm. 2. Pin1 位置在正印的左下 Pin1 mark orientation：bottom left 3. 標準 b=0.4, c=0.1, 若 part no 大於等於 10 碼，b=0.375, c=0.05 Generally, b=0.4, c=0.1. If more than 10 digits of part no., b=0.375, c=0.05.

Line	Item	FONT	a (mm)	b (mm)	c (mm)	d (mm)	e (mm)	對齊 Alignment
1	Part no.	Realtek standard	0.50	0.40/ 0.375	0.1/0. 05	0.1	-	Left
2	Lot no.	Realtek standard	0.50	0.40/ 0.375	0.1/0. 05	0.1	-	Left
3	Date Code (BDC/ADC)	Realtek standard	0.50	0.40/ 0.375	0.1/0. 05	0.1	-	Right

5. Ball Descriptions

The following signal type codes are used in the tables:

I:	Input	O:	Output
T/S:	Tri-State bi-directional input/output pin	S/T/S:	Sustained Tri-State
O/D:	Open Drain	P:	Power pin
N/A:	No Bonding pin		

5.1. Power On Trap Pin

Table 1. Power-On Trap Pins

Symbol	Type	Ball No	Description
TEST_MODE_SEL	I	A6	Shared with GPIO4 0: Normal operation mode 1: Test/debug mode
SPS_LDO_SEL	I	A5	Shared with GPIO5 0: Internal switching regulator select 1: Internal LDO select
EEPROM_SEL	I	F7	Shared with EESK pin 0: Internal NV memory select 1: External EEPROM select

5.2. SDIO Interface

Table 2. SDIO Interface

Symbol	Type	Ball No	Description
SD_CLK	I	C10	SDIO Clock Input
SD_CMD	IO	D10	SDIO Command Input
SD_D0	IO	E10	SDIO Data Line 0
SD_D1	IO	F10	SDIO Data Line 1
SD_D2	IO	G10	SDIO Data Line 2
SD_D3	IO	H10	SDIO Data Line 3

5.3. G-SPI Interface

Table 3. G-SPI Interface

Symbol	Type	Pin No	Description
SPI_CLK	I	C10	Serial clock (output from master)
SPI_OUT (MOSI)	I	D10	Output from Master and input to slave
SPI_IN (MISO)	O	E10	Input to Master and output from slave
SPI_INT	O	F10	Active low output(output from slave)
SPI_CS (SCSn)	I	H10	Active low (output from master)

5.4. HS-UART Transceiver Interface

Table 4. HS-UART Interface

Symbol	Type	Ball No	Description
UART_TX	O	B10	High-Speed UART Data Out
UART_CTS	I	D9	High-Speed UART CTS
UART_RTS	O	B9	High-Speed UART RTS
UART_RX	I	A10	High-Speed UART Data In

5.5. EEPROM Interface

Table 5. EEPROM Interface

Symbol	Type	Ball No	Description
EECS	O	C2	External EEPROM Chip Select
EESK	O	F7	External EEPROM Clock

5.6. PCM Interface

Table 6. PCM Interface

Symbol	Type	Pin No	Description
PCM_IN	I	B6	PCM data Input, shared with GPIO0
PCM_OUT	O	B5	PCM data Out, shared with GPIO1
PCM_SYNC	O	C6	PCM Synchronization control, shared with GPIO2
PCM_CLK	IO	C5	PCM Clock, shared with GPIO3

5.7. I²S Interface

Table 7. PCM Interface

Symbol	Type	Ball No	Description
I2S_IN	I	B6	I^2S Input, shared with GPIO0
I2S_OUT	O	B5	I^2S Out, shared with GPIO1
I2S_WS	O	C6	I^2S Word Synchronization control, shared with GPIO2
I2S_CLK	IO	C5	I^2S Clock, shared with GPIO3

5.8. RF Interface

Table 8. RF Interface

Symbol	Type	Ball No	Description
BTG RFIO_N	I/O	A1	BT/WLAN 2G RF Differential I/O N
BTG RFIO_P	I/O	B1	BT/WLAN 2G RF Differential I/O P
RFIP_WL5G	N/A	E1	NC
RFIO_WL5G	I/O	F1	WLAN 5G RF I/O
RFIO_WL2G	I/O	H1	WLAN 2G RF I/O
RFIP_WL2G	N/A	J1	NC
WL_TSSI	I	F4	External PA TSSI INPUT
DPDT_SEL_P	O	E4	External DPDT CONTROL
DPDT_SEL_N	O	F5	External DPDT CONTROL
PAPE_5G	O	G5	External 5G PAPE CONTROL
PAPE_2G	O	D5	External 2G PAPE CONTROL
LNAON_5G	O	G4	External 5G LNA CONTROL
LNAON_2G	O	D4	External 2G LNA CONTROL

5.9. LED Interface

Table 9. LED Interface

Symbol	Type	Ball No	Description
LED0	O	D6	LED Pin (Active Low)
LED1	O	C4	LED Pin (Active Low)

Symbol	Type	Ball No	Description
LED2	O	C3	LED Pin (Active Low), shared with GPIO8

5.10. Power Management Handshake Interface

Table 10. Power Management Handshake Interface

Symbol	Type	Ball No	Description
SD_RESET	I	J7	Shared with GPIO9 This Pin Can Externally Shutdown the RTL8821CS WLAN function when SD_RESET is pulled low. When this pin is pulled low, SDIO/G-SPI interface will be disabled.
BT_DIS#	I	C7	Shared with GPIO11. This Pin Can Externally Shutdown the RTL8821CS BT function when BT_DIS# is Pulled Low. When this pin is pulled low, UART interface will be also disabled. This pin can also be defined as the BT Radio-off function with host interface remaining connected.
CHIP_EN	I	H9	This Pin Can externally shut down the RTL8821CS (No Extra Power Switch Required). When this function is not required, external pull high is required.
WL_DIS_N	I	E5	Shared with GPIO15. This pin can be defined as the WLAN Radio-off function with host interface remaining connected. When this pin is pulled low, WLAN Radio will be disabled.
VBAT_LDO_EN	I	B7	This pin can externally shutdown the RTL8821CS VBAT LDO (a LDO supports 2.8V~5.5V input and 3.3V output) function when VBAT_LDO_EN is pulled low.

5.11. Clock and Other Pins

Table 11. Clock and Other Pins

Symbol	Type	Ball No	Description
XI	I	K3	26M/40MHz OSC Input Input of 26M/40MHz Crystal Clock Reference
XO	O	K4	Output of 26MHz/40MHz Crystal Clock Reference
SUS_CLK	I	C2	Shared with EECS. External 32K or RTC clock input.
GPIO0	IO	B6	General Purpose Input/ Output Pin
GPIO1	IO	B5	General Purpose Input/ Output Pin
GPIO2	IO	C6	General Purpose Input/ Output Pin
GPIO3	IO	C5	General Purpose Input/ Output Pin
GPIO4	IO	A6	General Purpose Input/ Output Pin
GPIO5	IO	A5	General Purpose Input/ Output Pin
GPIO6	IO	H5	General Purpose Input/ Output Pin
GPIO7	IO	J5	General Purpose Input/ Output Pin
GPIO8	IO	C3	General Purpose Input/ Output Pin
GPIO9	IO	J7	General Purpose Input/ Output Pin
GPIO10	IO	H8	General Purpose Input/ Output Pin
GPIO11	IO	C7	General Purpose Input/ Output Pin

Symbol	Type	Ball No	Description
GPIO12	IO	J6	General Purpose Input/ Output Pin
GPIO13	IO	F6	General Purpose Input/ Output Pin
GPIO14	IO	E6	General Purpose Input/ Output Pin
GPIO15	IO	E5	General Purpose Input/ Output Pin

5.12. Power Pins

Table 12. Power Pins

Symbol	Type	Ball No	Description
VBAT_LDO_IN	P	A8	Battery LDO input, 5.5V ~ 2.8V The power source supplied for this LDO should keep working during system power off. e.g. a battery like power source.
VBAT_LDO_OUT	P	A9	Battery LDO output, 3.3V
VBAT_LDO_EN	I	B7	Battery LDO enabled
LX_SPS	P	K10	Switching Regulator Output
VD33_SPS	P	K9	Switching Regulator Input Or Linear Regulator input from 3.3V to 1.5V
VD33_IO	P	K8	VDD3.3V for Digital IO
VD33_IO_1	P	B4	VDD3.3V for Digital IO (GPIO8,LED0,LED1,EECS)
VDD_IO_1	P	A7	VDD for GPIO0 to GPIO5 and GPIO11
VDD_IO	P	K7	VDD for GPIO6,GPIO7,GPIO9,GPIO10,GPIO12,GPIO13,GPIO14,GPIO15, CHIP_EN,EESK
VD10D_WL	P	J9	1.05V for WLAN digital power
VD10D_BT	P	B8	1.05V for BT digital power
GND_SPS	P	J10	Switching Regulator Ground
VIO_HOST	P	F9	supply voltage for SDIO IO
GND	P	F2,F3,G3,G6,G7,G9 ,H2,H3,H4,H6,H7,J 3,J4,J8,B3,C1,C8,C 9,D2,D3,D7,D8,E2, E3,E9	GND
VD1_BT	P	B2	VDD 1.05V for BT RF
VD33_PAD_BT	P	A2	VDD 3.3V for BT PAD
VD1_SYN_BT	P	A4	VDD 1.05V for BT synthesizer
VD33_SYN_BT	P	A3	VDD 3.3V for BT synthesizer
VD33_PA_WL	P	G1	VDD 3.3V for WLAN PA
VD33_PA_WL	P	G2	VDD 3.3V for WLAN PA
VD1_RF_WL	P	D1	VDD 1.05V for WLAN RF
VD1_RF_WL	P	K1	VDD 1.05V for WLAN RF
VD1_SYN_WL	P	J2	VDD 1.05V for WLAN synthesizer
VD33_SYN_WL	P	K2	VDD 3.3V for WLAN synthesizer
VD33X	P	K5	VDD 3.3V for crystal
VD10A	P	K6	VDD 1.05V for crystal

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 13. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. DC Characteristics

6.2.1. Power Supply Characteristics

Table 14. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VD33	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
VD10	1.05V Core Supply Voltage	0.945	1.05	1.155	V

6.2.2. Digital IO Pin DC Characteristics

Table 15. 3.3V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

PS. 3.3V and 1.2V ripple < 100mV

7. Interface Timing Specification

7.1. SDIO Interface AC Characteristics

For timing criteria, please check “SD specifications Part1 Physical Layer Specification Version 3.01”

7.2. SDIO/G-SPI Interface Signal Levels

The SDIO and G-SPI signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8821CS SDIO and G-SPI interfaces via the VIO_HOST pin (Ball F9).

7.2.1. SDIO/G-SPI Interface Characteristics

■ SDIO Interface Timing

For timing criteria, please check SDR12 specification in "SD specifications Part1 Physical Layer Specification Version 3.01"

■ G-SPI Interface Timing

A high-to-low transition on the SPI_CS pin is required to start a SPI bus transaction, and a low-to-high transition is required at the end the transaction.

SPI_IN and SPI_OUT data transient are driven by the falling edge of the SPI_CLK and latch the data at the rising edge of the SPI_CLK. The data bit shift out order on the SPI_IN and SPI_OUT is from MSB to LSB (MSB first, LSB last).

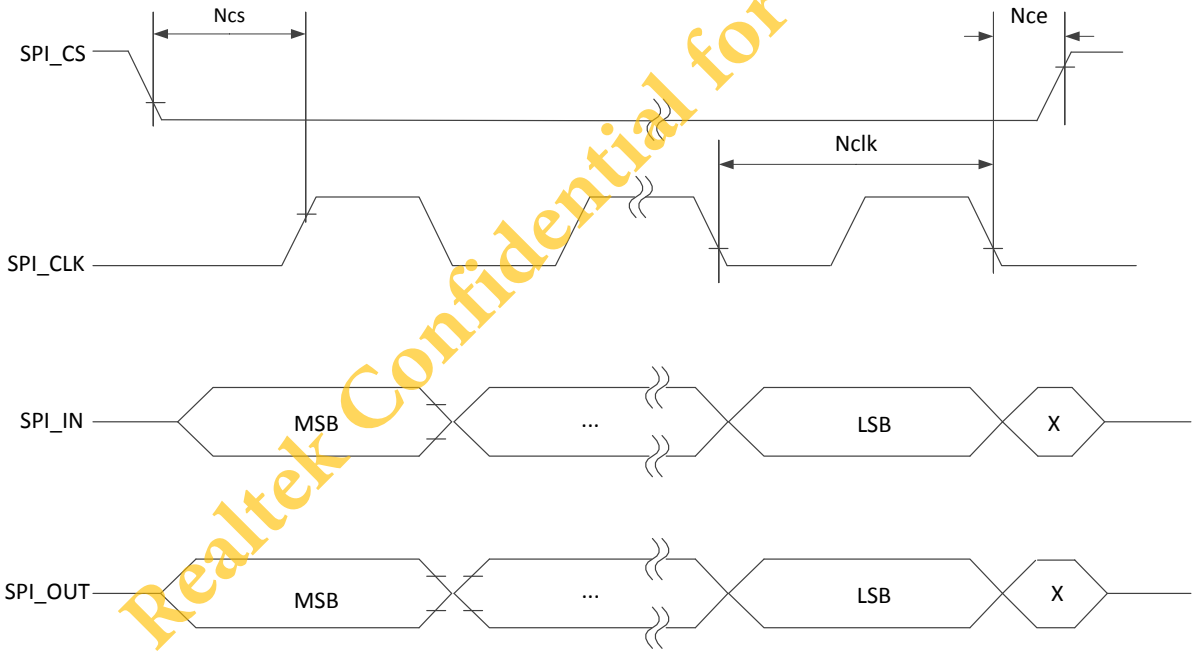


Figure 4. G-SPI Timing

Table 16. G-SPI Timing

Parameter	Min	Max	Unit
Nclk	-	25	MHz
Ncs	20	-	ns
Nce	20	-	ns

7.3. Power Management Handshake Interface Signal Level

■ SD_RESET Signal Level

The SD_RESET signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8821CS via the VDD_IO pin (Ball K7)

■ BT_DIS# Signal Level

The BT_DIS# signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8821CS via the VDD_IO_1 pin (Ball A7)

■ CHIP_EN Signal Level

The CHIP_EN signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8821CS via the VDD_IO_1 pin (Ball A7)

■ WL_DIS_N Signal Level

The WL_DIS_N signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8821CS via the VDD_IO pin (Ball K7)

■ VBAT_LDO_EN Signal Level

The VBAT_LDO_EN signal level ranges from 1.8V to 3.3V.

7.4. System Power Sequence

7.4.1. System Power On Sequence

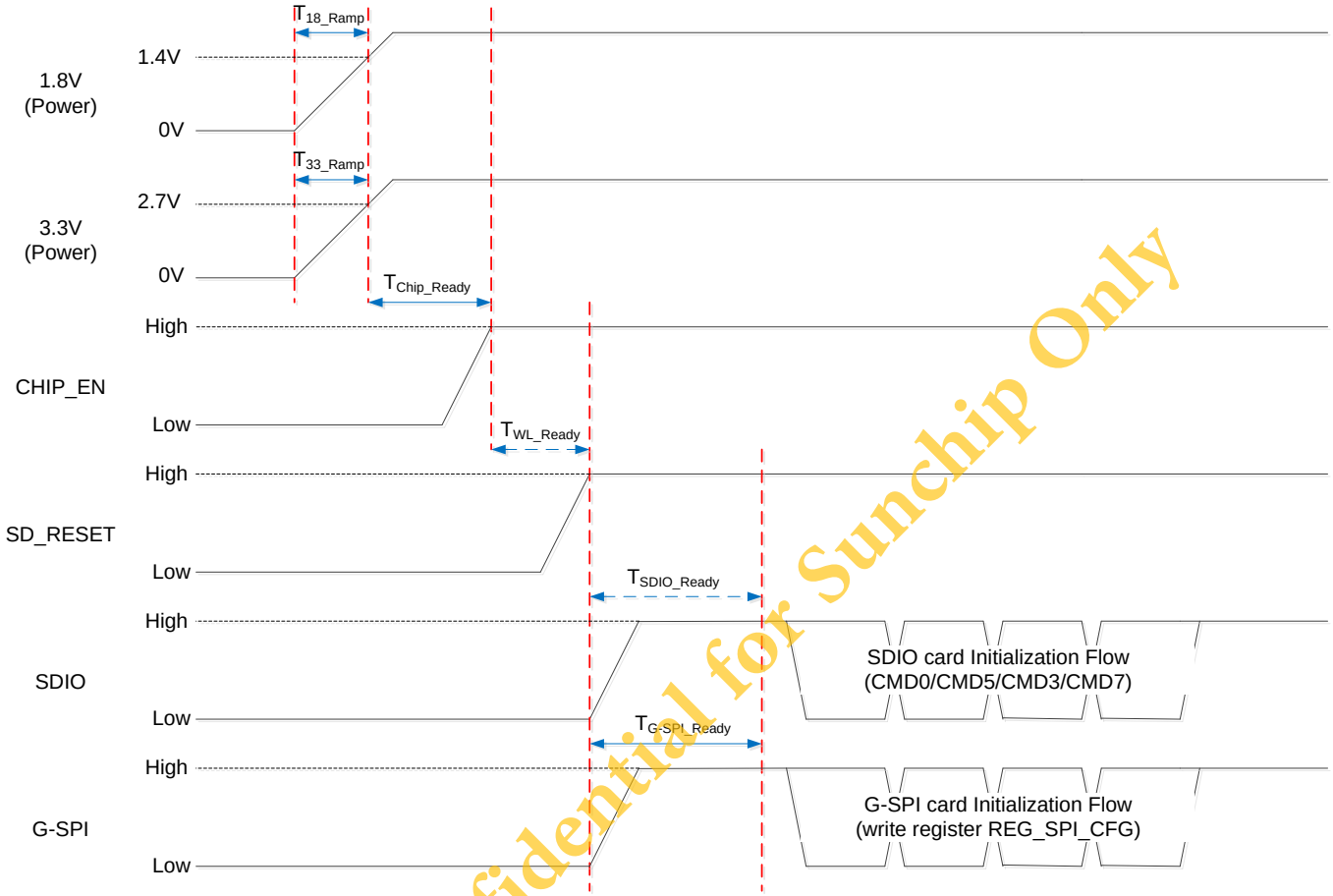


Figure 5. System Power-On Sequence

Table 17. System Power On Timing Parameters

	Min	Typical	Max	Unit	Description
T_{18_Ramp}	0.1	0.5	2.5	ms	The 1.8V main power ramp up duration.
T_{33_Ramp}	0.1	0.5	2.5	ms	The 3.3V main power ramp up duration.
T_{Chip_Ready}					CHIP_EN pull high timing
T_{WL_Ready}				ms	SD_RESET pull high timing
T_{SDIO_Ready}	1	2	10	ms	SDIO Not Ready Duration. In this state, the RTL8821CS may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.
$T_{G\text{-}SPI\_Ready}$	3	4	18	ms	The duration G-SPI device internal initialization. After

					$T_{G\text{-}SPI\_Ready}$, SPI host can then send command to write REG_SPI_CFG register. REG_SPI_CFG register is to control G-SPI endian and word length.

■ SDIO Interface Power On Sequence

After power-on, the SDIO interface is selected by the RTL8821CS automatically when a valid SDIO command is received. To attain better SDIO host compatibility, the following power-on sequence is recommended.

We recommend that the card detection procedures are divided into two phases: A 3.3V/1.8V power pre-charge phase and a formal power-up phase.

After main 3.3V ramp up and 1.8V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the SDIO block. eFUSE is then autoloaded to SDIO circuits during the T_{non_rdy} duration. After CMD5/5/3/7 procedures, card detection is executed.

■ G-SPI Interface Power On Sequence

The G-SPI interface is enabled automatically when a valid G-SPI command is first received. The recommended power on sequence is as follows:

After main 3.3V/1.8V ramp up, the power management unit will be enabled by power ready detection circuit, and enables G-SPI block. Efuse is then autoloaded to SPI circuits, and the internal power circuits are configured during $T_{G\text{-}SPI\_Ready}$ duration.

■ SD_RESET Power On Sequence

To attain SD_RESET capability, the following power sequence is recommended.

After main 3.3V/1.8V ramp up, the power management unit is enabled by the power ready detection circuit.

The power management unit enables the SD_RESET function. After power management unit being enabled, SD_RESET needs to keep high for ensuring WLAN and SDIO/G-SPI function being alive.

■ CHIP_EN Power On Sequence

To attain CHIP_EN capability, the following power sequence is recommended.

After main 3.3V/1.8V ramp up, the power management unit is enabled by the power ready detection circuit.

The power management unit enables the CHIP_EN function. After power management unit being enabled, CHIP_EN needs to keep high for ensuring RTL8821CS function being alive.

7.4.2. WLAN and SDIO/G-SPI Reset Sequence

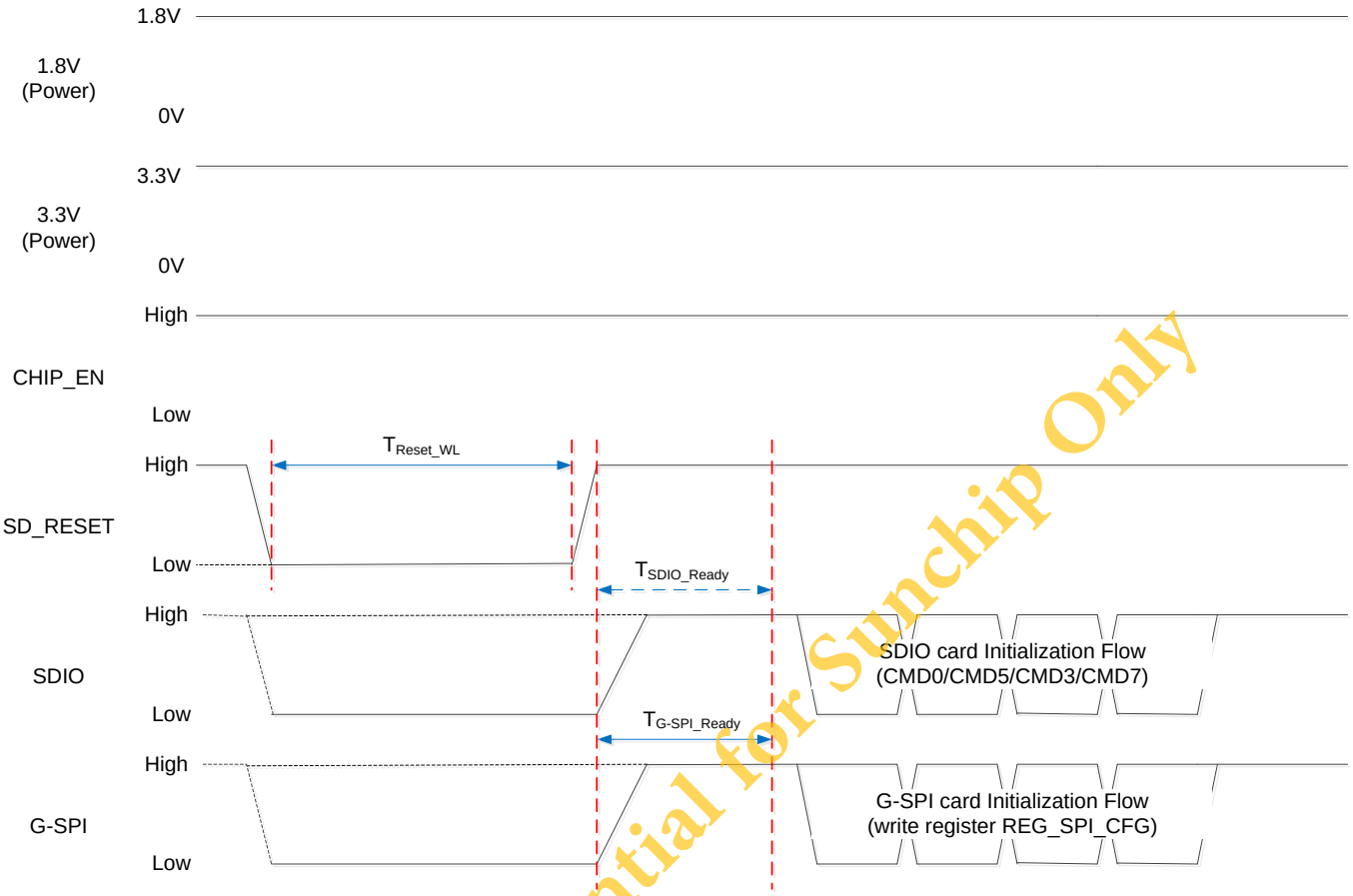


Figure 6. WLAN and SDIO/G-SPI Reset Sequence

Table 18. WLAN and SDIO/G-SPI Reset Timing Parameters

	Min	Typical	Max	Unit	Description
T_{Reset_WL}	10	10	X	ms	SD_RESET keep low duration
T_{SDIO_Ready}	1	2	10	ms	SDIO Not Ready Duration. In this state, the RTL8821CS may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.
$T_{G\text{-}SPI\_Ready}$	3	4	18	ms	The duration G-SPI device internal initialization. After $T_{G\text{-}SPI\_Ready}$, SPI host can then send command to write REG_SPI_CFG register. REG_SPI_CFG register is to control G-SPI endian and word length.

■ WLAN Reset Sequence

SD_RESET can externally reset the RTL8821CS WLAN function by pulled SD_RESET low and then pulled high. The keeping low duration must be more than T_{Reset_WL}.

When SD_RESET pulled low, SDIO/G-SPI interface will be disabled. After WLAN reset, SDIO/G-SPI card initialization is needed.

7.4.3. WLAN and SDIO/G-SPI Power Off Sequence

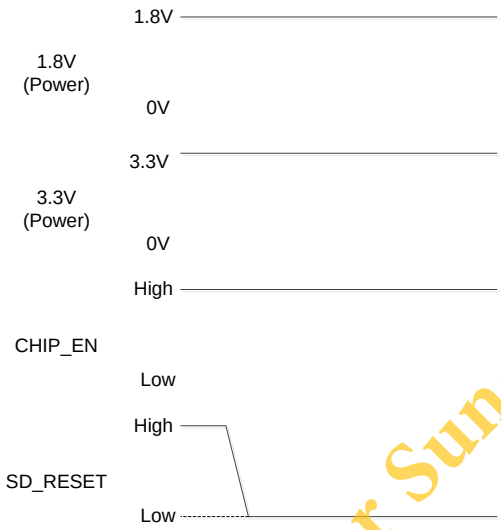


Figure 7. WLAN and SDIO/G-SPI Power Off Sequence

SD_RESET can externally shutdown the RTL8821CS WLAN function when SD_RESET is Pulled Low.

7.4.4. RTL8821CS Power Off Sequence

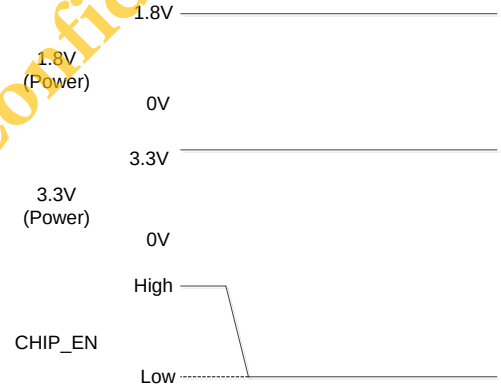


Figure 8. RTL8821CS Power Off Sequence

CHIP_EN can externally shutdown the RTL8821CS when CHIP_EN is Pulled Low.

7.4.5. WLAN Radio On/Off Sequence

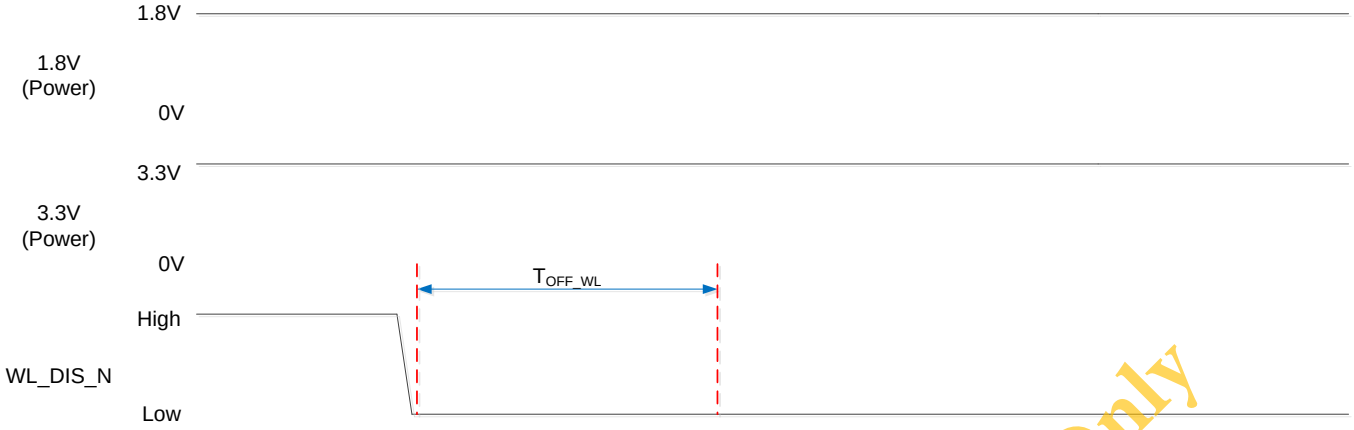


Figure 9. WLAN Radio Off Sequence

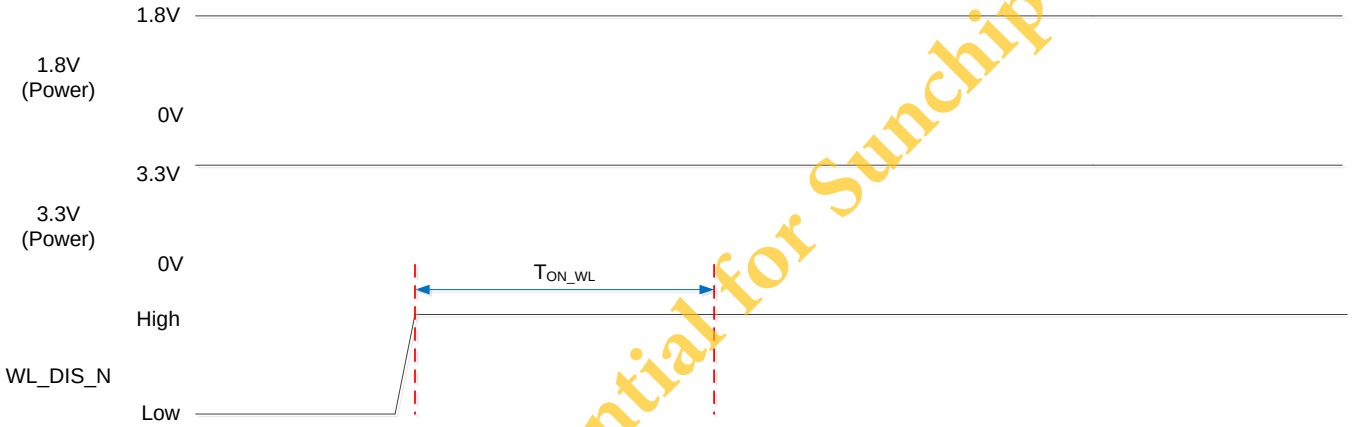


Figure 10. WLAN Radio On Sequence

WL_DIS_N can be defined as the WLAN Radio-off function with host interface remaining connected.
When WL_DIS_N is pulled low, WLAN Radio will be disabled. The keeping low duration must be more than T_{OFF_WL}.
When WL_DIS_N is pulled high, WLAN Radio will be enabled. The keeping high duration must be more than T_{ON_WL}.

Table 19. WLAN Radio On/Off Timing Parameters

	Min	Typical	Max	Unit	Description
T_{OFF_WL}	100	100	X	ms	WL_DIS_N keep low duration
T_{ON_WL}	100	100	X	ms	WL_DIS_N keep high duration

7.4.6. VBAT_LDO_EN Power Sequence

To attain VBAT_LDO_EN capability, the following power sequence is recommended.

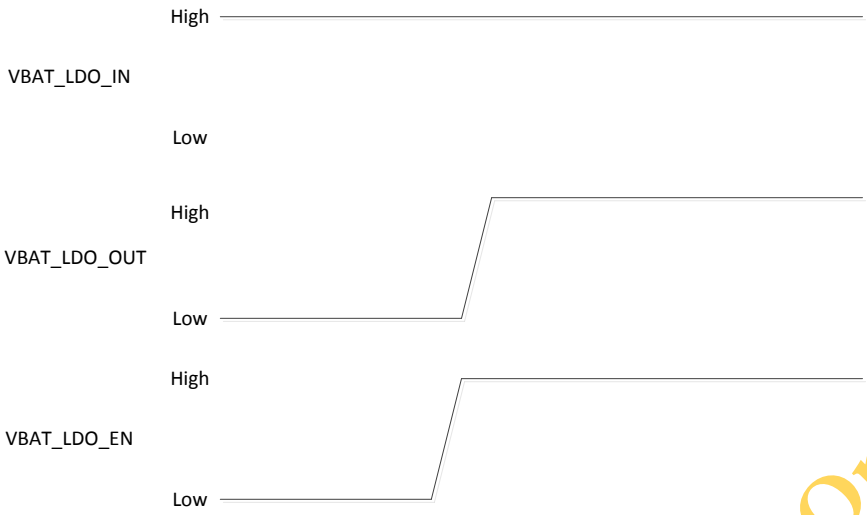


Figure 11. VBAT_LDO_EN Power On Sequence

Figure 12. VBAT_LDO_EN Power Off Sequence

After VBAT_LDO_EN ramp up, the battery LDO is enabled by the power ready detection circuit. After VBAT_LDO_EN drop down, the battery LDO is disabled by the power ready detection circuit. The power source supplied for this LDO (VBAT_LDO_IN) should keep working during system power off.

7.4.7. BT Power On/Off Sequence

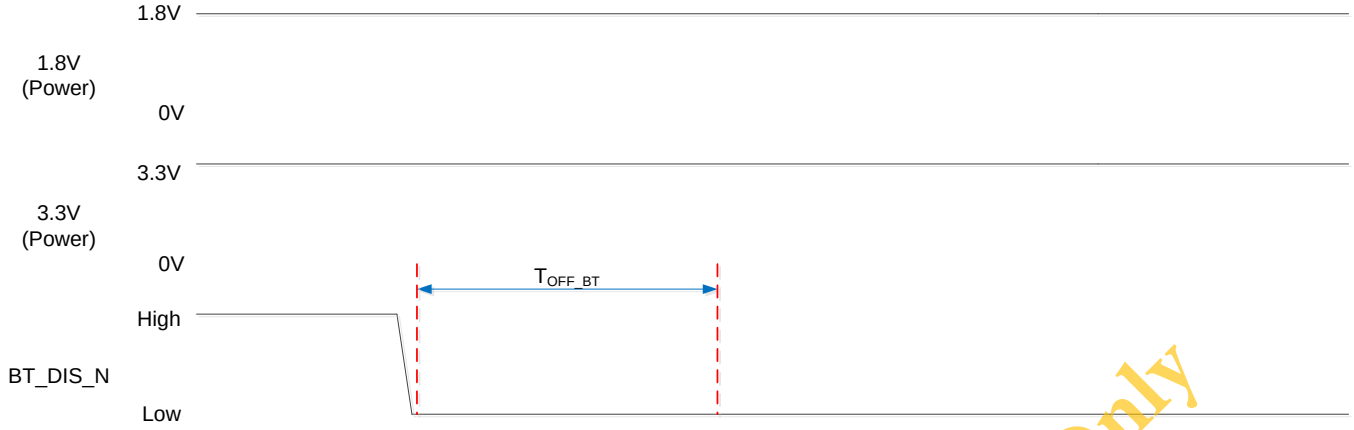


Figure 13. BT Power Off Sequence

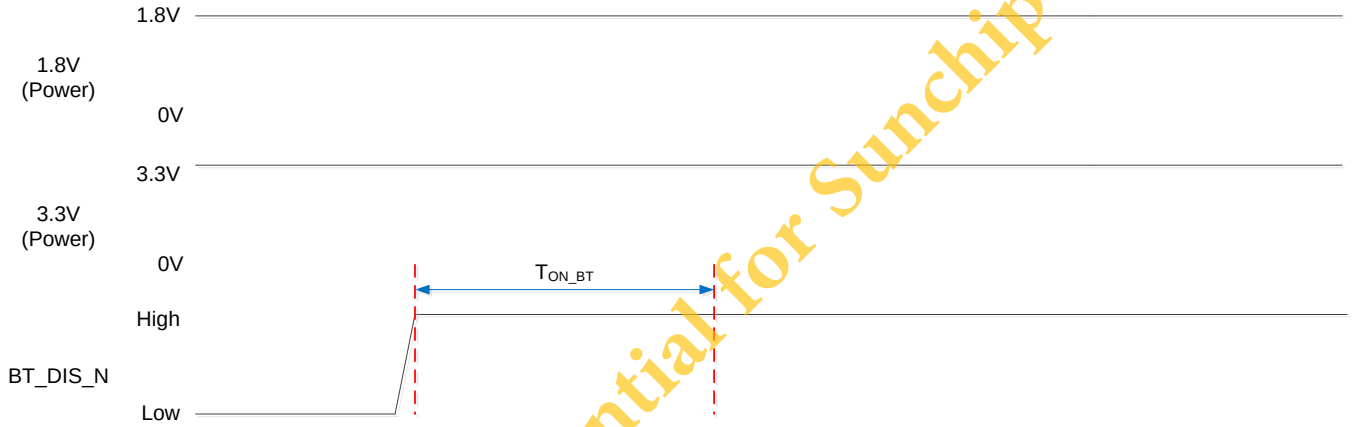


Figure 14. BT Power On Sequence

BT_DIS_N can be defined as the BT Power-off function with host interface remaining connected.
When BT_DIS_N is pulled low, BT will be disabled. The keeping low duration must be more than T_{OFF_BT}.
When BT_DIS_N is pulled high, BT will be enabled. The keeping high duration must be more than T_{ON_BT}.

Table 20. BT Radio On/Off Timing Parameters

	Min	Typical	Max	Unit	Description
T_{OFF_BT}	100	100	X	ms	BT_DIS_N keep low duration
T_{ON_BT}	100	100	X	ms	BT_DIS_N keep high duration

7.4.8. Power Reset Sequence

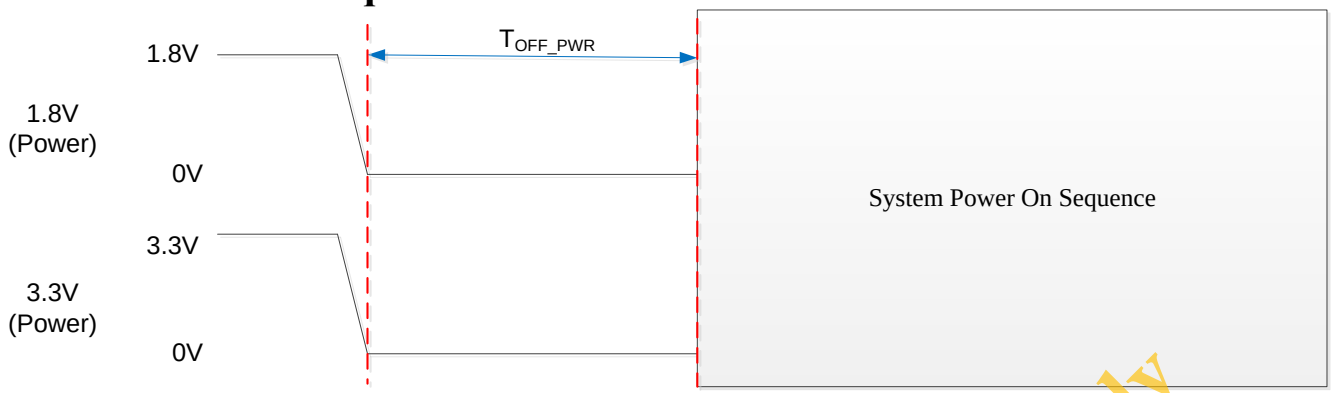


Figure 15. Power Reset Sequence

Main 3.3V/1.8V power should keep low at least T_{OFF_PWR} before calling system power on Sequence.

Table 21. Power Reset Timing Parameters

	Min	Typical	Max	Unit	Description
T_{OFF_PWR}	10	10	X	ms	3.3V/1.8V power keep low duration

7.5. UART Interface Characteristics

The RTL8821CS UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. The interface supports the Bluetooth UART HCI H4 and H5 specifications. The default baud rate is 115.2 kbaud. In order to support high and low speed baud rate, the RTL8821CS provides multiple UART clocks.

Table 22. UART Interface Power-On Timing Parameters

Desired Baud Rate	Error	Desired Baud Rate	Error
1200	0%	1382400	-0.22%
9600	0%	1444400	-0.20%
14400	0%	1500000	-0.31%
19200	0.01%	1843200	-0.22%
28800	0.01%	2000000	0%
38400	0.04%	2100000	0.25%
57600	0.01%	2500000	0%
76800	0.04%	2764800	-0.22%
115200	-0.08%	3000000	-0.31%
128000	0%	3250000	0.47%
153600	-0.08%	3692300	-0.38%
230400	-0.08%	3710000	0.29%
460800	-0.08%	3750000	0.39%
500000	0%	3800000	0.25%
921600	-0.22%	4000000	0%
1000000	0%		

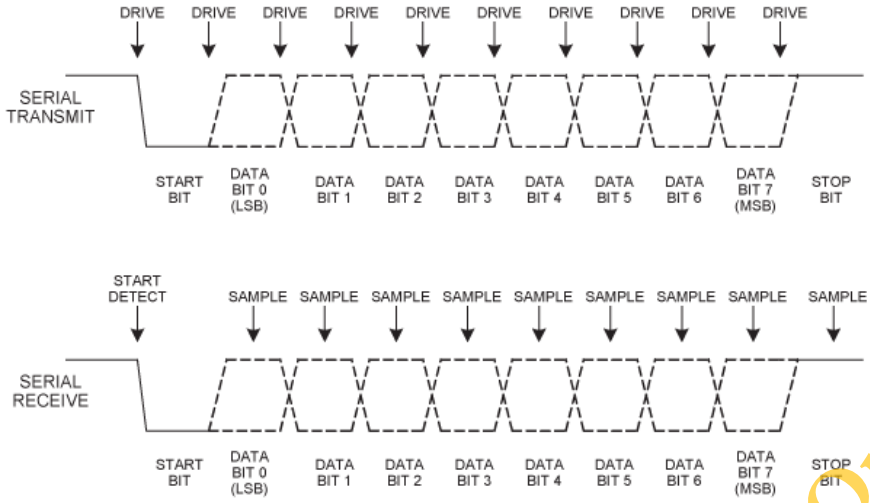


Figure 16. UART Interface Waveform

7.5.1. UART Interface Signal Levels

The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8821CS UART interface via the VIO_HOST pin.

7.5.2. UART Interface Power-On Sequence

The UART interface power-on sequence differs depending on whether or not host flow control is supported.

UART Hardware Flow Control Not Supported

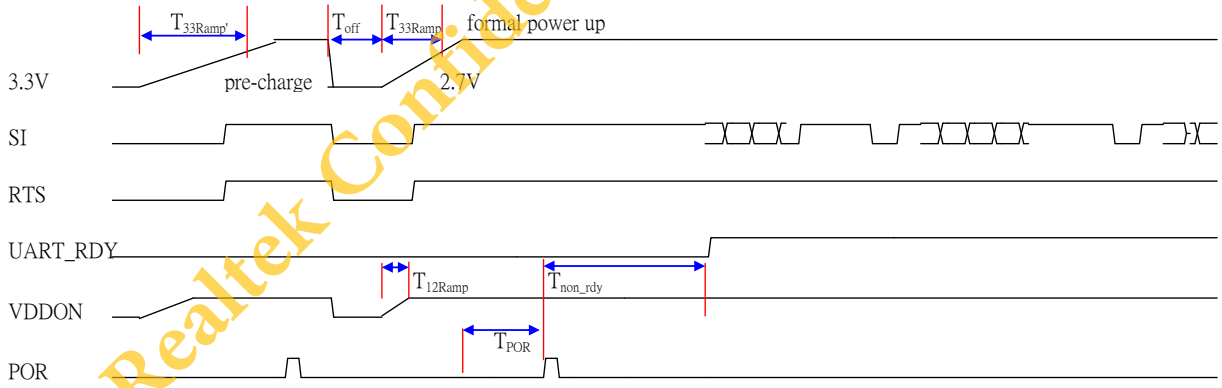


Figure 17. UART Power-On Sequence Without Hardware Flow Control

UART Hardware Flow Control Supported

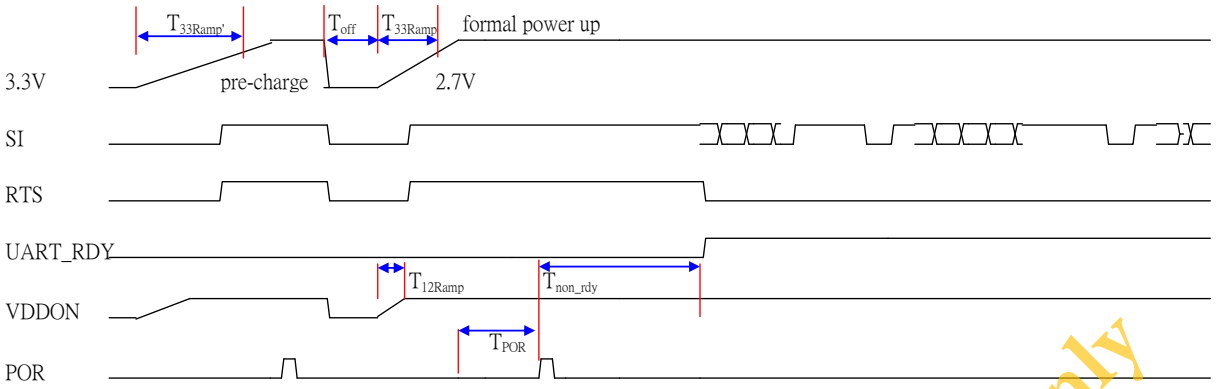


Figure 18. UART Power On Sequence With Hardware Flow Control

Table 23. UART Interface Power-On Sequence

Symbol	Description
T_{33ramp}	3.3V Power Pre-Charge Ramp Up Duration Before Formal Power Up. We recommend that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power on sequence. This procedure can eliminate host card detection issues when power ramp up duration is too long, or when a system warm reboot fails.
T_{off}	The duration 3.3V is cut off before formal power up.
T_{33ramp}	The 3.3V main power ramp up duration.
T_{12ramp}	The internal 1.2V ramp up duration.
T_{POR}	The duration from when the power-on reset releases and the power management unit executes power on tasks. A power on reset will detect both 3.3V and 1.2V power ramp up after a predetermined duration.
T_{non_rdy}	UART Not Ready Duration. In this state, the RTL8821CS will not respond to any commands.

We recommend that the card detection procedures are divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.

During the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V power is cut off and is turned on after the T_{off} period. The ramp up time is specified in the T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the Bluetooth block. The Bluetooth firmware then initializes all circuits, included the UART. In addition to wait the T_{non_rdy} time, if the host supports UART hardware flow control it can detect RTS signals and follow the formal UART flow control handshake.

Table 24. UART Interface Power On Timing Parameters

	Min	Typical	Max	Unit
T_{33ramp}	-	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{por}	2	2	8	ms

	Min	Typical	Max	Unit
$T_{non-rdy}$	1	2	10	ms

7.6. PCM Interface Characteristics

The RTL8821CS supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit A-law/μ-law, and 13/16-bit linear PCM formats
- Supports sign-extension and zero-padding for 8-bit and 13-bit samples
- Supports padding of Audio Gain to 13-bit samples
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports SCO/ESCO link

7.6.1. PCM Format

FrameSync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. A Long FrameSync indicates the start of ADC_Data at the rising edge of FrameSync (), and a Short FrameSync indicates the start of ADC_Data at the falling edge of FrameSync ().

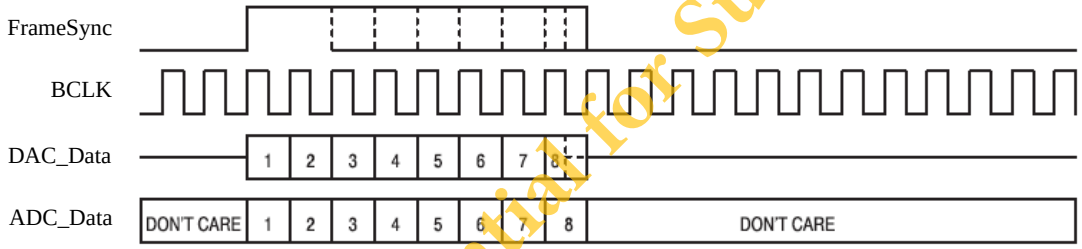


Figure 19. Long FrameSync

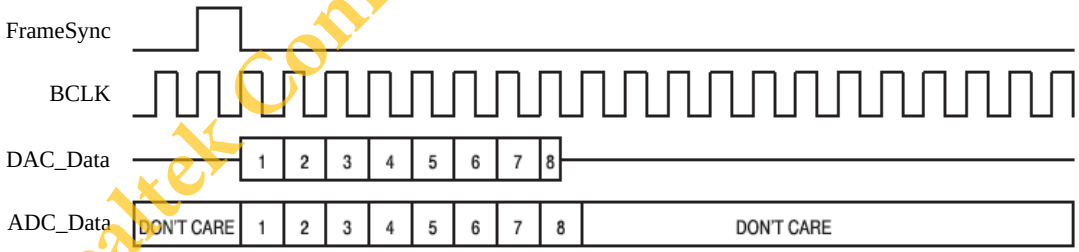


Figure 20. Short FrameSync

7.6.2. Sign Extension and Zero Padding for 8-Bit and 13-Bit Samples

For 16-bit linear PCM output, 3 or 8 unused bits may be sign extended/zero padded.

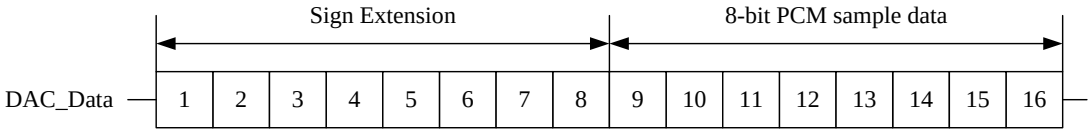


Figure 21. 16-Bit Output Data with 8-Bit PCM Sample Data and Sign Extension

Figure 22. 16-Bit Output Data with 8-Bit PCM Sample Data and Zero Padding

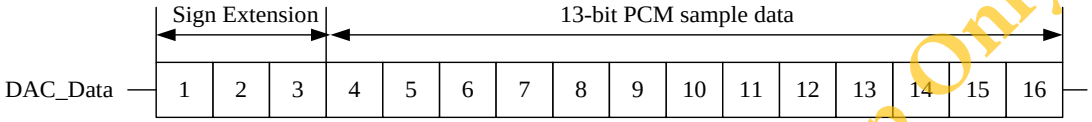


Figure 23. 16-Bit Output Data with 13-Bit PCM Sample Data and Sign Extension

For 16-bit linear PCM output, 3-bit programmable audio gain value can be padded to 13-bit sample data.

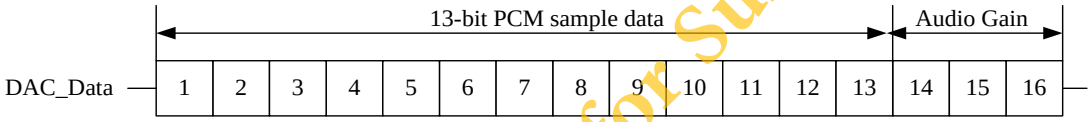


Figure 24. 16-Bit Output Data with 13-Bit PCM Sample Data and Audio Gain

7.6.3. PCM Interface Timing

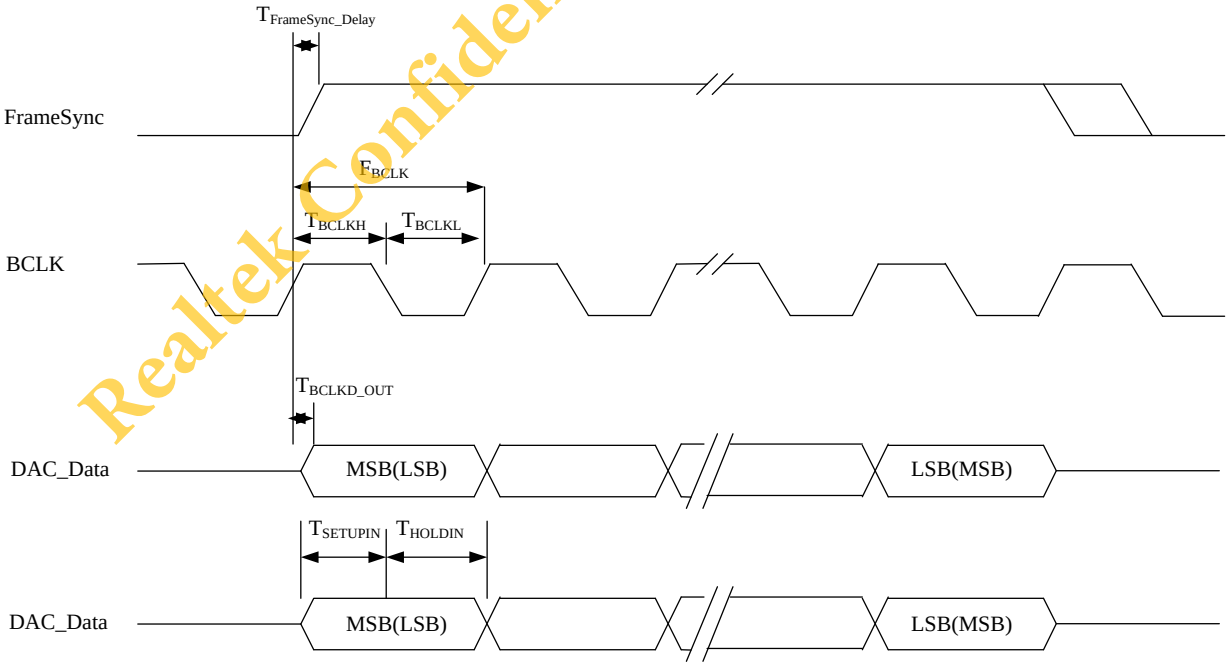


Figure 25. PCM Interface (Long FrameSync)

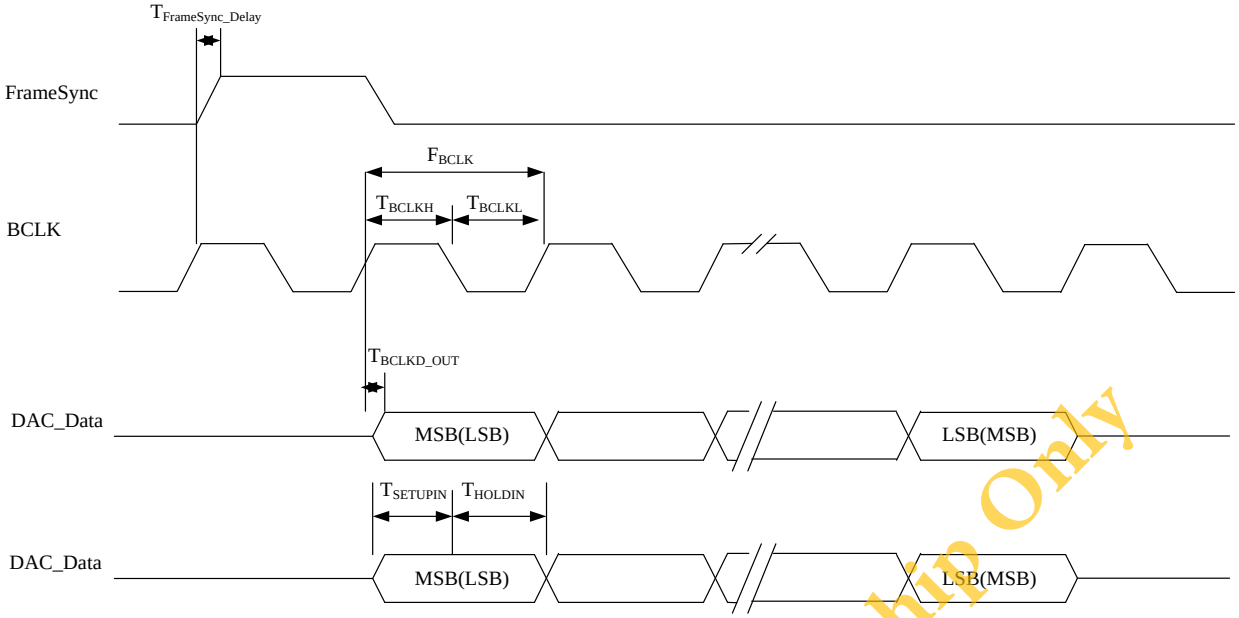


Figure 26. PCM Interface (Short FrameSync)

Table 25. PCM Interface Clock Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
F_{BCLK}	Frequency of BCLK (Master)	64	-	512	kHz
$F_{FrameSync}$	Frequency of Frame Sync (Master)	-	8	-	kHz
F_{BCLK}	Frequency of BCLK (Slave)	64	-	512	kHz
$F_{FrameSync}$	Frequency of Frame Sync (Slave)	-	8	-	kHz
D	Data Size	8	8	16	bits
N	Number of Slots Per Frame	1	1	1	Slots

Table 26. PCM Interface Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{BCLKH}	High Period of BCLK	980	-	-	ns
T_{BCLKL}	Low Period of BCLK	970	-	-	ns
$T_{FrameSync\_Delay}$	Delay Time from BCLK High to Frame Sync High	-	-	75	ns
T_{BCLKD_OUT}	Delay Time from BCLK High to Valid DAC_Data	-	-	125	ns
$T_{SETUPIN}$	Set-up Time for ADC_Data Valid to BCLK Low	10	-	-	ns
T_{HOLDIN}	Hold Time for BCLK Low to ADC_Data Invalid	125	-	-	ns

7.6.4. PCM Interface Signal Levels

The PCM signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8821CS PCM interface via the VIO_HOST pin .

7.7. I2S Interface Characteristics

RTL8821CS supports I^{2}S digital audio interface used for transmitting digital audio/voice data to/from Audio Codec. The Interface shares the same pins with PCM interface, but mutually exclusive in its stage.There are features supported by RTL8821CS:

- Support both Master and Slave mode
- Programmable MSB/LSB bit 1st SCK(Left-Justified) or 2nd SCK(I2S-Compatible) latch time
- Programmable SCK rising/falling edge trigger for latching data bits
  Support 8-bit a-Law/u-Law and 16-bit linear formats
- Support sign-extension and zero-padding for 8-bit and 13-bit samples
- Support padding of Audio Gain to 13-bit samples
- Programmable MSB/LSB first
- I2S Master clock output: 128/256kHz
- Support one SCO/ESCO link only

7.7.1. Master and Slave mode

RTL8821CS can be configured as either master or slave mode. As master mode, the RTL8821CS generate SCK and WS, thus controls the data transfer over DAC_Data and ADC_Data. RTL8821CS supports audio sampling rate 8kHz(FrameSync), depends on I^{2}S data format. The clock output(SCK) will be up to 256kHz.

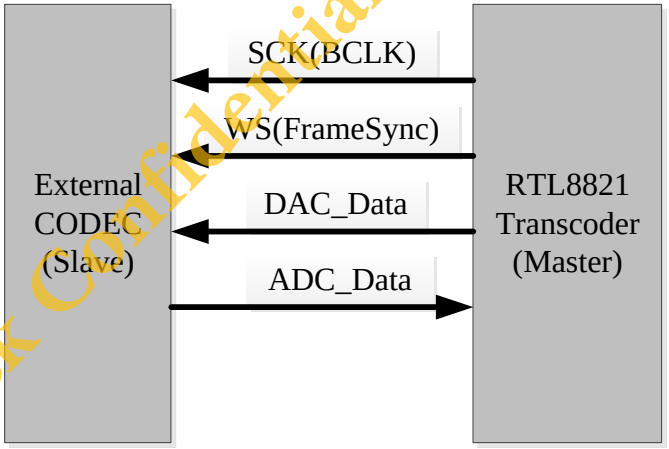


Figure 27. Master mode

In slave mode, RTL8821CS responds with DAC_Data and ADC_Data to SCK and WS it receives from Audio Codec. RTL8821CS can receive audio sampling rate 8kHz(WS), depends on I^{2}S data format. The clock input(BCLK) accepted will be up to 256kHz.

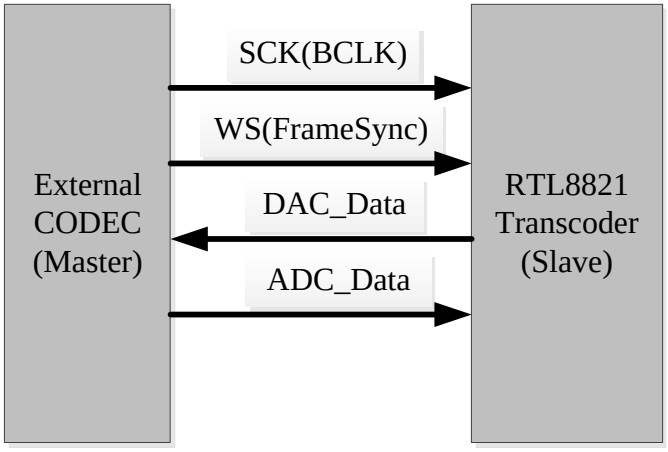


Figure 28. Slave Mode

7.7.2. Programmable MSB/LSB bit latch time(1st or 2nd SCK)

For compatibility with most Audio Codec, RTL8821CS has options to set when the first bit will be latched or driven after WS channel changed.

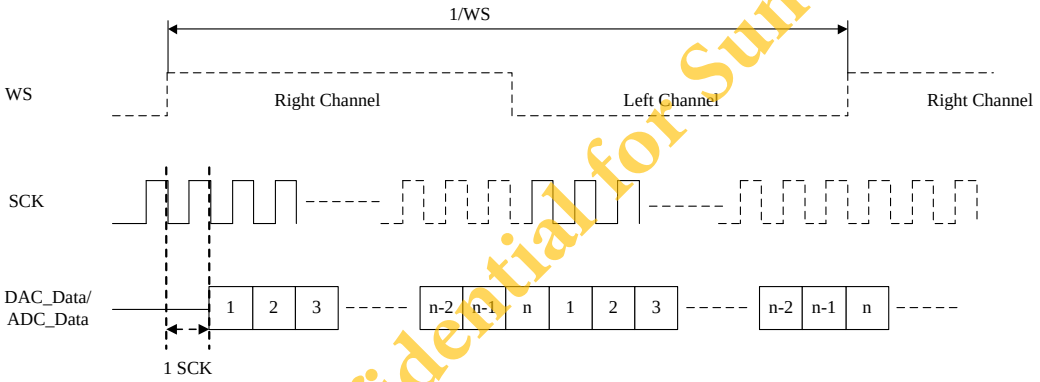


Figure 29. Latched/Driven at 2nd SCK(I2S-Compatible)

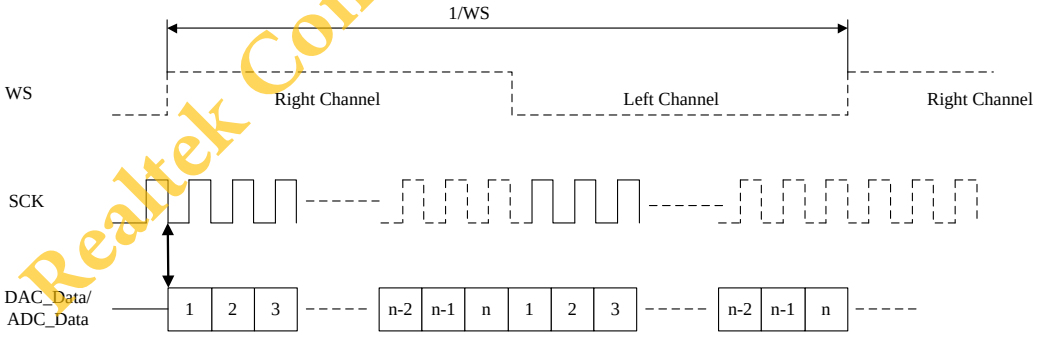


Figure 30. Latched/Driven at 1st SCK(Left-Justified)

7.7.3. Programmable SCK rising/falling edge trigger for latching data bits

For compatibility with most Audio Codec, RTL8821CS has options to set data latch/data drive phase.

7.7.4. 8-bit a-Law/u-Law and 13/16-bit linear PCM formats

For mostly compatible with most Audio Codec, RTL8821CS support 8-bit a-Law/u-Law and 8-bit, 16-bit linear formats.

7.7.5. Sign-extension and zero-padding for 8-bit and 13-bit samples

For 16-bit linear output format, 3 or 8 unused bits maybe filled with sign extension, padding with zeros.

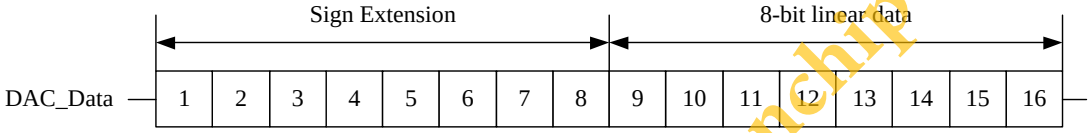


Figure 31. 16-bit output data with 8-bit linear data and Sign extension

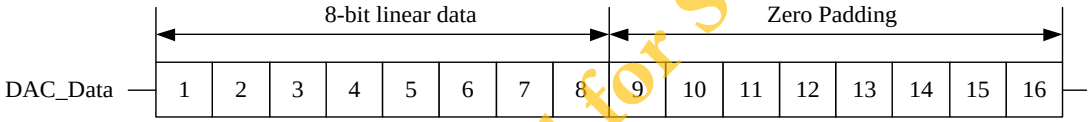


Figure 32. 16-bit output data with 8-bit linear data and Zero padding

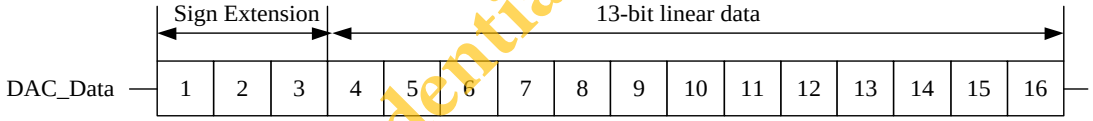


Figure 33. 16-bit output data with 13-bit linear data and Sign extension

7.7.6. Padding of Audio Gain to 13-bit samples

For 16-bit linear output format, 3-bit programmable audio gain value can be padded to 13-bit sample data

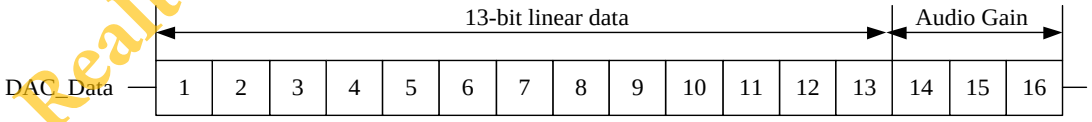


Figure 34. 16-bit output data with 13-bit linear data and Audio gain

7.7.7. Programmable MSB/LSB first

For mostly compatible with most Audio Codec, RTL8821CS support I²S data output/input with MSB/LSB as first bit.

7.7.8. PCM Master clock output: 64, 128, 256 or 512kHz

RTL8821CS supports audio sampling rate 8kHz(WS), depends on the I²S data format, in Master mode the clock output(SCK) will be 128, 256kHz.

7.7.9. one SCO/ESCO link only

One SCO/ESCO link is supported in RTL8821CS to connect over PCM interface

7.8. I²S Timming Information

Table 27 I²S Interface Clock Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
F_{SCK}	Frequency of SCK(Master)	128	-	256	kHz
F_{WS}	Frequency of WS(Master)		8		kHz
F_{SCK}	Frequency of SCK(Slave)	128	-	256	kHz
F_{WS}	Frequency of WS(Slave)		8		kHz
D	Data size	8	8	16	bits
N	Number of slots per frame	1	1	1	

Table 28 I²S Interface timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCKH}	High period of SCK	1960	-	-	ns
T_{SCKL}	Low period of SCK	1950	-	-	ns
T_{WS_Delay}	Delay time from SCK falling to WS high/low	-	-	75	ns
T_{SCKD_OUT}	Delay time from SCK falling to valid DAC_Data	-	-	125	ns

$T_{SETUPIN}$	Set-up time for ADC_Data valid to SCK rising	10	-	-	ns
T_{HOLDIN}	Hold time for SCK rising to ADC_Data invalid	125	-	-	ns

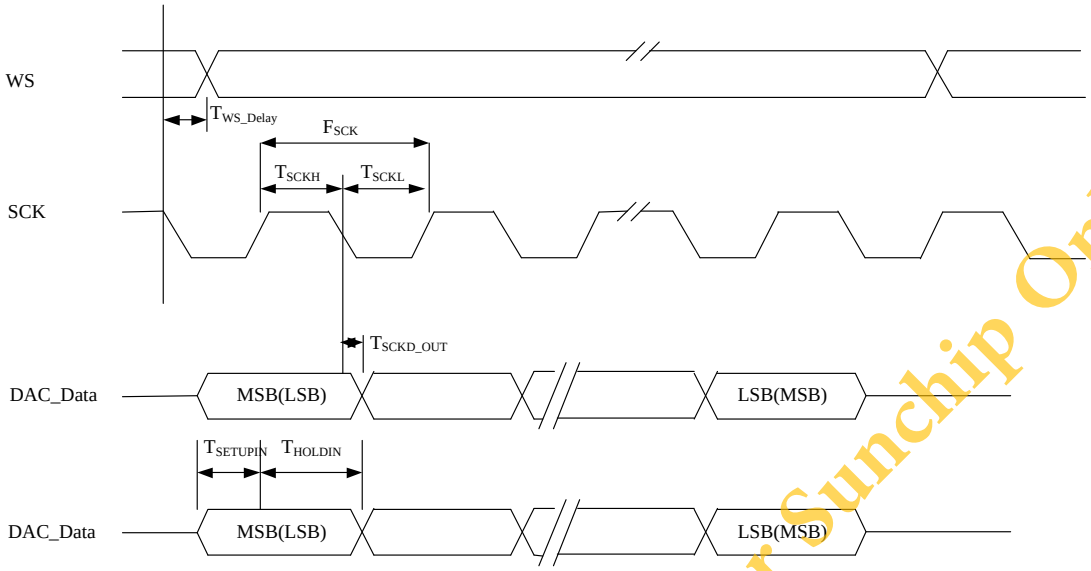
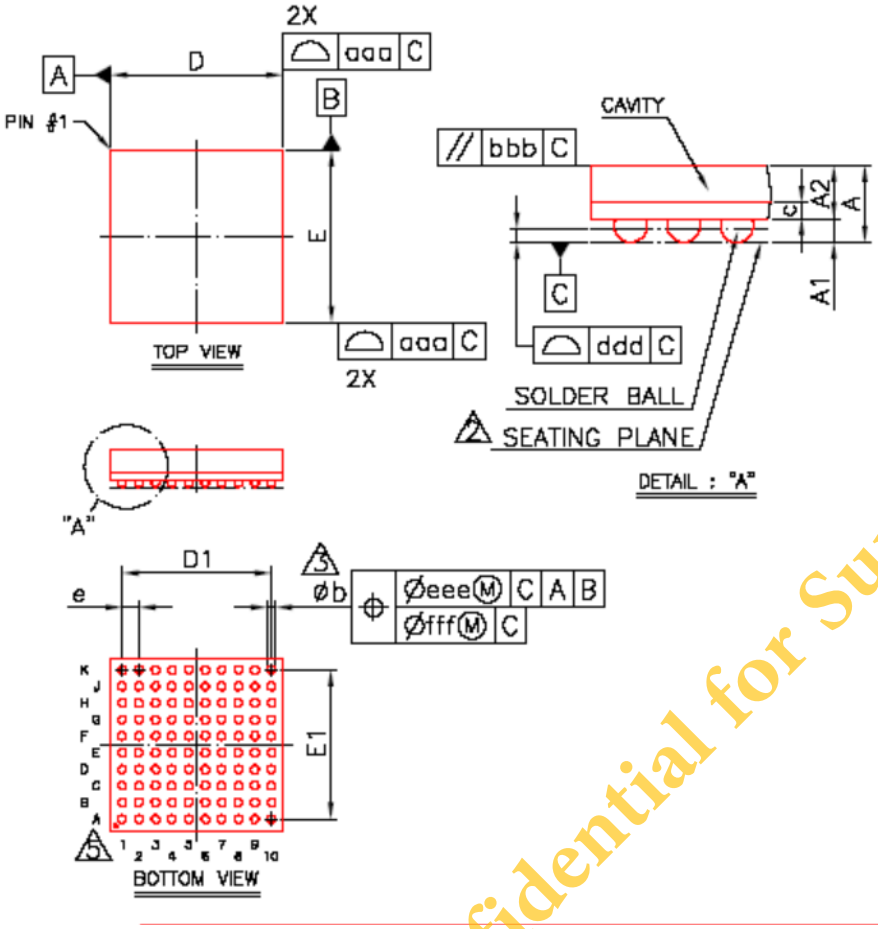


Figure 35. I²S Interface timing

8. Mechanical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.07	1.14	1.21	0.042	0.045	0.048
A1	0.13	0.18	0.23	0.005	0.007	0.009
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.008	0.010	0.012
D	5.10	5.20	5.30	0.201	0.205	0.209
E	5.10	5.20	5.30	0.201	0.205	0.209
D1	---	4.50	---	---	0.177	---
E1	---	4.50	---	---	0.177	---
e	---	0.50	---	---	0.020	---
b	0.20	0.25	0.30	0.008	0.010	0.012
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.08			0.003	
eee		0.15			0.006	
fff		0.05			0.002	
MD/ME		10/10				

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb,ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. REFERANCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5

TITLE : 100LD TFBGA (5.2X5.2 mm) PACKAGE OUTLINE			
APPR.			
PE.		DWG NO.	TEMP
PD.		REV NO.	B
QM.		DATE	10/06/'15
CHK.		DWG.	Victor Liu

9. Ordering Information

Table 29. Ordering Information

Part Number	Package	Status
RTL8821CS	TFBGA100 , 'Green' Package	To Be Available

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