RTL9201R-CG

USB 3.2 GEN1 to SATA GEN3 BRIDGE

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2022/03/31	First release.

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1. General Description

The Realtek RTL9201R-CG (hereafter referred to as the RTL9201R) USB (Universal Serial Bus) to SSD (Solid-State Disk) bridge combines a USB device with a SATA bus controller, and embedded memory.

The RTL9201R supports USB 3.2 GEN1 (Super Speed). It is compatible with USB High Speed and Full Speed. It can operate normally using auxiliary power. The Mass Storage transaction supports both Bulk Only Transfer (BOT) and USB Attached SCSI Protocol (UASP). For USB, it provides up to 5Gbps bandwidth.

The RTL9201R supports SATA Gen3. For SATA, it provides up to 6Gbps bandwidth. It has full backward compatibility for SATA Gen2/Gen1. To reduce power consumption, the RTL9201R supports link power management (Partial Mode/Slumber Mode/DEVSLP Mode).

The RTL9201R is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

The RTL9201R supports security of SHA256 (Secure Hash Algorithm 256 bits), CRC32 (Cyclic Redundancy Check 32 bits) and LBA (Logical Block Address) protection for security requirements.

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2. Features

General

- USB to SATA SSD bridge
- Integrated with Type-C connector
- Supports External Serial Peripheral Interface (SPI) Flash
- Supports Synchronous Serial Interface (SSI)
- Supports Customized LEDs (includes blinking frequency and duty cycle)
- Supports Pulse Width Modulation (PWM)
- Supports UART interface
- Supports GPIOs/OTP
- Supports I2C interface
- Built-in LDO (5V to 3.3V)
- Supports 25MHz crystal clock
- 48-pin QFN Green package

SATA

- Link speed up to 6GT/s
- Compatible with SATA Gen1/Gen2/Gen3
- Supports SATA link power management. Partial mode/Slumber mode/DEVSLP mode

AHCI

- Supports standard command set
- Dynamic power state translation
- Strong Error handling and recovery
- Supports full command set of SATA SCSI Translation (e.g., UNMAP, Security protocol in/out …)
- Supports Security Send and Receive
- Supports SMART/Health information

USB

- Link bandwidth up to 5Gbps
- Compatible with Full Speed/High Speed/Super Speed
- Supports Bulk Only Transfer (BOT) and USB Attached SCSI (UAS) protocol
- Supports USB link power management
- Supports SCSI command translation to SATA AHCI

Type-C

- Supports Cable Orientation Detection

Security

- Supports SHA256
- Supports CRC32
- Supports LBA Protection

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3. System Applications

- USB3.2 SS/HS with SATA SSD mass storage on motherboard, notebook, Embedded or mobile phone system supporting BOT and UASP mass storage specifications

4. Block Diagram

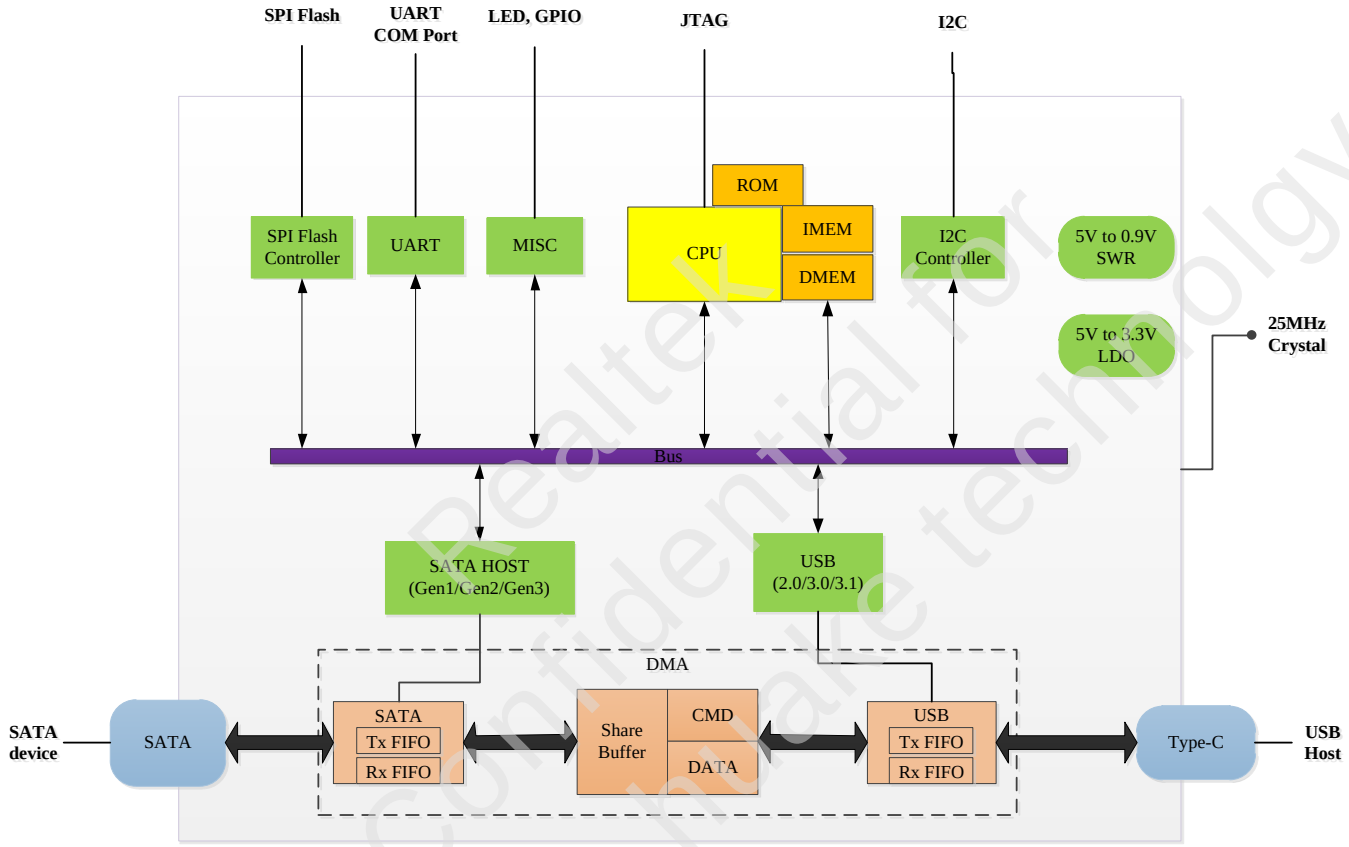

Figure 1. Block Diagram

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5. Pin Assignments

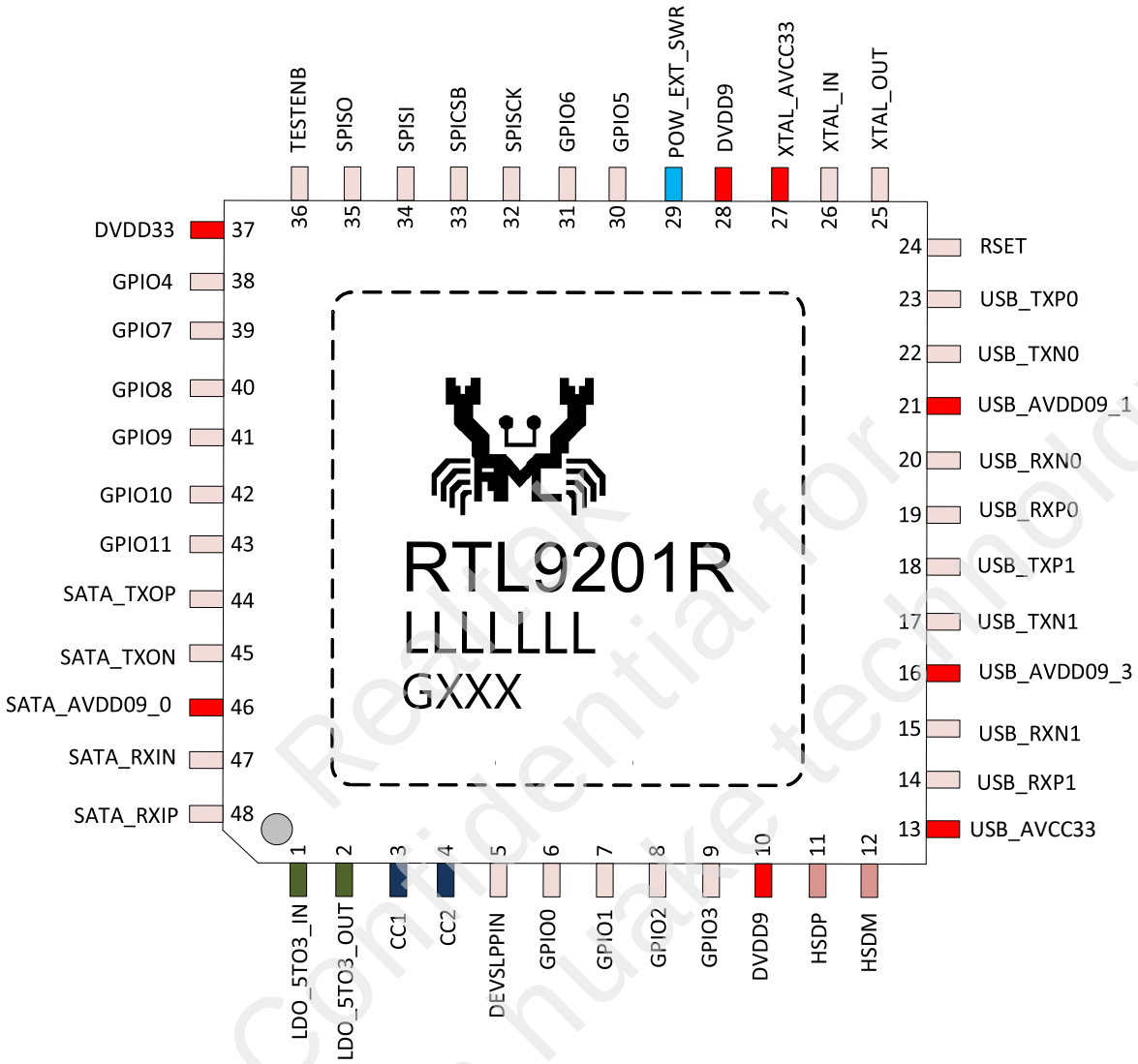

Figure 2. Pin Assignments

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6. Pin Descriptions

The signal type codes below are used in the following tables:

I: Input
O: Output
G: GND
T/S: Tri-State Bi-Directional Input/Output Pin
S/T/S: Sustained Tri-State
O/D: Open Drain
P: Power

6.1. USB Interface Pins

Table 1. USB Interface Pins

Symbol	Type	Pin No	Description
USB_TXP0	O	23	USB SS Transmit Differential Pair 0.
USB_TXN0	O	22	
USB_TXP1	O	18	USB SS Transmit Differential Pair 1.
USB_TXN1	O	17	
USB_RXP0	I	19	USB SS Receive Differential Pair 0.
USB_RXN0	I	20	
USB_RXP1	I	14	USB SS Receive Differential Pair 1.
USB_RXN1	I	15	
HSDP	IO	11	USB 2.0/USB 0.9 Differential Signal Pair.
HSDM	IO	12	

6.1. SATA Interface

Table 2. SATA Interface

Symbol	Type	Pin No	Description
SATA_RXIP	I	48	SATA Receive Differential Pair 0.
SATA _RXIN	I	47	
SATA _TXOP	O	44	SATA Transmit Differential Pair 0.
SATA _TXON	O	45	
DEV_SLP	O	5	SATA device sleep mode pin.

6.2. Clock

Table 3. Clock

Symbol	Type	Pin No	Description
XTAL_IN	I	26	Input of 25MHz Clock Reference.
XTAL_OUT	IO	25	Input of External Clock Source. Output of 25MHz Clock Reference.

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6.3. Regulator and Reference

Table 4. Regulator and Reference

Symbol	Type	Pin No	Description
LDO_5TO3_OUT	P/O	2	Linear Regulator (LDO) 3.3V Output. *Note: The embedded LDO is designed for RTL9201R internal use only. Do not provide this power source to other devices.*
LDO_5TO3_IN	P/I	1	Linear Regulator (LDO) 5V Input.
POW_EXT_SWR	O	29	Switching Regulator (Enable SWR Pin) 3.3V Output.
RSET	I	24	External reference resistor with 12Kohm +/-1%.

6.4. SPI (Serial Peripheral Interface) Flash Pins

Table 5. SPI Flash Pins

Symbol	Type	Pin No	Description
SPICS	O	33	SPI Flash Chip Select.
SPICK	O	32	SPI Flash Serial Data Clock.
SPISI	IO	34	Serial Data Input (for 1x flash).
SPISO	IO	35	Serial Data Output (for 1x flash).

6.5. SSI (Synchronous Serial Interface) Pins

Symbol	Type	Pin No	Description
SPICS	O	40	Chip Select.
SPICK	O	39	Serial Data Clock.
SPISI	IO	42	Serial Data Input. *Note: This is a share-pin with LED1/ GPIO10*
SPISO	IO	41	Serial Data Output. *Note: This is a share-pin with LED0/ GPIO9*

6.6. Type-C Interface

Table 6. Type-C Interface

Symbol	Type	Pin No	Description
CC1	IO	3	Type-C configuration channel and Data I/O.
CC2	IO	4	Type-C configuration channel and Data I/O.

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6.7. UART Interface

Table 7. UART Interface

Symbol	Type	Pin No	Description
UART_RXD	I	8	UART Interface Data In. *Note: This is a share-pin with GPIO2*
UART_TXD	O	9	UART Interface Data Out. *Note: This is a share-pin with GPIO3*

6.8. JTAG Interface

Table 8. JTAG Interface

Symbol	Type	Pin No	Description
SJTDO	O	40	Test Data Out.
SJTMS	I	41	Test Mode Select. *Note: This is a share-pin with LED0/ GPIO9*
SJTDI	I	42	Test Data In. *Note: This is a share-pin with LED1/ GPIO10*
SJTCLK	I	43	Test Clock.

6.9. LEDs

Table 9. LEDs

Symbol	Type	Pin No	Description
LED	O	42	LED Pin. *Note: This is a share-pin with GPIO10/ SJTDI*

Note: Refer to the latest schematic circuit for correct configuration.

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6.10. PWM (Pulse Width Modulation) Pins

Symbol	Type	Pin No	Description
PWM0	O	6	Test Data Out. *Note: This is a share-pin with GPIO0*
PWM1	O	7	Test Data Out. *Note: This is a share-pin with GPIO1*
PWM2	O	8	Test Data Out. *Note: This is a share-pin with GPIO2*
PWM3	O	9	Test Data Out. *Note: This is a share-pin with GPIO3*
PWM4	O	38	Test Data Out. *Note: This is a share-pin with GPIO4*
PWM5	O	39	Test Data Out. *Note: This is a share-pin with GPIO7*
PWM6	O	40	Test Data Out. *Note: This is a share-pin with GPIO8*
PWM7	O	41	Test Data Out. *Note: This is a share-pin with GPIO9*
PWM8	O	42	Test Data Out. *Note: This is a share-pin with GPIO10*

6.11. Power and Ground

Table 10. Power and Ground

Symbol	Type	Pin No	Description
SATA_AVDD09	P	46	SATA Digital 0.9V Power Supply.
USB_AVCC33	P	13	USB Analog 3.3V Power Supply.
USB_AVDD09	P	16, 21	USB Analog 0.9V Power Supply.
VDD33	P	37	Digital 3.3V Power Supply.
DVDD09	P	10, 28	Digital 0.9V Power Supply.
GND	G	49	Ground (Exposed Pad).

Note: Refer to the latest schematic circuit for correct configuration.

6.12. GPIO Pins

Table 11. GPIO Pins

Symbol	Type	Pin No	Description
GPIO0	IO	6	General Purpose Input/Output Pin (3.3V Input/Output).
GPIO1	IO	7	General Purpose Input/Output Pin (3.3V Input/Output).
GPIO4	IO	38	General Purpose Input/Output Pin.
GPIO5	IO	30	General Purpose Input/Output Pin.
GPIO6	IO	31	General Purpose Input/Output Pin.
GPIO7	IO	39	General Purpose Input/Output Pin.

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6.13. Shared-Pin Default Function

Table 12. Shared-Pin Default Function

Share-Pin No	Type	Default Function	Description
8	I	GPIO2	General Purpose Input/Output Pin.
9	O	GPIO3	General Purpose Input/Output Pin.
40	IO	GPIO8	General Purpose Input/Output Pin.
41	IO	GPIO9	General Purpose Input/Output Pin.
42	IO	GPIO10	General Purpose Input/Output Pin.
43	IO	GPIO11	General Purpose Input/Output Pin.

6.14. Other Pins

Table 13. Other Pins

Symbol	Type	Pin No	Description
TESTEN	I	36	Enable TEST Mode. 1: Enable. Enable JTAG debug function 0: Disable

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7. Functional Description

7.1. USB Bus Interface

The SIE (Serial Interface Engine) employs a robust hardwired USB protocol implementation so that the entire USB interface operation can be done without firmware intervention.

The USB Super speed plus (USB3.2 Gen1) extends the performance range by doubling the SuperSpeed USB clock rate to 5-6fu,Gbps and enhancing data encoding efficiency.

For bulk transaction (Bulk-in, Bulk-out and SuperSpeed(Plus) bulk streaming protocol), appropriate responses and handshake signals are generated by the SIE. The SIE analog transceiver is fully compatible with driver and receiver characteristics defined in USB Specification Rev. 3.2.

7.1.1. USB Interface

The RTL9201R supports two types of Mass storage interface: UASP and BOT. Both UASP & BOT run standard driver without installing additional vendor specific drivers. For UASP interface, the RTL9201R supports four Bulk endpoints, two for mass storage data transfer, and two for information transfer. For BOT interface, the RTL9201R supports two Bulk endpoints, and both data and information transfer share the same endpoints.

7.1.2. Endpoint 0

All USB devices support a common access mechanism for accessing information through this control pipe. Associated with the control pipe at endpoint 0 is the information required to fully describe the USB device.

7.1.3. Endpoint Bulk-In

The RTL9201R transfers mass storage data to the host via this endpoint. The maximum Bulk-In packet size is 1024 bytes. If the mass storage data is larger than 1024 bytes, the RTL9201R splits the data into multiple USB packets.

7.1.4. Endpoint Bulk-Out

The host sends mass storage data to the RTL9201R via this endpoint. The maximum Bulk-Out packet size is 1024 bytes. If the data length is larger than 1024 bytes, the host will send the data in multiple USB packets.

7.1.5. Streaming Bulk-In/Out Protocol

The RTL9201R supports multiple stream modes for the UASP protocol. The host and device manage the endpoint buffers by a ‘StreamID’. The RTL9201R also supports out-of-order data transfers required for mass storage device command queuing.

The host can burst multiple streaming packets to the device, and when the device has data available for a specific stream, it issues ERDY with a specific ‘StreamID’ to the host. Then, the host selects endpoint buffers with the ‘StreamID’, and starts the data transfer.

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7.2. SATA

The RTL9201R integrates a Serial ATA AHCI host controller that provides an interface between a host and device. This interface is a peer-to-peer connection, and the data is transmitted or received from one Serial ATA compatible device. It is designed to meet the Serial ATA 3.0 standard, and runs at a 6GHz signaling rate.

The RTL9201R supports Max link speed 6.0 Gb/s and is compatible with 1.5 Gb/s and 3.0 Gb/s.

7.2.1. Features

- The host controller is compatible with the SATA III extension specification
  - Supports Serial-ATA 3.1 Spec
  - Supports SATA III (1.5G/3G/6G) Spec
  - Supports SATA AHCI 1.31 Spec (first-party DMA)
  - Supports PIO transfer
  - Supports NCQ (Native Command Queuing)
  - Supports Power management including automatic partial-to-slumber transition
- PHY Layer (analog) function module is compatible with 1.0a Specification
  - Supports Out-of-Band signal generator and detector
  - Supports speed transition between 1.5Gbps and 3Gbps and 6Gbps
  - Supports Low Power Mode (Partial, Slumber, Device Sleep)
- Device status detection and auto speed negotiation
- Supports Low Power Mode

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7.3. SCSI Protocol

7.3.1. SCSI Command List

Table 14. SCSI Command List

SCSI Command	Op Code	Data Type
FORMAT UNIT	0x04	Data Out
INQUIRY	0x12	Data In
LOG SENSE	0x4D	Data In
MODE SELECT(6)	0x15	Data Out
MODE SELECT(10)	0x55	Data Out
MODE SENSE(6)	0x1A	Data In
MODE SENSE(10)	0x5A	Data In
Read(6)	0x08	Data In
Read(10)	0x28	Data In
Read(12)	0xA8	Data In
Read(16)	0x88	Data In
READ CAPACITY(10)	0x25	Data In
READ CAPACITY(16)	0x9E	Data In
REQUEST SENSE	0x03	Data In
START STOP UNIT	0x1B	N/A
SYNCHRONIZE CACHE(10)	0x35	N/A
SYNCHRONIZE CACHE(16)	0x91	N/A
TEST UNIT READY	0x0	N/A
UNMAP	0x42	Data Out
WRITE(6)	0x0A	Data Out
WRITE(10)	0x2A	Data Out
WRITE(12)	0xAA	Data Out
WRITE(16)	0x8A	Data Out
WRITE BUFFER	-	Data Out

7.3.2. Logical Block Addressing (LBA) Protection

The RTL9201R is capable of protecting up to two sets of LBA range. The LBA should not exceed the length of the 64-bit long address (maximum to 0xFFFF FFFF). A SCSI command will not be able to process successfully if its LBA range overlaps any protected LBAs.

7.3.3. Hidden Area

The hidden area is a specific area that cannot be accessed by SCSI operations. Any command with an LBA overlapped to the hidden area will automatically shift a software-defined length of offset, and the shifted LBA will be treated as the original LBA in the SCSI Command. This allows a range of LBA to become “invisible” to the host, but “visible” to the device.

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7.4. AHCI

The RTL9201R is compatible with AHCI Revision 1.3.1, which allows a SATA host to communicate with a non-volatile memory subsystem. The RTL9201R is also compatible with SCSI/ATA Translation Reference, which allows a SCSI over ATA command translation.

7.5. SPI (Serial Peripheral Interface) Flash

The RTL9201R supports the attachment of 32MB (maximum) external Serial Peripheral Interface (SPI) Flash. The SPI flash provides up to 32MB bytes of serial reprogrammable flash memory.

The SPI Flash is enabled by the RTL9201R through the Chip Select pin, and accessed via a 4-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), Chip Select (CS), and Serial Clock (SCK). The SPI flash utilizes an 8-bit instruction register. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low transition.

Compared to a parallel bus interface, the Serial Peripheral Interface provides simpler wiring and much less interaction (crosstalk) among the conductors in the cable. This minimizes the number of conductors, pins, and the IC package size, reducing the cost of making, assembling, and testing the electronics.

Note 1: SPI Flash size (firmware size) is based on features and customizable functions. For the exact flash size, contact Realtek FAE or your Realtek Agent.

Note 2: Realtek SPI Controller frequency default supports 62.5 MHz clock. If the slave SPI flash frequency is lower than 62.5MHz, contact Realtek FAE or your Realtek Agent. Realtek will decrease the corresponding clock to slave SPI flash.

Table 15. SPI Flash Interface

SPI Flash	Description
SPISO	Serial Data Output.
SPISI	Serial Data Input.
SPICLK	SPI Flash Serial Data Clock.
SPICS	SPI Flash Chip Select.

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7.6. SSI (Synchronous Serial Interface)

The SSI is enabled by the RTL9201R through the Chip Select pin, and accessed via a 4-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), Chip Select (CS), and Serial Clock (SCK). The SSI utilizes an 8-bit instruction register. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low transition.

Compared to a parallel bus interface, the SSI provides simpler wiring and much less interaction (crosstalk) among the conductors in the cable. This minimizes the number of conductors, pins, and the IC package size, reducing the cost of making, assembling, and testing the electronics.

Table 16. SSI Interface

SSI	Description
SPISO	Serial Data Output.
SPISI	Serial Data Input.
SPICLK	Serial Data Clock.
SPICS	Chip Select.

7.7. Customizable LED Configuration

The RTL9201R supports customizable LED operation modes via control registers 64h. An individual control register for each LED, and a global feature control register are provided to support customized LED signals, as described in Table 17 & Table 18.

Table 17. Customized LEDs

LEDSEL	Interface	LINK						Active	High/Low Active
-	USB or SATA	All_Speed	USB20 SATA Gen1	USB30 SATA Gen2	USB30 SATA Gen3	RVD	Power on	-	-
LED 0	Bit 1	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 14	Bit 15

Table 18. LED Feature Control Description

Feature Control	Description
High/Low Active	1: LED Low Active 0: LED High Active
Interface USB or SATA	1: SATA 0: USB
Active	LED blinks if the interface transmits or receives data.
LINK	LED blinks depending on the configured speed.

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The RTL9201R LED register default values are shown in Table 19.

Table 19. LED Register Default Value

LEDSEL	Interface	LINK						Active	High/Low Active
-	USB or SATA	All_ Speed	USB20 SATA Gen1	USB30 SATA Gen2	USB30 SATA Gen3	RVD	Power On	-	-
LED 0	0	0	0	0	0	0	1	1	0

When implementing customized LEDs:

Configure MISC register address offset 0x64 to support your own LED signals. For example, if the value is configured as C010h (1100000000010000b), the LED actions are bright when the USB link is on 30, with no blinking.

7.7.1. LED Blinking Frequency Control

The RTL9201R supports LED blinking frequency control via MISC address 68h. This controls LED blinking frequency and duty cycle. If the b_freq[1:0] is set as 0x3, and the b_duty_cycle[1:0] set as 0x3, the LED blinking frequency will be 80ms and the duty cycle will be 75%.

Table 20. LED Blinking Frequency Control (MISC Register Offset 0x68)

Bit	RW	Description
b_freq[1:0]	RW	LED Blinking Frequency. 0: 320ms 1: 240ms 2: 160ms (Default) 3: 80ms
b_duty_cycle[1:0]	RW	LED Blinking Duty Cycle. 0: 12.5% 1: 25% 2: 50% (Default) 3: 75%

7.8. PWM (Pulse Width Modulation)

The RTL9201R supports PWM control via MISC address 274h to 294h for PWM0~PWM8 . This controls PWM clk and duty cycle.

Table 21. PWM Control (MISC Register Offset 0x274 to 0x294)

Bit	RW	Description
b_pwm_csd[3:0]	RW	PWM clock source divisor. 0000: 2^(0+1) 0001: 2^(1+1) 1111: 2^(15+1)
b_pwm_cd[7:0]	RW	PWM clock duty. Real PWM clock duty = clock duty number +1.

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7.9. Power Management

The RTL9201R is compatible with ACPI to support an Operating System-directed Power Management (OSPM) environment.

7.10. USB Link Power Management

The RTL9201R supports full USB Link Power Management (LPM). It provides an efficient way for the host to manage power consumption.

- For USB 2.0, the RTL9201R supports L0/ L1 /Suspend (L2) mode
- For USB 3.2, the RTL9201R supports U1/U2/ Suspend (U3) mode
- UTMI clock & PCLK clock are disabled while in Suspend mode

If the USB host and hub support LPM, the host and hub can put the device into a low power state. The RTL9201R will deactivate some of its circuits to reduce power consumption in the low power state, and go back to full power when in active state.

7.11. SATA Power Management

The RTL9201R supports full SATA power management. Partial, slumber, and device sleep can all be realized by SW.

7.12. Security

The RTL9201R supports Security of SHA256 (Secure Hash Algorithm 256 bits) and CRC32 (Cyclic Redundancy Check 32 bits) that are irreversible algorithms and can be programmed fast. This increases the efficiency of processing.

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8. Characteristics

8.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 22. Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
AVDD33, VDD33	Supply Voltage 3.3V.	-0.3	3.6	V
AVDD09, DVDD09	Supply Voltage 0.9V.	-0.3	1.2	V
3.3V DCinput 3.3V DCoutput	Input Voltage. Output Voltage.	-0.3	3.6	V
0.9V DCinput 0.9V DCoutput	Input Voltage. Output Voltage.	-0.3	1.2	V
V_{CC1_MAX}	Max voltage for CC1 (VCONN switch off).	-	5.5	V
V_{CC2_MAX}	Max voltage for CC2 (VCONN switch off).	-	5.5	V
V_{VCONN_MAX}	Max operation voltage for VCONN.	-	5.5	V
V_{DROP_CC1}	Voltage drop at current = 300mA.	-	250	mV
V_{DROP_CC2}	Voltage drop at current = 300mA.	-	250	mV
VMON_FRS	Input FRS signal after external resistor.	-0.3	3.6	V
	Comparator detect voltage level.	1.66	1.96	V
VMON_PRS	Input PRS signal after external resistor.	-0.3	3.6	V
	Comparator detect voltage level.	0	1.5	V
I_{CC1}	-	-	400	mA
I_{CC2}	-	-	400	mA
VMON_FRS_APAD	Input signal.	-	2	V
VMON_PRS_APAD	Input signal.	-	2	V
IMON_APAD	Input signal.	-	2	V
N/A	Storage Temperature.	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

8.2. Recommended Operating Conditions

Table 23. Recommended Operating Conditions

Description	Pins	Min	Typ.	Max	Unit
Supply Voltage VDD.	SATA_AVDD33, VDD33, USB_AVDD33	3.14	3.3	3.46	V
	SATA_AVDD09, DVDD09, USB_AVDD09	0.855	0.9	0.955	V
Ambient Operating Temperature. T_A	-	0	-	70	°C
Maximum Junction Temperature.	-	-	-	125	°C

Note 1: Refer to the most updated schematic circuit for correct configuration.
Note 2: Internal voltage 3.3V of RTL9201R cannot be adjusted.

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8.3. Electrostatic Discharge Performance

Table 24. Electrostatic Discharge Performance

Test Item	Results
HBM ESD	All Pins: 3.5KV
MM ESD	All Pins: 100V
CDM ESD	All Pins: 1.5KV
Latch Up	I/O Pins: 200mA Power Pins: 1.5 x VDD

8.4. Crystal Requirements

Table 25. Crystal Requirements

Symbol	Description/Condition	Min	Typ.	Max	Unit
F_{ref}	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F_{ref} Stability	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=0°C~70°C.	-30	-	+30	ppm
F_{ref} Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=25°C.	-50	-	+50	ppm
F_{ref} System	Parallel Resonant Crystal Frequency Tolerance, On Board.	-80	-	+80	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	30	Ω
Jitter	Broadband Peak-to-Peak Jitter[2]	-	-	200	ps
DL	Drive Level.	-	-	0.3	mW

Note 1: Jitter measurement result can be confirmed after the Crystal component specification and board layout are reviewed by Realtek.

Note 2: C_{load} should be verified by the Crystal vendor.

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8.5. Oscillator Requirements

Table 26. Oscillator Requirements

Parameter	Condition	Min	Typ.	Max	Unit
Frequency	-	-	25	-	MHz
Frequency Stability	T_a = 0°C~70°C	-30	-	+30	ppm
Frequency Tolerance	T_a = 25°C	-50	-	+50	ppm
Duty Cycle	-	40	-	60	%
Broadband Peak-to-Peak Jitter[2]	-	-	-	200	ps
V_{ih}	-	1.4	-	-	V
V_{il}	-	-	-	0.4	V
Rise Time	-	-	-	10	ns
Fall Time	-	-	-	10	ns
Operation Temp Range	-	0	-	70	°C

Note 1: The CLK source can come from other places in the system, but it must accord with the parameters above.
Note 2: Broadband RMS=9ps; 25KHz to 25MHz RMS=3ps. If the items listed below are tested and confirmed by Realtek, this can be modified to Broadband RMS=9ps; 25KHz to25MHz RMS=3.5ps.
Test Items: 1. SNR, 2. Power Ripple, 3. RSET Ripple, 4. IEEE Gigabit Waveform, 5. Bit Error Rate Test.

8.6. Environmental Characteristics

Table 27. Environmental Characteristics

Parameter	Range	Units
Storage Temperature	-55 ~ +125	°C
Ambient Operating Temperature	0 ~ 70	°C
Moisture Sensitivity Level (MSL)	Level 3	N/A

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8.7. DC Characteristics

Table 28. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
LDO_5TO3_IN, SWR_5TO09_IN	5V Supply Mean Voltage	-	4.5	5	5.5	V
SATA_AVDD33 VDD33 USB_AVDD33	3.3V Supply Mean Voltage	-	3.14	3.3	3.46	V
SATA_AVDD09 DVDD09 USB_AVDD09	0.9V Supply Mean Voltage	-	0.855	0.9	0.945	V
V_{oh}	Minimum High Level Output Voltage	I_{oh} = -4mA	0.9*VDD33	-	VDD33	V
V_{ol}	Maximum Low Level Output Voltage	I_{ol} = 4mA	0	-	0.1*VDD33	V
V_{ih}	Minimum High Level Input Voltage for 3.3V Pinout	-	2	-	-	V
V_{il}	Maximum Low Level Input Voltage	-	-	-	0.8	V
I_{in}	Input Current	Vin = VDD33 or GND	0	-	0.5	µA

Note 1: Refer to the latest schematic circuit for correct configuration.
Note 2: All Supply Mean Voltage power noise <±5% of Mean Voltage.
*Note 3: The total operating current Isys5=Icc33+((Icc11*0.9)/ SWR_efficiency / 5), where SWR_efficiency=0.75 for SWR-mode.*
Note4: Internal voltage 3.3Vof the RTL9201R cannot be adjusted.

8.8. Reflow Profile Recommendations

Table 29. Reflow Profile Recommendations

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Minimum Preheat Temperature (T_{smin})	100°C	150°C
Maximum Preheat Temperature (T_{smax})	150°C	200°C
Preheat Time (t_S) from T_{smin} to T_{smax}	60~120 seconds	60~120 seconds
Ramp-Up Rate (T_L to T_p)	3°C/second max	3°C/second max
Liquidus Temperature (T_L)	183°C	217°C
Time (t_L) Maintained above T_L	60~150 seconds	60~150 seconds
Peak Package Body Temperature (T_p)	235°C	260°C
Time (t_p)^2 within 5°C of Peak T_P	20 seconds	20 seconds
Ramp-Down Rate (T_p to T_L)	6°C/second max	6°C/second max
Time 25°C to Peak Temperature (T_p)	6 minutes max	8 minutes max

Note 1: All temperatures refer to the topside of the package, measured on the package's body surface.
Note 2: Tolerance for Tp is defined as a supplier's minimum and a user's maximum.
Note 3: Reference document: IPC/JEDEC J-STD-020D.1.

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8.9. AC Characteristics

8.9.1. SPI Flash

8.9.1.1 SPI Flash Commands

Table 30. SPI Flash Commands

Command	Operation Code	Action
WREN	06h	Write Enable
WRDI	04h	Write Disable
RDID	9Fh	Read Manufacturer and Product ID
RDSR	05h	Read Status Register
WRSR	01h	Write Status Register
Read	03h	Read
Page Program	02h	Page Program
Sector Erase (4K)	20h	Erase The Selected Sector
Block Erase (64K)	D8h	Erase The Selected Block
Chip Erase	60h or C7h	Erase Whole Chip

8.9.1.2 SPI Flash Command Sequence

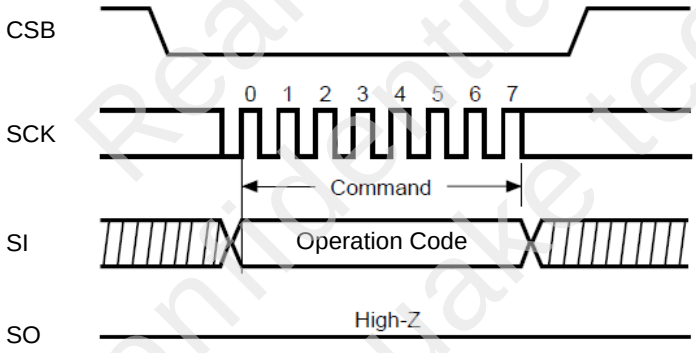

Figure 3. WREN/WRDI Command Sequence

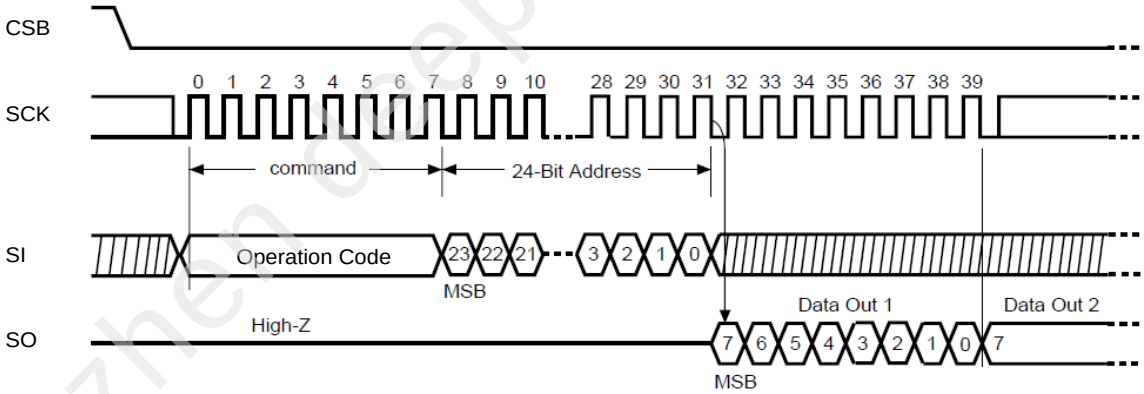

Figure 4. Read Command Sequence

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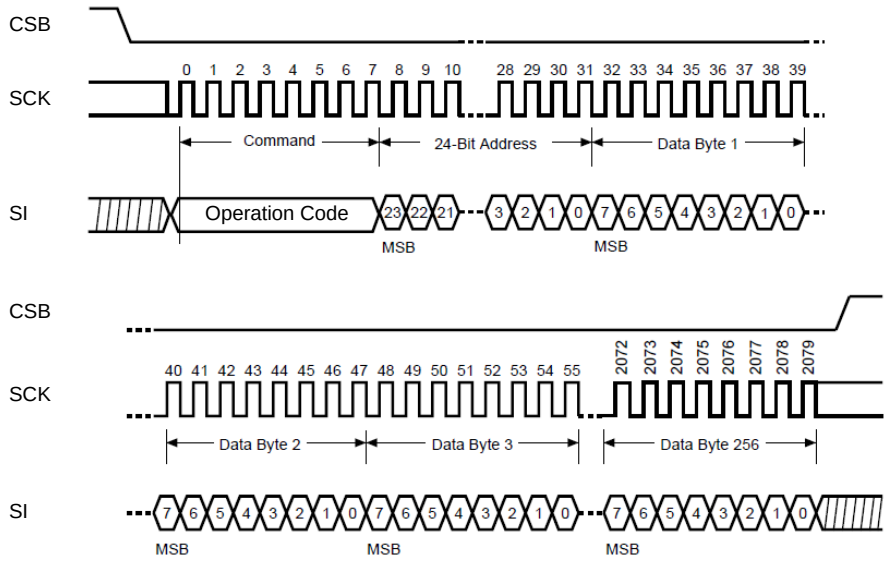

Figure 5. Page Program Command Sequence

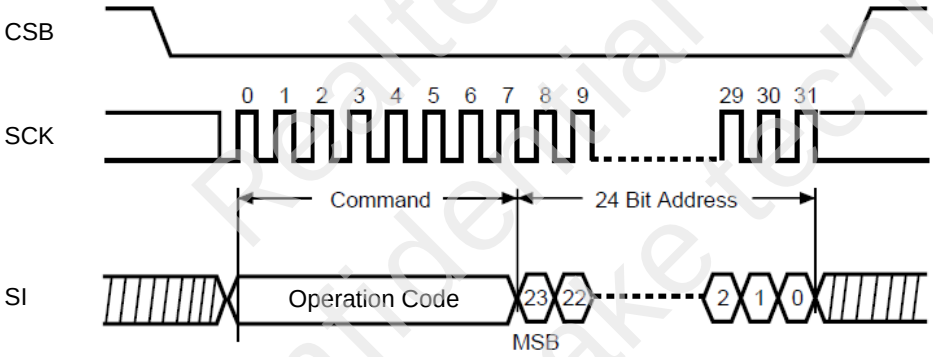

Figure 6. Sector/Block Erase Command Sequence

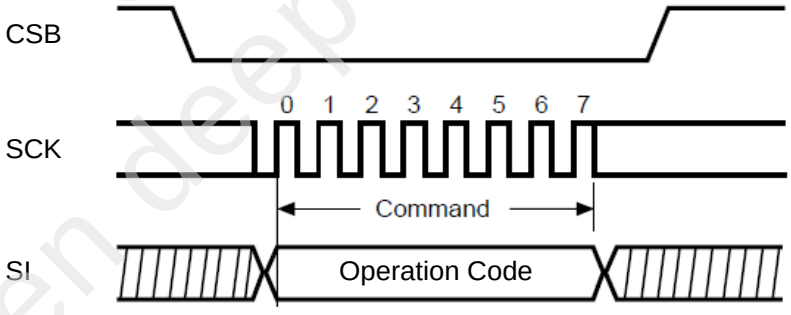

Figure 7. Chip Erase Command Sequence

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8.9.2. SPI Flash Interface Timing

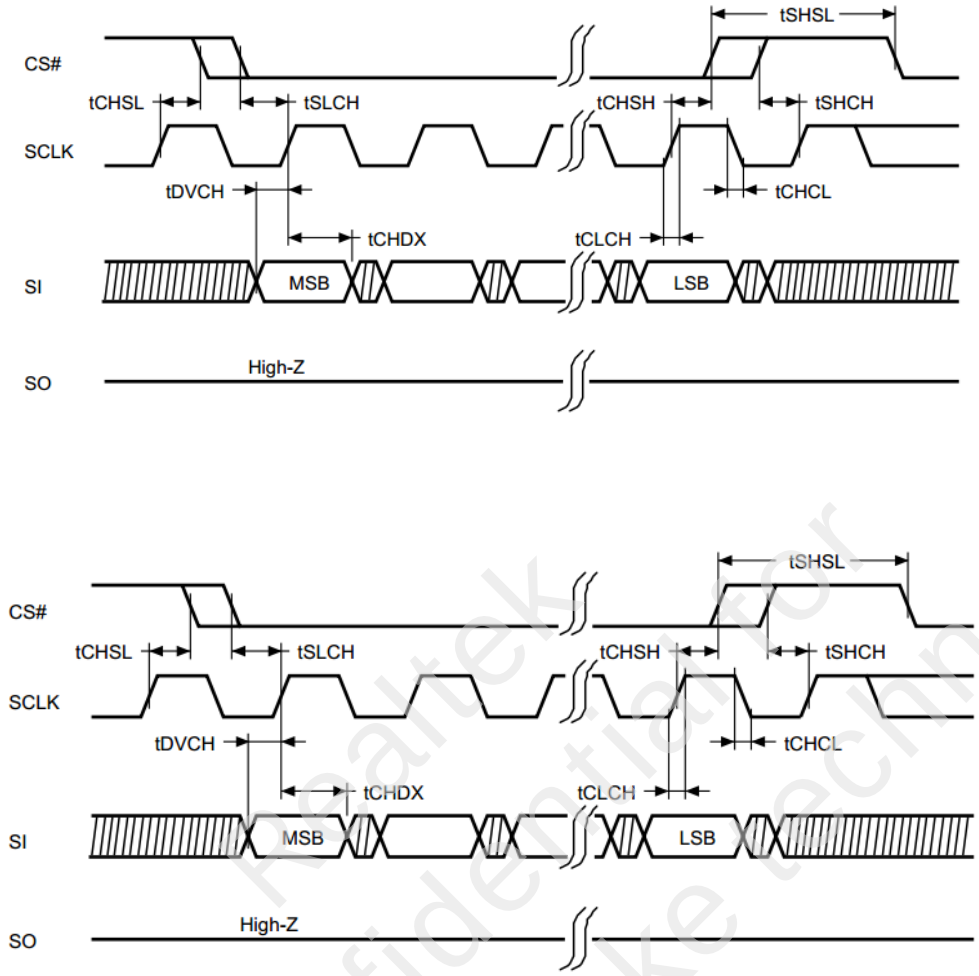

Figure 8. SPI Flash Interface Timing

Table 31. SPI Flash Access Timing Parameters

Symbol	Parameter	Min	Typ.	Max	Unit
fSCK	Clock Frequency controller can provide	62.5	-	-	MHz
tCH	Clock High Time	500/fSCK	-	-	ns
tCL	Clock Low Time	500/fSCK	-	-	ns
tCLCH	Clock Rise Time	0.1	-	-	V/ns
tCHCL	Clock Fall Time	0.1	-	-	V/ns
tDVCH	SI Setup Time (SI Valid to Clock High)	125/fSCK	-	-	ns
tCHDX	SI Hold Time (Clock High to SI invalid)	375/fSCK	-	-	ns
tSHQZ	SO Disable Time	-	-	-	ns
tCLQV	Clock Low to SO Valid	-	-	500/fSCK	ns
tCLQX	Output Hold Time	-	-	-	ns
tSOCH	SO Setup Time (SO Valid to Clock High)	0	-	-	ns
tSODX	SO Hold Time (Clock High to SO Invalid)	0	-	-	ns

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9. Power Sequence

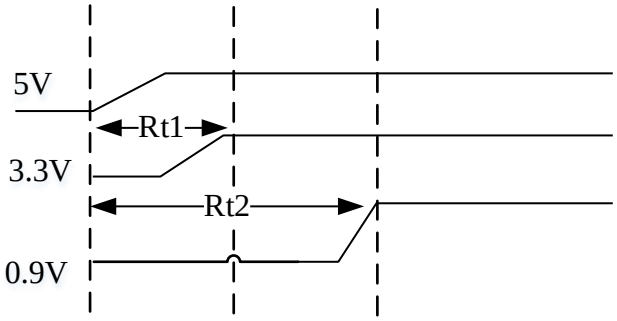

Figure 9. Power Sequence

Table 32. Power Sequence

Symbol	Parameter	Min	Max	Units
Rt1	5V Rise Time	80	-	µs
Rt2	5V to 3.3V Rise Time	360	-	µs
Rt3	5V to 0.9V Rise Time	2	-	ms

Note 1: If a situation occurs where 5V is not fully powered down, and power comes back on in a short time period (<50ms), the RTL9201R may be damaged. Please ensure this situation does not occur when testing.

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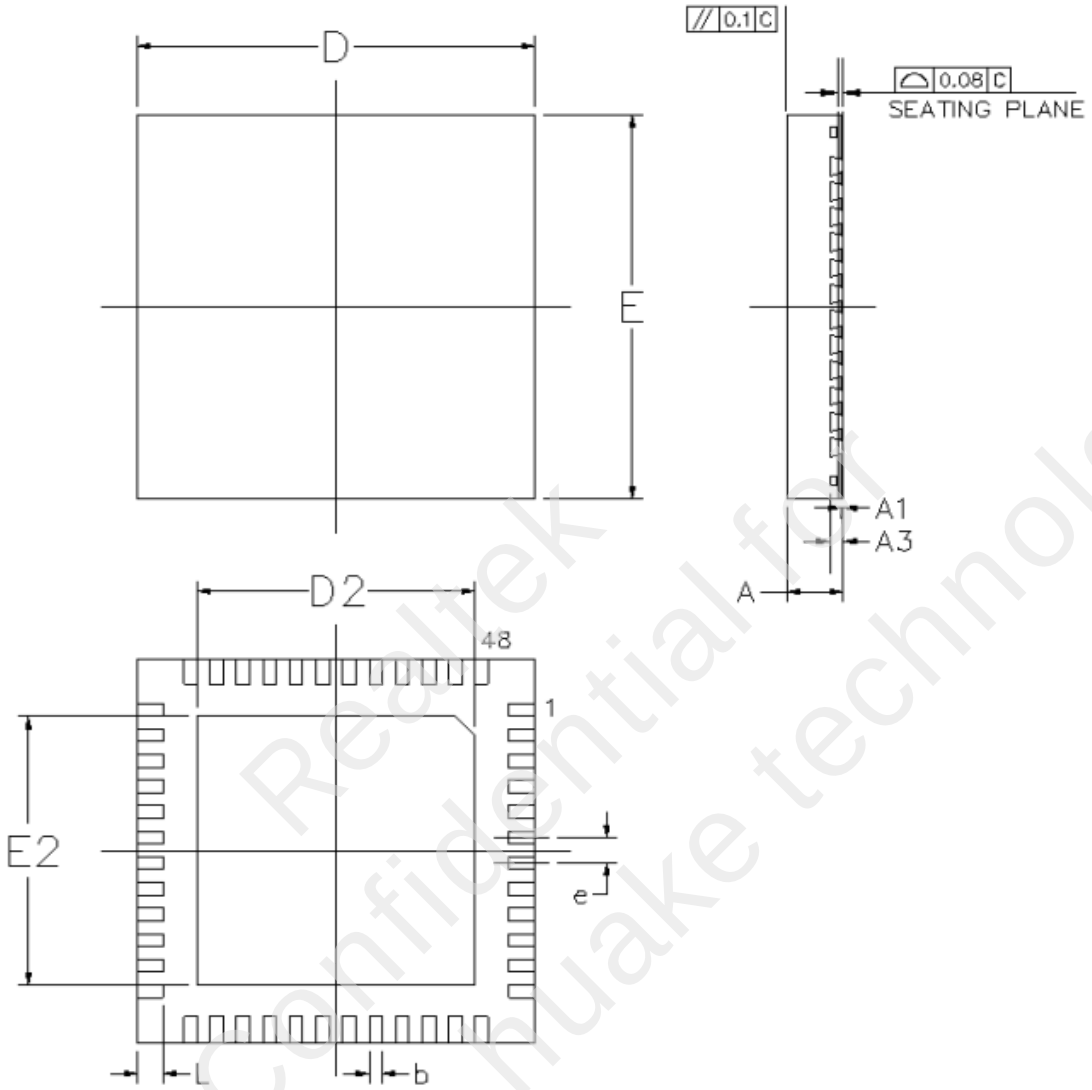
10. Mechanical Dimensions

Package 48 Leads 6mmx6mm



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	0.95	0.030	0.034	0.038
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	6.00BSC			0.236BSC		
D2/E2(E-pad size)	4.3	4.4	4.5	0.169	0.173	0.177
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

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11. Ordering Information

Table 33. Ordering Information

Part Number	Package
RTL9201R-CG	48-Pin QFN 'Green' Package

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