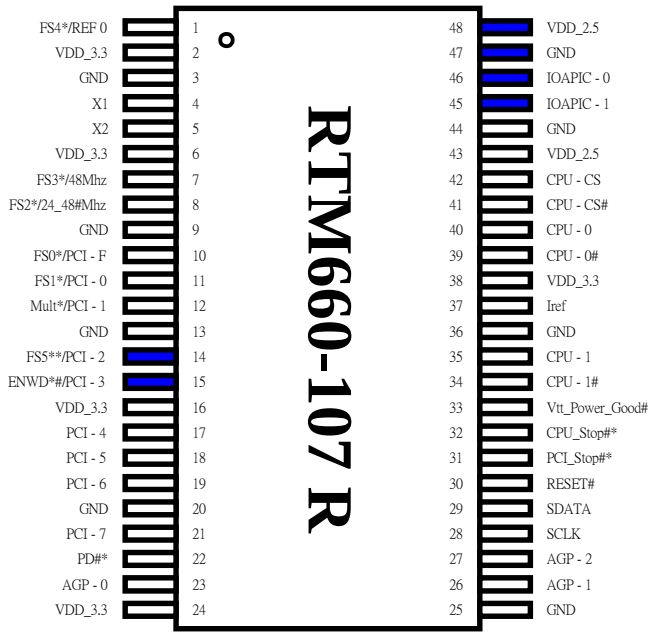
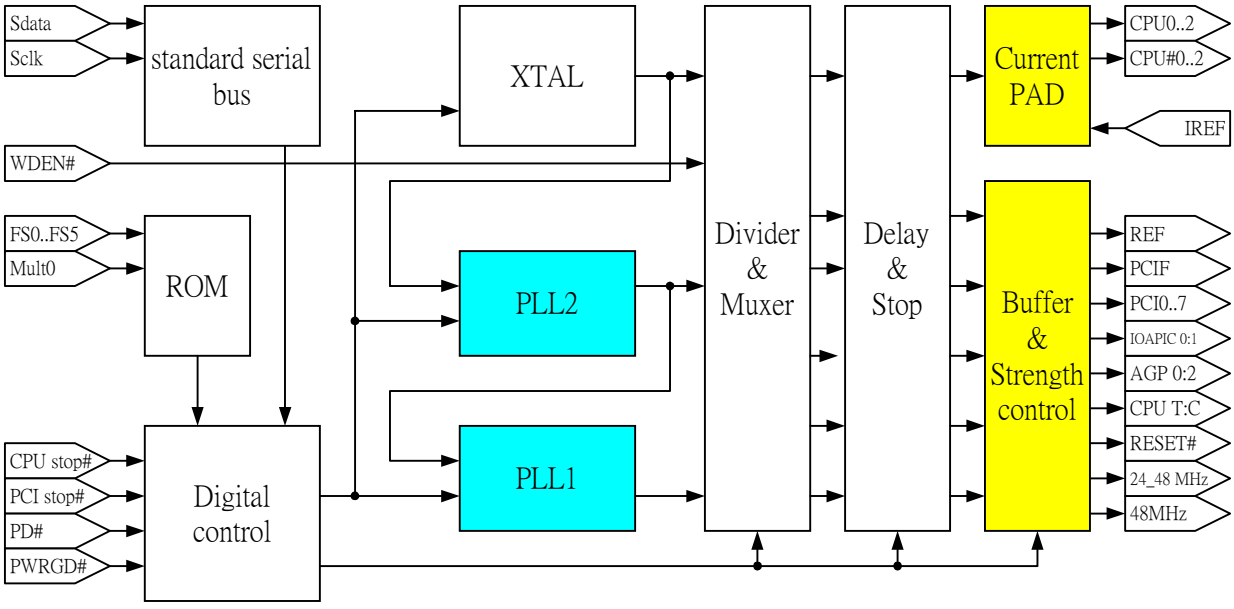
General Description

The RTM660-107R is a single chip frequency generator for VIA P4X266 with INTEL P4 Clock Synthesizer Driver Specification. The clock chip provides standard serial bus for programming device function. Base on the function above, the spread spectrum can be enable for reducing EMI.

Features

- Support Up to 266 MHz frequency.
- Power Down feature.
- Programmable Spread Spectrum depth.
- Programmable Spread Spectrum model.
- Programmable driving strength.
- Programmable skew delay.
- Programmable PLL frequency.
- Programmable Loop Filter.
- Programmable Smooth-Divider.
- Programmable current Iref.
- Programmable current Vg(Vref).
- Programmable Watch Dog & Smooth Reset circuit.
- DOS/WIN9x/WIN2000/WINNT AP.
- Enhance 266/233/200/166/133/100/66 CPU frequency ratio.





Pin Description

Pin Name	Pin No.	Type	Description
REF0	1	I/O	***Reference Clock:*** 3.3V 14.318 MHz clock output.
IOAPIC 1	45	O	***IOAPIC Clock: 2.5***V PCI/2 frequency clock output.
IOAPIC 0	46	O	***IOAPIC Clock: 2.5***V PCI/2 frequency clock output.
X1	4	I	***Crystal Input:*** This pin has dual functions. It can be used as an external 14.318MHz crystal connection or as an external reference frequency input.
X2	5	O	***Crystal Output:*** An input connection for an external 14.318MHz crystal connection. If using an external reference, this pin must be left unconnected.
CPU & CPU# 0:1	40, 39, 35, 34	O	***CPU Clock Outputs:*** Current mode Clock differential output. Output frequencies depending on the configuration of FS0:5.
CPU & CPU# CS	42, 41	O	***CPU Clock Outputs:*** 2.5V Clock differential output. Output frequencies depending on the configuration of FS0:5.
PCIF	10	I/O	***PCIF Clock:*** 3.3V 33 MHz PCI clock outputs.
PCI 0:3	11, 12, 14, 15	I/O	***PCI Clock 0 through 1:*** 3.3V 33 MHz PCI clock outputs..
PCI 4:7	17, 18, 19, 21	O	***PCI Clock 2 through 7:*** 3.3V 33 MHz PCI clock outputs.
RESET#	30	OD	***RESET# open drain Output:*** Watch Dog & smooth reset output, bounding option.
AGP_0:1	23, 26	O	***66 MHz Clock Output:*** 3.3V output clocks. The operating frequency is controlled by FS0:5.
AGP_2	27	O	***66 MHz Clock Output:*** 3.3V output clocks. The operating frequency is controlled by FS0:5.
48MHz	7	I/O	***48Mhz Clock Output:*** 3.3V fixed 48 MHz, non-spread spectrum clock output.
24_48# MHz	8	I/O	***24/48# MHz Clock Output***: 3.3V fixed 24/48# MHz, non-spread spectrum clock output.
FS*[0:4]	10, 11, 8, 7, 1	I/O	***Frequency Selection 0:4:*** This pin serves as the select strap to determine device's operating frequency as described in frequency Table. *Internal 150K pull-down.*
FS**5	14	I/O	***Frequency Selection 5:*** This pin serves as the select strap to determine device's operating frequency as described in frequency Table. *Internal 150K pull-down.*
Mult*	12	I/O	***Current Selection 1:*** This pin serves as the select strap to determine device's operating current. *Internal 150K pull-up.*
ENWD#*	15	I/O	***Enable watch-dog:*** This pin serves as the select strap to determine device's watch dog default. *Internal 150K pull-up.*
PD# *	22	I	***Power Down Control:*** LVTTL compatible input that places the device in power down mode when held low. *Internal 150K pull-up.*
PCI_Stop# *	31	I	***PCI Stop Control:*** LVTTL compatible input that places the device all PCI output stop at low when held low. *Internal 150K pull-up.*
CPU_Stop# *	32	I	***CPU Stop Control:*** LVTTL compatible input that places the device all CPU output stop at low when held low. *Internal 150K pull-up.*
Vtt_PWR_gd#	33	I	***Vtt Power Good:*** LVTTL compatible input that is a level sensitive strobe used to determine when FS[0:5] & Mult0 input are valid and OK to be sampled (active Low).
SDATA	29	I/O	Data pin for serial interface.
SCLK	28	I	Clock pin for serial interface.
Iref	37	I	***Iref:*** A precision resistor is attached to this pin which is connected to the internal current reference .
VDD3.3	2, 6, 16, 24, 38	P	***3.3V Power Connection:*** Power supply for SDRAM output buffers, PCI output buffers, reference output buffers and 48MHz output buffers. Connect to 3.3V.
VDD2.5	43, 48	P	***3.3V Power Connection:*** Power supply for SDRAM output buffers, PCI output buffers, reference output buffers and 48MHz output buffers. Connect to 3.3V.
GND	3, 9, 13, 20, 25, 36, 44, 47	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

*Note: Internal 150K pull-up(*) or pull down(**) resistors present on inputs marked with * /** respectively. Design should not rely solely on internal pull-up or pull down resistor to set I/O pins high or low respectively.*

Frequency Selection:

FS5	FS4	FS3	FS2	FS1	FS0	CPU	Ratio	3V66	PCI
0	0	0	0	0	0	102.00	1.50	68.00	34.00
0	0	0	0	0	1	105.00	1.50	70.00	35.00
0	0	0	0	1	0	108.00	1.50	72.00	36.00
0	0	0	0	1	1	111.00	1.50	74.00	37.00
0	0	0	1	0	0	114.00	1.50	76.00	38.00
0	0	0	1	0	1	117.00	1.50	78.00	39.00
0	0	0	1	1	0	120.00	1.50	80.00	40.00
0	0	0	1	1	1	123.00	1.50	82.00	41.00
0	0	1	0	0	0	126.00	1.50	84.00	42.00
0	0	1	0	0	1	130.00	1.50	86.67	43.33
0	0	1	0	1	0	136.00	2.00	68.00	34.00
0	0	1	0	1	1	140.00	2.00	70.00	35.00
0	0	1	1	0	0	144.00	2.00	72.00	36.00
0	0	1	1	0	1	148.00	2.00	74.00	37.00
0	0	1	1	1	0	152.00	2.00	76.00	38.00
0	0	1	1	1	1	156.00	2.00	78.00	39.00
0	1	0	0	0	0	160.00	2.00	80.00	40.00
0	1	0	0	0	1	164.00	2.00	82.00	41.00
0	1	0	0	1	0	166.60	2.50	66.64	33.32
0	1	0	0	1	1	170.00	2.50	68.00	34.00
0	1	0	1	0	0	175.00	2.50	70.00	35.00
0	1	0	1	0	1	180.00	2.50	72.00	36.00
0	1	0	1	1	0	185.00	2.50	74.00	37.00
0	1	0	1	1	1	190.00	2.50	76.00	38.00
0	1	1	0	0	0	66.80	1.00	66.80	33.40
0	1	1	0	0	1	100.90	1.50	67.27	33.63
0	1	1	0	1	0	200.40	3.00	66.80	33.40
0	1	1	0	1	1	133.90	2.00	66.95	33.48
0	1	1	1	0	0	66.00	1.00	66.00	33.00
0	1	1	1	0	1	100.00	1.50	66.67	33.33
0	1	1	1	1	0	200.00	3.00	66.67	33.33
0	1	1	1	1	1	133.00	2.00	66.50	33.25

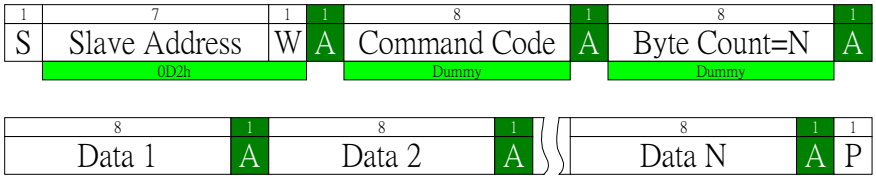
Phase Table

CPU	3V66	PCI
+ 66	+ 66	+ 33(+2ns)
+ 100	+ 66	+ 33(+2ns)
+ 133	+ 66	+ 33(+2ns)
+ 166	+ 66	+ 33(+2ns)
+ 200	+ 66	+ 33(+2ns)
+ 233	+ 66	+ 33(+2ns)
+ 266	+ 66	+ 33(+2ns)

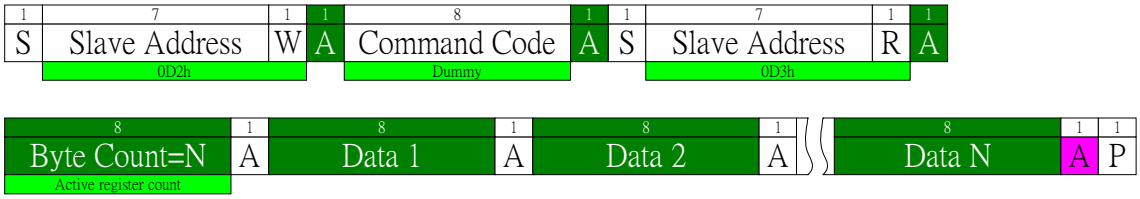
Standard Serial Bus Control:

Support standard serial bus block-mode and word-mode.
Byte Count = 08h(CR10h.bit0=0) / 18h(CR10h.bit0=1)

The Block Mode:

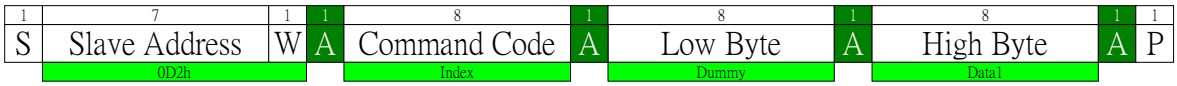


Block Write

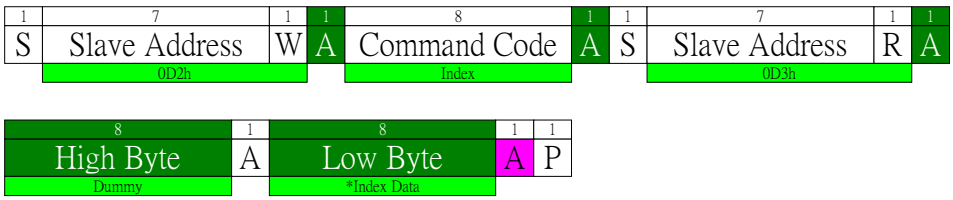


Block Read

The Word Mode:



Write Word



Read Word

Note slave address is D2h.

Register Description

CR 00h										
Bit	**Description**									**Default**
Bit7	0 = frequency is selected by latched input FS[5:0] 1 = frequency is selected by CR00h – bit 5, 4, 3, 2, 1, 0									0
Bit6	0 = spread spectrum disable 1 = spread spectrum enable									0
Bit5=0	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**CPU**	**Ratio**	**3V66**	**PCI**	0
Bit4	0	0	0	0	0	102.00	1.50	68.00	34.00	0
Bit3	0	0	0	0	1	105.00	1.50	70.00	35.00	0
Bit2	0	0	0	1	0	108.00	1.50	72.00	36.00	0
Bit1	0	0	0	1	1	111.00	1.50	74.00	37.00	0
Bit0	0	0	1	0	0	114.00	1.50	76.00	38.00	0
	0	0	1	0	1	117.00	1.50	78.00	39.00	0
	0	0	1	1	0	120.00	1.50	80.00	40.00	0
	0	0	1	1	1	123.00	1.50	82.00	41.00	0
	0	1	0	0	0	126.00	1.50	84.00	42.00	0
	0	1	0	0	1	130.00	1.50	86.67	43.33	
	0	1	0	1	0	136.00	2.00	68.00	34.00	
	0	1	0	1	1	140.00	2.00	70.00	35.00	
	0	1	1	0	0	144.00	2.00	72.00	36.00	
	0	1	1	0	1	148.00	2.00	74.00	37.00	
	0	1	1	1	0	152.00	2.00	76.00	38.00	
	0	1	1	1	1	156.00	2.00	78.00	39.00	
	1	0	0	0	0	160.00	2.00	80.00	40.00	
	1	0	0	0	1	164.00	2.00	82.00	41.00	
	1	0	0	1	0	166.60	2.50	66.64	33.32	
	1	0	0	1	1	170.00	2.50	68.00	34.00	
	1	0	1	0	0	175.00	2.50	70.00	35.00	
	1	0	1	0	1	180.00	2.50	72.00	36.00	
	1	0	1	1	0	185.00	2.50	74.00	37.00	
	1	0	1	1	1	190.00	2.50	76.00	38.00	
	1	1	0	0	0	66.80	1.00	66.80	33.40	
	1	1	0	0	1	100.90	1.50	67.27	33.63	
	1	1	0	1	0	200.40	3.00	66.80	33.40	
	1	1	0	1	1	133.90	2.00	66.95	33.48	
	1	1	1	0	0	66.00	1.00	66.00	33.00	
	1	1	1	0	1	100.00	1.50	66.67	33.33	
	1	1	1	1	0	200.00	3.00	66.67	33.33	
	1	1	1	1	1	133.00	2.00	66.50	33.25	

Note1: Default at power-up will be for latched logic inputs to define frequency, Bit 5:0 are default to 000000.

CR 00h										
Bit	**Description**									**Default**
Bit7	0 = frequency is selected by latched input FS[5:0] 1 = frequency is selected by CR00h – bit 5, 4, 3, 2, 1, 0									0
Bit6	0 = spread spectrum disable 1 = spread spectrum enable									0
Bit5=1	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**CPU**	**Ratio**	**3V66**	**PCI**	0
Bit4	0	0	0	0	0	103.00	1.50	68.67	34.33	0
Bit3	0	0	0	0	1	106.00	1.50	70.67	35.33	0
Bit2	0	0	0	1	0	109.00	1.50	72.67	36.33	0
Bit1	0	0	0	1	1	112.00	1.50	74.67	37.33	0
Bit0	0	0	1	0	0	115.00	1.50	76.67	38.33	0
	0	0	1	0	1	118.00	1.50	78.67	39.33	0
	0	0	1	1	0	121.00	1.50	80.67	40.33	0
	0	0	1	1	1	124.00	1.50	82.67	41.33	0
	0	1	0	0	0	127.00	1.50	84.67	42.33	0
	0	1	0	0	1	131.00	1.50	87.33	43.67	
	0	1	0	1	0	137.00	2.00	68.50	34.25	
	0	1	0	1	1	141.00	2.00	70.50	35.25	
	0	1	1	0	0	145.00	2.00	72.50	36.25	
	0	1	1	0	1	149.00	2.00	74.50	37.25	
	0	1	1	1	0	153.00	2.00	76.50	38.25	
	0	1	1	1	1	157.00	2.00	78.50	39.25	
	1	0	0	0	0	161.00	2.00	80.50	40.25	
	1	0	0	0	1	165.00	2.00	82.50	41.25	
	1	0	0	1	0	167.60	2.50	67.04	33.52	
	1	0	0	1	1	171.00	2.50	68.40	34.20	
	1	0	1	0	0	176.00	2.50	70.40	35.20	
	1	0	1	0	1	181.00	2.50	72.40	36.20	
	1	0	1	1	0	186.00	2.50	74.40	37.20	
	1	0	1	1	1	191.00	2.50	76.40	38.20	
	1	1	0	0	0	67.80	1.00	67.80	33.90	
	1	1	0	0	1	101.90	1.50	67.93	33.97	
	1	1	0	1	0	201.40	3.00	67.13	33.57	
	1	1	0	1	1	134.90	2.00	67.45	33.73	
	1	1	1	0	0	67.00	1.00	67.00	33.50	
	1	1	1	0	1	101.00	1.50	67.33	33.67	
	1	1	1	1	0	201.00	3.00	67.00	33.50	
	1	1	1	1	1	134.00	2.00	67.00	33.50	

Note1: Default at power-up will be for latched logic inputs to define frequency, Bit 5:0 are default to 000000.

CR 01h				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	Reserved		R/W	0
Bit6	Reserved		R/W	0
Bit5	Reserved		R/W	0
Bit4	Reserved		R/W	0
Bit3	Reserved		R/W	0
Bit2	0 = CPU-CS-F & CPU-CS-F# stop 1 = CPU-CS-F & CPU-CS-F# running	42, 41	R/W	1
Bit1	0 = CPU-1 & CPU-1# stop 1 = CPU-1 & CPU-1# running	35, 34	R/W	1
Bit0	0 = CPU-0 & CPU-0# stop 1 = CPU-0 & CPU-0# running	40, 39	R/W	1

CR 02h				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	Reserved		R/W	0
Bit6	Reserved		R/W	0
Bit5	Reserved		R/W	0
Bit4	Reserved		R/W	0
Bit3	Reserved		R/W	0
Bit2	0 = AGP-2 stop 1 = AGP-2 running	27	R/W	1
Bit1	0 = AGP-1 stop 1 = AGP-1 running	26	R/W	1
Bit0	0 = AGP-0 stop 1 = AGP-0 running	23	R/W	1

CR 03h				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	0 = PCI-7 stop 1 = PCI-7 running	21	R/W	1
Bit6	0 = PCI-6 stop 1 = PCI-6 running	19	R/W	1
Bit5	0 = PCI-5 stop 1 = PCI-5 running	18	R/W	1
Bit4	0 = PCI-4 stop 1 = PCI-4 running	17	R/W	1
Bit3	0 = PCI-3 stop 1 = PCI-3 running	15	R/W	1
Bit2	0 = PCI-2 stop 1 = PCI-2 running	14	R/W	1
Bit1	0 = PCI-1 stop 1 = PCI-1 running	12	R/W	1
Bit0	0 = PCI-0 stop 1 = PCI-0 running	11	R/W	1

CR 04h				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	1 = Select 24 Mhz output 0 = Select 48 Mhz output	8	R/W	1
Bit6	0 = IOAPIC-1 stop 1 = IOAPIC-1 running	45	R/W	1
Bit5	0 = IOAPIC-0 stop 1 = IOAPIC-0 running	46	R/W	1
Bit4	Reserved		R/W	1
Bit3	0 = REF 0 stop 1 = REF 0 running	1	R/W	1
Bit2	0 = 48 Mhz stop 1 = 48 Mhz running	7	R/W	1
Bit1	0 = 24_ 48# Mhz stop 1 = 24_ 48# Mhz running	8	R/W	1
Bit0	0 = PCI-F stop 1 = PCI-F running	10	R/W	1

CR 05h				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	Enable watch dog default 0 = enable Enable watch dog default 1 = disable	15	R	Latched
Bit6	Mult 1 power on latched	12	R	Latched
Bit5	FS5	14	R	Latched
Bit4	FS4	1	R	Latched
Bit3	FS3	7	R	Latched
Bit2	FS2	8	R	Latched
Bit1	FS1	11	R	Latched
Bit0	FS0	10	R	Latched

CR 06h				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	Reserved		R/W	1
Bit6	Reserved		R/W	1
Bit5	Reserved		R/W	1
Bit4	Reserved		R/W	1
Bit3	Reserved		R/W	1
Bit2	Reserved		R/W	1
Bit1	Reserved		R/W	1
Bit0	Reserved		R/W	1

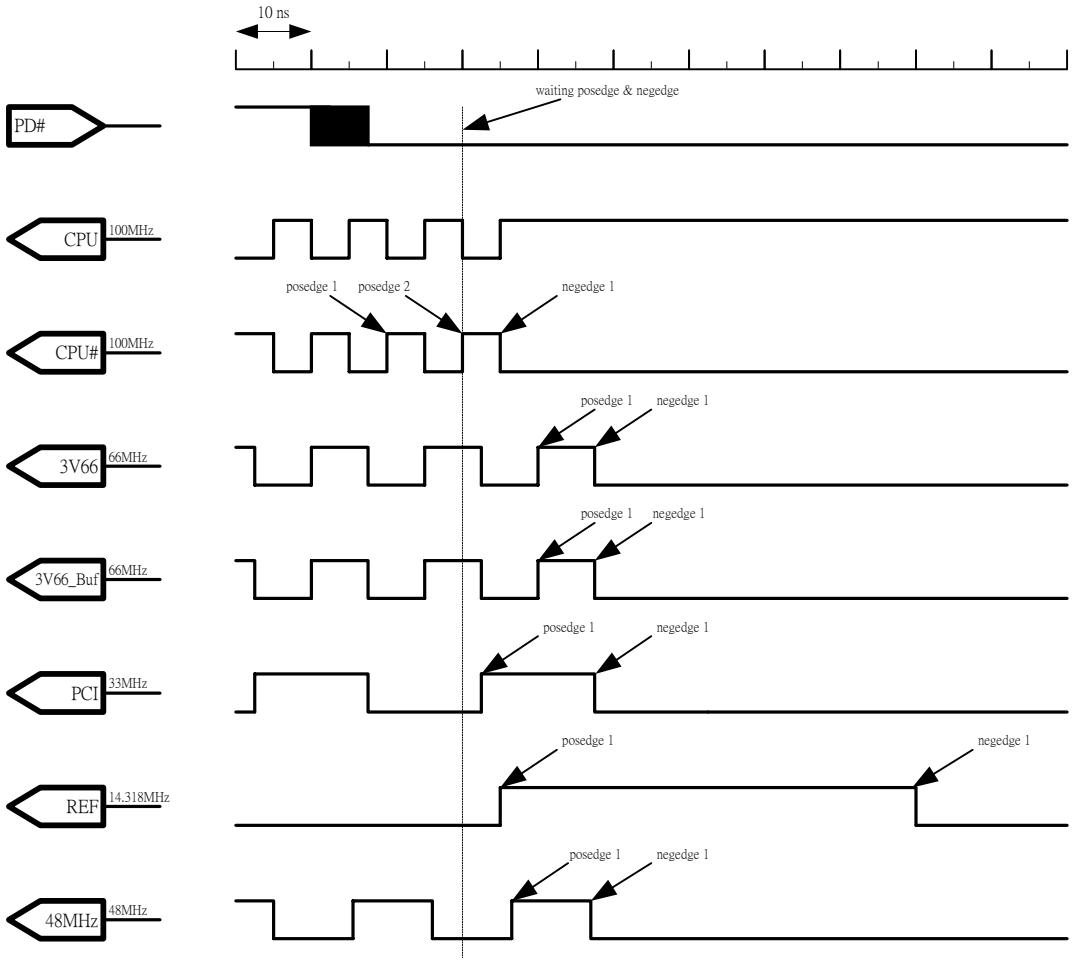
CR 07h				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	Reserved		R/W	1
Bit6	Reserved		R/W	1
Bit5	Reserved		R/W	1
Bit4	Reserved		R/W	1
Bit3	Reserved		R/W	1
Bit2	Reserved		R/W	1
Bit1	Reserved		R/W	1
Bit0	Reserved		R/W	1

CR 08h			
Bit	**Description**	**TYPE**	**Default**
Bit7	Revision Code	R	1
Bit6	Revision Code	R	1
Bit5	Revision Code	R	1
Bit4	Revision Code	R	1
Bit3	Vendor ID	R	1
Bit2	Vendor ID	R	1
Bit1	Vendor ID	R	1
Bit0	Vendor ID	R	1

Power Down Function

PD#	CPU	CPU#	AGP	PCI-F	PCI	REF	48	24/48	Osc	VCOs	I_{total}
0	Iref*2	float	Low	Low	Low	Low	Low	Low	Off	Off	25/45 mA
1	On	On	On	On	On	On	On	On	On	On	280 mA

Power Down Waveform



Note

1. After PD# is sampled active (Low) for 2 consecutive rising edges of CPUCLK#, all the output clocks are driven Low on their next High to Low transition.

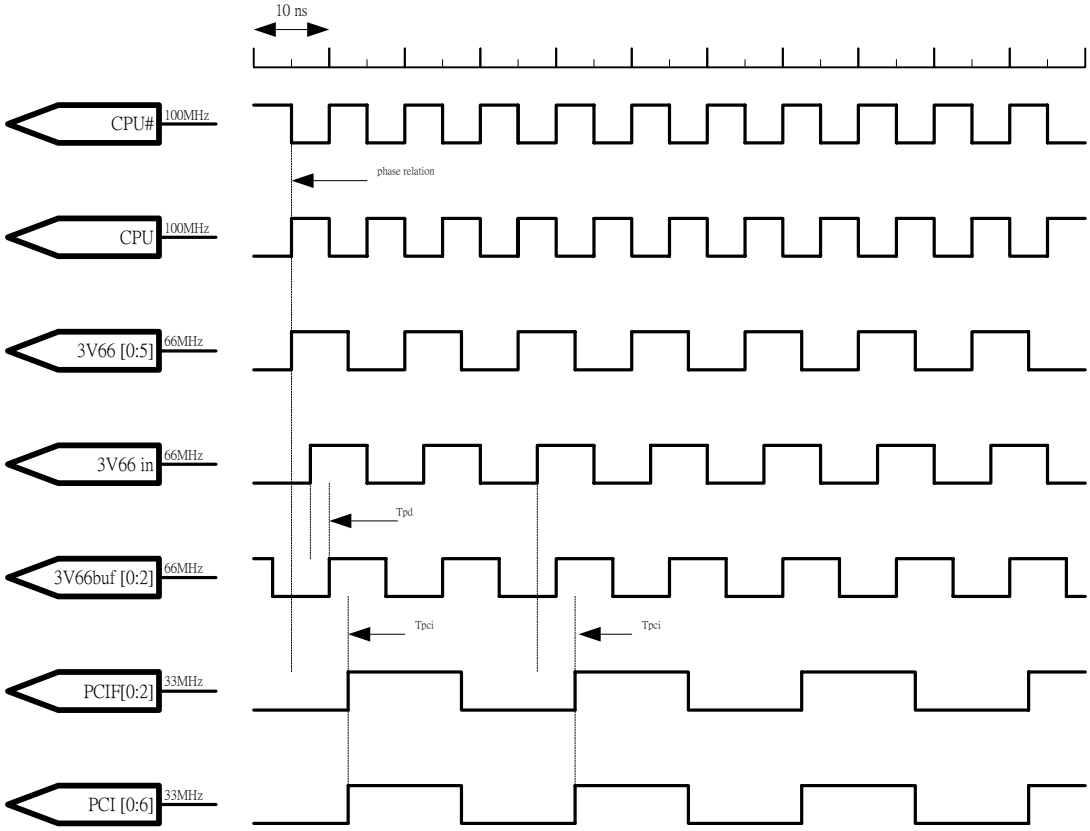
2. Power-up latency <3ms.

3. Waveform shown for 100MHz

Group Skew

GROUP	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
3V66 [0:5]	Group skew	3V66 @ 1.5V	0		500	ps
3V66 Buffer [0:2]	Group skew	3V66 @ 1.5V	0		175	ps
PCIF [0:2] & PCI [0:6]	Group skew	PCI @ 1.5V	0		500	ps
3V66 [0:5] to PCI	3V66-PCI skew	3V66@ 1.5V, PCI @ 1.5V	1.5	2.1	3.5	ns
3V66 input to 3V66 Buffer	3V66 buffer delay	3V66@ 1.5V	2.5		4.5	ns
3V66 Buffer to PCI	3V66-PCI skew	3V66@ 1.5V, PCI @ 1.5V	1.5	2.1	3.5	ns

Group Skew Waveform



Host Swing Select Function – CK Titan

Mult	Z	Rref	Iref	Output current	Voh @ Z
0	50	221 1% 475 1%	5.00 mA 2.32 mA	4*Iref	1.00V @ 50 0.47V @ 50
1	50	221 1% 475 1%	5.00 mA 2.32 mA	6*Iref	1.50V @ 50 0.70V @ 50
0	60	221 1% 475 1%	5.00 mA 2.32 mA	4*Iref	1.20V @ 60 0.56V @ 60
1	60	221 1% 475 1%	5.00 mA 2.32 mA	6*Iref	1.80V @ 60 0.84V @ 60

Iref=Vref(1.1)/Rref

DC specifications

Symbol	Parameter	Min.	Max.	Units	Notes
Absolute VDD A	3.3V core supply Voltage	-0.5	4.6	V	
Absolute VDD I/O	3.3V I/O supply Voltage	-0.5	4.6	V	
Ts	Storage Temperature	-65	150	°C	
Ta	Ambient Temperature	0	70	°C	
Absolute Vih	3.3V input high voltage	-0.5	4.6	V	
Absolute Vil	3.3V input low voltage	-0.5		V	
ESD	Input ESD protection			V	Human body mode
Operating Vdd A	3.3V core supply Voltage	3.135	3.465	V	
Operating Vdd I/O	3.3V I/O supply Voltage	3.135	3.465	V	
Operating Vih	3.3V input high voltage	2.0	Vdd+0.3	V	
Operating Vil	3.3V input low voltage	Vss-0.3	0.8	V	
Operating Iil	Input leakage current	-5	+5	uA	
Operating Voh	3.3V output high voltage	2.4		V	Ioh=-1mA
Operating Vol	3.3V output low voltage		0.4	V	Iol=1mA
Cin	Input pin capacitance		5	pF	
Cxtal	XTAL pin capacitance	13.5	22.5	pF	17..20 pF
Cout	Output pin capacitance		6	pF	
Lpin	Pin inductance		7	nH	

AC specifications

Electrical Characteristics – CPU 0.7V

T_A = 0 - 70C, CPU V_{out} =0.7 V, Vol=0.14V, Voh=0.56V, Test load Rs=33.2 Rp=49.9

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency		66/100/133/166/200/233/266 Mhz	66		266	MHz
Output Impedance				50		Ω
Overshoot Voltage					850	mV
Undershoot Voltage			-150			mV
Rising edge ring back						mV
Falling edge ring back						mV
Output High Current				6*Iref		mA
Output Low Current				0		mA
Vcross			280		430	mV
Vcross rising Vrriation					90	mV
Vcross all Vrriation					110	mV
Rise Time		Vol=0.14V, Voh=0.56V	175		600	ps
Fall Time		Vol=0.14V, Voh=0.56V	175		600	ps
Rise Time Variation		Vol=0.14V, Voh=0.56V			150	ps
Fall Time Variation		Vol=0.14V, Voh=0.56V			150	ps
Rise/Fall matching		2*(Trise-Tfall)/ (Trise+Tfall)			20	%
Duty Cycle			45	50	55	%
Skew					250	ps
Jitter					200	ps

Electrical Characteristics – CPU 1.0V

T_A = 0 - 70C, CPU V_{out} =1.0 V, Vol=0.2V, Voh=0.8V, Test load Rs=33.2 Rp=49.9

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency		66/100/133/166/200/233/266 Mhz	66		266	MHz
Output Impedance				50		Ω
Overshoot Voltage					1450	mV
Undershoot Voltage			-200			mV
Rising edge ring back					850	mV
Falling edge ring back			350			mV
Output High Current				4*Iref		mA
Output Low Current				0		mA
Vcross			510		760	mV
Vcross rising Vrriation					90	mV
Vcross all Vrriation					110	mV
Rise Time		Vol=0.2V, Voh=0.8V	300		600	ps
Fall Time		Vol=0.2V, Voh=0.8V	300		600	ps
Rise Time Variation		Vol=0.2V, Voh=0.8V			150	ps
Fall Time Variation		Vol=0.2V, Voh=0.8V			150	ps
Rise/Fall matching		2*(Trise-Tfall)/ (Trise+Tfall)			20	%
Duty Cycle			45	50	55	%
Skew					250	ps
Jitter					200	ps

Electrical Characteristics - PCI

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency				33		MHz
Output Impedance		VO = VDD*(0.5)	12		55	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 3.153V	-29		-23	mA
Output Low Current		VOL @MIN= 2.0V , VOL@ MAX= 0.4V	27		29	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	0.5		2	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	0.5		2	ns
Duty Cycle		VT = 1.5 V	45	50	55	%
Skew		VT = 1.5 V			500	ps
Jitter		VT = 1.5 V			500	ps

Electrical Characteristics - AGP

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency						MHz
Output Impedance		VO = VDD*(0.5)	12		55	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.55	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 3.153V	-29		-23	mA
Output Low Current		VOL @MIN= 2.0V , VOL@ MAX= 0.4V	27		29	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	0.5		2	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	0.5		2	ns
Duty Cycle		VT = 1.5 V	45	50	55	%
Skew		VT = 1.5 V			500	ps
Jitter		VT = 1.5 V			250	ps

Electrical Characteristics - REF

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency				14.318		MHz
Output Impedance		VO = VDD*(0.5)	10		55	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 3.153V	-33		-33	mA
Output Low Current		VOL @MIN= 2.0V , VOL@ MAX= 0.4V	30		38	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	1		4	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	1		4	ns
Duty Cycle		VT = 1.5 V	45	50	55	%
Skew		VT = 1.5 V				ps
Jitter		VT = 1.5 V			1000	ps

Electrical Characteristics – 48MHz

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency				48		MHz
Output Impedance		VO = VDD*(0.5)	20		60	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 3.153V	-29		-23	mA
Output Low Current		VOL @MIN= 2.0V , VOL@ MAX= 0.4V	27		29	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	0.5		2	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	0.5		2	ns
Duty Cycle		VT = 1. 5 V	45	50	55	%
Skew		VT = 1.5 V			250	ps
Long term jitter		10us period jitter @VT = 1.5 V			2	ns
Jitter		VT = 1.5 V			500	ps

Electrical Characteristics – 24/48# MHz

T_A = 0 - 70C, V_{DDL} = 3.3 V +/-5%; CL = 10 - 20 pF (unless otherwise stated)

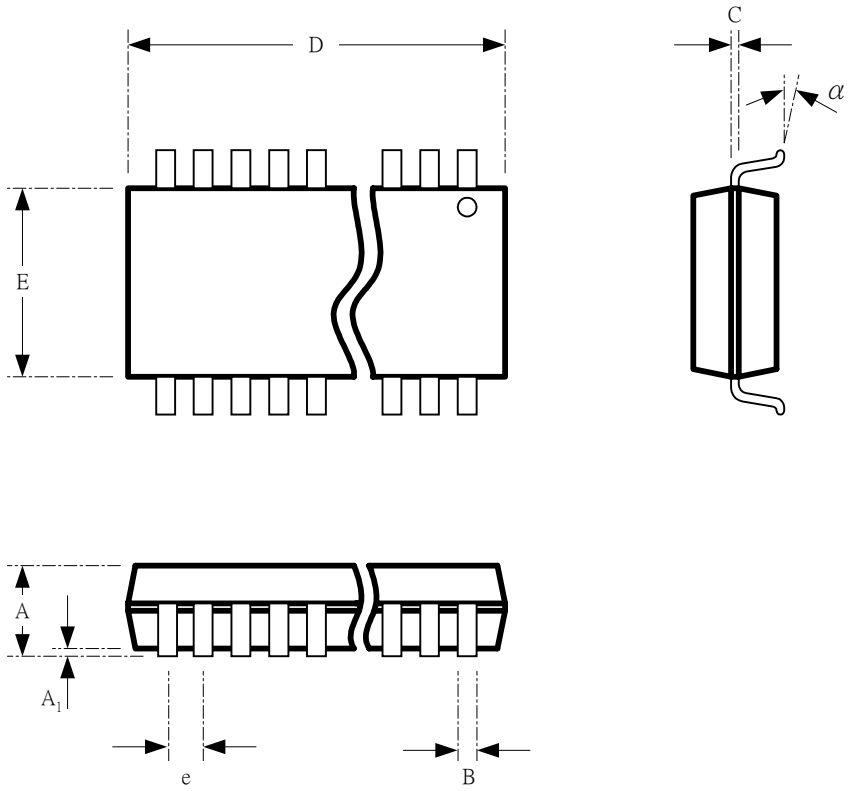
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency				24/48		MHz
Output Impedance		VO = VDD*(0.5)	20		60	Ω
Output High Voltage		IOH = -1 mA	2.4			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 3.153V	-29		-23	mA
Output Low Current		VOL @MIN= 2.0V , VOL@ MAX= 0.4V	27		29	mA
Rise Time		VOL = 0.4 V, VOH = 2.4 V	0.5		2	ns
Fall Time		VOH = 2.4 V, VOL = 0.4 V	0.5		2	ns
Duty Cycle		VT = 1. 5 V	45	50	55	%
Skew		VT = 1.5 V			250	ps
Long term jitter		125us period jitter @VT = 1.5 V			6	ns
Jitter		VT = 1.5 V			500	ps

Electrical Characteristics - IOAPIC

T_A = 0 - 70C, V_{DDL} = 2.5 V +/-5%; CL = 10 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output Frequency				16.5		MHz
Output Impedance		VO = VDD*(0.5)	12		55	Ω
Output High Voltage		IOH = -1 mA	2.0			V
Output Low Voltage		IOL = 1 mA			0.4	V
Output High Current		VOH @MIN= 1.0V , VOH@ MAX= 2.375V	-29		-23	mA
Output Low Current		VOL @MIN= 1.2V , VOL@ MAX= 0.3V	27		29	mA
Rise Time		VOL = 0.4 V, VOH = 2.0 V	1		4	ns
Fall Time		VOH = 2.0 V, VOL = 0.4 V	1		4	ns
Duty Cycle		VT = 1.5 V	45	50	55	%
Skew		VT = 1.5 V			500	ps
Jitter		VT = 1.5 V			500	ps

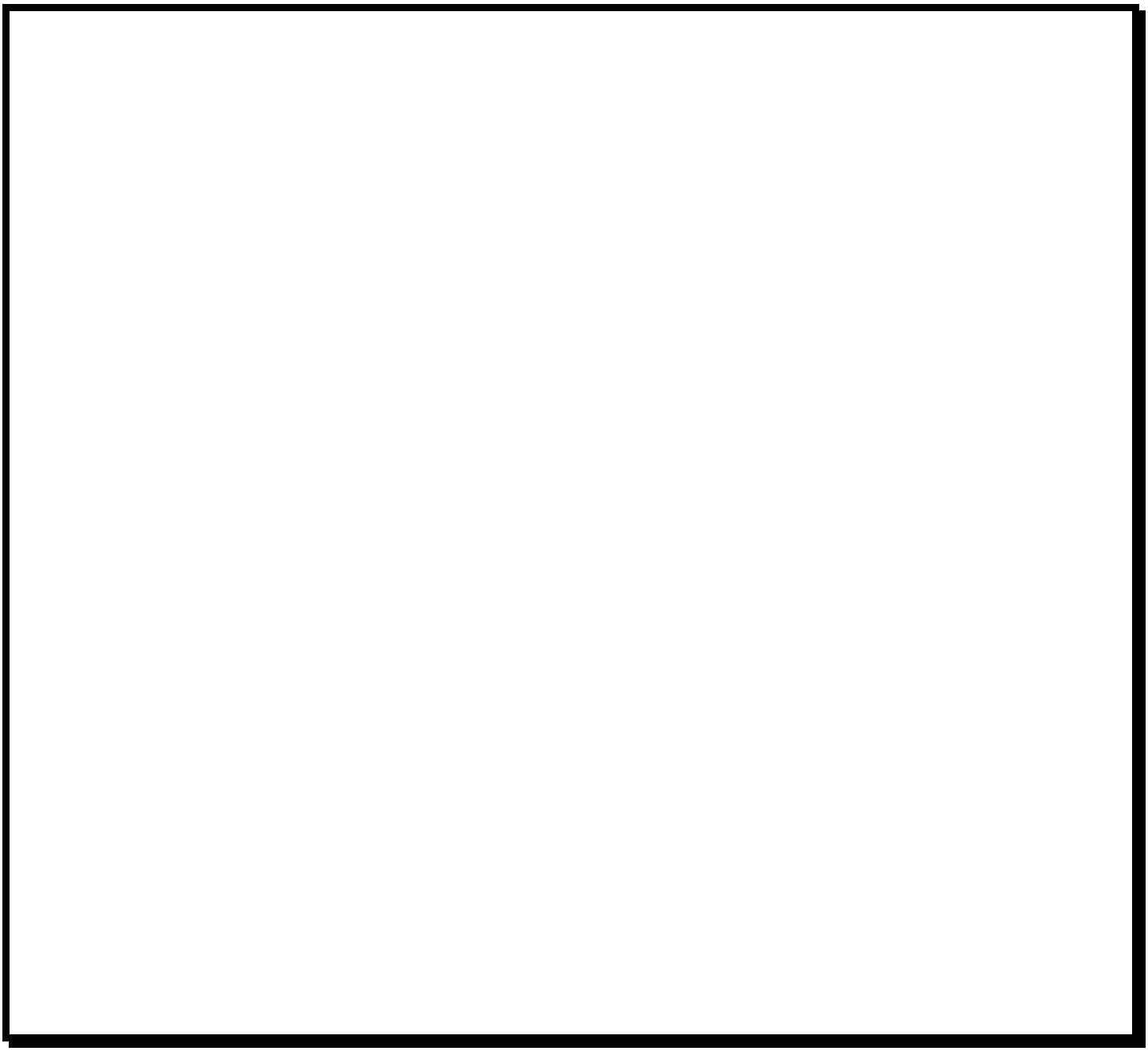
Package outline



SSOP Package:(unit using inches)

Symbol	Common Dimensions			Variations	D			N
	Min.	Type	Max.		Min.	Type	Max.	
A	0.095	0.101	0.110	AC	0.620	0.625	0.630	48
A1	0.008	0.012	0.016	AD	0.720	0.725	0.730	56
B	0.008	0.010	0.0135					
C	0.005	0.0075	0.010					
D	See Variations							
E	0.292	0.296	0.299					
e	0.025BSC							
α	0°	5°	10°					

Demo board circuit:



Please refer to the main board design guide.

Quartz crystal requirements for RTM660 series.

1. Frequency and Oscillation Circuits

RTM660 series are designed to work from a crystal with 14.31818MHz.
Fig-1 shows the equivalent circuits of crystal and oscillation circuits within RTM660 series.

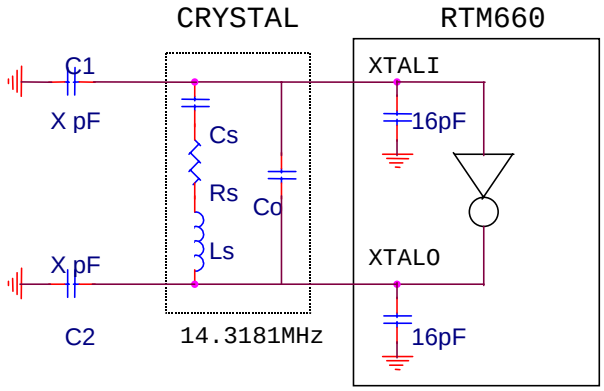


Fig-1 oscillation circuits

$$Fs \cong \frac{1}{2\pi\sqrt{Ls * Cs}}$$

The series resonant frequency, and parallel resonant frequency

$$Fp \cong \frac{1}{2\pi\sqrt{\frac{Ls * Cs * Co}{Cs + Co}}}$$

The oscillated frequency between *Fs* and *Fp*

$$Fo = Fs * \sqrt{1 + \frac{Cs}{Co + CL}}$$

where CL=((C1+16pF)*(C2+16pF)) / ((C1+16pF)+(C2+16pF))

2. Crystal Requirements

General Specifications	Requirements
Holder Type	HC-49 U/S
Crystal Freq.	14.31818 MHz
Oscillation Mode	Fundamental
Load Cap. (CL)	16 ~32 pF
Freq. Tolerance(25℃)	+/- 30 ppm
Effective Series Resistance (Rs)	40 ohm max
Effective Shunt Capacitance (Co)	7 pF
Drive Level	< 0.1 mW
Insulation Resistance	500 Mohm min. at DC 100V

Table-1 Crystal General Specification

3. Load Capacitance (CL)

To operate between Fs and Fp requires external load capacitance. Although RTM660 series has embed internal 16 pF capacitors at XTALI and XTALO, the oscillated frequency may be a little higher than 14.31818 MHz if no C1 and C2 placed.

To reduce the REF clock jitter and get more accurate frequency, the external capacitor C1 and C2 must be used.

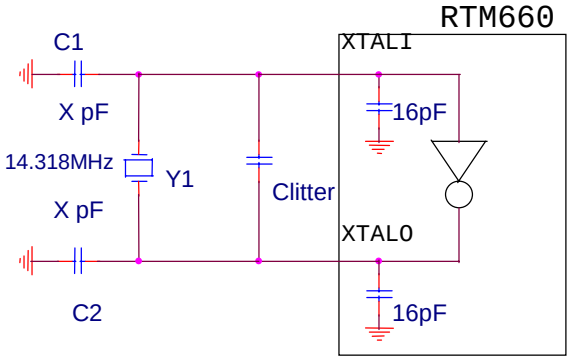


Fig-2 Clitter due to PCB Trace

In ideal case, ignore the Clitter at suggested C1=C2=16pF, the equivalent load capacitance is

$$CL = ((16pF + 16pF) * (16pF + 16pF)) / ((16pF + 16pF) + (16pF + 16pF)) = 16pF$$

According to Table-1 specification, the crystal with *CL* is 16pF is adapted. But in most case, the litter capacitor (Clitter) generated by PCB trace is existent. So the real CL is

$$CL = (C1 + 16pF) // (C2 + 16pF) + Clitter$$

Consider the litter capacitance , crystal with CL=20pF is allowable.

4. Reference table

C_L (pF)	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
C_1=C_2 (pF)	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48

Table-2 Crystal C_L General Specification

Enhance register

CR 10h [16]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:4]	Reserved	R/W	[0000]
Bit3	Reserved	R/W	0
Bit2	0 = normal 1 = watch dog enable. Action is internal reset & external reset	R/W	Latched [26#]
Bit1	0 = serial Bus block mode 1 = serial Bus word mode	R/W	0
Bit0	0 = write protected CR[11h:28h] 1 = writable CR[11h:28h]	R/W	0

CR 11h [17]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:2]	Reserved	R/W	**[0000_00]**
Bit[1:0]	M code bit[9:8] for PLL1	R/W	**[00]**

CR 12h [18]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	M code bit[7:0] for PLL1	R/W	**[0110_0011]**

CR 13h [19]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:2]	Reserved	R/W	**[0000_00]**
Bit[1:0]	M code bottom level bit[9:8] for PLL1 sperad spectrum	R/W	**[00]**

CR 14h [20]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	M code bottom level bit[7:0] for PLL1 sperad spectrum	R/W	**[0110_0011]**

CR 15h [21]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:6]	Reserved	R/W	**[00]**
Bit[5:0]	N code bit[5:0] for PLL1	R/W	**[01_0110]**

** CPU Frequency = 24*(M+2)/(N+2) … Suggest N=22(016h)*

CR 16h [22]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:5]	Watch dog tmer [base =1.25 second] [000] = 3 base second [001] = 4 base second [010] = 5 base second [011] = 6 base second [100] = 7 base second [101] = 8 base second [110] = 9 base second [111] = 10 base second	R/W	[001]
Bit[4:0]	Reserved	R/W	[0_0000]

CR 17h [23]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:3]	Reserved	R/W	[0000_0]
Bit2	0 = stop XTAL while PD# 1 = free running XTAL	R/W	1
Bit1	0 = disable last serial BUS write latched with reset# output 1 = enable last serial BUS write latched with reset# output & reset CR10h bit0, 1	R/W	0
Bit0	Reserved	R/W	0

CR 18h [24]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:4]	St = Spread spectrum change top level by CR19h.bit[1:0] base	R/W	[0111]
Bit[3:0]	Sb = Spread spectrum change bottom level by CR19h.bit[1:0] base	R/W	[0110]

Note: St ≥Sb>0

CR 19h [25]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:2]	Reserved	R/W	[0000_00]
Bit[1:0]	Spread spectrum change level by (ref / N) base 00 = 2 base 01 = 4 base 10 = 8 base 11 = 16 base	R/W	[10]

CR 1ah [26]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Cp_1 Base = 6.25 pF 0 = disconnect 1 = parallel Cp_1 with 6.25 pF	R/W	0
Bit6	0 = disconnect 1 = parallel Cp_1 with 6.25 pF	R/W	1
Bit5	0 = disconnect 1 = parallel Cp_1 with 6.25 pF	R/W	1
Bit4	0 = disconnect 1 = parallel Cp_1 with 6.25 pF	R/W	1
Bit3	I_1 Base = 5uA 0 = disconnect 1 = parallel I_1 with 40 uA	R/W	0
Bit2	0 = disconnect 1 = parallel I_1 with 20 uA	R/W	0
Bit1	0 = disconnect 1 = parallel I_1 with 10 uA	R/W	0
Bit0	0 = disconnect 1 = parallel I_1 with 5 uA	R/W	1

CR 1bh [27]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Reserved	R/W	0
Bit[6:4]	R_{s1} = 500Ω x ([6:4]+1)	R/W	[000]
Bit3	Cs_1 Base = 400 pF 0 = disconnect 1 = parallel Cs_1 with 25 pF	R/W	1
Bit2	0 = disconnect 1 = parallel Cs_1 with 25 pF	R/W	1
Bit1	0 = disconnect 1 = parallel Cs_1 with 25 pF	R/W	1
Bit0	0 = disconnect 1 = parallel Cs_1 with 25 pF	R/W	1

CR 1ch [28]			
Bit	**Description**	**TYPE**	**Default**
Bit7	0 = CPU drive strength normal 1 = CPU drive strength enhance	R/W	1
Bit6	0 = PCI drive strength normal 1 = PCI drive strength enhance	R/W	0
Bit5	0 = PCI-F drive strength normal 1 = PCI-F drive strength enhance	R/W	0
Bit4	0 = AGP drive strength normal 1 = AGP drive strength enhance	R/W	0
Bit3	0 = IOAPIC drive strength normal 1 = IOAPIC drive strength enhance	R/W	0
Bit2	0 = REF 0/1 drive strength normal 1 = REF 0/1 drive strength enhance	R/W	0
Bit1	0 = 48MHz drive strength normal 1 = 48MHz drive strength enhance	R/W	0
Bit0	0 = 24_48# MHz drive strength normal 1 = 24_48# MHz drive strength enhance	R/W	0

CR 1dh [29]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:6]	00 = Vg set 1.0 V 01 = Vg set 1.1 V 10 = Vg set 1.2 V 11 = Vg set 1.3 V	R/W	[01]
Bit[5:4]	Iref ratio 00 = 4*I ref 10 = 5*I ref 01 = 6*I ref 11 = 7*I ref	R/W	[00]
Bit3	0 = Iref ratio select latched Mult[0:1] 1 = Iref ratio select CR 1dh bit[5:4]	R/W	0
Bit2	Reserved	R/W	0
Bit1	Reserved	R/W	0
Bit0	Reserved	R/W	0

CR 1eh [30]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Cp_2 Base = 6.25 pF 0 = disconnect 1 = parallel Cp_2 with 6.25 pF	R/W	0
Bit6	0 = disconnect 1 = parallel Cp_2 with 6.25 pF	R/W	0
Bit5	0 = disconnect 1 = parallel Cp_2 with 6.25 pF	R/W	0
Bit4	0 = disconnect 1 = parallel Cp_2 with 6.25 pF	R/W	0
Bit3	I_2 Base = 10uA 0 = disconnect 1 = parallel I_2 with 80uA	R/W	1
Bit2	0 = disconnect 1 = parallel I_2 with 40uA	R/W	1
Bit1	0 = disconnect 1 = parallel I_2 with 20uA	R/W	1
Bit0	0 = disconnect 1 = parallel I_2 with 10uA	R/W	1

CR 1fh [31]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:6]	Reserved	R/W	[00]
Bit[5:3]	000 = AGP select /2 (CPU = 66) 001 = AGP select /3 (CPU = 100) 010 = AGP select /4 (CPU = 133) 011 = AGP select /5 (CPU = 166) 100 = AGP select /6 (CPU = 200) 101 = AGP select /7 (CPU = 233) 110 = AGP select /8 (CPU = 266) 111 = AGP select /X (CPU = X)	R/W	ROM/REG [001]
Bit2	0 = Divider select by ROM 1 = Divider select by REG CR1fh.bit[7:3]	R/W	0
Bit1	M N code latching buffer while writen 1	W	0
Bit0	0=PLL1 programmable disable 1=PLL1 programmable enable	R/W	0

CR 20h [32]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Reserved	R/W	0
Bit[6:4]	R_{S2} = 500Ωx ([6:4]+1)	R/W	[111]
Bit3	C_{S2} Base = 25pF 0 = disconnect 1 = parallel C_{S2} with 25pF	R/W	1
Bit2	0 = disconnect 1 = parallel C_{S2} with 25pF	R/W	1
Bit1	0 = disconnect 1 = parallel C_{S2} with 25pF	R/W	1
Bit0	0 = disconnect 1 = parallel C_{S2} with 25pF	R/W	1

CR 21h [33]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:6]	CPU-0 group delay selection by 500 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]
Bit[5:4]	CPU-1 group delay selection by 500 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]
Bit[3:2]	CPU-CS group delay selection by 500 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]
Bit[1:0]	AGP group delay selection by 500 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]

CR 22h [34]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:6]	PCI group delay selection by 500 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]
Bit[5:4]	PCI-F group delay selection by 500 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]
Bit3	0 = normal 1 = enable test mode (PLL1) = (PLL1)/4 & (PLL2) = (PLL2)/1 & Watch Dog timer base =1 u second & RESET# pulse = 1 u second	R/W	0
Bit2	0 = PCI to AGP delay 2.0 ns 1 = PCI to AGP delay 3.0 ns	R/W	0
Bit[1:0]	Reserved group delay selection by 500 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]

CR 23h [35]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	Reserved for clock buffer	R/W	[1111-1111]

CR 24h [36]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	Reserved for clock buffer	R/W	[1111-1111]

CR 25h [37]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:2]	Reserved	R/W	**[0000_00]**
Bit[1:0]	M code bit[9:8] for PLL2	R	**[01]**

CR 26h [38]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	M code bit[7:0] for PLL2	R	**[0010_0101]**

CR 27h [39]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:6]	Reserved	R/W	**[00]**
Bit[5:0]	N code bit[5:0] for PLL2	R	**[00_1001]**

** PLL Frequency = 14.31818*(M+2)/(N+2)… Suggest N=9(09h)*