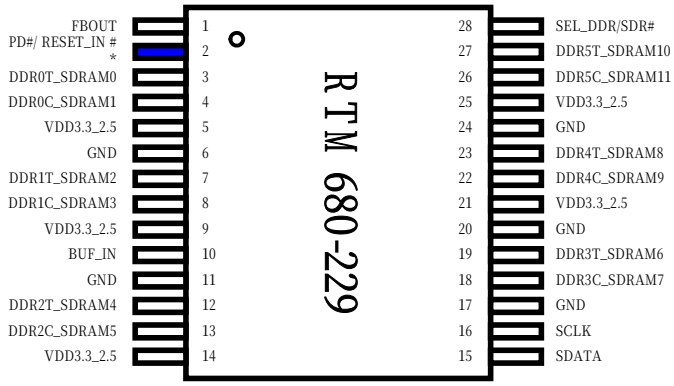
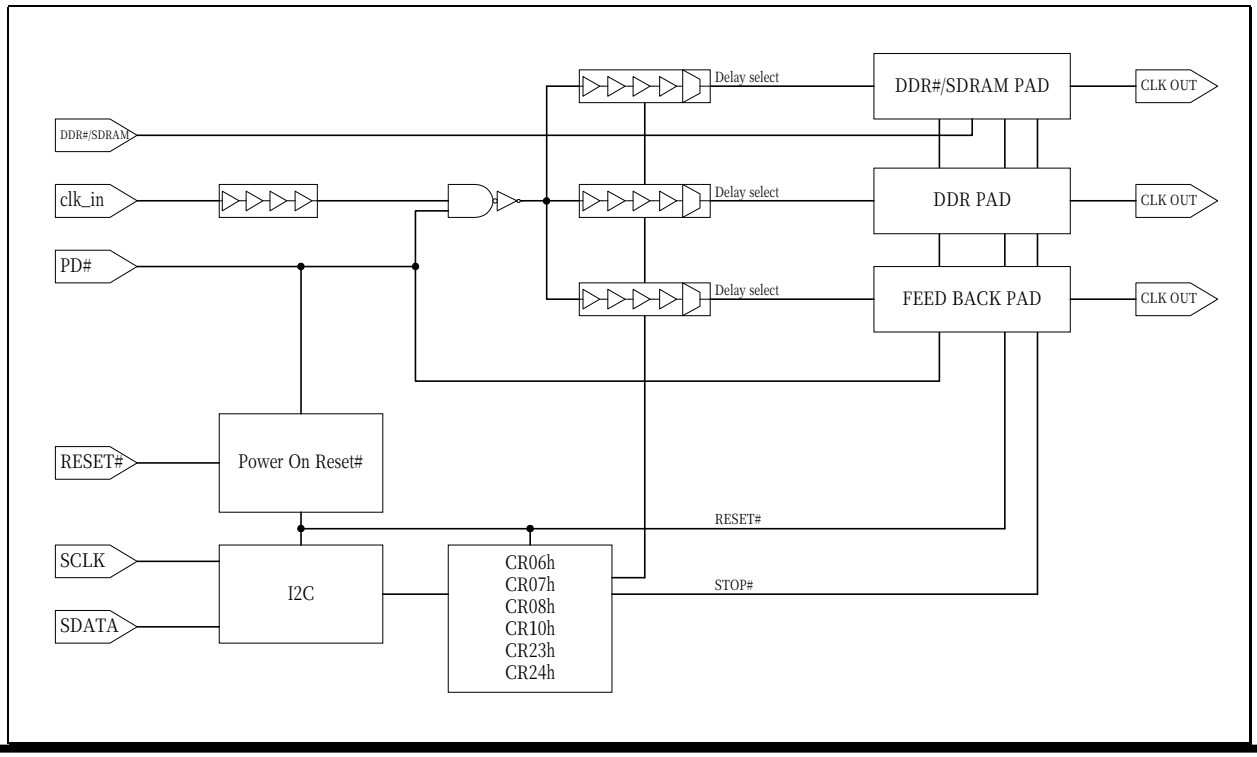
General Description

The RTM 680-229 is a 3.3V/2.5V DDR / SDRAM fan out buffer. The RTM680-229 can be used in conjunction with the RTM560/660/360 or similar clock synthesizer for the VIA 266/333/400 chipset. The clock chip provides standard serial bus for programming device function. And RTM 680-229 also builds in the enhance function.

Features

- Support Up to 400MHz DDR.
- Programmable clock skew.
- Programmable drive strength.
- Power Down feature.
- 1 input to 12 output buffer
- 1 feedback clock
- Supports 2 DDR DIMMs.
- Supports 3 SDRAM DIMMs.
- Supports 2 type package ID (D2/D6) by bonding option.





Pin Description

Pin Name	228 R	Type	Description
SEL_DDR/SDR#	28	I	***DDR mode Select:*** Select input for DDR or SDRAM mode 0=SDRAM mode. 1=DDR mode.
SDATA	15	I/O	Data pin for serial interface.
SCLK	16	I	Clock pin for serial interface.
BUF_IN	10	I	***Buffer Input:*** Single ended buffer input. 2.5V inout for DDR mode;3.3V for SDRAM mode.
FBOUT	1	O	***Feedback output:*** Output voltage depend on VDD3.3_2.5V.
PD # *	2	I	***Power Down Control:*** LVTTL compatible input that places the device in power down mode when held low. All pin tri-state. .(S/W option)
RESET_IN # *	2	I	***RESET in :*** LVTTL compatible input that places the device to initial state when held low.(S/W option)
DDR(0:5)T SDRAM(0, 2, 4, 6, 8, 10)	3, 7, 12 19, 23, 27	O	***True Clock of differential pair outputs or 3.3V SDRAM clock outputs:*** These outputs provide copies of BUF_IN. Voltage swing depends on VDD3.3_2.5 power supply.
DDR(0:5)C SDRAM(1, 3, 5, 7, 9, 11)	4, 8, 13, 18, 22, 26	O	***Complementary True Clock of differential pair outputs or 3.3V SDRAM clock outputs:*** These outputs provide complementary copies of BUF_IN depending on SEL_DDR input. Voltage swing depends on VDD3.3_2.5 power supply.
VDD3.3_2.5	5, 9, 14, 21, 25	P	***3.3V or 2.5V Power Connection:*** Connect to 2.5V power in DDR mode. Connect to 3.3V in SDRAM mode.
GND	6, 11, 17, 20, 24	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

Note: Internal 120K pull-up[*] or pull down[**] resistors present. Design should not rely solely on internal pull-up or pull down resistor to set I/O pins high or low respectively.

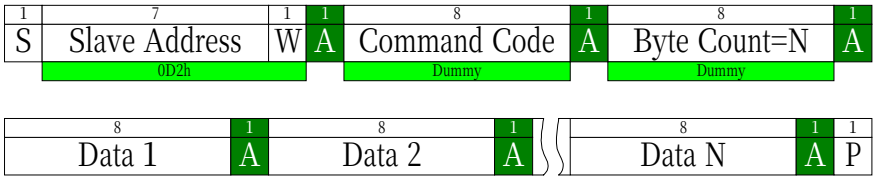
Functionality

Mode	PIN 48	VDD3.3_2.5	Pin 3, 4, 7, 8, 13, 14, 18, 19, 22, 23, 26, 27
DDR Mode	SEL_DDR=1	2.5V	These outputs will be DDR outputs
SDRAM Mode	SEL_DDR=0	3.3V	These outputs will be standard SDRAM outputs

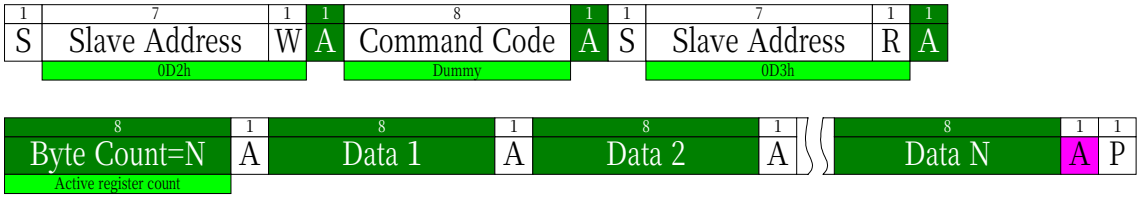
Standard Serial Bus Control:

Support standard serial bus block-mode and word-mode and ***direct word mode***.
Byte Count = 08h(CR10h.bit0=0) / 18h(CR10h.bit0=1) & ID = D2/D6
Direct-word-mode index = 1xxx-xxxx Binary (MSB=1)

The Block Mode:

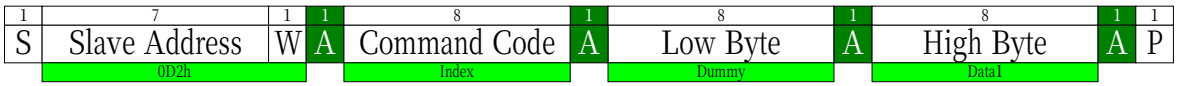


Block Write

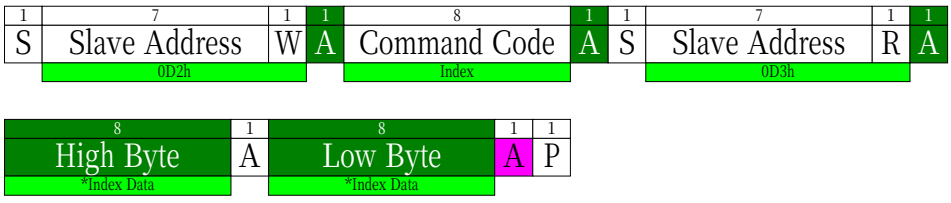


Block Read

The Word Mode:



Write Word



Read Word

Note slave address is D2h/D6h.

Register Description

CR 06h [6]				
Bit	**Description**	**PIN**	**Type**	**Default**
Bit7	0 = Select SDRAM 1 = Select DDR	48	R	PIN 48
Bit6	0 = Pin 36 select Power_Down# 1 = Pin 36 select RESET_IN#	36	R/W	1 Latched
Bit5	Reserved		R/W	1
Bit4	Reserved		R/W	1
Bit3	0 = DDR5T_SDRAM10 /DDR5C_SDRAM11 stop 1 = DDR5T_SDRAM10 /DDR5C_SDRAM11 running	27, 26	R/W	1
Bit2	Reserved		R/W	1
Bit1	0 = DDR4T_SDRAM8 /DDR4C_SDRAM9 stop 1 = DDR4T_SDRAM8 /DDR4C_SDRAM9 running	23, 22	R/W	1
Bit0	Reserved		R/W	1

CR 07h [7]				
Bit	**Description**	**PIN**	**Type**	**Default**
Bit7	Reserved		R/W	1
Bit6	0 = DDR3T_SDRAM6 /DDR3C_SDRAM7 stop 1 = DDR3T_SDRAM6 /DDR3C_SDRAM7 running	19, 18	R/W	1
Bit5	0 = DDR2T_SDRAM4 /DDR2C_SDRAM5 stop 1 = DDR4T_SDRAM4 /DDR4C_SDRAM5 running	12, 13	R/W	1
Bit4	Reserved		R/W	1
Bit3	Reserved		R/W	1
Bit2	0 = DDR1T_SDRAM2 /DDR1C_SDRAM3 stop 1 = DDR1T_SDRAM2 /DDR1C_SDRAM3 running	7, 8	R/W	1
Bit1	Reserved		R/W	1
Bit0	0 = DDR0T_SDRAM0 /DDR0C_SDRAM1 stop 1 = DDR0T_SDRAM0 /DDR0C_SDRAM1 running	3, 4	R/W	1

CR 08h			
Bit	**Description**	**TYPE**	**Default**
Bit7	Revision Code	R	1
Bit6	Revision Code	R	1
Bit5	Revision Code	R	1
Bit4	Revision Code	R	1
Bit3	Revision Code	R	0
Bit2	Revision Code	R	0
Bit1	Revision Code	R	0
Bit0	Revision Code	R	0

CR 10h [16]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Reserved	R/W	1
Bit6	Reserved	R/W	1
Bit5	Reserved	R/W	1
Bit4	Reserved	R/W	1
Bit3	Reserved	R/W	1
Bit2	Reserved	R/W	1
Bit1	0 = serial Bus block mode 1 = serial Bus word mode	R/W	0
Bit0	0 = Byte count is 008h 1 = Byte count is 018h	R/W	0

CR 23h [35]			
Bit	**Description**	**TYPE**	**Default**
Bit7	0 = DDR[0:2] / SDRAM[0:5] & Feedback drive strength normal 1 = DDR[0:2] / SDRAM[0:5] & Feedback drive strength 2X	R/W	0
Bit6	0 = DDR[3:5] / SDRAM[6:11] drive strength normal 1 = DDR[3:5] / SDRAM[6:11] drive strength 2X	R/W	0
Bit[5:4]	DDR/SDRAM (Pin 3, 4, 7, 8, 12, 13) output pin delay selection by 300 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]
Bit3	Reserved	R/W	1
Bit[2:1]	DDR/SDRAM (Pin 27, 26, 23, 22, 19, 18) output group delay selection by 300 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]
Bit0	Reserved	R/W	1

CR 24h [36]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:3]	Reserved	R/W	[11111]
Bit[2:1]	Feedback output pin delay selection by 300 ps base [00] 0 base delay [01] 1 base delay [10] 2 base delay [11] 3 base delay	R/W	[00]
Bit0	Reserved	R/W	1

CR 28h [40]			
Bit	**Description**	**TYPE**	**Default**
Bit[7:0]	Write CR28h with any value will reset CR10h bit 0, 1	W	**[1111_1111]**

CR 29h [41]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Cp_1 Base = 6.25 pF 0 = disconnect 1 = parallel Cp_1 with 6.25 pF	R/W	0
Bit6	0 = disconnect 1 = parallel Cp_1 with 6.25 pF	R/W	0
Bit5	0 = disconnect 1 = parallel Cp_1 with 6.25 pF	R/W	0
Bit4	0 = disconnect 1 = parallel Cp_1 with 6.25 pF	R/W	0
Bit3	I_1 Base = 10uA 0 = 1* I_1 (normal) 1 = 2* I_1	R/W	0
Bit2	0 = disconnect 1 = parallel I_1 with 40uA	R/W	1
Bit1	0 = disconnect 1 = parallel I_1 with 20uA	R/W	0
Bit0	0 = disconnect 1 = parallel I_1 with 10uA	R/W	0

CR 2ah [42]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Reserved	R/W	1
Bit[6:4]	Reserved	R/W	[111]
Bit3	C_{s1} Base = 25pF 0 = disconnect 1 = parallel C_{s1} with 100pF	R/W	1
Bit2	0 = disconnect 1 = parallel C_{s1} with PLL1 X – pF	R/W	1
Bit1	0 = disconnect 1 = parallel C_{s1} with MbiasY – pF	R/W	1
Bit0	0 = disconnect 1 = parallel C_{s1} with PLL2 Z – pF	R/W	1

CR 2bh [43]			
Bit	**Description**	**TYPE**	**Default**
Bit7	Reserved	R/W	1
Bit6	R_{S1} = 2000Ω base // R 2000Ω	R/W	0
Bit5	R_{S1} = 2000Ω base // R 2000Ω	R/W	0
Bit4	R_{S1} = 2000Ω base // R 2000Ω	R/W	0
Bit3	R_{S1} = 2000Ω base // R 2000Ω	R/W	0
Bit2	R_{S1} = 2000Ω base // R 2000Ω	R/W	0
Bit1	R_{S1} = 2000Ω base // R 2000Ω	R/W	0
Bit0	R_{S1} = 2000Ω base // R 2000Ω	R/W	0

CR 2ch [44]				
Bit	**Description**	**PIN**	**Type**	**Default**
Bit7	Reserved		R/W	1
Bit6	0 = disable PLL1 OPAMP 1 = enable PLL1 OPAMP		R/W	0
Bit[5:4]	Phase detector frequency (unusing stop) 00 = /1 01 = /2 10 = /4 11 = /6		R/W	[00]
Bit[3:2]	Reserved		R/W	[11]
Bit[1:0]	Reserved		R/W	[11]

Electrical Characteristics - Input/Supply/Common Output Parameters

TA = 0 - 85C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	IIH	VI = VDD or GND				µA
Input Low Current	IIL	VI = VDD or GND				µA
Operating Supply Current	IDD2.5	CL = 0pf				mA
Operating Supply Current	IDDPD	CL = 0pf			100	uA
Output High Current	IOH	VDD = 2.3V, VOUT = 1V	-18			mA
Output Low Current	IOL	VDD = 2.3V, VOUT = 1.2V	26			mA
High Impedance Output Current	IOZ	VDD=2.7V, Vout=VDD or GND			±10	uA
Input Clamp Voltage	VIK	Iin = -18mA				V
High-level output voltage	VOH	VDD = min to max, IOH = -1 mA				V
High-level output voltage	VOH	VDD = 2.3V, IOH = -12 mA				V
Low-level output voltage	VOL	VDD = min to max, IOL =1 mA			0.1	V
Low-level output voltage	VOL	VDD = 2.3V, IOH=12 mA			0.6	V
Input Capacitance	CIN	VI = GND or VDD		2		pF
Output Capacitance	COUT	VOUT = GND or VDD		3		pF

Recommended Operating Condition

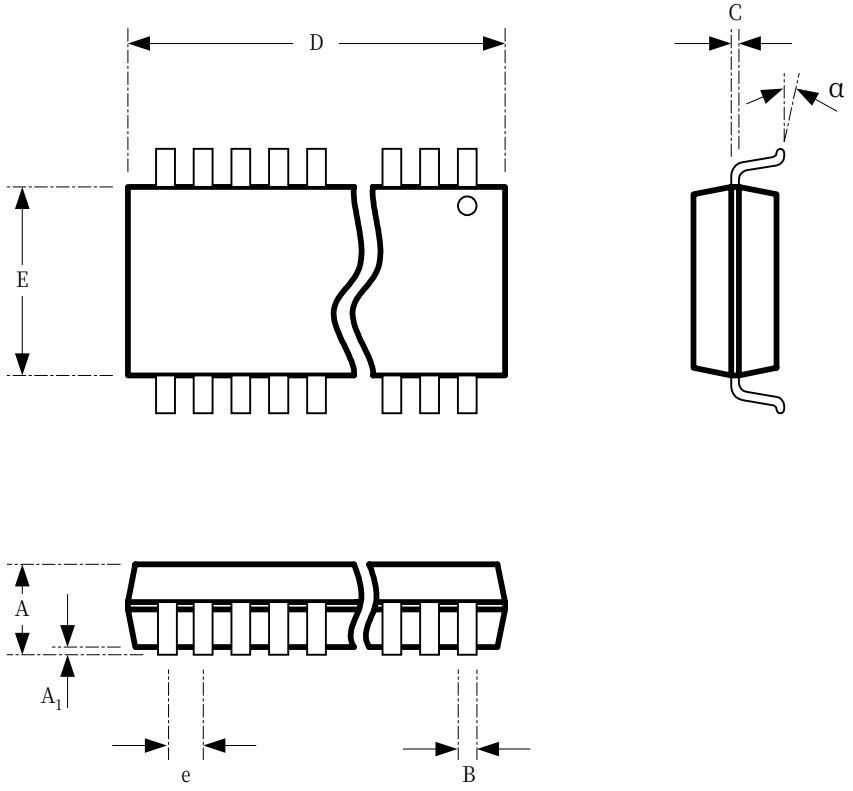
TA = 0 - 85C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog/core supply voltage	AVDD		2.3	2.5	2.7	V
Input High Voltage	VIH	OE input				V
Input Low Voltage	VIL	OE input				V
Input voltage level	VIN					V
Input differential-pair crossing voltage	VIC					V
Output differential-pair crossing voltage	VOC					V

Switching Characteristics

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Maximum Operating Frequency			66		200	MHz
Input clock duty cycle	Dtin		40		60	%
Output to Output Skew	Tskew				100	ps
Pulse skew	Tskewp				100	ps
Duty cycle	DC	66 MHz to 100 MHz	48		52	%
Duty cycle	DC	101 MHz to 167 MHz	47		53	%
Rise Time, Fall Time	tr, tf	Load = 120 ohm / 16pF	650		950	ps
SDRAM Buffer LH Prop. Delay		Input edge greater than 1V/ns				ns
SDRAM Buffer HL Prop. Delay		Input edge greater than 1V/ns				ns
SDRAM Buffer Enable Delay		Input edge greater than 1V/ns				ns
SDRAM Buffer Disable Delay		Input edge greater than 1V/ns				ns

Package outline



SSOP Package:(unit using inches)

Symbol	Common Dimensions			Variations	D			N
	Min.	Type	Max.		Min.	Type	Max.	
A	0.068	0.073	0.078	AE	0.397	0.402	0.407	28
A1	0.002	0.005	0.008					
B	0.008	0.010	0.0135					
C	0.004	0.0060	0.008					
D	See Variations							
E	0.205	0.209	0.212					
e	0.025BSC							
α	0°	4°	8°					

Demo board circuit: