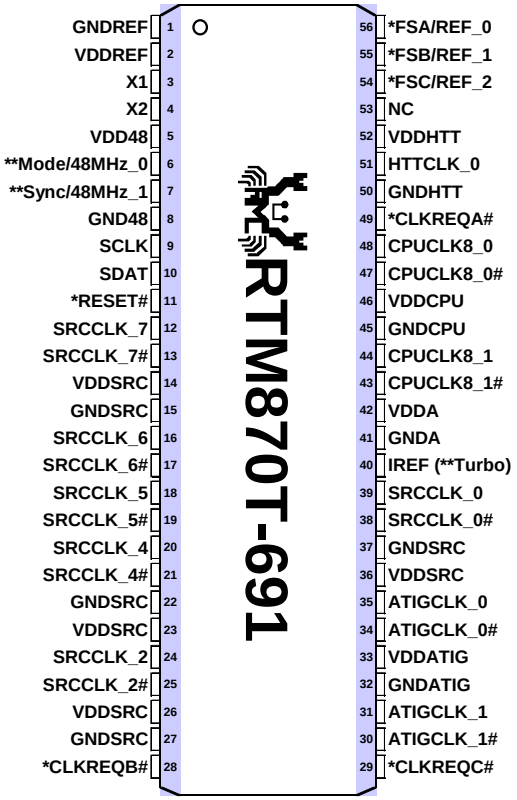
General Description

RTM870T-691 is a TSSOP56 low power main clock for ATI RS600 system using AMD K8 processors & SB600 Southbridge



Output Features:

- 3 – REF clock
- 2 – USB 48MHz clock
- 1 – Hyper Transport 66MHz clock seed
- 6 – 0.8V push-pull differential SRCCLK pairs
- 2 – 0.8V push-pull differential ATIGCLK pairs
- 2– 3.3V push-pull differential CPUCLK pairs

AC Specifications:

- CPUCLK outputs Cycle-to-Cycle jitter < 100ps
- SRCCLK outputs Cycle-to-Cycle jitter < 125ps
- ATIGCLK outputs Cycle-to-Cycle jitter < 125ps
- REF outputs Cycle-to-Cycle jitter < 200ps
- HTT outputs Cycle-to-Cycle jitter < 180ps
- 48MHz USB outputs Cycle-to-Cycle jitter < 130ps
- +/- 300ppm Frequency accuracy on CPU, SRC, ATIG clocks

Option Function

Mode(PIN6)	PIN40
0	NC
1	Turbo

Application Features:

- 3 – Clock Request pins for SRC and ATIG clocks
- Spread Spectrum for EMI reduction
- Outputs controllable by SMBus

SRC Output Control

	Control REQ# Register	
REQ#	0(default)	1
0	by register	enable
1(default)	by register	disable

Frequency Table

FSC	FSB	FSA	CPU	HTT	SRC	ATIG	USBI	SSC
0	0	0	266.67	66.66	100.00	100.00	48.00	+/- 0.25%
0	0	1	133.33	66.66	100.00	100.00	48.00	+/- 0.25%
0	1	0	200.00	66.66	100.00	100.00	48.00	+/- 0.25%
0	1	1	166.67	66.66	100.00	100.00	48.00	+/- 0.25%
1	0	0	333.33	66.66	100.00	100.00	48.00	+/- 0.25%
1	0	1	100.00	66.66	100.00	100.00	48.00	+/- 0.25%
1	1	0	400.00	66.66	100.00	100.00	48.00	+/- 0.25%
1	1	1	200.00	66.66	100.00	100.00	48.00	+/- 0.25%

Pin Description

In order to reduce pin counts, and therefore package size and cost, some pins have multiple functions. In those cases, the functions are separated with a "/" symbol. Refer to the 'Pin Assignment' diagram for a graphical representation.

Pin	Pin Name	Type	Description
1	GNDREF	G	GND pin.
2	VDDREF	P	3.3V power supply
3	X1	I	Crystal Input: external 14.318MHz crystal connection.
4	X2	O	Crystal output: external 14.318MHz crystal connection.
5	VDD48	P	3.3V power supply
6	48MHz_0	O	3.3V 48MHz clock output.
	**Mode	I	Option Function for Turbo mode. *150K pull-down*
7	48MHz_1	O	3.3V 48MHz clock output.
	**Sync	I	Latch input pin whether PCIE are synchronous with CPU: 1: PCIEX clocks are synchronous with CPU / ATIG clocks are asynchronous with CPU. 0: PCIEX clocks are asynchronous with CPU / ATIG clocks are synchronous with CPU.
8	GND48	G	GND pin.
9	SCLK	I	Clock pin of SMBus circuitry
10	SDAT	I/O	Data pin of SMBus circuitry
11	RESET#	I	Real time active low input. When active, FS inputs are relatched and the SMBus is reset.*150K pull-up*
12	SRCCLK_7	O	True clock of differential SRC clock pair
13	SRCCLK_7#	O	Complement clock of differential SRC clock pair
14	VDDSRC	P	3.3V power supply
15	GNDSRC	G	GND pin.
16	SRCCLK_6	O	True clock of differential SRC clock pair
17	SRCCLK_6#	O	Complement clock of differential SRC clock pair
18	SRCCLK_5	O	True clock of differential SRC clock pair
19	SRCCLK_5#	O	Complement clock of differential SRC clock pair
20	SRCCLK_4	O	True clock of differential SRC clock pair
21	SRCCLK_4#	O	Complement clock of differential SRC clock pair
22	GNDSRC	G	GND pin.
23	VDDSRC	P	3.3V power supply
24	SRCCLK_2	O	True clock of differential SRC clock pair
25	SRCCLK_2#	O	Complement clock of differential SRC clock pair
26	VDDSRC	P	3.3V power supply
27	GNDSRC	G	GND pin.
28	*CLKREQ_B#	I	Output enable for SRC outputs. SMBus selects which outputs are controlled 0 = enabled, 1 = tri-stated *150K pull-up*

Note1. * Symbol stands for an internal 150KΩ pull-up resistor.

Note2. ** Symbol stands for an internal 150KΩ pull-down resistor.

Pin Description (Continued)

Pin	Pin Name	Type	Description
29	*CLKREQ_C#	I	Output enable for SRC outputs. SMBus selects which outputs are controlled 0 = enabled, 1 = tri-stated *150K pull-up*
30	ATIGCLK_1#	O	Complement clock of differential ATIG clock pair
31	ATIGCLK_1	O	True clock of differential ATIG clock pair
32	GNDATIG	G	GND pin.
33	VDDATIG	P	3.3V power supply
34	ATIGCLK_0#	O	Complement clock of differential ATIG clock pair
35	ATIGCLK_0	O	True clock of differential ATIG clock pair
36	VDDSRC	P	3.3V power supply
37	GNDSRC	G	GND pin.
38	SRCCLK_0#	O	Complement clock of differential SRC clock pair
39	SRCCLK_0	O	True clock of differential SRC clock pair
40	IREF	N/A	NC
	**Turbo	I	Turbo function*150K pull-down*
41	GNDA	G	GND pin.
42	VDDA	P	3.3V power supply
43	CPUCLK8_1#	O	Complement clock of differential CPU clock pair. These are 3.3V push-pull model outputs.
44	CPUCLK8_1	O	True clock of differential CPU clock pair. These are 3.3V push-pull model outputs.
45	GNDCPU	G	GND pin.
46	VDDCPU	P	3.3V power supply
47	CPUCLK8_0#	O	Complement clock of differential CPU clock pair. These are 3.3V push-pull model outputs.
48	CPUCLK8_0	O	True clock of differential CPU clock pair. These are 3.3V push-pull model outputs.
49	*CLKREQ_A#	I	Output enable for SRC outputs. SMBus selects which outputs are controlled 0 = enabled, 1 = tri-stated *150K pull-up*
50	GNDHTT	G	GND pin.
51	HTTCLK_0	I	3.3V Hyper Transport output
52	VDDHTT	P	3.3V power supply
53	NC	N/A	No Connection
54	*FSC	I	Frequency selection. *150K pull-up (Trigger level Logic 0 <0.35mV, Logic 1 > 0.7mV)*
	REF2	O	14.318MHz reference clock.
55	*FSB	I	Frequency selection. *150K pull-up (Trigger level Logic 0 <0.35mV, Logic 1 > 0.7mV)*
	REF1	O	14.318MHz reference clock.
56	*FSA	I	Frequency selection. *150K pull-up (Trigger level: Logic 0 <0.35mV, Logic 1 > 0.7mV)*
	REF0	O	14.318MHz reference clock.

Note1. * Symbol stands for an internal 150KΩ pull-up resistor.

Note2. ** Symbol stands for an internal 150KΩ pull-down resistor.

Pin Description (Continued)

Address CR 00h [0] Output Control (FF)				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	Reserved	-	R/W	1
Bit6	0 = CPUCLK8_1 Output Disable 1 = CPUCLK8_1 Output Enable	47,48	R/W	1
Bit5	0 = CPUCLK8_0 Output Disable 1 = CPUCLK8_0 Output Enable	43,44	R/W	1
Bit4	0 = HTTCLK_0 Output Disable 1 = HTTCLK_0 Output Enable	51	R/W	1
Bit3	Reserved	-	R/W	1
Bit2	0 = ATIGCLK_1 Output Disable 1 = ATIGCLK_1 Output Enable	30,31	R/W	1
Bit1	0 = ATIGCLK_0 Output Disable 1 = ATIGCLK_0 Output Enable	34,35	R/W	1
Bit0	Reserved	-	R/W	1

Address CR 01h [1] Output Control (FF)				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	0 = 48MHz_1 Output Disable 1 = 48MHz_1 Output Enable	6	R/W	1
Bit6	0 = 48MHz_0 Output Disable 1 = 48MHz_0 Output Enable	7	R/W	1
Bit5	0 = REF2 Output Disable 1 = REF2 Output Enable	54	R/W	1
Bit4	0 = REF1 Output Disable 1 = REF1 Output Enable	55	R/W	1
Bit3	0 = REF0 Output Disable 1 = REF0 Output Enable	56	R/W	1
Bit2	*FS C power-on latched	54	R	Latched
Bit1	*FS B power-on latched	55	R	Latched
Bit0	*FS A power-on latched	56	R	Latched

Address CR 02h [2] Output Control (FF)				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	0 = SRCCLK_7 Output Disable 1 = SRCCLK_7 Output Enable	12,13	R/W	1
Bit6	0 = SRCCLK_6 Output Disable 1 = SRCCLK_6 Output Enable	16,17	R/W	1
Bit5	0 = SRCCLK_5 Output Disable 1 = SRCCLK_5 Output Enable	18,19	R/W	1
Bit4	0 = SRCCLK_4 Output Disable 1 = SRCCLK_4 Output Enable	20,21	R/W	1
Bit3	Reserved	-	R/W	1
Bit2	0 = SRCCLK_2 Output Disable 1 = SRCCLK_2 Output Enable	24,25	R/W	1
Bit1	Reserved	-	R/W	1
Bit0	0 = SRCCLK_0 Output Disable 1 = SRCCLK_0 Output Enable	38,39	R/W	1

Address CR 03h [3] Output Control (00)				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	CLKREQ_A# Controls SRCCLK_7 0 = Does not control 1 = Controls	12,13	R/W	0
Bit6	CLKREQ_A# Controls SRCCLK_6 0 = Does not control 1 = Controls	16,17	R/W	0
Bit5	CLKREQ_A# Controls SRCCLK_5 0 = Does not control 1 = Controls	18,19	R/W	0
Bit4	CLKREQ_A# Controls SRCCLK_4 0 = Does not control 1 = Controls	20,21	R/W	0
Bit3	Reserved	-	R/W	0
Bit2	CLKREQ_B# Controls SRCCLK_2 0 = Does not control 1 = Controls	24,25	R/W	0
Bit1	Reserved	-	R/W	0
Bit0	CLKREQ_B# Controls SRCCLK_0 0 = Does not control 1 = Controls	38,39	R/W	0

Address CR 04h [4] Output Control (00)				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	Reserved	-	R/W	0
Bit6	CLKREQ_C# Controls ATIGCLK_1 0 = Does not control 1 = Controls	30,31	R/W	0
Bit5	CLKREQ_C# Controls ATIGCLK_0 0 = Does not control 1 = Controls	34,35	R/W	0
Bit4	Reserved	-	R/W	0
Bit[3:0]	Reserved	-	R/W	0000

Address CR 05h [5] Output Control (00)				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit[7:4]	Resvered	-	R/W	0000
Bit3	Differential Ouptut Disable Mode of CPUCLK1 0 = Driven 1 = Hi-Z	-	R/W	0
Bit2	Differential Ouptut Disable Mode of CPUCLK0 0 = Driven 1 = Hi-Z	-	R/W	0
Bit1	Reserved	-	R/W	0
Bit0	Differential Ouptut Disable Mode of SRCCLK[7:0] and ATIGCLK[3:0] 0 = Driven 1 = Hi-z	-	R/W	0

Address CR 06h [6] (61)					
Bit	**Description**		**Pin**	**Type**	**Default**
Bit7	Device ID7 (MSB)	DEVICE ID	-	R	0
Bit6	Device ID6		-	R	1
Bit5	Device ID5		-	R	1
Bit4	Device ID4		-	R	0
Bit3	Device ID3		-	R	0
Bit2	Device ID2		-	R	0
Bit1	Device ID1		-	R	0
Bit0	Device ID0 (LSB)		-	R	1

Address CR 07h [7] (1E)				
Bit	**Description**	**Pin**	**Type**	**Default**
Bit7	Revision Code	-	R	0
Bit6	Revision Code	-	R	0
Bit5	Revision Code	-	R	0
Bit4	Revision Code	-	R	1
Bit3	Vender Code	-	R	1
Bit2	Vender Code	-	R	1
Bit1	Vender Code	-	R	1
Bit0	Vender Code	-	R	0

Address CR 08h [8] Frequency table (00)

Bit	Description	Type	Default
Bit7	0 = frequency is selected by CR08h [5:0] disable 1 = frequency is selected by CR08h [5:0] enable	R/W	0
Bit6	Mode power-on latched (Pin_6) '0'(default) = Pin48 => NC, Pin64 => REF0 '1' = Pin48 => Turbo, Pin64 => REF0	R/W	0
Bit5	0 = SRC is asynchronous with CPU (PLL3) 1 = SRC is synchronous with CPU (PLL1)	R	0

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	HTT	SRC	ATIG	USB	SSC	
0	0	0	0	0	266.67	66.66	100.00	100.00	48.00	+/- 0.25%	
0	0	0	0	1	133.33	66.66	100.00	100.00	48.00	+/- 0.25%	
0	0	0	1	0	200.00	66.66	100.00	100.00	48.00	+/- 0.25%	
0	0	0	1	1	166.67	66.66	100.00	100.00	48.00	+/- 0.25%	
0	0	1	0	0	333.33	66.66	100.00	100.00	48.00	+/- 0.25%	
0	0	1	0	1	100.00	66.66	100.00	100.00	48.00	+/- 0.25%	
0	0	1	1	0	400.00	66.66	100.00	100.00	48.00	+/- 0.25%	
0	0	1	1	1	200.00	66.66	100.00	100.00	48.00	+/- 0.25%	
0	1	0	0	0	269.33	67.33	100.00	101.00	48.00	+/- 0.25%	
0	1	0	0	1	134.67	67.33	100.00	101.00	48.00	+/- 0.25%	
0	1	0	1	0	202.00	67.33	100.00	101.00	48.00	+/- 0.25%	
0	1	0	1	1	168.33	67.33	100.00	101.00	48.00	+/- 0.25%	
0	1	1	0	0	336.67	67.33	100.00	101.00	48.00	+/- 0.25%	
0	1	1	0	1	101.00	67.33	100.00	101.00	48.00	+/- 0.25%	
0	1	1	1	0	404.00	67.33	100.00	101.00	48.00	+/- 0.25%	
0	1	1	1	1	202.00	67.33	100.00	101.00	48.00	+/- 0.25%	
1	0	0	0	0	266.90	66.73	100.00	100.09	48.00	+/- 0.25%	
1	0	0	0	1	133.90	66.97	100.00	100.45	48.00	+/- 0.25%	
1	0	0	1	0	200.90	66.97	100.00	100.45	48.00	+/- 0.25%	
1	0	0	1	1	166.90	66.76	100.00	100.10	48.00	+/- 0.25%	
1	0	1	0	0	333.90	66.78	100.00	100.17	48.00	+/- 0.25%	
1	0	1	0	1	100.90	67.27	100.00	100.17	48.00	+/- 0.25%	
1	0	1	1	0	400.90	66.82	100.00	100.23	48.00	+/- 0.25%	
1	0	1	1	1	200.90	66.97	100.00	100.45	48.00	+/- 0.25%	
1	1	0	0	0	274.67	68.67	100.00	103.00	48.00	+/- 0.25%	
1	1	0	0	1	137.33	68.67	100.00	103.00	48.00	+/- 0.25%	
1	1	0	1	0	206.00	68.67	100.00	103.00	48.00	+/- 0.25%	
1	1	0	1	1	171.67	68.67	100.00	103.00	48.00	+/- 0.25%	
1	1	1	0	0	343.33	68.67	100.00	103.00	48.00	+/- 0.25%	
1	1	1	0	1	103.00	68.67	100.00	103.00	48.00	+/- 0.25%	
1	1	1	1	0	412.00	68.67	100.00	103.00	48.00	+/- 0.25%	
1	1	1	1	1	206.00	68.67	100.00	103.00	48.00	+/- 0.25%	

Bit4 0
Bit3 0
Bit2 0
Bit1 0
Bit0 0

Address CR 09h [9] PLL1/3 SSC control (66)			
Bit	**Description**	**Type**	**Default**
Bit7	Reserved	R/W	0
Bit6	0 = PLL1 spread spectrum is disable 1 = PLL1 spread spectrum is enable	R/W	1
Bit[5:4]	PLL1 SSC range control 00 = - 0.5% 01 = - 1.0% 10 = +/- 0.25% 11 = +/- 0.5%	R/W	10
Bit3	Reserved	R/W	0
Bit2	0 = PLL3 spread spectrum is disable 1 = PLL3 spread spectrum is enable	R/W	1
Bit[1:0]	PLL3 SSC range control 00 = - 0.5% 01 = - 1.0% 10 = +/- 0.25% 11 = +/- 0.5%	R/W	10

Address CR 0ah [10] Low power PAD control (44)			
Bit	**Description**	**Type**	**Default**
Bit7	Reserved	R/W	0
Bit[6:4]	Reserved	R/W	100
Bit3	Reserved	R/W	0
Bit[2:0]	ATIG[3:0] / SRC[7:0] LP pad swing control. 000 = 600mV 001 = 650mV 010 = 700mV 011 = 750mV 100 = 800mV 101 = 850mV 110 = 900mV 111 = 950mV	R/W	100

Address CR 0bh [11] Low power PAD control (CF)			
Bit	**Description**	**Type**	**Default**
Bit7	Reserved	R/W	1
Bit6	0 = ATIG[3:0] slew rate 1.00X 1 = ATIG[3:0] slew rate 2.00X	R/W	1
Bit[5:4]	00 = CPU_K8 driven strength 1.00X 01 = CPU_K8 driven strength 1.25X 10 = CPU_K8 driven strength 1.50X 11 = CPU_K8 driven strength 2.00X	R/W	00
Bit3	0 = SRC[7:4] slew rate 1.00X 1 = SRC[7:4] slew rate 2.00X	R/W	1
Bit2	0 = SRC[3:0] slew rate 1.00X 1 = SRC[3:0] slew rate 2.00X	R/W	1
Bit1	0 = All LP PAD driving 1.00X 0 = All LP PAD driving 2.00X	R/W	1
Bit0	0 = Reset_reset in = Reset out 1 = Reset_reset in = Reset in	R/W	1

Address CR 0ch [12] Turbo control (00)			
Bit	**Description**	**Type**	**Default**
Bit[7:5]	Reserved	R/W	000
Bit4	Turbo-0 pin flag status 0 = Turbo-0 disable 1 = Turbo-0 enable	R	monitor
Bit[3:1]	RESERVED	R/W	000
Bit0	Turbo mode control 0 = Turbo-0 disable 1 = Turbo-0 enable	R/W	0

Turbo	PLL1	PLL3	Remark
0	ROM CR11/13h	CR12/13h	Power-on Default / Normal Programmable
1	CR0d/0eh	CR0fh	Program Turbo

Address CR 0dh [13] Turbo PLL1 VCO (02)			
Bit	**Description**	**Type**	**Default**
Bit[7:2]	RESERVED	R/W	0000-00
Bit[1:0]	PLL1 Turbo VCO_1 code[6:5]	R/W	10

Address CR 0eh [14] Turbo PLL1 VCO (80)			
Bit	**Description**	**Type**	**Default**
Bit[7:3]	PLL1 Turbo VCO_1 code bit[4:0]	R/W	1000-0
Bit[2:0]	PLL1 Turbo VCO_2 code bit[3:1]	R/W	000

Address CR 0fh [15] Turbo PLL3 VCO (A0)			
Bit	**Description**	**Type**	**Default**
Bit[7:1]	PLL3 Turbo VCO_1 code bit[6:0]	R/W	1010-000
Bit[0]	PLL3 Turbo VCO_2 code bit[3]	R/W	0

Address CR 10h [16] (50)			
Bit	**Description**	**Type**	**Default**
Bit[7:4]	Watch dog tmer [base =0.5 second] T = (bit[7:4] +2) * base second	R/W	0101
Bit3	Reset on command issued flag: 0 = normal 1 = alarmed	R	0
Bit2	0 = normal 1 = watch dog enable. Action is internal reset & external reset	R/W	0
Bit1	Mass-production test mode 0 = normal 1 = enable Watch Dog timer base =1u second, RESET# pulse = 1uS (PLL2 ->200MHz)	R/W	0
Bit0	Watch dog issued flag: 0 = normal 1 = alarmed	R	0

Address CR 11h [17] PLL1 VCO-code_1 (50)			
Bit	**Description**	**Type**	**Default**
Bit7	Reserved	R/W	0
Bit[6:0]	VCO code_1 bit[7:0] of PLL1 PLL1 VCO = PLL1 VCO code_1 * 10 + PLL1 VCO code_2	R/W	101-0000

Address CR 12h [18] PLL3 VCO-code_1 (50)			
Bit	**Description**	**Type**	**Default**
Bit7	Reserved	R/W	0
Bit[6:0]	VCO code_1 bit[7:0] of PLL3 PLL3 VCO = PLL3 VCO code_1 * 10 + PLL3 VCO code_2	R/W	101-0000

Address CR 13h [19] PLL1/3 VCO-code_2 (00)			
Bit	**Description**	**Type**	**Default**
Bit[7:4]	VCO code_2 PLL1 PLL1 VCO = PLL1 VCO code_1 * 10 +PLL1 VCO code_2	R/W	0000-0
Bit[3:0]	VCO code_2 PLL3 PLL3 VCO = PLL3 VCO code_1 * 10 +PLL3 VCO code_2	R/W	000

Address CR 14h [20] Group delay control (00)			
Bit	**Description**	**Type**	**Default**
Bit[7:4]	Reserved	R/W	0000
Bit[3:0]	HTT group delay selection by 75 ps base	R/W	0000

Address CR 15h [21] Group delay control (00)			
Bit	**Description**	**Type**	**Default**
Bit[7:4]	CPU-0 group delay selection by 75 ps base	R/W	0000
Bit[3:0]	CPU-1 group delay selection by 75 ps base	R/W	0000

Skew delay = base x (delay-selection)

Address CR 16h [22] Group delay control (00)			
Bit	**Description**	**Type**	**Default**
Bit[7:4]	Reserved	R/W	0000
Bit[3:0]	SRC[7:0] group delay selection by 75 ps base	R/W	0000

Skew delay = base x (delay-selection)

Address CR 17h [23] Group delay control (00)			
Bit	**Description**	**TYPE**	**Default**
Bit[7:6]	00 = HTT duty positive duty = 50% 01 = HTT duty positive duty = 48.3% 10 = HTT duty positive duty = 47.8% 11 = HTT duty positive duty = 46.7%	R/W	00
Bit[5:4]	Reserved	R/W	00
Bit[3:0]	ATIG[3:0] delay selection by 75 ps base	R/W	0000

Skew delay = base x (delay-selection)

Address CR 18h [24] PLL2 M code (00)			
Bit	**Description**	**Type**	**Default**
Bit[7:0]	reserved	R/W	0000-0000

Address CR 19h [25] PLL2 M/N code (00)			
Bit	**Description**	**Type**	**Default**
Bit[7:0]	reserved	R/W	0000-0000

Address CR 1ah [26] (A0)			
Bit	**Description**	**Type**	**Default**
Bit[7:6]	00 = 48MHz[1:0] PAD driving 1.00X 01 = 48MHz[1:0] PAD driving 1.25X 10 = 48MHz[1:0] PAD driving 1.50X 11 = 48MHz[1:0] PAD driving 2.00X	R/W	10
Bit[5:4]	00 = HTT PAD driving 1.00X 01 = HTT PAD driving 1.25X 10 = HTT PAD driving 1.50X 11 = HTT PAD driving 2.00X	R/W	10
Bit[3:2]	00 = REF[2:0] PAD driving 1.00X 01 = REF[2:0] PAD driving 1.25X 10 = REF[2:0] PAD driving 1.50X 11 = REF[2:0] PAD driving 2.00X	R/W	00
Bit[1:0]	Reserved	R/W	00

Address CR 1bh [27] (A8)			
Bit	**Description**	**Type**	**Default**
Bit[7:6]	00 = 48MHz[1:0] slew rate 1.00X 01 = 48MHz[1:0] slew rate 1.25X 10 = 48MHz[1:0] slew rate 1.50X 11 = 48MHz[1:0] slew rate 2.00X	R/W	10
Bit[5:4]	00 = HTT slew rate 1.00X 01 = HTT slew rate 1.25X 10 = HTT slew rate 1.50X 11 = HTT slew rate 2.00X	R/W	10
Bit[3:2]	00 = REF[2:0] slew rate 1.00X 01 = REF[2:0] slew rate 1.25X 10 = REF[2:0] slew rate 1.50X 11 = REF[2:0] slew rate 2.00X	R/W	10
Bit[1:0]	Reserved	R/W	00

Address CR 1ch [28] Divider MUX suspend power (40)			
Bit	**Description**	**TYPE**	**Default**
Bit7	Reserved	R	0
Bit[6:4]	CPU divider 000 = PLL1/2 001 = PLL1/3 010 = PLL1/4 011 = PLL1/6 100 = PLL1/8 101 = PLL1/5 110 = Reserved 111 = Reserved	R/W	100
Bit3	Reserved	R	0
Bit[2:0]	HTT divider 000 = PLL1/12 001 = PLL1/15 010 = PLL3/12 011 = PLL2/4.5 fix66 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved	R/W	000

Address CR 1dh [29] Divider MUX suspend power (02)			
Bit	**Description**	**TYPE**	**Default**
Bit7	Reserved	R/W	0
Bit[6:4]	ATIG divider 000 = PLL1/8 001 = PLL1/10 010 = PLL3/8 011 = PLL2/3 fix100 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved	R/W	000
Bit3	Reserved	R/W	0
Bit[2:0]	SRC divider 000 = PLL1/8 001 = PLL1/10 010 = PLL3/8 011 = PLL2/3 fix100 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved	R/W	010

Address CR 1eh [30] Divider MUX suspend power (00)			
Bit	**Description**	**TYPE**	**Default**
Bit[7:5]	Reserved	R/W	000
Bit4	Test mode 0 = USB48 1 = 24MHz	R/W	0
Bit[3:1]	Reserved	R/W	000
Bit0	0 = disable last serial SMBus write latched with reset# output 1 = enable last serial SMBus write latched with reset# output	R/W	0

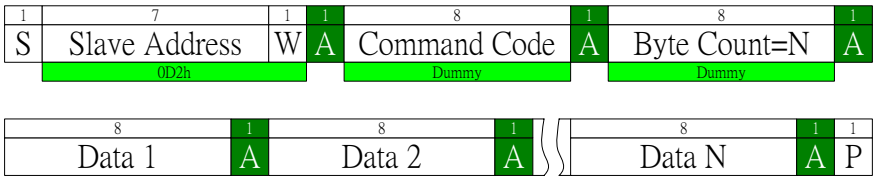
Address CR 1fh [31] (00)			
Bit	**Description**	**TYPE**	**Default**
Bit7	reserved	R/W	0
Bit6	0 = SRC select nomal phase 1 = SRC select inverse phase	R/W	0
Bit5	0 = ATIG select nomal phase 1 = ATIG select inverse phase	R/W	0
Bit4	0 = HTT select nomal phase 1 =HTT select inverse phase	R/W	0
Bit3	Reserved	R/W	0
Bit2	(PLL3 VCO latch enable) 0=PLL3 programmable disable 1=PLL3 programmable enable & latching	R/W	0
Bit1	0 = Divider select by ROM 1 = Divider select by REG , divider code& clock phase select latching buffer while writen 1	R/W	0
Bit0	(PLL1 VCO-code mode) 0=PLL1 programmable disable and from ROM code 1=PLL1 programmable enable & latching	R/W	0

Divider switch must glitch-free

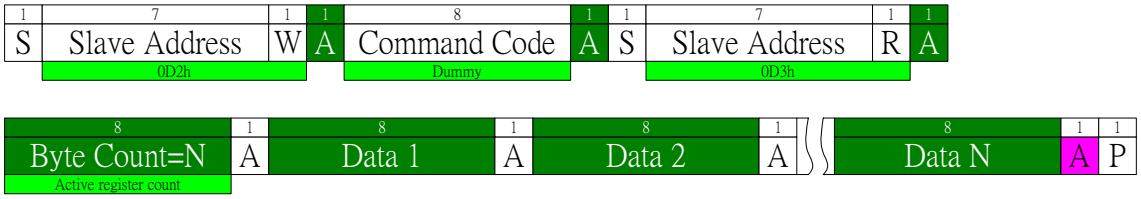
Functionality

Standard Serial Bus Control:
Support standard serial bus block-mode and direct word-mode.
Byte Count = 020h
Direct-word-mode index = 1xxx-xxxx Binary (MSB=1)

Block Mode

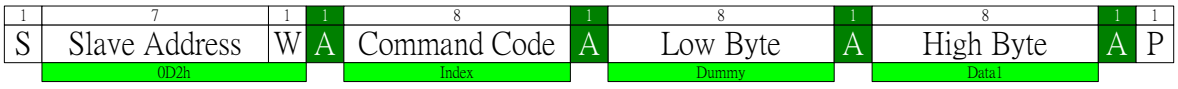


Block Write

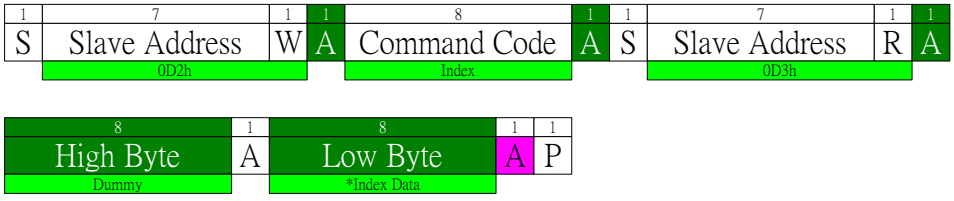


Block Read

Word Mode



Write Word



Read Word

Note: slave address is D2h.

Electrical Characteristics

DC Specifications

Symbol	Parameter	Minimum	Maximum	Units	Notes
Absolute VDD A	3.3V core supply Voltage	**-0.5**	4.6	V	
Absolute VDD I/O	3.3V I/O supply Voltage	**-0.5**	4.6	V	
Ts	Storage Temperature	-65	150	℃	
Ta	Ambient Temperature	0	70	℃	
Absolute Vih	3.3V input high voltage	-0.5	4.6	V	
Absolute Vil	3.3V input low voltage	-0.5		V	
Operating Vih_FS	3.3V input high voltage	0.7	Vdd+0.3	V	
Operating Vil_FS	3.3V input low voltage	Vss-0.3	0.35	V	
ESD	Input ESD protection	2000		V	Human body mode
Operating Vdd A	3.3V core s upply Voltage	**3.135**	3.465	V	
Operating Vdd I/O	3.3V I/O supply Voltage	**3.135**	3.465	V	
Operating Vih	3.3V input high voltage	2.0	Vdd+0.3	V	
Operating Vil	3.3V input low voltage	Vss-0.3	0.8	V	
Operating Iil	Input leakage current	-5	+5	μA	
Operating Voh	3.3V output high voltage	2.4		V	I_{OH}=-1mA
Operating Vol	3.3V output low voltage		0.4	V	I_{OL}=1mA
Cin	Input pin capacitance	3	5	pF	
Cxtal	XTAL pin capacitance	3	5	pF	17~20 pF
Cout	Output pin capacitance		6	pF	
Lpin	Pin inductance		7	nH	

AC Specifications

CPU 3.3V

T_A = 0~ 70℃, CPU V_{OUT} =0.7 V, V_{OL}=0.14V, V_{OH}=0.56V, Test load: R_S=33Ω,R_P=49.9Ω,C_L=2pF

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Frequency		200MHZ		200		MHz
Output Impedance			15	35	55	
Rising edge		Measured at AMD64 processor's test load +/- 400mV (differential measurement)	2		10	V/ns
Falling edge			2		10	V/ns
Differential Voltage	V_{DIFF}	Measured at AMD64 processor's test load +/- 400mV (single-ended measurement)	0.4	1.25	2.3	V
Change in V_{DIFF_DC} Magnitude	$\triangle V_{DIFF}$		-150		150	mV
Command Mode Voltage	V_{CM}		1.05	1.25	1.45	V
V low	$\triangle V_{CM}$		-200		200	mV
Duty Cycle		Measurement taken from differential waveform	45		53	%
Group Skew		Measurement taken from differential waveform			250	ps
Cycle-to-Cycle Jitter		Measurement taken from differential waveform	0	100	200	ps

PCIE 0.7V

T_A = 0 ~ 70℃, CPU V_{OUT} =0.7 V, V_{OL}=0.14V, V_{OH}=0.56V, Test load: R_S=33Ω,R_P=49.9Ω,C_L=2pF

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Frequency				100		MHz
Output Impedance			3000			
Overshoot Voltage					VH+0.3	V
Undershoot Voltage			-0.3			V
Rising edge ring back					0.2	V
Falling edge ring back					0.2	V
Output High Current				6*Iref		mA
Output Low Current				0		mA
V high			660	700	850	mV
V low			-150	0		mV
V cross			250		550	mV
V cross rising Variation					Calc	mV
V cross all Variation					140	mV
Rise Time		V_{OL}=0.175V, V_{OH}=0.525V	175		700	ps
Fall Time		V_{OL}=0.175V, V_{OH}=0.525V	175		700	ps
Rise Time Variation		V_{OL}=0.175V, V_{OH}=0.525V			125	ps
Fall Time Variation		V_{OL}=0.175V, V_{OH}=0.525V			125	ps
Rise/Fall matching		$2*(T_{rise}-T_{fall})/ (T_{rise}+T_{fall})$			20	%
Duty Cycle			45	50	55	%
Pin-to-Pin Skew					100	ps
Cycle-to-Cycle Jitter		**Measurement taken from differential waveform**			125	ps

USB 48MHz

T_A = 0 ~70℃, V_{DD} = 3.3 V +/-5%; Test loads : Rs=12Ω,C_L=4pF with dual loads(unless otherwise stated)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Frequency				48		MHz
Output Impedance		$V_O = V_{DD}$*0.5	20		60	
Output High Voltage		I_{OH} = -1 mA	2.4			V
Output Low Voltage		I_{OL} = 1 mA			0.4	V
Output High Current		V_{OH} @MIN= 1.0V , V_{OH} @ MAX= 3.153V	-29		-23	mA
Output Low Current		V_{OL} @MIN= 2.0V , V_{OL} @ MAX= 0.4V	27		29	mA
Rise Time		V_{OL} = 0.8 V, V_{OH} = 2.0 V	0.6		1.2	ns
Fall Time		V_{OH} = 2.0 V, V_{OL} = 0.8 V	0.6		1.2	ns
Duty Cycle		V_T = 1. 5 V	45	50	55	%
Long term jitter		125 μ s period jitter @ V_T = 1. 5 V			6	ns
Cycle-to-Cycle Jitter		V_T = 1. 5 V			130	ps

REF

T_A = 0 ~ 70℃, V_{DD} = 3.3 V +/-5%; Test loads: Rs=12Ω,C_L=4pF with triple loads (unless otherwise stated).

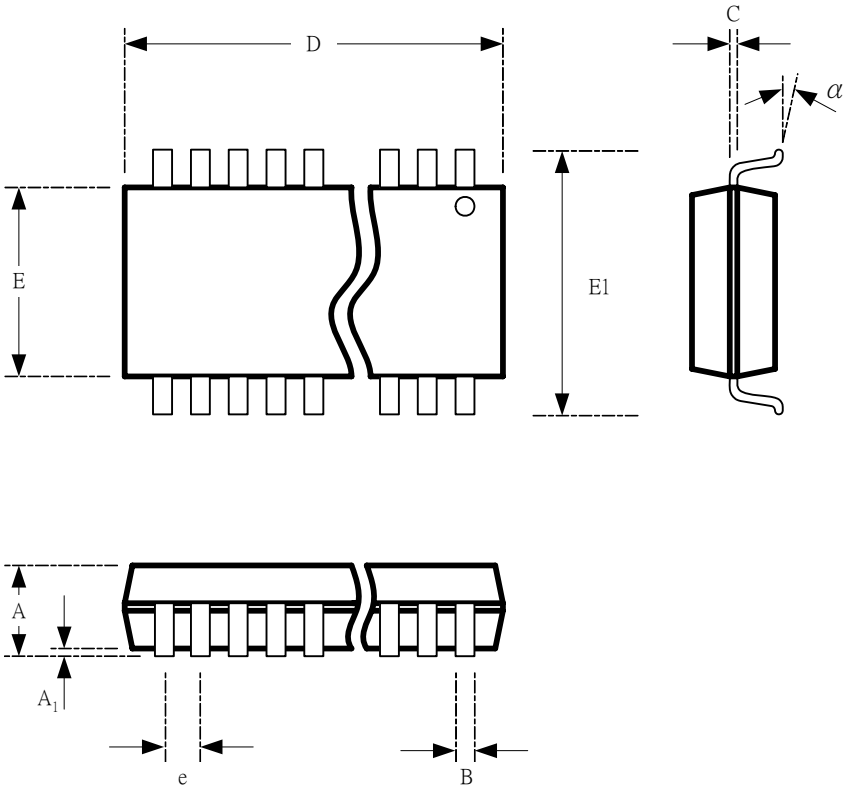
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Frequency				14.318		MHz
Output Impedance		$V_O = V_{DD}$*0.5	10		55	
Output High Voltage		I_{OH} = -1 mA	2.4			V
Output Low Voltage		I_{OL} = 1 mA			0.4	V
Output High Current		V_{OH} @MIN= 1.0V , V_{OH} @ MAX= 3.153V	-33		-33	mA
Output Low Current		V_{OL} @MIN= 2.0V , V_{OL} @ MAX= 0.4V	30		38	mA
Rise Time		V_{OL} = 0.8 V, V_{OH} = 2.0 V	0.3		1.2	ns
Fall Time		V_{OH} = 2.0 V, V_{OL} = 0.8 V	0.3		1.2	ns
Duty Cycle		V_T = 1. 5 V	45	50	55	%
Pin-to-Pin Skew		V_T = 1. 5 V				ps
Cycle-to-Cycle Jitter		V_T = 1. 5 V			200	ps

HTT

T_A = 0 ~ 70℃, V_{DD} = 3.3 V +/-5%; Test loads Rs=12Ω,C_L=4pF with dual loads (unless otherwise stated)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Frequency				33		MHz
Output Impedance		$V_O = V_{DD}*0.5$	12		55	
Output High Voltage		I_{OH} = -1 mA	2.4			V
Output Low Voltage		I_{OL} = 1 mA			0.4	V
Output High Current		V_{OH} @MIN= 1.0V , V_{OH} @ MAX= 3.153V	-29		-23	mA
Output Low Current		V_{OL} @MIN= 2.0V , V_{OL} @ MAX= 0.4V	27		29	mA
Rise Time		V_{OL} = 0.8 V, V_{OH} = 2.0 V	0.3		1.2	ns
Fall Time		V_{OH} = 2.0 V, V_{OL} = 0.8 V	0.3		1.2	ns
Duty Cycle		VT = 1.5 V	45	50	55	%
Pin-to-Pin Skew		VT = 1.5 V			500	ps
Cycle-to-Cycle Jitter		VT = 1.5 V			250	ps

Mechanical Dimensions



TSSOP Package:(unit using inches)

Symbol	Common Dimensions			Variations	D			N
	Minimum	Typical	Maximum		Minimum	Typical	Maximum	
A			0.047	AD	0.547	0.551	0.555	56
A1	0.002		0.006					
B	0.008TYP							
C	0.004		0.008					
D	See Variations							
E	0.236	0.240	0.244					
E1	0.315	0.319	0.323					
e	0.020BSC							
α	0°		8°					

Quartz Crystal Requirements
Frequency and Oscillation Circuits

RTM265 series are designed to work from a crystal with 14.31818MHz.

Fig-1 shows the equivalent circuits of crystal and oscillation circuits within RTM265 series.

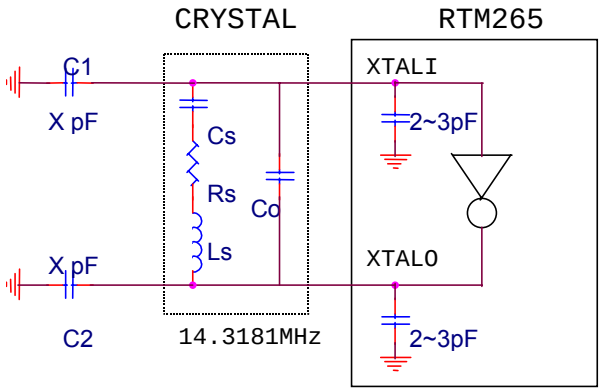


Fig-1 oscillation circuits

$$Fs \cong \frac{1}{2\pi\sqrt{Ls * Cs}}$$

The series resonant frequency, and parallel resonant frequency:

$$Fp \cong \frac{1}{2\pi\sqrt{\frac{Ls * Cs * Co}{Cs + Co}}}$$

The oscillated frequency between *Fs* and *Fp*

$$Fo = Fs * \sqrt{1 + \frac{Cs}{Co + CL}}$$

where C_L=[(C_1+2pF)*(C_2+2pF)] / [(C_1+2pF)+(C_2+2pF)]

Crystal Requirements

General Specifications	Requirements
Holder Type	HC-49 U/S
Crystal Freq.	14.31818 MHz
Oscillation Mode	Fundamental
Load Cap. (C_L)	10 ~32 pF
Freq. Tolerance(25°C)	+/- 30 ppm
Effective Series Resistance (Rs)	40 ohm max
Effective Shunt Capacitance (Co)	7 pF
Drive Level	< 0.1 mW
Insulation Resistance	500 MΩ min. at DC 100V

Table-1 Crystal General Specification

Load Capacitance (CL)

To operate between Fs and Fp requires external load capacitance. So C_1 and C_2 must be used.

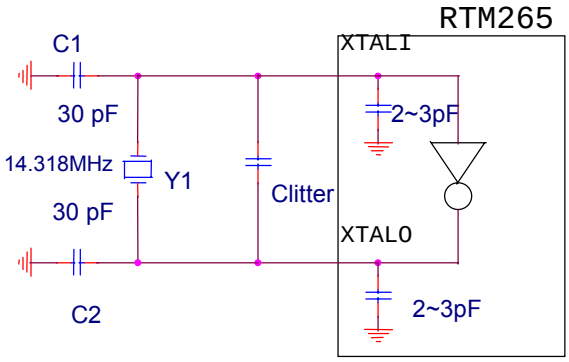


Fig-2 Clitter due to PCB Trace

In ideal case, ignore the C_{litter} at suggested C_1=C_2=54pF, the equivalent load capacitance is:

$$C_L = ((30pF + 2pF) * (30pF + 2pF)) / ((30pF + 2pF) + (30pF + 2pF)) = 16pF$$

According to Table-1, the crystal with C_L=16pF is adapted. But in most case, the litter capacitor (C_{litter}) generated by PCB trace is existent. So the real C_L is

$$C_L = (C1 + 2pF) // (C2 + 2pF) + C_{litter}$$

Consider the litter capacitance , crystal with C_L=28pF is allowable.

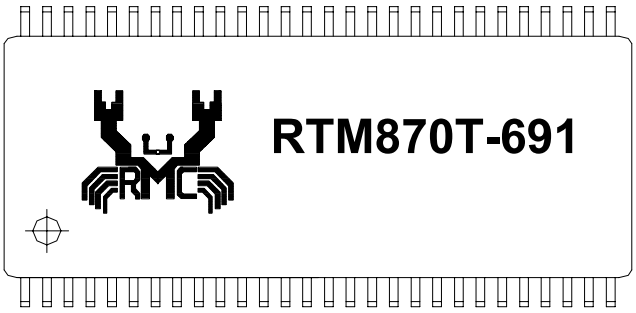
Reference Table

C_L (pF)	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
C_1=C_2 (pF)	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48	50	52	54	56	58	60	62

Table-2 Crystal CL General Specification

For detail application about the selection of C_1 & C_2, please refer to crystal design guide.

Package information.
Lead(Pb)-free Package



For products with lead-free package, a 'L' letter is shown in the beginning of the last group of numbers.

Otherwise, only 4 numbers will be shown in the last group of numbers.

Ordering Information

Part Number	Description
RTM870T-691-LF	Lead-free package meets RoHS requirement
RTM870T-691-LFT	Lead-free package (Tape & Reel) meets RoHS requirement

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