

General Application:

RTM876-660 is a 56 pin single-chip frequency generator.

RTM876-660 Support Pin Features

- 2 - Differential pairs push-pull CPU @0.8V or @3.3V
- 6 - Differential pairs push-pull PCI-E @0.8V
- 1 - Differential pairs push-pull SATA @0.8V or PCI-E @0.8V
- 1 - Differential pairs push-pull DOT96/ SATA@0.8V or 2-Link @3.3V
- 7 - PCI @3.3V
- 2 - 48MHz @3.3V
- 3 - REF @3.3V, 14.318MHz

Others Features

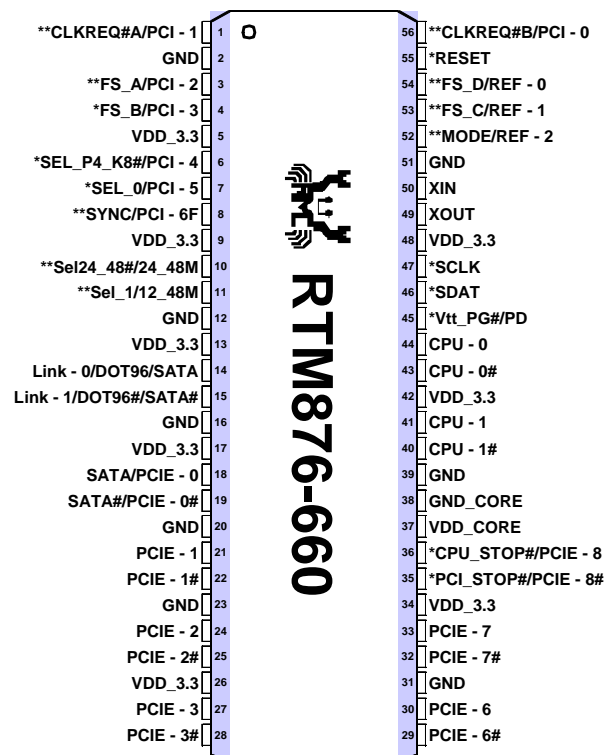
- Programmable frequency with CPU/PCI-E/AGP/PCI
- CPU working range support from 100MHz to 400MHz
- Independent clock group Spread spectrum for EMI control
- Power Management function support
- Watchdog programmable time base reset output
- 4-steps programmable drive strength
- 16-steps programmable skew adjustment with 75p resolution
- 4-stages dynamic frequency switch with innovative AFM over-clock profile
- PCIe clock phase jitter < 86ps.

TOP VIEW: SSOP56 package

- * internal pull high
- ** internal pull low

H/W Latch Frequency Table

SYNC BIT4	FSD BIT3	FSC BIT2	FSB BIT1	FSA BIT0	CPU-0	CPU-1	PCIE	SATA	LINK	PCI	SSC
0	0	0	0	0	266.66	266.66	100.00	FIX100	66.66	33.33	+/-0.25%
0	0	0	0	1	133.33	133.33	100.00	FIX100	66.66	33.33	+/-0.25%
0	0	0	1	0	200.00	200.00	100.00	FIX100	66.66	33.33	+/-0.25%
0	0	0	1	1	166.66	166.66	100.00	FIX100	66.66	33.33	+/-0.25%
0	0	1	0	0	333.33	333.33	100.00	FIX100	66.66	33.33	+/-0.25%
0	0	1	0	1	100.00	100.00	100.00	FIX100	66.66	33.33	+/-0.25%
0	0	1	1	0	400.00	400.00	100.00	FIX100	66.66	33.33	+/-0.25%
0	0	1	1	1	200.00	240.00	A-100	FIX100	A-133.33	A-33.33	+/-0.25%
0	1	0	0	0	266.66	266.66	A-100	FIX100	133.33	33.33	+/-0.25%
0	1	0	0	1	133.33	133.33	A-100	FIX100	133.33	33.33	+/-0.25%
0	1	0	1	0	200.00	200.00	A-100	FIX100	133.33	33.33	+/-0.25%
0	1	0	1	1	166.66	166.66	A-100	FIX100	A-133.33	33.33	+/-0.25%
0	1	1	0	0	333.33	333.33	A-100	FIX100	A-133.33	33.33	+/-0.25%
0	1	1	0	1	100.00	100.00	A-100	FIX100	133.33	33.33	+/-0.25%
0	1	1	1	0	400.00	400.00	A-100	FIX100	133.33	33.33	+/-0.25%
0	1	1	1	1	200.00	250.00	A-100	FIX100	A-133.33	33.33	+/-0.25%
1	0	0	0	0	266.66	266.66	A-100	FIX100	66.66	33.33	+/-0.25%
1	0	0	0	1	133.33	133.33	A-100	FIX100	66.66	33.33	+/-0.25%
1	0	0	1	0	200.00	200.00	A-100	FIX100	66.66	33.33	+/-0.25%
1	0	0	1	1	166.66	166.66	A-100	FIX100	66.66	33.33	+/-0.25%
1	0	1	0	0	333.33	333.33	A-100	FIX100	66.66	33.33	+/-0.25%
1	0	1	0	1	100.00	100.00	A-100	FIX100	66.66	33.33	+/-0.25%
1	0	1	1	0	400.00	400.00	A-100	FIX100	66.66	33.33	+/-0.25%
1	0	1	1	1	200.00	240.00	FIX100	FIX-125	FIX-125	FIX-33.33	+/-0.25%
1	1	0	0	0	266.66	266.66	100.00	FIX100	FIX-125	33.33	+/-0.25%
1	1	0	0	1	133.33	133.33	100.00	FIX100	FIX-125	33.33	+/-0.25%
1	1	0	1	0	200.00	200.00	100.00	FIX100	FIX-125	33.33	+/-0.25%
1	1	0	1	1	166.66	166.66	100.00	FIX100	FIX-125	33.33	+/-0.25%
1	1	1	0	0	333.33	333.33	100.00	FIX100	FIX-125	33.33	+/-0.25%
1	1	1	0	1	100.00	100.00	100.00	FIX100	FIX-125	33.33	+/-0.25%
1	1	1	1	0	400.00	400.00	100.00	FIX100	FIX-125	33.33	+/-0.25%
1	1	1	1	1	200.00	250.00	100.00	FIX100	FIX-125	33.33	+/-0.25%



Advanced Application

Other Input H/W latch pin Selection

PIN10	PIN10
Sel24_48#	24_48M
0	48MHz
1	24MHz

PIN52	PIN35/36
MODE	PCIE-8 [TC]/PCISTOP,CPUSTOP
0	PCIE-8 T/C
1	PCI_STOP/CPU_STOP

PIN6	PIN40,41,43,44
Sel_P4_K8	CPU-0/1
0	P4 3.3V
1	K8 0.8V

PIN11	PIN7	PIN14/15	PIN18/19	PIN11	NOTE
SEL_1	SEL_0	LINK/DOT/SATA	SATA/PCIE	12M_48M	CHIPSET
0	0	Link	SATA	12M	SiS

Power Management description

CLKREQ# Functionality

NOTE:CLKREQ function is select by setting CR02[7] = 1

		CR20[7]		CR20[6]		CR20[5]		CR20[4]	
		0	1	0	1	0	1	0	1
CLKREQA#	0	pcie-7 running	pcie-7 running	pcie-6 running	pcie-6 running	-	-	-	-
	1	pcie-7 running	pcie-7 stop	pcie-6 running	pcie-6 stop	-	-	-	-
CLKREQB#	0	-	-	-	-	pcie-5 running	pcie-5 running	pcie-4 running	pcie-4 running
	1	-	-	-	-	pcie-5 running	pcie-5 stop	pcie-4 running	pcie-4 stop

PD Functionality

PD	CPU	CPU#	PCIE	PCIE#	LINK	PCIF/PCI	48/24	REF	SATA
1	Driven or Low	Low	Driven or Low	Low	Low	Low	Low	Low	Low
0	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

PCI_STOP# Functionality

PCI_STOP#	CPU	CPU#	PCIE	PCIE#	LINK	PCIF/PCI	48/24	REF	SATA
1	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal
0	Normal	Normal	Driven or Low	Low	Normal	Low	Normal	Normal	Normal

CPU_STOP# Functionality

CPU_STOP#	CPU	CPU#	PCIE	PCIE#	LINK	PCIF/PCI	48/24	REF	SATA
1	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal
0	Driven or Low	Low	Normal	Normal	Normal	Normal	Normal	Normal	Normal

Pin Description

Note : (*) Internal 120K pull-up resistors present, (**) Internal 120K pull-down resistors present, [#] mean active when pull low.

Pin No.	Pin Name	Internal Pull	Type	Description
1	PCI - 1		O	3.3V 33MHz PCI output.
	**CLKREQ#A	low	I	3.3V LVTTTL CLKREQ function selection pin for PCIE7/6(SELECT by CR02[7],CR20[7-6]) 0 = pcie free running 1 = CLKREQ stop
2	GND		G	Ground pin.
3	**FS_A	low	I	1.8V LVTTTL frequency selection pin., refer to HW latch frequency table
	PCI - 2		O	3.3V 33MHz PCI output.
4	*FS_B	high	I	1.8V LVTTTL frequency selection pin. ., refer to HW latch frequency table
	PCI - 3		O	3.3V 33MHz PCI output.
5	VDD_3.3		P	3.3V power input pin.
6	*SEL_P4_K8#	high	I	3.3V LVTTTL CPU mode selection pin. 0 = K8 mode 1 = P4 mode
	PCI - 4		O	3.3V 33MHz PCI output.
7	*SEL_0	high	I	3.3V LVTTTL chipset mode selection pin. Refer to CHIPSET SELECT table
	PCI - 5		O	3.3V 33MHz PCI output.
8	PCI - 6F		O	3.3V 33MHz PCI output.
	**SYNC	low	I	1.8V LVTTTL frequency selection pin. ., refer to HW latch frequency table
9	VDD_3.3		P	3.3V power input pin.
10	**Sel24_48#	low	I	3.3V LVTTTL frequency selection pin. 1 = 24MHz 0 = 48MHz
	24_48M		O	3.3V 24/48MHz PCI output.
11	**Sel_1	low	I	3.3V LVTTTL chipset mode selection pin. . Refer to CHIPSET SELECT table
	12_48M		O	3.3V 12_48MHz frequency output pin, selected by chipset selection table
12	GND		G	Ground pin.
13	VDD_3.3		P	3.3V power input pin.
14	Link - 0		O	3.3V 66/133 MHz PCI output. Refer to chipset selection table
	DOT96		O	0.8V DOT96 "true" differential output. Refer to chipset selection table
	SATA		O	0.8V PCIE "true" differential output. Refer to chipset selection table
15	Link - 1		O	3.3V 66/133 MHz PCI output. Refer to chipset selection table
	DOT96#		O	0.8V DOT96 "complementary" differential output. Refer to chipset selection table
	SATA#		O	0.8V PCIE "complementary" differential output. Refer to Refer to chipset selection table
16	GND		G	Ground pin.
17	VDD_3.3		P	3.3V power input pin.
18	SATA		O	0.8V SATA "true" differential output.
	PCIE - 0		O	0.8V PCIE "true" differential output.
19	SATA#		O	0.8V SATA "complementary" differential output.
	PCIE - 0#		O	0.8V PCIE "complementary" differential output.
20	GND		G	Ground pin.
21	PCIE - 1		O	0.8V PCIE "true" differential output.
22	PCIE - 1#		O	0.8V PCIE "complementary" differential output.
23	GND		G	Ground pin.
24	PCIE - 2		O	0.8V PCIE "true" differential output.
25	PCIE - 2#		O	0.8V PCIE "complementary" differential output.
26	VDD_3.3		P	3.3V power input pin.
27	PCIE - 3		O	0.8V PCIE "true" differential output.
28	PCIE - 3#		O	0.8V PCIE "complementary" differential output.
29	PCIE - 6#		O	0.8V PCIE "complementary" differential output.
30	PCIE - 6		O	0.8V PCIE "true" differential output.
31	GND		G	Ground pin.
32	PCIE - 7#		O	0.8V PCIE "complementary" differential output.

33	PCIE - 7		O	0.8V PCIE "true" differential output.
34	VDD_3.3		P	3.3V power input pin.
35	PCIE - 8#		O	0.8V PCIE "true" differential output.
	*PCI_STOP#	high	I	3.3V LVTTTL PCI_STOP pin 0 = assertion ; 1= de-assertion
36	PCIE - 8		O	0.8V PCIE "complementary" differential output.
	*CPU_STOP#	high	I	3.3V LVTTTL CPU_STOP pin 0 = assertion ; 1= de-assertion
37	VDD_CORE		P	3.3V power input pin.
38	GND_CORE		G	Ground pin.
39	GND		G	Ground pin.
40	CPU - 1#		O	0.8V cpu "complementary" differential output.
41	CPU - 1		O	0.8V cpu "true" differential output.
42	VDD_3.3		P	3.3V power input pin.
43	CPU - 0#		O	0.8V cpu "complementary" differential output.
44	CPU - 0		O	0.8V cpu "true" differential output.
45	*Vtt_PG#	high	I	3.3V LVTTTL Vtt power good input pin low active one- shot function. 0 = assertion 1 = de-assertion
	*PD	high	I	3.3V LVTTTL Vtt power down pin 0 = de-assertion 1= assertion
46	*SDAT	high	I/O	SMBUS serial interface data pin.
47	*SCLK	high	I	SMBUS serial interface clock pin.
48	VDD_3.3		P	3.3V power input pin.
49	XOUT		O	Crystal output pin.
50	XIN		I	Crystal input pin.
51	GND		G	Ground pin.
52	REF - 2		O	3.3V 14.318MHz output.
	**MODE	Low	I	3.3V LVTTTL CPU_STOP/PCI_STOP function selection pin 0 = PIN34/35 = PCIE-8 1 = PIN34/35 = PCI_STOP/CPU_STOP
53	**FS_C	low	I	1.8V LVTTTL frequency selection pin. , refer to HW latch frequency table
	REF - 1		O	3.3V 14.318MHz output.
54	**FS_D	low	I	1.8V LVTTTL frequency selection pin. , refer to HW latch frequency table
	REF - 0		O	3.3V 14.318MHz output.
55	RESET#		O	Reset output pin
	*RESET_IN#	high	I	Reset input pin(only in SiS chipset selection) 0 = assertion 1 = de-assertion
56	PCI - 0		O	3.3V 33MHz PCI output.
	**CLKREQ#B	low	I	3.3V LVTTTL CLKREQ function selection pin for PCIE4/5(SELECT by CR02[7],CR20[5-4]) 0 = pcie free running 1 = CLKREQ stop

Register Description

Address CR 00h [0]				
Bit	Description	Pin	Type	Default
Bit7	12_48M selection. 0 = 12MHz 1 = 48MHz		R/W	[Latched]
Bit6	MODE selection 0 = PCIe-8 T/C (pin34/35) 1 = PCI_STOP/CPU_STOP (pin34/35)		R/W	[Latched]
Bit5	0 = CPU-1T/C disable (P4K8) 1 = CPU-1T/C enable (P4K8)		R/W	1
Bit4	0 = CPU-0 T/C disable (P4K8) 1 = CPU-0 T/C enable (P4K8)		R/W	1
Bit3	0 = DOT96_SATA T/C disable 1 = DOT96_SATA T/C enable		R/W	1
Bit2	0 = PCIe-8 T/C disable 1 = PCIe-8 T/C enable		R/W	1
Bit1	0 = PCIe-7 T/C disable 1 = PCIe-7 T/C enable		R/W	1
Bit0	0 = PCIe-6 T/C disable 1 = PCIe-6 T/C enable		R/W	1

Address CR 01h [1]				
Bit	Description	Pin	Type	Default
Bit7	Reserved		R/W	1
Bit6	Reserved		R/W	1
Bit5	0 = PCIe-3 T/C disable 1 = PCIe-3 T/C enable		R/W	1
Bit4	0 = PCIe-2 T/C disable 1 = PCIe-2 T/C enable		R/W	1
Bit3	0 = PCIe-1 T/C disable 1 = PCIe-1 T/C enable		R/W	1
Bit2	0 = PCIe-0 T/C SATA disable 1 = PCIe-0 T/C SATA enable		R/W	1
Bit1	0 = Link-1 disable 1 = Link -1 enable		R/W	[Latched]
Bit0	0 = Link -0 disable 1 = Link -0 enable		R/W	[Latched]

Address CR 02h [2]

Bit	Description	Pin	Type	Default
Bit7	PCI0/CLKREQ#B/ PCI1/CLKREQ#A select 0 = PCI- 0/ PCI-1 1 = CLKREQ#B/ CLKREQ#A		R/W	0
Bit6	0 = PCI-6 disable 1 = PCI-6 enable		R/W	1
Bit5	0 = PCI-5 disable 1 = PCI-5 enable		R/W	1
Bit4	0 = PCI-4 disable 1 = PCI-4 enable		R/W	1
Bit3	0 = PCI-3 disable 1 = PCI-3 enable		R/W	1
Bit2	0 = PCI-2 disable 1 = PCI-2 enable		R/W	1
Bit1	0 = PCI-1 disable 1 = PCI-1 enable		R/W	1
Bit0	0 = PCI-0 disable 1 = PCI-0 enable		R/W	1

Address CR 03h [2]

Bit	Description	Pin	Type	Default
Bit7	0 = 12_48MHz disable 1 = 12_48MHz enable		R/W	1
Bit6	0 = 24_48MHz disable 1 = 24_48MHz enable		R/W	1
Bit5	0 = REF - 2 disable 1 = REF - 2 enable		R/W	1
Bit4	0 = REF - 1 disable 1 = REF - 1 enable		R/W	1
Bit3	0 = REF - 0 disable 1 = REF - 0 enable		R/W	1
Bit2	0 = RESET_RESET IN = RESET OUT 1 = RESET_RESET IN = RESET IN		R/W	0
Bit1	0 = Drive PCI-E T/C when PD# is asserted 1 = Float PCI-E T/C when PD# is asserted		R/W	1
Bit0	0 = Drive CPU-0/1 T/C when PD# is asserted (P4)(K8) 1 = Float CPU-0/1 T/C when PD# is asserted (P4)(K8)		R/W	1

Address CR 04h [4]

Bit	Description	Pin	Type	Default
Bit[7:6]	00 = PCI[0:6] slew rate 1.00X 01 = PCI[0:6] slew rate 1.25X 10 = PCI[0:6] slew rate 1.50X 11 = PCI[0:6] slew rate 2.00X		R/W	01
Bit[5:4]	00 = LINK[0:2] slew rate 1.00X 01 = LINK [0:2] slew rate 1.25X 10 = LINK [0:2] slew rate 1.50X 11 = LINK [0:2] slew rate 2.00X		R/W	10
Bit[3:2]	00 = 48MHz / 24_48MHz slew rate 1.00X 01 = 48MHz /24_48MHz slew rate 1.25X 10 = 48MHz /24_48MHz slew rate 1.50X 11 = 48MHz /24_48MHz slew rate 2.00X		R/W	11
Bit[1:0]	00 = REF[0:1] slew rate 1.00X 01 = REF[0:1] slew rate 1.25X 10 = ERF[0:1] slew rate 1.50X 11 = REF[0:1] slew rate 2.00X		R/W	01

Address CR 05h [5]

Bit	Description	Pin	Type	Default
Bit 7	0 = CPU slew rate 1x 1 = CPU slew rate 2x		R/W	0
Bit 6	0 = DOT/PCI-E / SATA slew rate 1x 1 = DOT/PCI-E / SATA slew rate 2x		R/W	0
Bit 5	Select_1 power-on latched		R	Latched
Bit 4	Select_0 power-on latched		R	Latched
Bit 3	0 = all LP pad driving 1x 1 = all LP pad driving 2x		R/W	1
Bit[2:0]	LP pad swing control. 000:600mV 001:650mV 010:700mV 011:750mV 100:800mV 101:850mV 110:900mV 111:950mV		R/W	100

Address CR 06h [6]

Bit	Description	Pin	Type	Default
Bit7	0 = 24_48# select 48M 1 = 24_48 #select 24M		R/W	[Latched]
Bit6	Select_P4_K8# power-on latched 0 = K8 mode 1 = P4 mode		R	Latched
Bit5	**FSF power-on latched		R	Latched
Bit4	**SYNC(FSE) power-on latched		R	Latched
Bit3	**FSD power-on latched		R	Latched
Bit2	**FSC power-on latched		R	Latched
Bit1	*FSB power-on latched		R	Latched
Bit0	**FSA power-on latched		R	Latched

Address CR 07h [7]

Bit	Description	Type	Default
Bit7	Revision Code	R	0
Bit6	Revision Code	R	0
Bit5	Revision Code	R	0
Bit4	Revision Code	R	1
Bit3	Vender Code	R	1
Bit2	Vender Code	R	1
Bit1	Vender Code	R	1
Bit0	Vender Code	R	0

REALTEK Vender ID = 0Eh; Revision ID=01h(B)

Address CR 08h [8]

Bit	Description	Default																																																																																																																																																																																																																																																																																																																																																																																																																																																										
Bit7	0 = not using CR08 frequency. 1 = frequency is selected by CR08h[5:0]	0																																																																																																																																																																																																																																																																																																																																																																																																																																																										
Bit6	Reserved	0																																																																																																																																																																																																																																																																																																																																																																																																																																																										
Bit [5:0]	<table border="1"> <thead> <tr> <th>FSF</th> <th>SYNC</th> <th>FSD</th> <th>FSC</th> <th>FSB</th> <th>FSA</th> <th>CPU- 0</th> <th>CPU- 1</th> <th>PCIE</th> <th>SATA</th> <th>LINK</th> <th>PCI</th> <th>SSC</th> </tr> <tr> <th>BIT5</th> <th>BIT4</th> <th>BIT3</th> <th>BIT2</th> <th>BIT1</th> <th>BIT0</th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>266.66</td><td>266.66</td><td>100.00</td><td>FIX100</td><td>66.66</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>133.33</td><td>133.33</td><td>100.00</td><td>FIX100</td><td>66.66</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>200.00</td><td>200.00</td><td>100.00</td><td>FIX100</td><td>66.66</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>166.66</td><td>166.66</td><td>100.00</td><td>FIX100</td><td>66.66</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>333.33</td><td>333.33</td><td>100.00</td><td>FIX100</td><td>66.66</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>100.00</td><td>100.00</td><td>100.00</td><td>FIX100</td><td>66.66</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>400.00</td><td>400.00</td><td>100.00</td><td>FIX100</td><td>66.66</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>200.00</td><td>240.00</td><td>A-100</td><td>FIX100</td><td>A-133.33</td><td>A-33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>266.66</td><td>266.66</td><td>A-100</td><td>FIX100</td><td>133.33</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>133.33</td><td>133.33</td><td>A-100</td><td>FIX100</td><td>133.33</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>200.00</td><td>200.00</td><td>A-100</td><td>FIX100</td><td>133.33</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>166.66</td><td>166.66</td><td>A-100</td><td>FIX100</td><td>A-133.33</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>333.33</td><td>333.33</td><td>A-100</td><td>FIX100</td><td>A-133.33</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>100.00</td><td>100.00</td><td>A-100</td><td>FIX100</td><td>133.33</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>400.00</td><td>400.00</td><td>A-100</td><td>FIX100</td><td>133.33</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>200.00</td><td>250.00</td><td>A-100</td><td>FIX100</td><td>A-133.33</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>266.66</td><td>266.66</td><td>A-100</td><td>FIX100</td><td>66.66</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>133.33</td><td>133.33</td><td>A-100</td><td>FIX100</td><td>66.66</td><td>33.33</td><td>+/-0.25%</td></tr> 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<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>200.00</td><td>240.00</td><td>FIX100</td><td>FIX100</td><td>FIX-125</td><td>FIX33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>266.66</td><td>266.66</td><td>100.00</td><td>FIX100</td><td>FIX -125</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>133.33</td><td>133.33</td><td>100.00</td><td>FIX100</td><td>FIX -125</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>200.00</td><td>200.00</td><td>100.00</td><td>FIX100</td><td>FIX -125</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>166.66</td><td>166.66</td><td>100.00</td><td>FIX100</td><td>FIX -125</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>333.33</td><td>333.33</td><td>100.00</td><td>FIX100</td><td>FIX -125</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>100.00</td><td>100.00</td><td>100.00</td><td>FIX100</td><td>FIX -125</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>400.00</td><td>400.00</td><td>100.00</td><td>FIX100</td><td>FIX -125</td><td>33.33</td><td>+/-0.25%</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>200.00</td><td>250.00</td><td>100.00</td><td>FIX100</td><td>FIX -125</td><td>33.33</td><td>+/-0.25%</td></tr> </tbody> </table>	FSF	SYNC	FSD	FSC	FSB	FSA	CPU- 0	CPU- 1	PCIE	SATA	LINK	PCI	SSC	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0								0	0	0	0	0	0	266.66	266.66	100.00	FIX100	66.66	33.33	+/-0.25%	0	0	0	0	0	1	133.33	133.33	100.00	FIX100	66.66	33.33	+/-0.25%	0	0	0	0	1	0	200.00	200.00	100.00	FIX100	66.66	33.33	+/-0.25%	0	0	0	0	1	1	166.66	166.66	100.00	FIX100	66.66	33.33	+/-0.25%	0	0	0	1	0	0	333.33	333.33	100.00	FIX100	66.66	33.33	+/-0.25%	0	0	0	1	0	1	100.00	100.00	100.00	FIX100	66.66	33.33	+/-0.25%	0	0	0	1	1	0	400.00	400.00	100.00	FIX100	66.66	33.33	+/-0.25%	0	0	0	1	1	1	200.00	240.00	A-100	FIX100	A-133.33	A-33.33	+/-0.25%	0	0	1	0	0	0	266.66	266.66	A-100	FIX100	133.33	33.33	+/-0.25%	0	0	1	0	0	1	133.33	133.33	A-100	FIX100	133.33	33.33	+/-0.25%	0	0	1	0	1	0	200.00	200.00	A-100	FIX100	133.33	33.33	+/-0.25%	0	0	1	0	1	1	166.66	166.66	A-100	FIX100	A-133.33	33.33	+/-0.25%	0	0	1	1	0	0	333.33	333.33	A-100	FIX100	A-133.33	33.33	+/-0.25%	0	0	1	1	0	1	100.00	100.00	A-100	FIX100	133.33	33.33	+/-0.25%	0	0	1	1	1	0	400.00	400.00	A-100	FIX100	133.33	33.33	+/-0.25%	0	0	1	1	1	1	200.00	250.00	A-100	FIX100	A-133.33	33.33	+/-0.25%	0	1	0	0	0	0	266.66	266.66	A-100	FIX100	66.66	33.33	+/-0.25%	0	1	0	0	0	1	133.33	133.33	A-100	FIX100	66.66	33.33	+/-0.25%	0	1	0	0	1	0	200.00	200.00	A-100	FIX100	66.66	33.33	+/-0.25%	0	1	0	0	1	1	166.66	166.66	A-100	FIX100	66.66	33.33	+/-0.25%	0	1	0	1	0	0	333.33	333.33	A-100	FIX100	66.66	33.33	+/-0.25%	0	1	0	1	0	1	100.00	100.00	A-100	FIX100	66.66	33.33	+/-0.25%	0	1	0	1	1	0	400.00	400.00	A-100	FIX100	66.66	33.33	+/-0.25%	0	1	0	1	1	1	200.00	240.00	FIX100	FIX100	FIX-125	FIX33.33	+/-0.25%	0	1	1	0	0	0	266.66	266.66	100.00	FIX100	FIX -125	33.33	+/-0.25%	0	1	1	0	0	1	133.33	133.33	100.00	FIX100	FIX -125	33.33	+/-0.25%	0	1	1	0	1	0	200.00	200.00	100.00	FIX100	FIX -125	33.33	+/-0.25%	0	1	1	0	1	1	166.66	166.66	100.00	FIX100	FIX -125	33.33	+/-0.25%	0	1	1	1	0	0	333.33	333.33	100.00	FIX100	FIX -125	33.33	+/-0.25%	0	1	1	1	0	1	100.00	100.00	100.00	FIX100	FIX -125	33.33	+/-0.25%	0	1	1	1	1	0	400.00	400.00	100.00	FIX100	FIX -125	33.33	+/-0.25%	0	1	1	1	1	1	200.00	250.00	100.00	FIX100	FIX -125	33.33	+/-0.25%	000010
FSF	SYNC	FSD	FSC	FSB	FSA	CPU- 0	CPU- 1	PCIE	SATA	LINK	PCI	SSC																																																																																																																																																																																																																																																																																																																																																																																																																																																
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Address CR 09h [9]

Bit	Description	Type	Default
Bit[7]	CPU output status with assertion of CPU_STOP# 0 = driven 1 = low.	R/W	0
Bit[6]	0 = PLL1 spread spectrum disable 1 = PLL1 spread spectrum enable	R/W	Latched
Bit[5:4]	PLL1 SSC Range control 00 = -0.5% 01 = -1.0% 10 = ±0.25% 11 = ±0.5%	R/W	Latched
Bit[3]	PCIE output status with assertion of PCI_STOP# 0 = driven 1 = low.	R/W	0
Bit[2]	0 = PLL3 spread spectrum disable 1 = PLL3 spread spectrum enable	R/W	Latched
Bit[1:0]	PLL3 SSC Range control 00 = -0.5% 01 = -1.0% 10 = ±0.25% 11 = ±0.5%	R/W	Latched

PLL1/PLL3 SSC Range control table

PLL1 SSC Range			PLL3 SSC Range		
S1	S0	Spread Amount	S1	S0	Spread Amount
0	0	-0.5%	0	0	-0.5%
0	1	-1.0%	0	1	-1.0%
1	0	±0.25%	1	0	±0.25%
1	1	±0.5%	1	1	±0.5%

Address CR 0ah [10]

Bit	Description	TYPE	Default
Bit7	CPU-1 control bit with assertion of CPU_STOP# 0 = Freeing running 1 = Stop with CPU_STOP#	R/W	0
Bit6	CPU-0 control bit with assertion of CPU_STOP# 0 = Freeing running 1 = Stop with CPU_STOP#	R/W	0
Bit5	Turbo-1 pin flag status 0 = Turbo-1 enable 1 = Turbo-1 disable	R	[monitor]
Bit4	Turbo-0 pin flag status 0 = Turbo-0 enable 1 = Turbo-0 disable	R	[monitor]
Bit3	PCI-6F control bit with assertion of PCI_STOP# 0 = Freeing running 1 = Stop with PCI_STOP#	R/W	0
Bit2	PCI-E control bit with assertion of PCIE_STOP# 0 = Freeing running 1 = Stop with PCIE_STOP#	R/W	0
Bit1	Turbo mode control 0 = Turbo-1 disable 1 = Turbo-1 enable	R/W	0
Bit0	Turbo mode control 0 = Turbo-0 disable 1 = Turbo-0 enable	R/W	0

PIN38 Turbo-1	PIN56 Turbo-0	PLL1	PLL3	Remark
0	0	ROM CR11/13h	CR12/13h	Power-on Default / Normal Programmable
0	1	CR0b/0ch	CR0fh	Program Turbo -0
1	0	CR0b/0dh	CR14h	Program Turbo -1
1	1	CR0b/0eh	CR15h	Program Turbo -2

Address CR 0bh [11]

Bit	Description	Type	Default
Bit[7:6]	RESERVED	R/W	00
Bit[5:4]	PLL1 Turbo-0 VCO_1 code[6:5]	R/W	[10]
Bit[3:2]	PLL1 Turbo-1 VCO_1 code[6:5]	R/W	00
Bit[1:0]	PLL1 Turbo-2 VCO_1 code[6:5]	R/W	00

Address CR 0ch [12]

Bit	Description	Type	Default
Bit[7:3]	PLL1 Turbo-0 VCO_1 code bit[4:0]	R/W	[1000-0]
Bit[2:0]	PLL1 Turbo-0 VCO_2 code bit[3:1]	R/W	[000]

Address CR 0dh [13]

Bit	Description	TYPE	Default
Bit[7:3]	PLL1 Turbo-1 VCO_1 code bit[4:0]	R/W	[1000-0]
Bit[2:0]	PLL1 Turbo-1 VCO_2 code bit[3:1]	R/W	[000]

Address CR 0eh [14]

Bit	Description	TYPE	Default
Bit[7:3]	PLL1 Turbo-2 VCO_1 code bit[4:0]	R/W	[1000-0]
Bit[2:0]	PLL1 Turbo-2 VCO_2 code bit[3:1]	R/W	[000]

Address CR 0fh [15]

Bit	Description	TYPE	Default
Bit[7:1]	PLL3 Turbo-0 VCO_1 code bit[6:0]	R/W	[1010-000]
Bit[0]	PLL3 Turbo-0 VCO_2 code bit[3]	R/W	[0]

Address CR 10h [16]

Bit	Description	Type	Default
Bit[7:4]	Watch dog timer [base =0.5 second] $T = (\text{bit}[7:4] + 2) * \text{base second}$	R/W	[0101]
Bit3	Reset on demand done flag 0 = not done. 1 = done	R	0
Bit2	0 = normal 1 = watch dog enable. Action is internal reset & external reset	R/W	0
Bit1	(Mass-production test mode) 0 = normal 1 = enable Watch Dog timer base =1u second, RESET# pulse = 1uS and test mode MUX select.,	R/W	0
Bit0	Watch dog done flag 0 = not done 1 = done	R	0

Address CR 11h [17]

Bit	Description	Type	Default
Bit[7]	Reserved	R/W	0
Bit[6:0]	PLL1 VCO code_1 [6:0] PLL1 VCO = VCO code_1 * 10 + VCO code_2	R/W	[101-0000]

Address CR 12h [18]

Bit	Description	Type	Default
Bit[7]	Reserved	R/W	0
Bit[6:0]	PLL3_VCO code_1 [6:0] PLL3 VCO = PLL3 VCO code_1 * 10 + PLL3 VCO code_2	R/W	[101-0000]

Address CR 13h [19]

Bit	Description	Type	Default
Bit[7:4]	PLL1_VCO code_2 [3:0] PLL1 VCO = PLL1 VCO code_1 * 10 + PLL1 VCO code_2	R/W	[0000]
Bit[3:0]	PLL3_VCO code_2 [3:0] PLL3 VCO = PLL3 VCO code_1 * 10 + PLL3 VCO code_2	R/W	[0000]

Address CR 14h [20]

Bit	Description	Type	Default
Bit[7:1]	PLL3 Turbo-1 VCO_1 code bit[6:0]	R/W	[1010-000]
Bit[0]	PLL3 Turbo-1 VCO_2 code bit[3]	R/W	[0]

Address CR 15h [21]

Bit	Description	Type	Default
Bit[7:1]	PLL3 Turbo-2 VCO_1 code bit[6:0]	R/W	[1010-000]
Bit[0]	PLL3 Turbo-2 VCO_2 code bit[3]	R/W	[0]

Address CR 16h [22]

Bit	Description	Type	Default
Bit[7:0]	M code bit[7:0] for PLL2	R/W	[1011_0110]

Address CR 17h [23]

Bit	Description	Type	Default
Bit[7:6]	M code bit[9:8] for PLL2	R/W	[01]
Bit[5:0]	N code bit[5:0] for PLL2	R/W	[01_0011]

Address CR 18h [24]			
Bit	Description	Type	Default
Bit[7:6]	00 = PCI[0:6] PAD driving 1.00X 01 = PCI[0:6] PAD driving 1.25X 10 = PCI[0:6] PAD driving 1.50X 11 = PCI[0:6] PAD driving 2.00X	R/W	01
Bit[5:4]	00 = LINK[0:2] PAD driving 1.00X 01 = LINK [0:2] PAD driving 1.25X 10 = LINK [0:2] PAD driving 1.50X 11 = LINK [0:2] PAD driving 2.00X	R/W	01
Bit[3:2]	00 = 48MHz / 24_48MHz PAD driving 1.00X 01 = 48MHz /24_48MHz PAD driving 1.25X 10 = 48MHz /24_48MHz PAD driving 1.50X 11 = 48MHz /24_48MHz PAD driving 2.00X	R/W	01
Bit[1:0]	00 = REF[0:1] PAD driving 1.00X 01 = REF[0:1] PAD driving 1.25X 10 = ERF[0:1] PAD driving 1.50X 11 = REF[0:1] PAD driving 2.00X	R/W	01

Address CR 19h [25]			
Bit	Description	Type	Default
Bit[7:4]	(P4/K8)CPU-0 group delay selection by 75 ps base	R/W	[1000]
Bit[3:0]	(P4/K8)CPU-1 group delay selection by 75 ps base	R/W	[1000]

Skew delay = base x (delay-selection)

Address CR 1ah [26]			
Bit	Description	Type	Default
Bit[7:4]	PCI-E [0:8] group delay selection by 75 ps base	R/W	[0110]
Bit[3:0]	PCI[0:6] group delay selection by 75 ps base	R/W	[1010]

Skew delay = base x (delay-selection)

Address CR 1bh [27]			
Bit	Description	TYPE	Default
Bit[7:4]	SATA group delay selection by 75 ps base	R/W	[1000]
Bit[3:0]	LINK group delay selection by 75 ps base	R/W	[0000]

Skew delay = base x (delay-selection)

Address CR 1ch [28]				
Bit	Description		TYPE	Default
Bit7	RESERVED		R	0
Bit[6:4]	CPU divider		R/W	ROM/REG [010]
	000 = PLL1/2 001 = PLL1/3 010 = PLL1/4 011 = PLL1/6	100 = PLL1/8 101 = PLL1/5 110 = Reserved 111 = Reserved		
Bit[3]	RESERVED		R	0
Bit[2:0]	HCLK divider		R/W	ROM/REG [010]
	000 = PLL1/2 001 = PLL1/3 010 = PLL1/4 011 = PLL1/6	100 = PLL1/8 101 = PLL1/5 110 = Reserved 111 = Reserved		

Address CR 1dh [29]				
Bit	Description		TYPE	Default
Bit7	RESERVED		R	0
Bit[6:4]	Link divider		R/W	ROM/REG [001]
	000= PLL1/6 001= PLL1/12 010= PLL1/15 011= PLL3/6	100= PLL3/12 101= PLL2/2.25(fix133) 110= PLL2/4.5(fix66) 111= Reserved		
Bit3	RESERVED		R	0
Bit[2:0]	PCI-E divider		R/W	ROM/REG [000]
	000 = PLL1/8 001 = PLL1/10 010 = PLL3/8 011 = PLL2 fix100	100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved		

Address CR 1eh [30]				
Bit	Description		TYPE	Default
Bit7	Reserved		R	0
Bit[6:4]	PCI divider		R/W	ROM/REG [000]
	000 = PLL1/24 001 = PLL1/30 010 = PLL3/24 011 = PLL2 /9	100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved		
Bit3	Reserved		R/W	0
Bit[2:1]	00 = K8 CPU PAD driving 1.00X 01 = K8 CPU PAD driving 1.25X 10 = K8 CPU PAD driving 1.50X 11 = K8 CPU PAD driving 2.00X		R/W	00
Bit0	0 = disable last serial BUS write latched with reset# output 1 = enable last serial BUS write latched with reset# output		R/W	0

Address CR 1fh [31]				
Bit	Description	TYPE	Default	
Bit[7:5]	SATA divider		R/W	011
	000 = PLL1/8 001 = PLL1/10 010 = PLL3/8 011 = PLL2 fix100	100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved		
Bit4	Reserved	R/W	0	
Bit3	(PLL2 M/N code) 0=PLL2 programmable disable 1=PLL2 programmable enable & latching	R/W	0	
Bit2	(PLL3 VCO-code mode) 0=PLL3 programmable disable 1=PLL3 programmable enable & latching	R/W	0	
Bit1	0 = Divider select by ROM 1 = Divider select by REG , divider code& clock phase select latching buffer while writen 1	R/W	0	
Bit0	(PLL1 VCO-code mode) 0=PLL1 programmable disable and from ROM CODE 1=PLL1 programmable enable & latching	R/W	0	

Address CR 20h [32]			
Bit	Description	TYPE	Default
Bit7	PCIE-7 T/C controled with CLKREQ#A 0 = PCIE-7 T/C free running. 1 = PCIE-7 T/C stoppable by CLKREQ#A	R/W	0
Bit6	PCIE-6 T/C controled with CLKREQ#A 0 = PCIE-6 T/C free running. 1 = PCIE-6 T/C stoppable by CLKREQ#A	R/W	0
Bit5	PCIE-5 T/C controled with CLKREQ#B 0 = PCIE-5 T/C free running. 1 = PCIE-5 T/C stoppable by CLKREQ#B	R/W	0
Bit4	PCIE-4 T/C controled with CLKREQ#B 0 = PCIE-4 T/C free running. 1 = PCIE-4 T/C stoppable by CLKREQ#B	R/W	0
Bit3	0 = REF positive duty = 50% 1= REF positive duty = 48%	R/W	0
Bit2	0 = 48M positive duty = 50% 1= 48M positive duty = 48%	R/W	0
Bit[1:0]	00 = PCI positive duty = 50% 01 = PCI positive duty = 48.3% 10 = PCI positive duty = 47.8% 11= PCI positive duty = 46.7%	R/W	00

Functionality

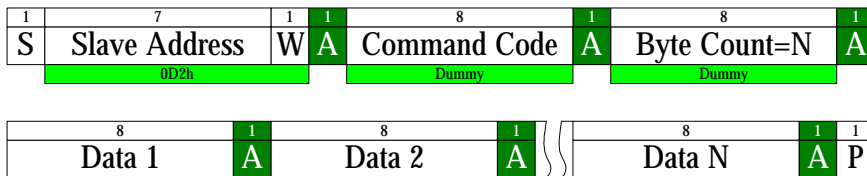
Standard Serial Bus Control:

Support standard serial bus block-mode and direct word-mode.

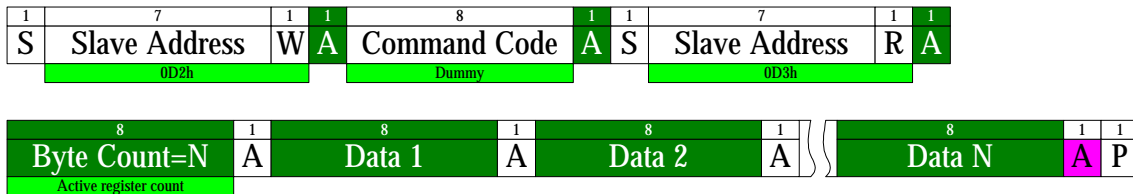
Byte Count = 008h

Direct-word-mode index = 1xxx-xxxx Binary (MSB=1)

Block Mode

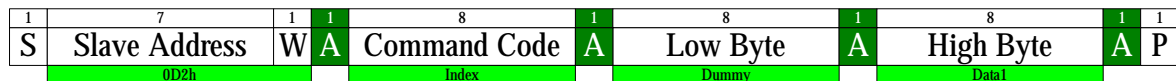


Block Write

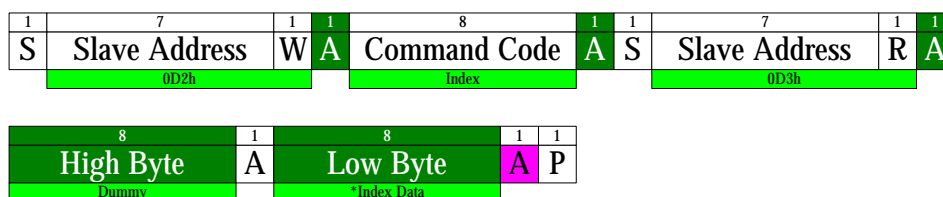


Block Read

Word Mode

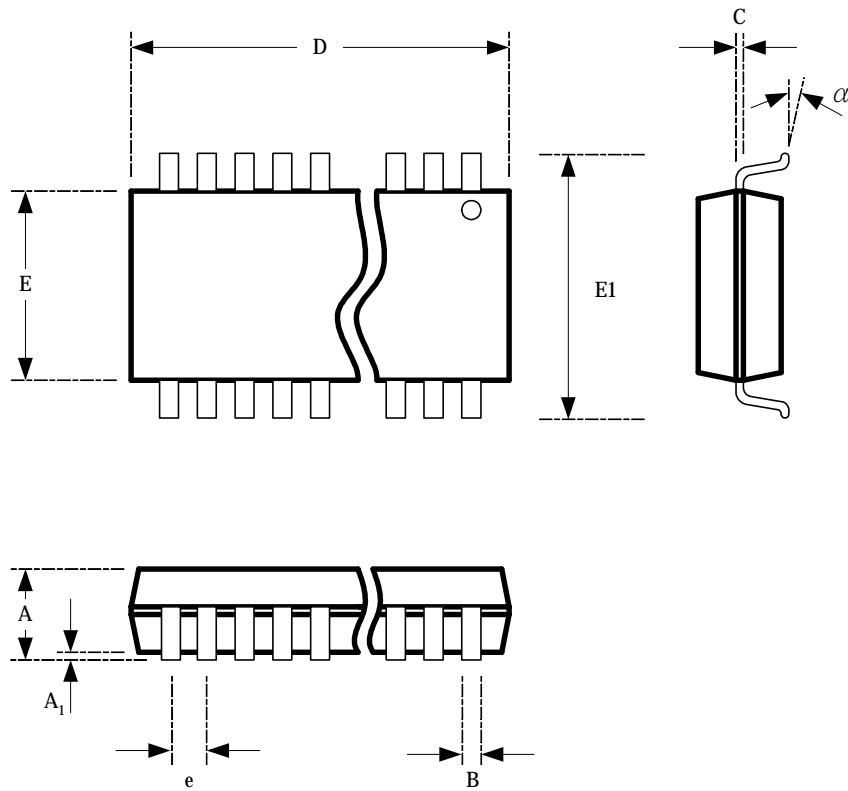


Write Word



Read Word

Note: slave address is D2h.

Mechanical Dimensions

SSOP Package:(unit using inches)

Symbol	Common Dimensions			Variation	D			N
	Minimum	Typical	Maximum		Minimum	Typical	Maximum	
A	0.095	0.101	0.110	AD	0.720	0.725	0.730	56
A1	0.008	0.012	0.016					
B	0.008	0.010	0.0135					
C	0.005	0.0075	0.010					
D	See Variations							
E	0.292	0.296	0.299					
E1	0.395	0.415	0.420					
e	0.025BSC							
α	0°	5°	10°					

Quartz Crystal Requirements

Frequency and Oscillation Circuits

RTM363 series are designed to work from a crystal with 14.31818MHz.

Fig-1 shows the equivalent circuits of crystal and oscillation circuits within RTM867 series.

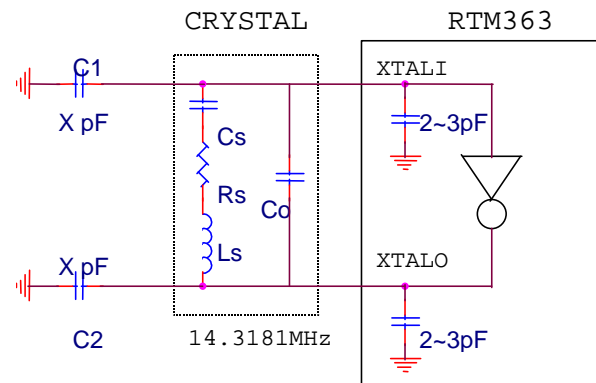


Fig-1 oscillation circuits

$$F_s \cong \frac{1}{2p\sqrt{L_s * C_s}}$$

The series resonant frequency, and parallel resonant frequency:

$$F_p \cong \frac{1}{2p\sqrt{\frac{L_s * C_s * C_o}{C_s + C_o}}}$$

The oscillated frequency between F_s and F_p

$$F_o = F_s * \sqrt{1 + \frac{C_s}{C_o + C_L}}$$

where $C_L = [(C_1 + 2pF) * (C_2 + 2pF)] / [(C_1 + 2pF) + (C_2 + 2pF)]$

Crystal Requirements

General Specifications	Requirements
Holder Type	HC-49 U/S
Crystal Freq.	14.31818 MHz
Oscillation Mode	Fundamental
Load Cap. (CL)	10 ~32 pF
Freq. Tolerance(25°C)	+/- 30 ppm
Effective Series Resistance (Rs)	40 ohm max
Effective Shunt Capacitance (Co)	7 pF
Drive Level	< 0.1 mW
Insulation Resistance	500 Mohm min. at DC 100V

Table-1 Crystal General Specification

Load Capacitance (C_L)

To operate between F_s and F_p requires external load capacitance. So C₁ and C₂ must be used.

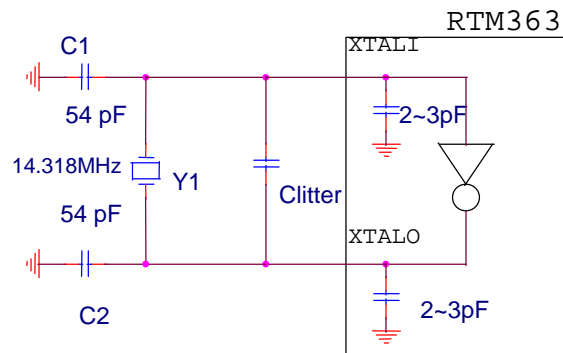


Fig-2 Clitter due to PCB Trace

In ideal case, ignore the C_{litter} at suggested C₁=C₂=54pF, the equivalent load capacitance is:

$$C_L = ((54 pF + 2 pF) * (54 pF + 2 pF)) / ((54 pF + 2 pF) + (54 pF + 2 pF)) = 28 pF$$

According to Table-1, the crystal with C_L=28pF is adapted. But in most case, the litter capacitor (C_{litter}) generated by PCB trace is existent. So the real C_L is

$$C_L = (C_1 + 2 pF) / (C_2 + 2 pF) + C_{litter}$$

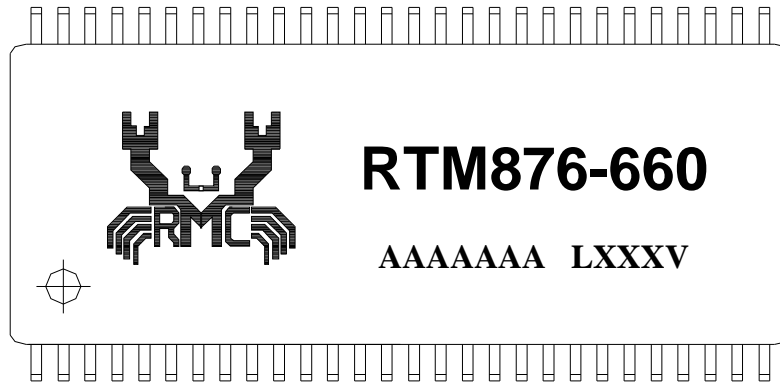
Consider the litter capacitance , crystal with C_L=28pF is allowable.

Reference Table

C_L (pF)	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
$C_1=C_2$ (pF)	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48	50	52	54	56	58	60	62

Table-2 Crystal C_L General Specification

For detail application about the selection of C_1 & C_2 , please refer to crystal design guide.

Package information.**Lead(Pb)-free Package**

For products with lead-free package, a 'L' letter is shown in the beginning of the last group of numbers. Otherwise, only 4 numbers will be shown in the last group of numbers.

Ordering Information

Part Number	Description
RTM876-660	
RTM876-660-LF	Lead-free package meets RoHS requirement

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