3A Ultra-Low Dropout Voltage Regulators with Soft-Start

1 General Description

The RTQ2527D is a very low-dropout linear regulator which operates from input voltage as low as 0.8V. The device is capable of supplying 3A of output current with a typical dropout voltage of only 120mV. A VBIAS supply is required to run the internal reference and LDO circuitry while output current comes directly from the VIN supply for high efficiency regulation. User-programmable soft-start limits the input inrush current and minimizes stress on the input power. The enable input and power good output allow easy sequencing with external regulators. This complete flexibility provides an easy-to-use robust power management solution for a wide variety of applications.

The RTQ2527D is stable with output capacitor greater than or equal to 2.2μF. A precise reference and error amplifier deliver 1% accuracy over load, line and temperature. Overcurrent limit and over-temperature protection are also included. The RTQ2527D is available in the WDFN-10L 3x3 package.

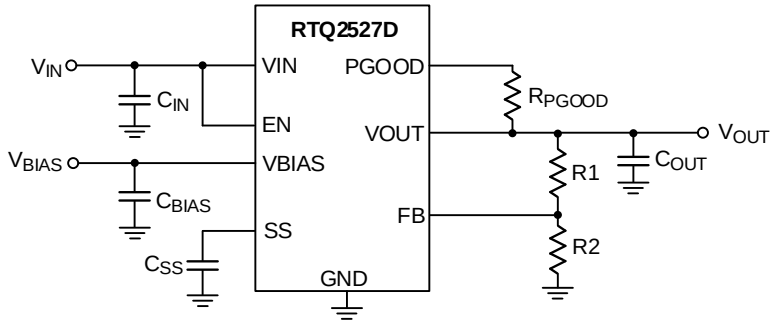
2 Features

- **Ultra-low V_{IN} Range: 0.8V to 5.5V**
- **VBIAS Voltage Range: 2.7V to 5.5V**
- **VOUT Voltage Range: 0.8V to 3.6V**
- **Low Dropout: 120mV Typ. at 3A, V_{BIAS} = 5V**
- **1% Accuracy Over Line/Load/ Temperature**
- **PGOOD Indicator for Easy Sequence Control**
- **Programmable Soft-Start Provides Linear Voltage Startup**
- **Stable with Any Output Capacitor ≥ 2.2μF**
- **Overcurrent and Over-Temperature Protection**

3 Applications

- PCs, Servers, Modems, and Set-Top-Boxes
- FPGA Applications
- DSP Core and I/O Voltages
- Instrumentation
- Post-Regulation Applications
- Applications With Sequencing Requirements

4 Simplified Application Circuit



5 Ordering Information

RTQ2527D □□□

- Pin 1 Orientation
  (2): Quadrant 2, Follow EIA-481
  (Empty means Pin1 orientation is Quadrant 1)
- Package Type
  QW: WDFN-10L 3x3 (W-Type)
- Lead Plating System
  G: Richtek Green Policy Compliant

Note:

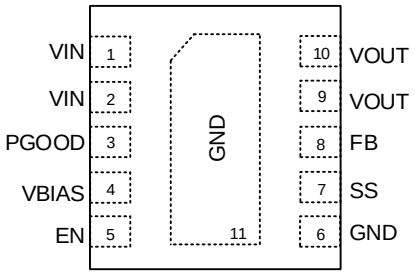
Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

W7=: Product Code
YMDAN: Date Code

7 Pin Configuration

(TOP VIEW)



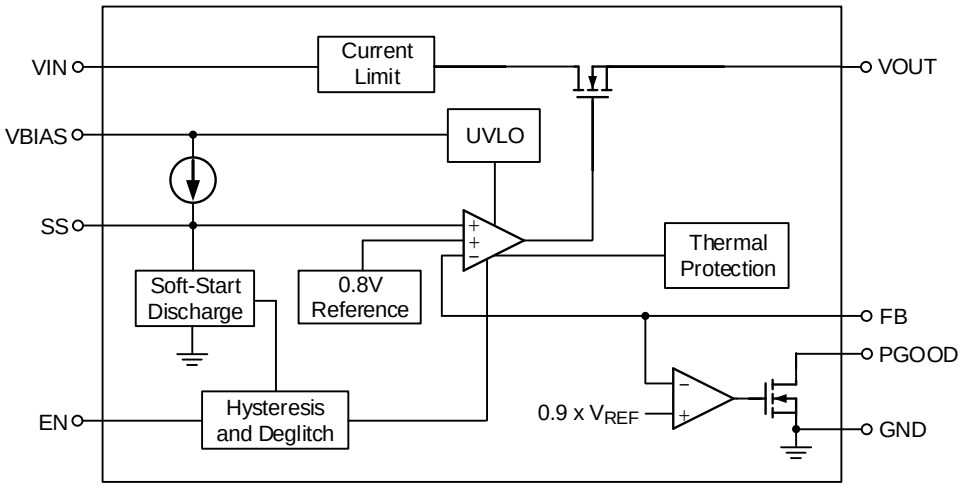
WDFN-10L 3x3

Table of Contents

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2	VIN	Power input of the device.
3	PGOOD	Power good indicator output. This pin is an open-drain output and is active high when the output voltage reaches 88% of the target. The pin is pulled to ground when the output voltage is lower than its specified thresholds, including EN shutdown, OCP and OTP.
4	VBIAS	Bias input pin. Providing input voltage for internal control circuitry.
5	EN	Chip enable (Active-High). Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. Connect to VIN if not being used.
6, 11 (Exposed Pad)	GND	Ground. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
7	SS	Connect a capacitor between this pin and the ground to set the soft-start ramp time of the output voltage.
8	FB	Feedback pin. Connect this pin to an external voltage divider to set the output voltage.
9, 10	VOUT	Regulated output voltage. A minimum of 2.2μF capacitor should be placed directly at this pin.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Output Voltage, VOUT ---------- –0.3V to 6.3V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

11 ESD Ratings

(Note 2)

- ESD Susceptibility
- HBM (Human Body Model)---------- 2kV

12 Recommended Operating Conditions

(Note 3)

- Supply Input Voltage---------- 0.8V to 5.5V
- Junction Temperature Range---------- –40°C to 125°C

13 Thermal Information

(Note 4 and Note 5)

Thermal Parameter		WDFN-10L 3x3	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	40.4	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	70.4	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	13.6	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	41.5	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	1.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	25.2	°C/W

14 Electrical Characteristics

(V_{EN} = 1.1V, V_{IN} = V_{OUT} + 0.3V, V_{BIAS} = 5V, C_{BIAS} = 0.1µF, C_{IN} = C_{OUT} = 10µF, C_{SS} = 1nF, I_{OUT} = 50mA, T_J = -40°C to 125°C, unless otherwise specified. Typical values are at T_A = 25°C)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		V_{IN}		V_{OUT} + V_{DROP}	--	5.5	V
VBIAS Pin Voltage		V_{BIAS}		2.7	--	5.5	V
Internal Reference		V_{REF}		0.792	0.8	0.808	V
Output Voltage Range		V_{OUT}	V_{IN} = 5V, I_{OUT} = 3A	V_{REF}	--	3.6	V
Accuracy			2.97V ≤ V_{BIAS} ≤ 5.5V, 50mA ≤ I_{OUT} ≤ 3A	–1	±0.5	1	%
Line Regulation		V_{LINE_REG}	$V_{OUT\ (Normal)}$ + 0.3 ≤ V_{IN} ≤ 5.5V	--	0.03	--	%/V
Load Regulation		V_{LOAD_REG}	50mA ≤ I_{OUT} ≤ 3A	--	0.09	--	%/A
VIN Dropout Voltage		V_{DROP_VIN}	I_{OUT} = 3A, V_{BIAS} - $V_{OUT\ (Normal)}$ ≥ 3.25V	--	120	180	mV
VBIAS Dropout Voltage		V_{DROP_VBIAS}	I_{OUT} = 3A, V_{IN} = V_{BIAS}	--	--	1.4	V
			I_{OUT} = 2A, V_{IN} = V_{BIAS}	--	--	1.3	V
			I_{OUT} = 1A, V_{IN} = V_{BIAS}	--	--	1.2	V
			I_{OUT} = 0.5A, V_{IN} = V_{BIAS}	--	--	1.1	V
Current Limit		I_{LIM}	V_{OUT} = 80% × $V_{OUT\ (Normal)}$	3.1	5	6.3	A
Bias Pin Current		I_{BIAS}		--	1	2	mA
Shutdown Supply Current (I_{GND})		I_{SHDN}	V_{EN} = 0.4V	--	1	50	µA
Feedback Pin Current		I_{FB}		-1	0.15	1	µA
Power-Supply Rejection (VIN to VOUT)		PSRR (Note 6)	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V	--	60	--	dB
			300kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V	--	30	--	
Power-Supply Rejection (VBIAS to VOUT)			1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V	--	50	--	dB
			300kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V	--	30	--	
Output Noise Voltage		Noise (Note 6)	100Hz to 100kHz, I_{OUT} = 1.5A, C_{SS} = 0.001µF	--	25 x V_{OUT}	--	μV_{RMS}
Minimum Startup Time		t_{STR} (Note 6)	R_{LOAD} for I_{OUT} = 1A, C_{SS} = open	--	200	--	µs
Soft-Start Charging Current		I_{SS}	V_{SS} = 0.4V	--	440	--	µA
Enable Input Voltage	Logic_High	V_{IH}		1.1	--	5.5	V
	Logic_Low	V_{IL}		0	--	0.4	
Enable Pin Hysteresis		V_{EN_HYS}		--	50	--	mV
Enable Pin Deglitch Time		V_{EN_DG}		--	20	--	µs
Enable Pin Current		I_{EN}	V_{EN} = 5V	--	0.1	1	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PGOOD Trip Threshold	V_{IT}	V_{OUT} decreasing	86	91	95	%V_{OUT}
PGOOD Trip Hysteresis	V_{HYS}		--	3	--	%V_{OUT}
PGOOD Output Low Voltage	V_{PGOOD_L}	I_{PGOOD} = 1mA(sinking), $V_{OUT} < V_{IT}$	--	--	0.3	V
PGOOD Leakage Current	V_{PGOOD_LK}	V_{PGOOD} = 5.25V, $V_{OUT} > V_{IT}$	--	0.1	1	μA
Thermal Shutdown Temperature	T_{SD}	Shutdown, temperature increasing	--	165	--	°C
		Reset, temperature decreasing	--	140	--	

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precautions are recommended.

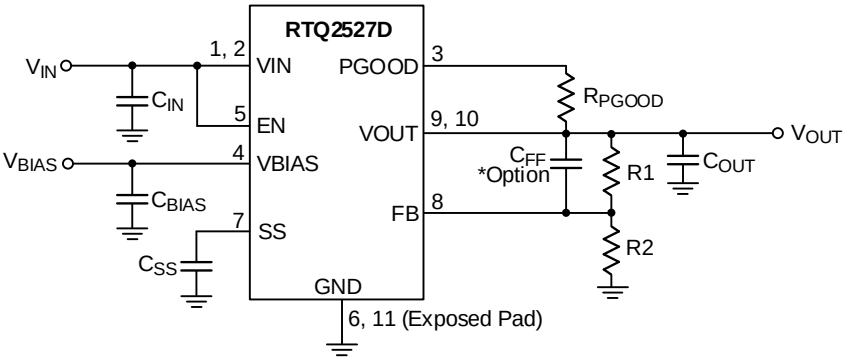
Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 5. $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

Note 6. Guaranteed by design.

15 Typical Application Circuit



*: The feedforward capacitor is optional for the transient response and circuit stability improvement.

Table 1. Suggested Component Value

VOUT (V)	R1 (kΩ)	R2 (kΩ)
0.8	Short	Open
0.9	0.619	4.99
1.0	1.13	4.52
1.05	1.37	4.42
1.1	1.87	4.99
1.2	2.49	4.99
1.5	4.12	4.75
1.8	3.57	2.87
2.5	3.57	1.69
3.3	3.57	1.15

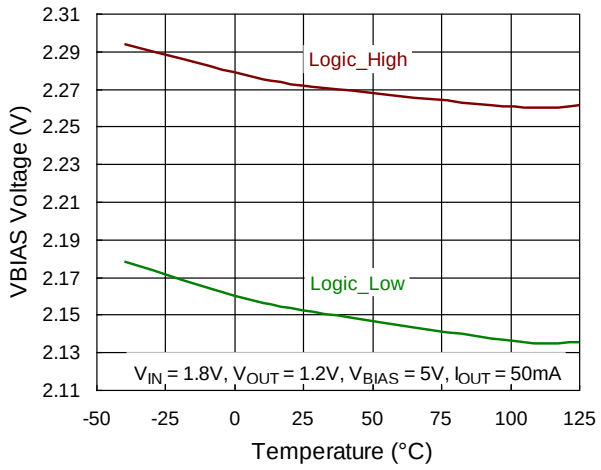
Table 2. Recommended External Components

Component	Description	Vendor P/N
CIN, *COUT	10µF, 16V, X7S, 0805	GCM21BC71C106KE36 (Murata)
CSS	1nF, 50V, X7R, 0603	GCD188R71H102KA01 (Murata)
CBIAS	0.1µF, 50V, X7R, 0603	GCJ188R71H104KA12 (Murata)

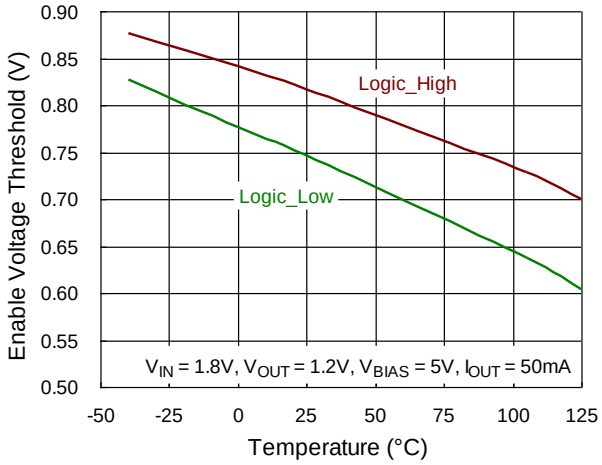
*: Considering the effective capacitance derated with biased voltage level, the COUT component needs satisfy the effective capacitance at least 2.2µF or above at targeted output level for stable and normal operation.

16 Typical Operating Characteristics

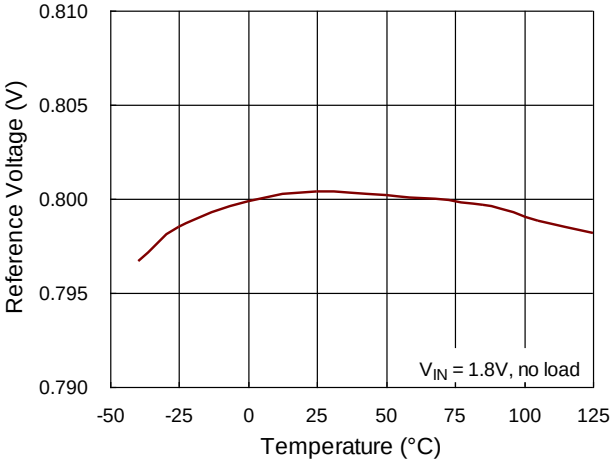
VBIAS Voltage UVLO vs. Temperature



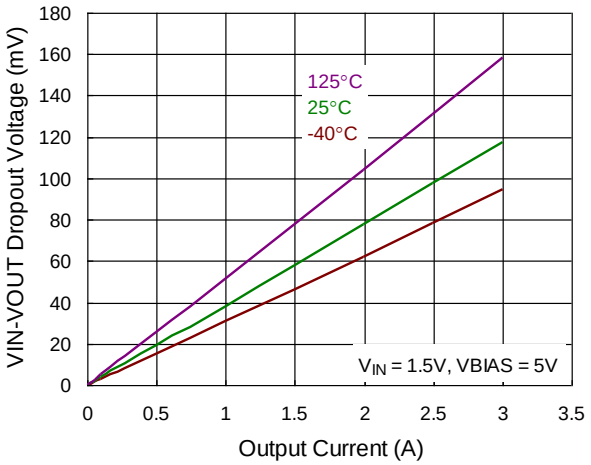
Enable Voltage Threshold vs. Temperature



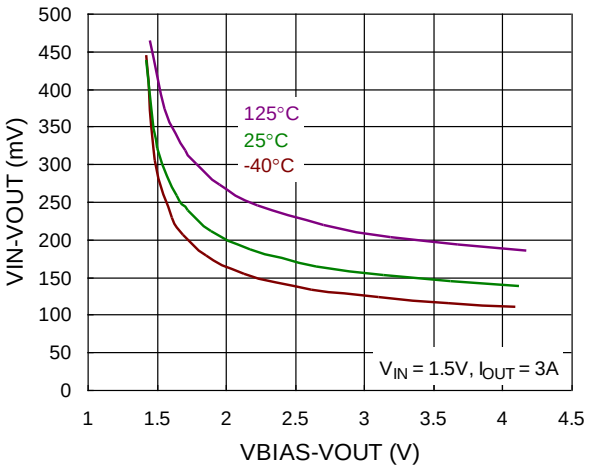
Reference Voltage vs. Temperature



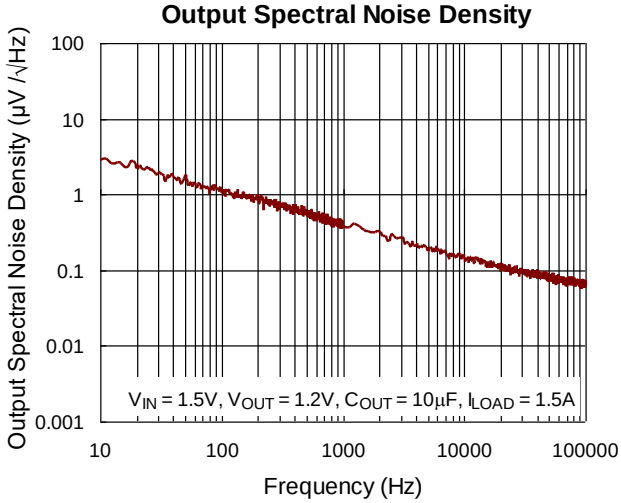
Dropout Voltage vs. Output Current



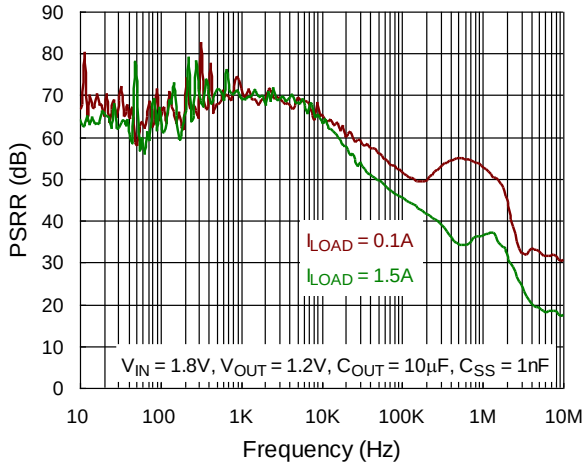
VIN Dropout Voltage vs. (VBIAS - VOUT)



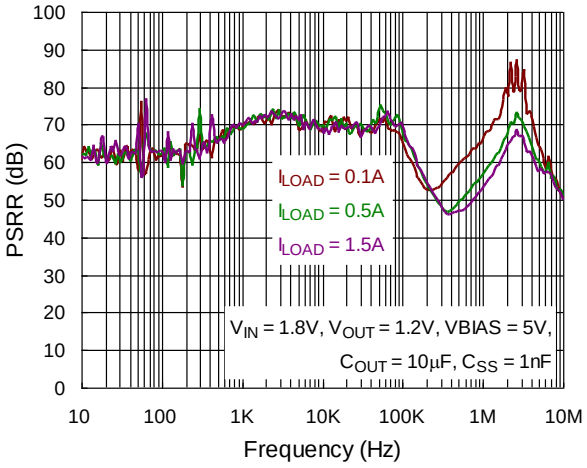
Output Spectral Noise Density



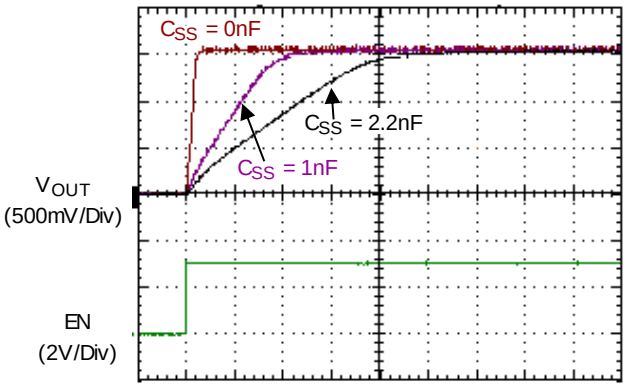
VIN PSRR vs. Frequency



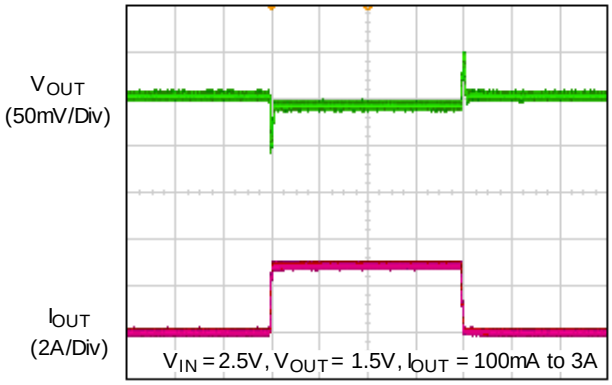
VBIAS PSRR vs. Frequency



Power Up Response



Load Transient Response



17 Operation

The RTQ2527D is a very low dropout linear regulator which operates from input voltage as low as 0.8V. It provides a highly accurate output that is capable of supplying 3A of output current with a typical dropout voltage of only 120mV. Output voltage range is from 0.8V to 3.6V.

17.1 VIN and VBIAS Supply

The VBIAS input supplies the internal reference and LDO circuitry while all output current comes directly from the VIN input for high efficiency regulation. With external VBIAS 3.25V above VOUT, it offers the RTQ2527D very low dropout performance (180mV Max. at 3A), which allows the device to be used in place of a DC-DC converter and still achieve good efficiency. This helps designers to achieve the smallest, simplest, and lowest cost solution.

For applications where an auxiliary bias voltage is not available or low dropout is not required. VBIAS is suggested to be 1.4V above VOUT and attention on power rating and thermal is needed.

17.2 Enable and Shutdown

The EN pin is active high. Applying a voltage above 1.1V ensures the LDO regulator turns on, while the regulator turns off if the V_{EN} is below 0.4V. The enable circuitry has typical 50mV hysteresis and deglitching for use with relatively slow ramping analog signals. That helps to avoid on-off cycling resulting from of small glitches in the V_{EN} signal. A fast rise-time signal must be used to enable the RTQ2527D if precise turn-on timing is required. If not used, EN can be connected to either VIN or VBIAS. If EN is connected to VIN, it should be connected as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

17.3 Soft-Start

The RTQ2527D includes a soft-start feature to prevent excessive current flow during start-up. When the LDO is enabled, an internal soft-start current (I_{SS}) charges the external soft-start capacitor (C_{SS}) to build a ramp-up voltage internally. The RTQ2527D achieves a linear and monotonic soft-start by tracking the voltage ramp until the voltage exceeds the internal reference. The soft-start ramp time can be calculated using Equation 1:

$$t_{SS}(s) = \frac{V_{REF} \times C_{SS}}{I_{SS}} = \frac{0.8V \times C_{SS}(F)}{0.44\mu A} \quad .....(1)$$

17.4 Power Good

When the output voltage is greater than V_{IT} + V_{HYS}, the output voltage is considered good and the open-drain PGOOD pin goes high impedance and is typically pulled high with external resistor. If V_{OUT} drops below V_{IT} or if V_{BIAS} drops below 1.9 V, the open-drain output turns on and pulls the PGOOD output low. The PGOOD pin also asserts when the device is disabled, OCP or OTP triggered.

17.5 Overcurrent Protection

The RTQ2527D has built-in overcurrent protection. When overcurrent (typ. 4.6A) is detected, the RTQ2527D starts foldback and limits the current at typical 2.25A. It allows the device to supply surges of up to 4.6A and prevent the device over-heating if short circuit happens.

17.6 Thermal Protection

The RTQ2527D includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation, and will shut down the LDO when the junction temperature exceeds approximately 165°C. It will re-enable the LDO once the junction temperature drops back to approximately 140°C. The RTQ2527D will cycle in and out of thermal shutdown without latch-up or damage until the overstress condition is removed. Long term overstress (T_J > 125°C) should be avoided as it can degrade the performance or shorten the life of the part.

18 Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The RTQ2527D is a low dropout regulator that features soft-start capability. It provides EN and PGOOD for easy system sequence control, and built-in overcurrent and thermal protection for safe operation.

18.1 Dropout Voltage

Because of the two power supply inputs, VIN and VBIAS, and one VOUT regulator output, there are two Dropout voltages specified. The first is the VIN Dropout voltage, which is the voltage difference (V_{IN} – V_{OUT}) when V_{OUT} starts to decrease by percent specified in the Electrical Characteristics table.

The second, VBIAS dropout voltage, is the voltage difference (V_{BIAS} – V_{OUT}) when VIN and VBIAS pins are joined together and V_{OUT} starts to decrease. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. In these applications, V_{BIAS} is suggested to be 1.4V above V_{OUT} and attention on power rating and thermal is needed.

18.2 Input, Output, and Bias Capacitor Selection

The device is designed to be stable for all available types and values of output capacitors ≥ 2.2μF. The device is also stable with multiple capacitors in parallel, which can be of any type or value. The capacitance required on the VIN and VBIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for VIN is 1μF and minimum recommended capacitor for VBIAS is 0.1μF. If VIN and VBIAS are connected to the same supply, the recommended minimum capacitor for VBIAS is 4.7μF. Good quality, low ESR capacitors should be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors should be placed as close the pins as possible for optimum performance.

18.3 Adjusting the Output Voltage

The output voltage of the RTQ2527D is adjustable from 0.8V to 3.6V by external voltage divider resisters as shown in Typical Application Circuit. R1 and R2 can be used to calculate the output voltage. In order to achieve the maximum accuracy specifications, R2 should be ≤ 4.99kΩ.

18.4 Power-Up Sequence Requirement

The RTQ2527D supports power on the input VIN, VBIAS, and EN pins in any order without damaging the device. Generally, connecting the EN and VIN for most application is acceptable, as long as V_{IN} and V_{EN} are greater than the EN threshold (min. = 1.1V) and the input ramp rate of V_{IN} and V_{BIAS} is faster than the output settled soft-start ramp rate. If the VIN/BIAS input source ramp rate is slower than the output settled soft-start time, the output will track the input supply ramp up level and minus the dropout voltage until it reaches the settled output voltage level. For the other case, if EN is connected with VBIAS, and the provided V_{IN} is present before V_{BIAS}, the output soft-start will work as programmed. If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the settled soft-start time has expired, then V_{OUT} tracks V_{IN} ramp up. If the soft-start time has not expired, output tracks V_{IN} ramp up until output reaches the value set by the charging soft-start capacitor.

18.5 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)}=(T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a WDFN-10L 3x3 package, the thermal resistance, $\theta_{JA(EVB)}$, is 41.5°C/W on a high effective-thermal-conductivity four- layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (41.5°C/W) = 2.41W for a WDFN-10L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

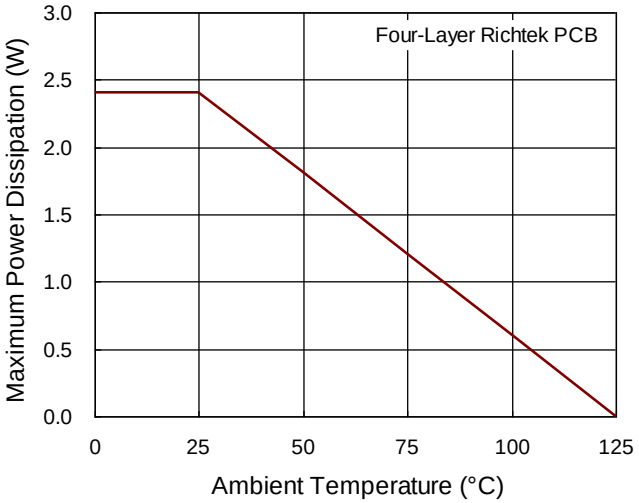


Figure 1. Derating Curve of Maximum Power Dissipation

18.6 Layout Considerations

For best performance of the RTQ2527D, the PCB layout suggestions below are highly recommended:

1. Input capacitor must be placed as close as possible to the IC to minimize the power loop area.
2. Minimize the power trace length and avoid using vias for the input and output capacitors connection.

Figure 2 shows the examples for the layout reference which helps the inductive parasitic components minimization, load transient reduction and good circuit stability.

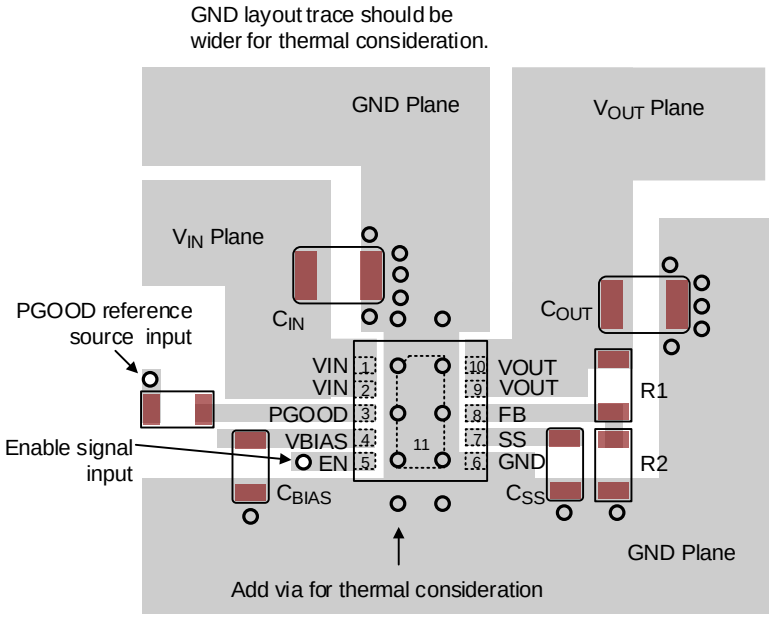
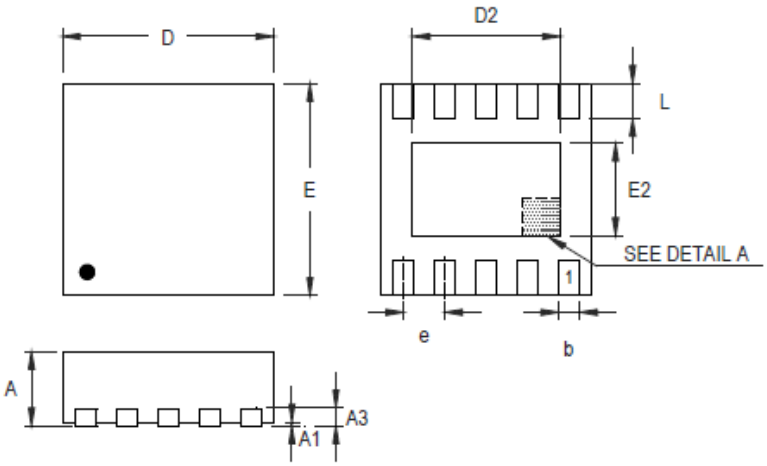
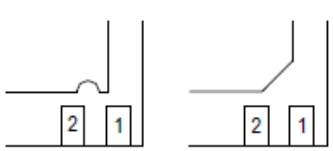


Figure 2. PCB Layout Guide

19 Outline Dimension





DETAIL A

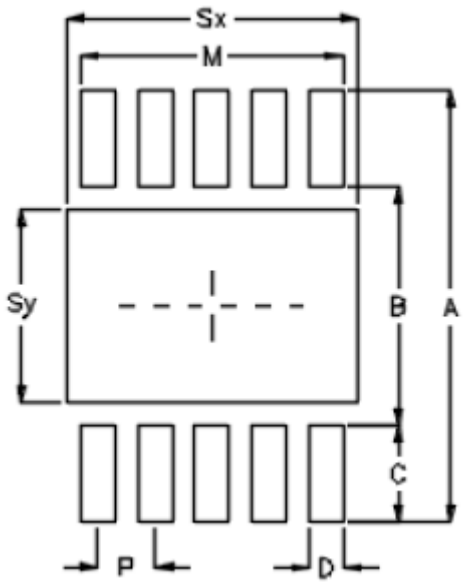
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

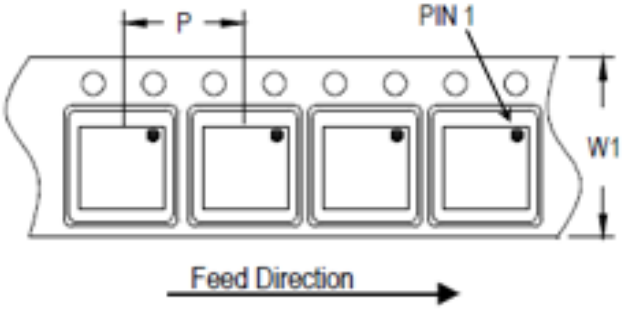
20 Footprint Information

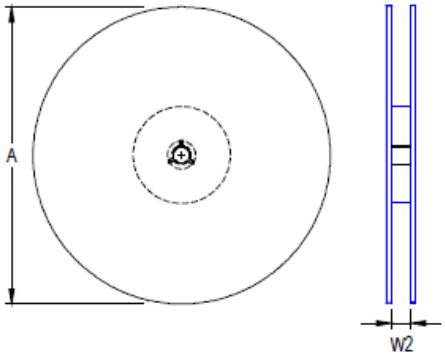


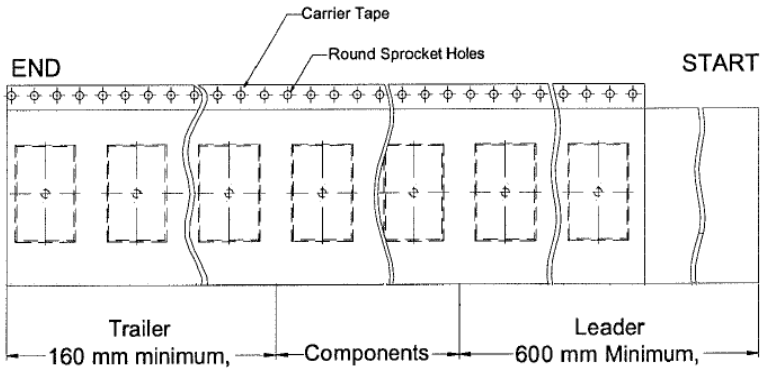
Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/X/ZDFN3*3-10	10	0.50	3.80	2.10	0.85	0.30	2.55	1.70	2.30	±0.05

21 Packing Information

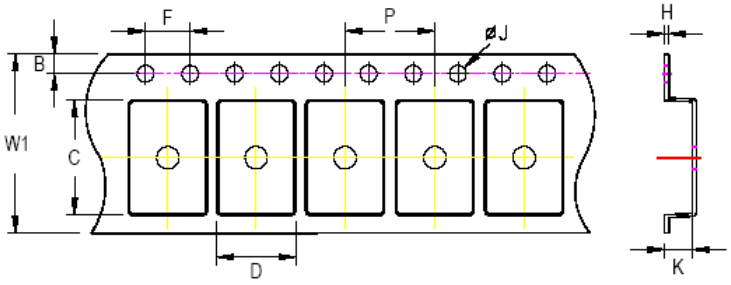
21.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN/DFN 3x3	7”	1,500	Box A	18.3*18.3*8.0	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	1	1,500	For Combined or Partial Reel.			

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

Datasheet Revision History

Version	Date	Description	Item
00	2023/12/6	Final	Ordering Information on P2 Marking Information on P2