4A, 6.5V, Low-Noise, Low-Dropout Linear Regulator

1 General Description

The RTQ2537E is a high-current (4A), low-noise (6.8μV_{RMS}), high accuracy (1% over line, load, and temperature), low-dropout linear regulator (LDO) capable of sourcing 4A with an extremely low dropout (maximum 240mV). The device supports a single input supply voltage as low to 1.1V, which makes it easy to use.

The low-noise, high PSRR, and high output current capability make the RTQ2537E ideal to power noise-sensitive devices such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and RF components. With very high accuracy, remote sensing, and soft-start capabilities to reduce inrush current, the RTQ2537E is ideal for powering digital loads such as FPGAs, DSPs, and ASICs.

The external enable control and power good indicator function make the control sequence easier. The output noise immunity is enhanced by adding an external bypass capacitor on the NR/SS pin. The device is fully specified over the temperature range of T_J = –40°C to 125°C and is offered in the VQFN-20L 3.5x3.5 package.

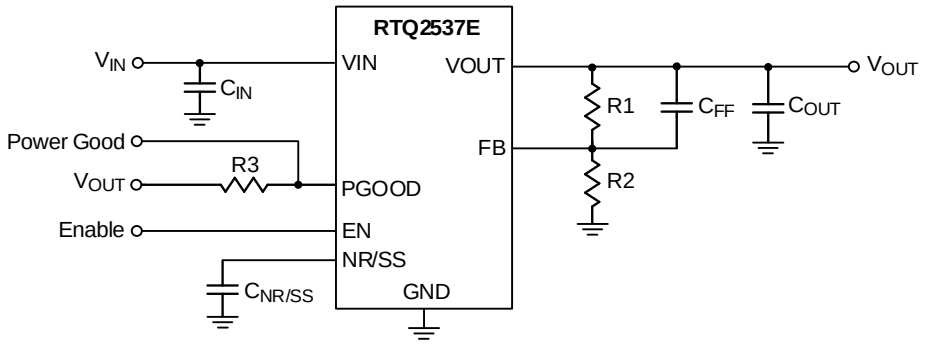
2 Features

- **Input Voltage Range: 1.1V to 6.5V**
- **Two Output Voltage Modes**
  - **0.5V to 5.5V (Set by a Resistive Divider)**
  - **0.5V to 2.075V (Set via PCB Layout, No External Resistor Required)**
- **Accurate Output Voltage Accuracy (1%) Over Line, Load, and Temperature**
- **PSRR: 44dB at 500kHz**
- **Noise Immunity**
  - **6.8μV_{RMS} at 0.5V Output**
  - **16μV_{RMS} at 5V Output**
- **Dropout Voltage: 240mV Maximum at 4A**
- **Enable Control**
- **Programmable Soft-Start Output**
- **Stable with a 47μF or Larger Ceramic Output Capacitor**
- **Support Power-Good Indicator Function**
- **Junction Temperature Range: –40°C to 125°C**

3 Applications

- Portable Electronic Devices
- Wireless Infrastructures: SerDes, FPGA, DSP
- RD, IF, Components: VCO, ADC, DAC, LVDS

4 Simplified Application Circuit



5 Ordering Information

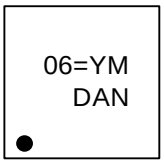
RTQ2537 □□-□□

- Packing
  B: Pin 1 Orientation
  (Quadrant 2, Follow EIA-481)
- Product Grade
  T: Industrial Grade
- Package Type
  N: VQFN-20L 3.5x3.5 (V-Type)
- V_{REF}
  E: 0.5V_{REF}

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information



06=: Product Code
YMDAN: Date Code

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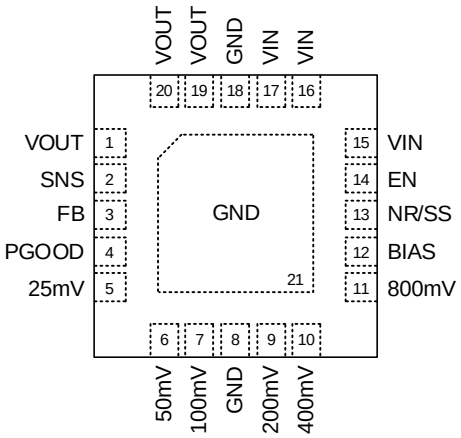
7 Pin Configuration

(TOP VIEW)



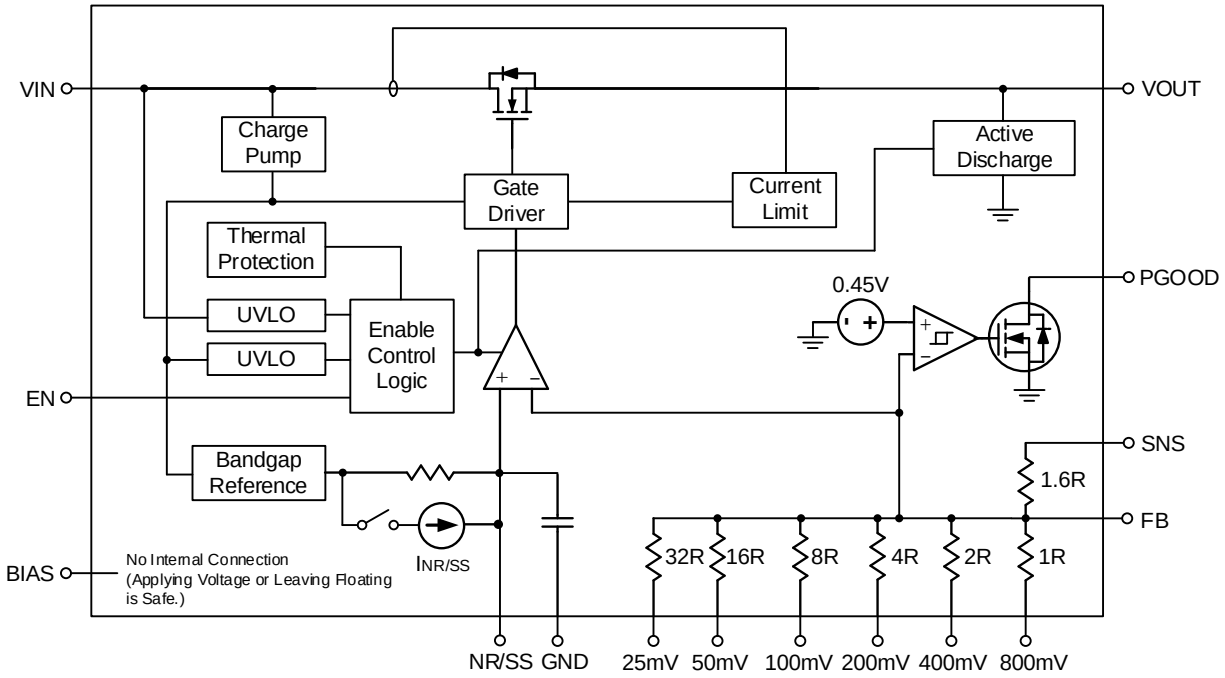
VQFN-20L 3.5x3.5

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 19, 20	VOUT	LDO output pins. A 47μF or larger ceramic capacitor (22μF or greater effective capacitance) is required for stability. Place the output capacitor as close to the device as possible and minimize the impedance between the VOUT pin and the load.
2	SNS	Output voltage sense input pin. Connect this pin only if using the configuration without external resistors. Keep the SNS pin floating if the VOUT voltage is set by an external resistor.
3	FB	Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 0.5V typically.
4	PGOOD	Power good indicator output. This is an open-drain output that is active high when the output voltage reaches 88% of the target. The pin is pulled to ground when the output voltage is lower than its specified thresholds, including EN shutdown, OCP, and OTP.
5, 6, 7, 9, 10, 11	25mV, 50mV, 100mV, 200mV, 400mV, 800mV	Output voltage setting pins. Connect these pins to ground or leave floating. Connecting these pins to ground increases the output voltage by the value of the pin name; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) if the VOUT voltage is set by an external resistor.
8, 18, 21 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
12	BIAS	This pin has no internal IC connection. A BIAS input voltage below 6.5V can be applied to this pin (for compatibility with other vendors), or this pin can be left open (floating). Either option is safe and will not affect IC operation.

Pin No.	Pin Name	Pin Function
13	NR/SS	Noise-reduction and soft-start pin. Decoupling this pin to GND with an external capacitor $C_{NR/SS}$ can reduce output noise to very low levels and also slow down the rising of VOUT, providing a soft-start behavior. For low-noise applications, a 10nF to 1μF $C_{NR/SS}$ is suggested.
14	EN	Enable control input. Connecting this pin to a logic high enables the regulator, and driving this pin low puts it into shutdown mode. The device can have V_{IN} and V_{EN} sequenced in any order without causing damage to the device. However, to ensure the soft-start function works as intended, certain sequencing rules must be applied. Enabling the device after V_{IN} is present is preferred.
15, 16, 17	VIN	Supply input. A general 47μF ceramic capacitor should be placed as close as possible to this pin for better noise rejection.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 1)

- VIN, PGOOD, EN ---------- –0.3V to 7V
- VOUT ---------- –0.3V to 7V
- NR/SS, FB ---------- –0.3V to 3.6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 2)

- ESD Susceptibility
- HBM (Human Body Model) ---------- 2kV

Note 2. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 3)

- Supply Input Voltage, VIN ---------- 1.1V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Note 3. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 4 and Note 5)

Thermal Parameter		VQFN-20L 3.5x3.5	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	38.5	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	50.57	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	2.47	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	39.33	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	5.79	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.06	°C/W

Note 4. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 5. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

Over operating temperature range. (T_J = –40°C to 125°C), (1.1V ≤ V_{IN} ≤ 6.5V and V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.5V, VOUT connected to 50Ω to GND, V_{EN} = 1.1 V, C_{IN} = 10µF, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PGOOD pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.)

(Note 6)

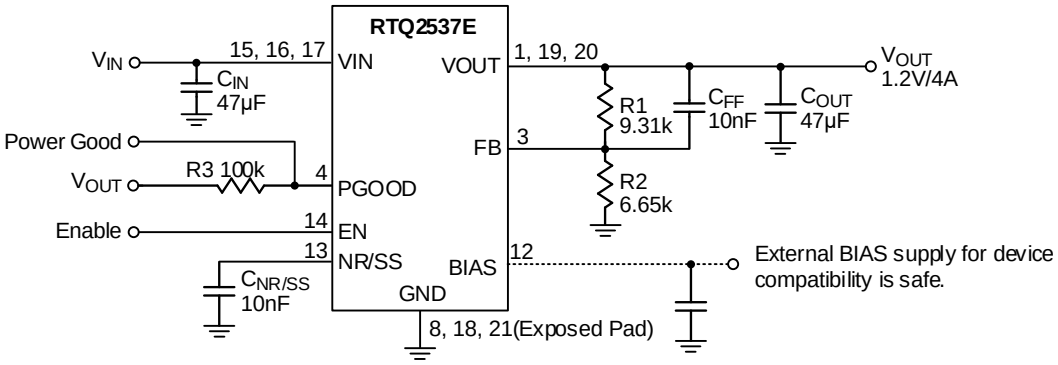
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Supply Input Voltage	V_{IN}		1.1	--	6.5	V
Reference Voltage	V_{REF}		--	0.5	--	V
NR/SS Pin Voltage	$V_{NR/SS}$		--	0.5	--	V
Undervoltage Lockout Rising Threshold	V_{UVLO_R}	V_{IN} increasing	--	1.02	1.085	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	Hysteresis	--	100	--	mV
Output Voltage	V_{OUT}	Using external resistors	0.5	--	5.5	V
		Using voltage setting pins (25mV, 50mV, 100mV, 200mV, 400mV, 800mV)	0.5	--	2.075	V
Output Voltage Accuracy (Note 7)	V_{OUT_ACC}	V_{IN} = V_{OUT} + 0.3V, 0.5V ≤ V_{OUT} ≤ 5.5V, 1mA ≤ I_{OUT} ≤ 4A	–1	--	1	%
Line Regulation	V_{LINE_REG}	I_{OUT} = 1mA, 1.1V ≤ V_{IN} ≤ 6.5V	--	0.05	--	%/V
Load Regulation	V_{LOAD_REG}	1mA ≤ I_{OUT} ≤ 4A	--	0.08	--	%/A
Dropout Voltage	V_{DROP}	V_{IN} = 1.1V to 6.5V, I_{OUT} = 4A, V_{FB} = 0.5V – 3%	--	110	240	mV
Current Limit	I_{LIM}	V_{OUT} = 90%$V_{OUT(TARGET)}$, V_{IN} = $V_{OUT(TARGET)}$ + 400mV	4.5	5.4	6.8	A
Short-Circuit Current Limit	I_{SC}	R_{LOAD} = 20mΩ, under foldback operation	--	2	--	A
Ground Pin Current	I_{GND}	Minimum load, V_{IN} = 6.5V, I_{OUT} = 5mA	--	3	4	mA
		Maximum load, V_{IN} = 1.4V, I_{OUT} = 4A	--	4.3	5.5	mA
Shutdown Current	I_{SHDN}	PGOOD = Open, V_{IN} = 6.5V, V_{EN} = 0.5V	--	1.2	25	µA
EN Pin Current	I_{EN}	V_{IN} = 6.5V, V_{EN} = 0V and 6.5V	–0.1	--	0.1	µA
EN Input Voltage Rising threshold	V_{EN_R}	Enable device	1.1	--	6.5	V
EN Input Voltage Falling threshold	V_{EN_F}	Disable device	0	--	0.5	V
Power-Good Voltage Threshold	V_{PGOOD}	For the direction PGOOD signal falling with decreasing VOUT	0.82 x V_{OUT}	0.883 x V_{OUT}	0.93 x V_{OUT}	V
Power-Good Voltage Hysteresis	V_{PGOOD_HYS}	For PGOOD signal rising	--	2% x V_{OUT}	--	V
PGOOD Pin Low-Level Output Voltage	V_{PGOOD_L}	V_{OUT} < V_{PGOOD}, I_{PGOOD} = –1mA (current into device)	--	--	0.4	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
PGOOD Pin Leakage Current	I_{PGOOD_LK}	V_{OUT} > V_{PGOOD}, V_{PGOOD} = 6.5V		--	--	1	μA
NR/SS Pin Charging Current	$I_{NR/SS}$	$V_{NR/SS}$ = GND, V_{IN} = 6.5V		4	--	9	μA
FB Pin Current	I_{FB}	V_{IN} = 6.5V		−100	--	100	nA
Power Supply Rejection Ratio	PSRR	V_{IN} = 1.2V, I_{OUT} = 4A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 47μF//10μF//10μF	f = 10kHz, V_{OUT} = 0.5V	--	45	--	dB
			f = 500kHz, V_{OUT} = 0.5V	--	44	--	
		V_{IN} - V_{OUT} = 0.4V, I_{OUT} = 4A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 47μF//10μF//10μF	f = 10kHz, V_{OUT} = 5V	--	37	--	
			f = 500kHz, V_{OUT} = 5V	--	31	--	
Output Noise	V_N	BW = 10Hz to 100kHz I_{OUT} = 4A, $C_{NR/SS}$ = 100nF, C_{FF} = 10nF, C_{OUT} = 47μF//10μF//10μF	V_{IN} = 1.1V V_{OUT} = 0.8V	--	6.8	--	μV_{RMS}
			V_{IN} = 3.6V V_{OUT} = 3.3V	--	10	--	
			V_{OUT} = 5V	--	16	--	
Over-Temperature Protection Threshold	T_{OTP}			--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}			--	20	--	

Note 6. $V_{OUT(TARGET)}$ is the expected V_{OUT} value set by the external feedback resistors. The 50Ω load is disconnected when the test conditions specify an I_{OUT} value.

Note 7. External resistor tolerance is not taken into account.

15 Typical Application Circuit



$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) = 0.5V \times \left(1 + \frac{9.31k}{6.65k}\right) = 1.2V$$

Figure 1. Configuration Circuit for V_{OUT} Adjusted by a Resistor Divider

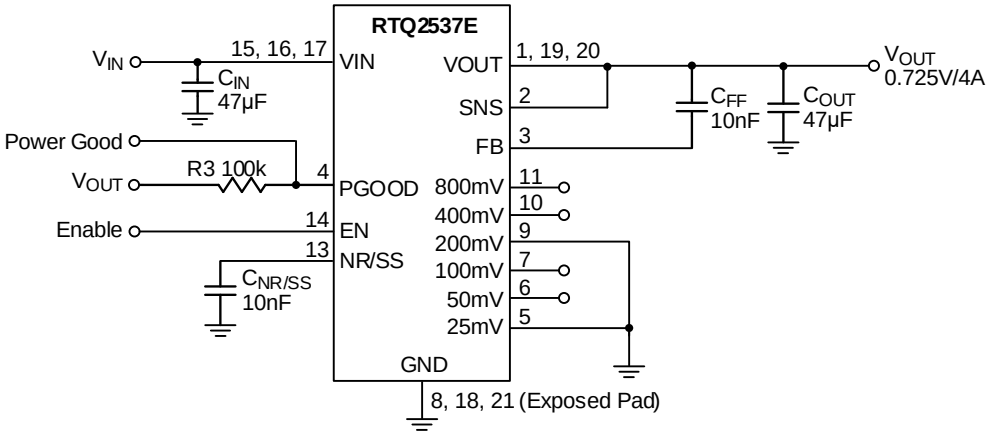
Table 1. Recommended Feedback-Resistor Values

Output Voltage (V)	External Resistor Divider Combination	
	R1(kΩ)	R2(kΩ)
0.8	12	20
0.9	12	15
1	12.4	12.4
1.2	9.31	6.65
1.5	12.4	6.2
1.8	10.2	3.92
2.5	10.2	2.55
3.3	10.7	1.91
4.5	12	1.5
5	10.2	1.13
5.5	10.2	1.02

Table 2. Recommended External Components

Component	Description	Vendor P/N
C_{FF}, $C_{NR/SS}$	10nF, 50V, X7R, 0603	GRM033R71E103KE14 (Murata)
C_{IN}, C_{OUT}(1)	47µF, 16V, X6S, 1210	GRT32EC81C476KE13L (Murata)

Note 8. Marked with (1) indicates: Considering the effective capacitance derated with the biased voltage level, the COUT component needs to satisfy the effective capacitance at least 22µF or above at targeted output level for stable and normal operation.



$V_{OUT} = V_{REF} + 25mv + 200mV = 0.5V + 25mV + 200mV = 0.725V$

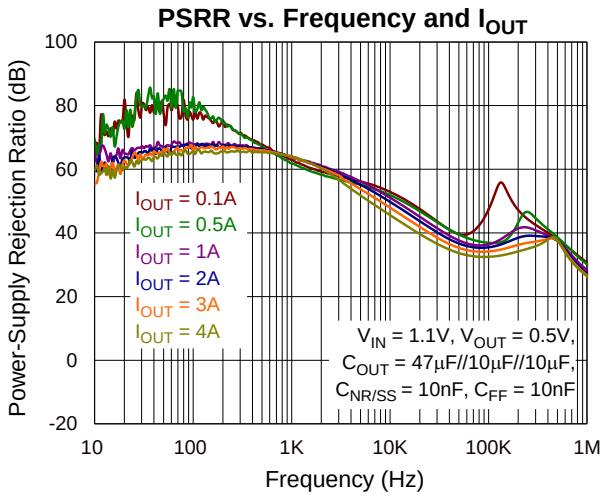
(Table 3 provides a full list for different V_{OUT} targets and the corresponding pin settings.)

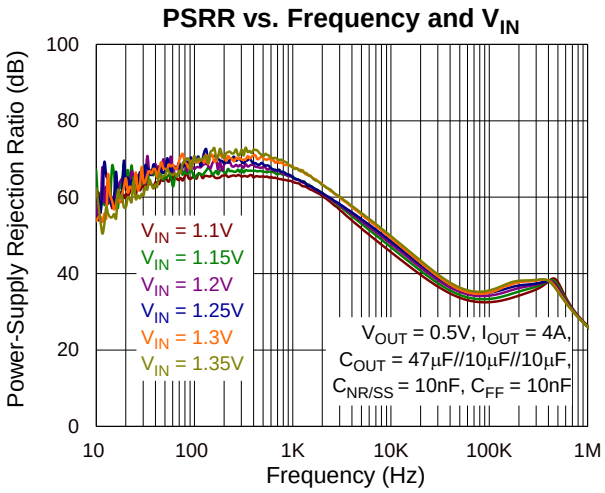
Figure 2. Configuration Circuit for Adjusted V_{OUT} via PCB Layout

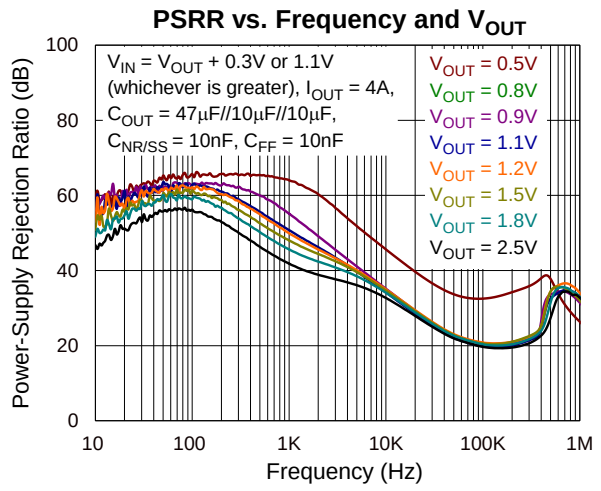
Table 3. V_{OUT} Select Pin Settings for Different Targets

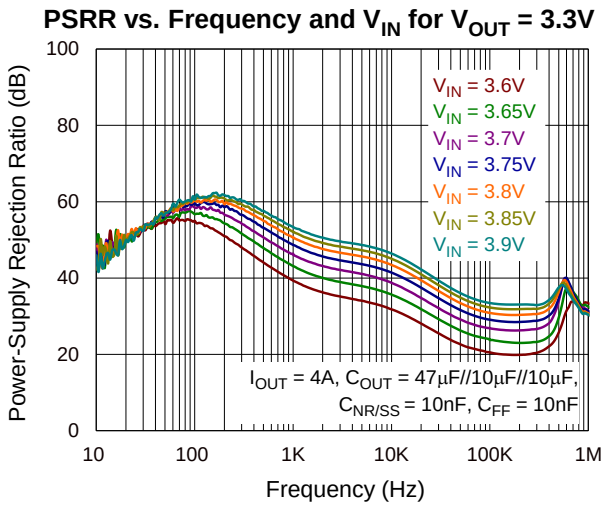
V_{OUT} (V)	25mV	50mV	100mV	200mV	400mV	800mV	V_{OUT} (V)	25mV	50mV	100mV	200mV	400mV	800mV
0.5	Open	Open	Open	Open	Open	Open	1.3	Open	Open	Open	Open	Open	GND
0.525	GND	Open	Open	Open	Open	Open	1.325	GND	Open	Open	Open	Open	GND
0.55	Open	GND	Open	Open	Open	Open	1.35	Open	GND	Open	Open	Open	GND
0.575	GND	GND	Open	Open	Open	Open	1.375	GND	GND	Open	Open	Open	GND
0.6	Open	Open	GND	Open	Open	Open	1.4	Open	Open	GND	Open	Open	GND
0.625	GND	Open	GND	Open	Open	Open	1.425	GND	Open	GND	Open	Open	GND
0.65	Open	GND	GND	Open	Open	Open	1.45	Open	GND	GND	Open	Open	GND
0.675	GND	GND	GND	Open	Open	Open	1.475	GND	GND	GND	Open	Open	GND
0.7	Open	Open	Open	GND	Open	Open	1.5	Open	Open	Open	GND	Open	GND
0.725	GND	Open	Open	GND	Open	Open	1.525	GND	Open	Open	GND	Open	GND
0.75	Open	GND	Open	GND	Open	Open	1.55	Open	GND	Open	GND	Open	GND
0.775	GND	GND	Open	GND	Open	Open	1.575	GND	GND	Open	GND	Open	GND
0.8	Open	Open	GND	GND	Open	Open	1.6	Open	Open	GND	GND	Open	GND
0.825	GND	Open	GND	GND	Open	Open	1.625	GND	Open	GND	GND	Open	GND
0.85	Open	GND	GND	GND	Open	Open	1.65	Open	GND	GND	GND	Open	GND
0.875	GND	GND	GND	GND	Open	Open	1.675	GND	GND	GND	GND	Open	GND
0.9	Open	Open	Open	Open	GND	Open	1.7	Open	Open	Open	Open	GND	GND
0.925	GND	Open	Open	Open	GND	Open	1.725	GND	Open	Open	Open	GND	GND
0.95	Open	GND	Open	Open	GND	Open	1.75	Open	GND	Open	Open	GND	GND
0.975	GND	GND	Open	Open	GND	Open	1.775	GND	GND	Open	Open	GND	GND
1	Open	Open	GND	Open	GND	Open	1.8	Open	Open	GND	Open	GND	GND
1.025	GND	Open	GND	Open	GND	Open	1.825	GND	Open	GND	Open	GND	GND
1.05	Open	GND	GND	Open	GND	Open	1.85	Open	GND	GND	Open	GND	GND
1.075	GND	GND	GND	Open	GND	Open	1.875	GND	GND	GND	Open	GND	GND
1.1	Open	Open	Open	GND	GND	Open	1.9	Open	Open	Open	GND	GND	GND
1.125	GND	Open	Open	GND	GND	Open	1.925	GND	Open	Open	GND	GND	GND
1.15	Open	GND	Open	GND	GND	Open	1.95	Open	GND	Open	GND	GND	GND
1.175	GND	GND	Open	GND	GND	Open	1.975	GND	GND	Open	GND	GND	GND
1.2	Open	Open	GND	GND	GND	Open	2	Open	Open	GND	GND	GND	GND
1.225	GND	Open	GND	GND	GND	Open	2.025	GND	Open	GND	GND	GND	GND
1.25	Open	GND	GND	GND	GND	Open	2.05	Open	GND	GND	GND	GND	GND
1.275	GND	GND	GND	GND	GND	Open	2.075	GND	GND	GND	GND	GND	GND

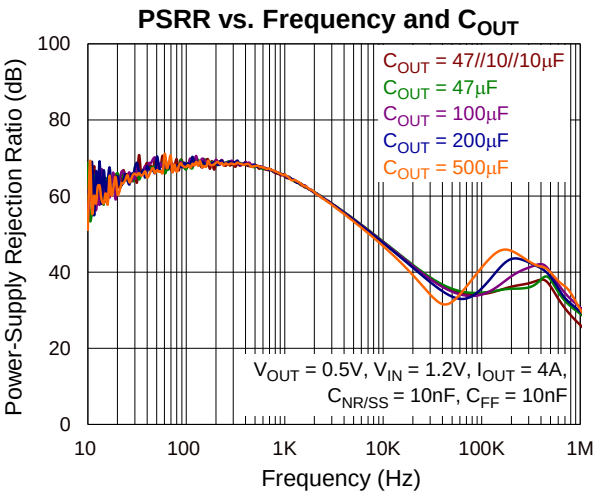
16 Typical Operating Characteristics

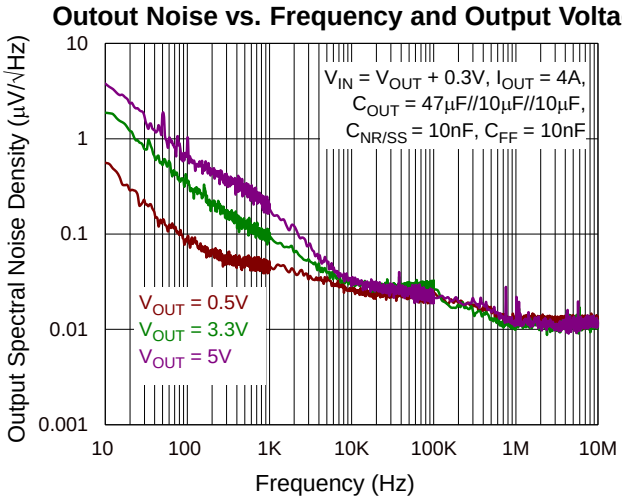




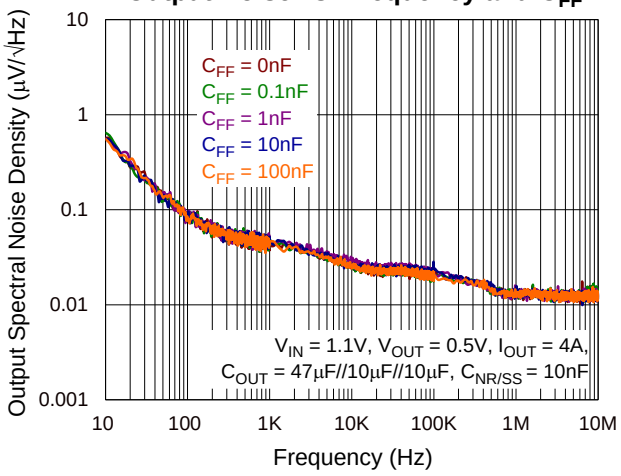




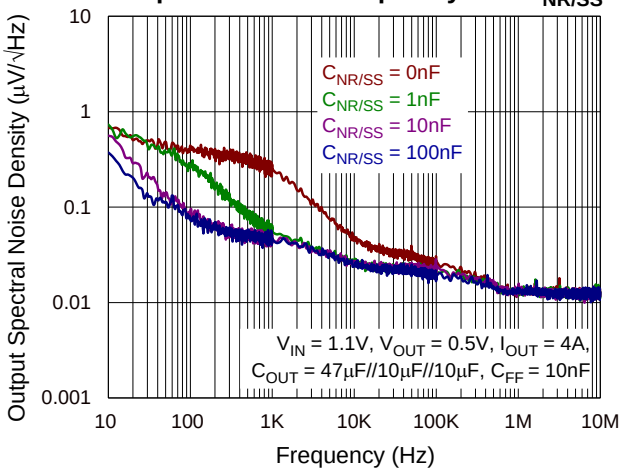




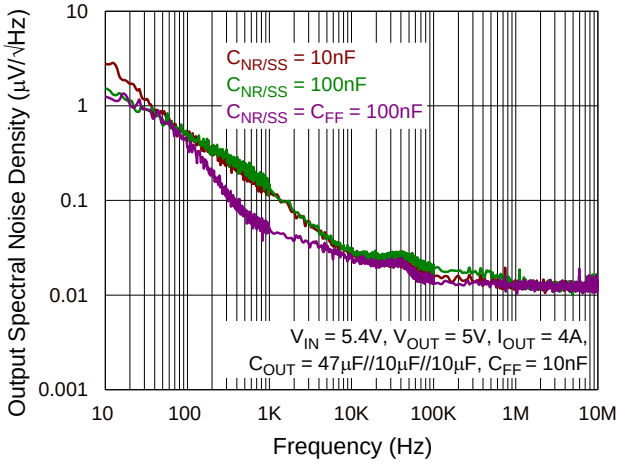
Output Noise vs. Frequency and C_{FF}



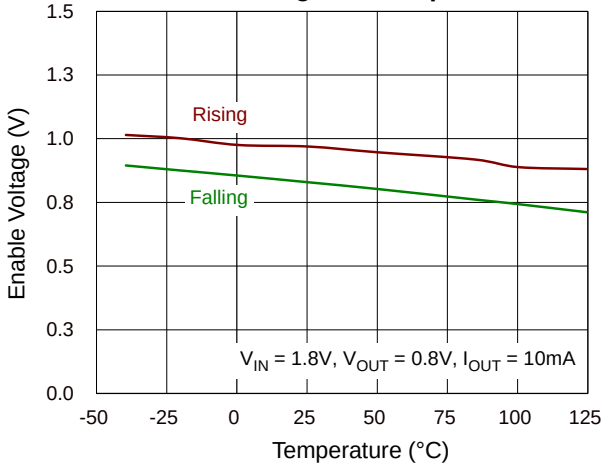
Output Noise vs. Frequency and $C_{NR/SS}$



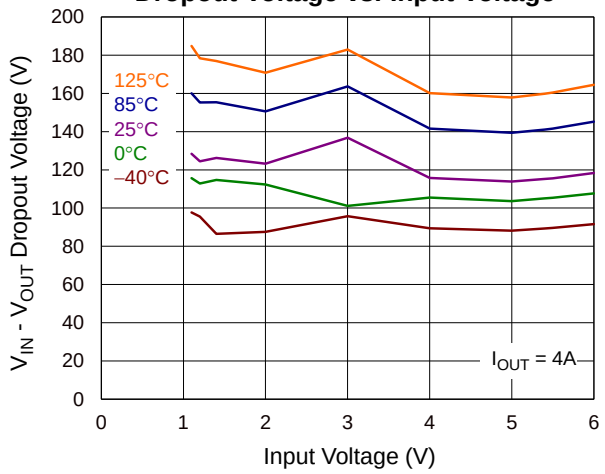
Output Noise at 5V Output



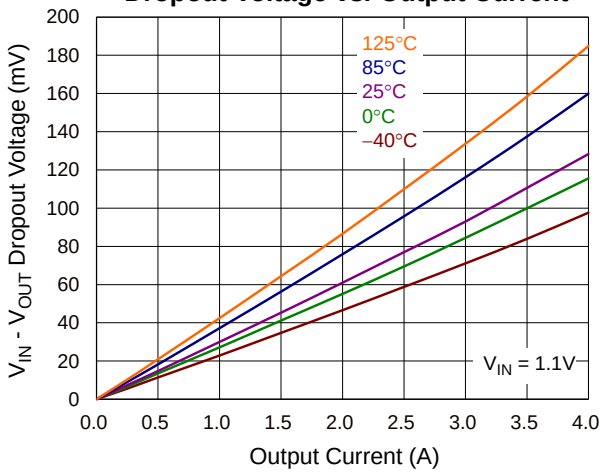
Enable Voltage vs. Temperature



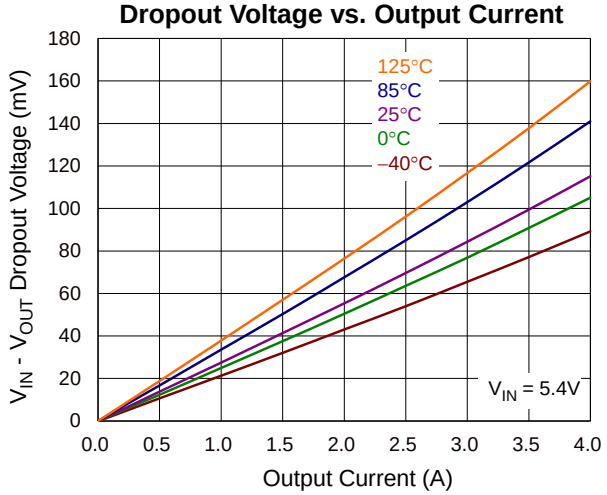
Dropout Voltage vs. Input Voltage



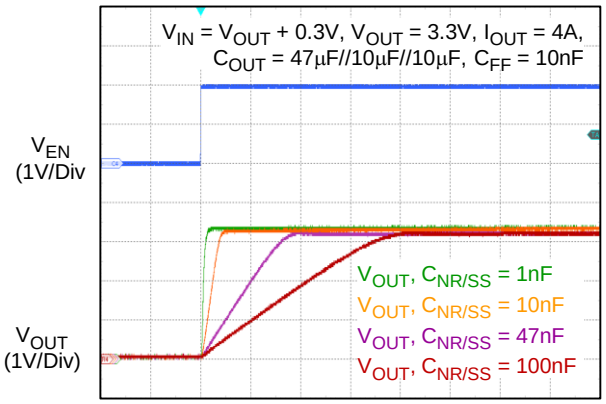
Dropout Voltage vs. Output Current



Dropout Voltage vs. Output Current

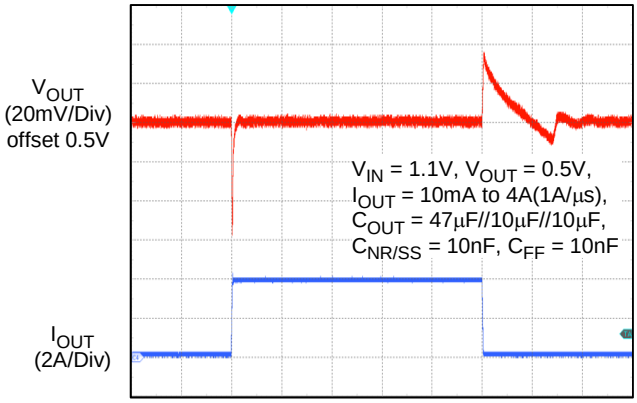


Power-On Response



Time (4ms/Div)

Load Transient Response



Time (100µs/Div)

17 Operation

The RTQ2537E operates with a single supply input ranging from 1.1V to 6.5V and is capable of delivering up to 4A current to the output. The device features high PSRR and low noise to provide a clean supply to the application.

A low-noise reference and error amplifier are included to reduce device noise. The NR/SS capacitor filters the noise from the reference, and the feed-forward capacitor filters the noise from the error amplifier. The high power-supply rejection ratio (PSRR) of the RTQ2537E minimizes the coupling of input supply noise to the output.

17.1 Enable and Shutdown

The RTQ2537E provides an EN pin, as an external chip enable control, to enable or disable the device. V_{EN} below 0.5V turns the regulator off and enters shutdown mode, while V_{EN} above 1.1V turns the regulator on. When the regulator is shut down, the ground current is reduced to a maximum of 25μA. The enable circuitry has hysteresis (typically 120mV) for use with relatively slowly ramping analog signals.

If not used, connect the EN pin as close as possible to the largest capacitance on the input to prevent voltage droops on the VIN line from triggering the enable circuit.

17.2 VOUT Programming Pins

The built-in matched feedback resistor network of the RTQ2537E can set the output voltage. The output voltage can be programmed from 0.8V to 2.075V in 25mV steps when tying these programming pins 5, 6, 7, 9, 10, and 11 to ground. Tying any of the VOUT programming pins to SNS can lower the value of the upper resistor divider. Hence the VOUT programming resolution is increased.

17.3 Programmable Soft-Start

The noise-reduction capacitor ($C_{NR/SS}$) reduces noise and programs the soft-start ramp time during turn-on. When EN and UVLO exceed the respective threshold voltage, the RTQ2537E activates a quick-start circuit to charge the noise reduction capacitor ($C_{NR/SS}$) and then the output voltage ramps up.

17.4 Power Good

The power-good circuit monitors the feedback pin voltage to indicate the status of the output voltage. The open-drain PGOOD pin requires an external pull-up resistor to an external supply, and any downstream device can receive power-good as a logic signal that can be used for sequencing. A pull-up resistor from 10kΩ to 100kΩ is recommended. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device or devices.

After start-up, the PGOOD pin becomes high impedance when the feedback voltage exceeds V_{PGOOD_HYS} (typically 90% of 0.5V reference voltage level). The PGOOD is pulled to GND when the feedback pin voltage falls below the V_{PGOOD}. When EN is low, the current limit or OTP levels are reached.

17.5 Undervoltage Lockout (UVLO)

The UVLO circuit monitors the input voltage to prevent the device from turning on before V_{IN} rises above the V_{UVLO} threshold. The UVLO circuit also disables the output of the device when V_{IN} falls below the lockout voltage ($V_{UVLO\_R} - V_{UVLO\_HYS}$). The UVLO circuit responds quickly to glitches on V_{IN} and attempts to disable the output of the device if V_{IN} collapses.

17.6 Internal Current Limit (I_{LIM})

The RTQ2537E continuously monitors the output current to protect the device against high load current faults or short events. The current limit circuitry is not intended to allow operation above the rated current of the device. Continuously running the RTQ2537E above the rated current degrades the reliability of the device.

During current limit, the output voltage falls when the load impedance decreases. If the output voltage is low,

excessive power may cause the output thermal shutdown.

A foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If the load current demand exceeds the foldback current limit before EN goes high, the device does not turn on.

17.7 Over-Temperature Protection (OTP)

The RTQ2537E implements over-temperature protection. The device is disabled when the junction temperature (T_J) exceeds 160°C (typical). The LDO automatically turns on again when the temperature falls below 140°C (typical).

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

17.8 Output Active Discharge

When the device is disabled, the RTQ2537E discharges the LDO output (via VOUT pins) through an internal current sink to ground. Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply collapses because reverse current can possibly flow from the output to the input. External current protection should be added if the device works at a reverse voltage state.

18 Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The RTQ2537E is a high-current, low-noise, high-accuracy, low-dropout linear regulator which is capable of sourcing 4A with a maximum dropout of 240mV. The input voltage operating range is 1.1V to 6.5V, and the adjustable output voltage is 0.5V to 5.5V, which can be set according to the external resistor setting to get the required output target.

18.1 Output Voltage Setting

The output voltage of the RTQ2537E can be set using external resistors to achieve different output targets.

By using external resistors, the output voltage is determined by the values of R1 and R2, as shown in Figure 3. The values of R1 and R2 can be calculated for any voltage value using the following formula:

$$V_{OUT} = 0.5 \times \frac{R1 + R2}{R2}$$

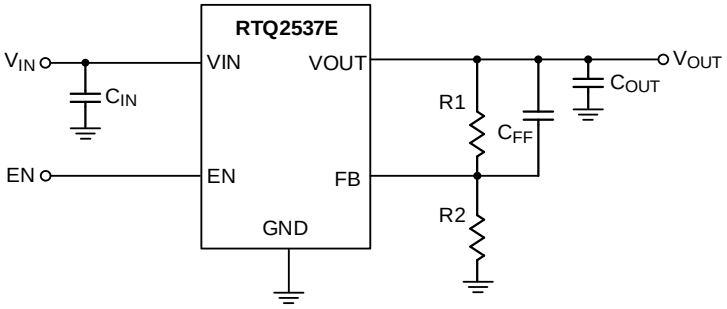
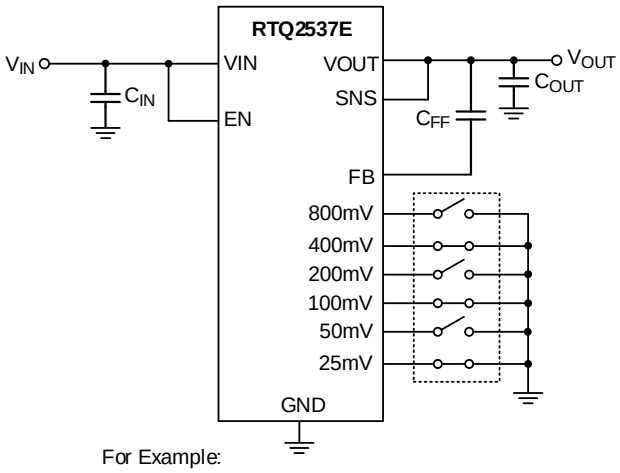


Figure 3. Output Voltage Set by External Resistors

The RTQ2537E can also short pins 5, 6, 7, 9, 10, and 11 to ground and program the regulated output voltage level without external resistors after the SNS pin is connected to the VOUT. Pins 5, 6, 7, 9, 10, and 11 are connected to internal resistor pairs. Each pin is either connected to ground (active) or left open (floating).

Voltage programming is set by the sum of the internal reference voltage (V_{REF} = 0.5V) plus the accumulated sum of the respective voltages assigned to each active pin, as illustrated in Figure 4.



For Example:

V_{OUT} = 0.5V + (Output Setting Pins to Ground)

= 0.5V + (0.4V + 0.1V + 0.025V) = 1.025V

Figure 4. Output Setting without External Resistors

Table 3 summarizes these voltage values associated with each active pin setting for reference. By leaving all programming pins open, or floating, the output is programmed to the minimum possible output voltage, which is equal to V_{REF} (0.5V). The maximum output target can be supported up to 2.075V after all pins 5, 6, 7, 9, 10, and 11 are shorted with ground at the same time.

18.2 Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at a specific output current. The dropout voltage V_{DROP} can also be expressed as the voltage drop on the pass-FET at a specific output current (I_{RATED}) while the pass-FET is fully operating in the ohmic region. The pass-FET can be characterized as a resistance $R_{DS(ON)}$. Thus, the dropout voltage can be defined as ($V_{DROP} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{RATED}$). For normal operation, the suggested LDO operating range is ($V_{IN} > V_{OUT} + V_{DROP}$) for good transient response and PSRR performance. However, operation in the ohmic region will degrade the performance severely.

18.3 C_{IN} and C_{OUT} Selection

The RTQ2537E is designed to support low-series- resistance (ESR) ceramic capacitors. X7R, X5R, and COG rated ceramic capacitors are recommended due to their good capacitive stability across different temperatures, whereas the use of Y5V-rated capacitors is not recommended because of their large capacitance variations.

However, the capacitance of ceramic capacitors varies with operating voltage and temperature, and design engineers must be aware of these characteristics. Ceramic capacitors are usually recommended to be derated by 50%. A 47μF or greater output ceramic capacitor (or 22μF effective capacitance) is suggested to ensure stability. Input capacitance is selected to minimize transient input drop during load current steps. For general applications, an input capacitor of at least 47μF is highly recommended for minimal input impedance. If the trace inductance between the RTQ2537E input pin and power supply is high, a fast load transient can cause VIN voltage level ringing above the absolute maximum voltage rating which damages the device. Adding more input capacitors can restrict the ringing and keep it below the device absolute maximum ratings.

Generally, a 47μF 1210-sized ceramic capacitor in parallel with two 10μF 0805-sized ceramic capacitors ensures the minimum effective capacitance at high input voltage and high output voltage requirements. Place these capacitors as close to the pins as possible for optimum performance and to ensure stability.

18.4 Feed-Forward Capacitor (C_{FF})

The RTQ2537E is designed to be stable without the external feed-forward capacitor (C_{FF}). However, a 10nF external feed-forward capacitor optimizes the transient, noise, and PSRR performances. A higher capacitance of C_{FF} can also be used, but the start-up time will be longer and the power-good signal will incorrectly indicate that the output voltage is settled.

18.5 Soft-Start and Noise Reduction ($C_{NR/SS}$)

The RTQ2537E is designed for a programmable, monotonic soft-start time during the output rising, which can be achieved via an external capacitor ($C_{NR/SS}$) on the NR/SS pin. Using an external $C_{NR/SS}$ is recommended for general applications; it is not only for the in-rush current minimization but also to help reduce the noise component from the internal reference.

During the monotonic start-up procedure, the error amplifier of the RTQ2537E tracks the voltage ramp of the external soft-start capacitor ($C_{NR/SS}$) until the voltage approaches the internal reference of 0.5V. The soft-start ramp time can be calculated with Equation a1, which depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference of 0.5V (V_{REF}).

$$t_{SS} = \frac{(V_{REF} \times C_{NR/SS})}{I_{NR/SS}} \quad (a1)$$

For noise-reduction, $C_{NR/SS}$ in conjunction with an internal noise-reduction resistor forms a low-pass filter (LPF) and filters out the noise from the internal bandgap reference before it is amplified via the error amplifier, thus reducing the total device noise floor.

18.6 Input Inrush Current

During start-up, the input Inrush current into the VIN pin consists of the sum of load current and the charging current of the output capacitor. The inrush current is difficult to measure because the input capacitor must be removed, which is not recommended. Generally, the soft-start inrush current can be estimated by Equation b1, where $V_{OUT}(t)$ is the instantaneous output voltage of the power-on ramp, $dV_{OUT}(t)/dt$ is the slope of the V_{OUT} ramp, and R_{LOAD} is the resistive load impedance.

$$I_{OUT}(t) = \frac{\left(C_{OUT} \times dV_{OUT}(t)\right)}{dt} + \left(\frac{V_{OUT}(t)}{R_{LOAD}}\right) \quad (b1)$$

18.7 Undervoltage Lockout (UVLO)

The Undervoltage Lockout (UVLO) threshold is the minimum input operational voltage range that ensures the device stays disabled. Figure 5 explains that the UVLO circuits are triggered between three different input voltage events (durations a, b, and c), assuming $V_{EN} \geq V_{EN\_H}$ all the time. For duration “a”, the input voltage starts rising. When VIN is over the UVLO rising threshold, VOUT starts the power-on process. Then when V_{OUT} reaches the target level, it is under regulation. During “b”, although the power line has a voltage drop, it does not drop below the UVLO low threshold (falling threshold). As a result, the device maintains normal operation, and VOUT is still regulated. At duration “c”, VIN drops below the UVLO falling threshold, so the control loop is disabled and there is no regulation. Meanwhile, VOUT drops. For general applications, an instant power line transient with a long power trace at the VIN pin may have VIN level unstable and force a trap, as shown in duration “c”, which makes VOUT collapse. In this case, adding more input capacitance or improving input trace layout on PCB are effective to improve input power stabilization.

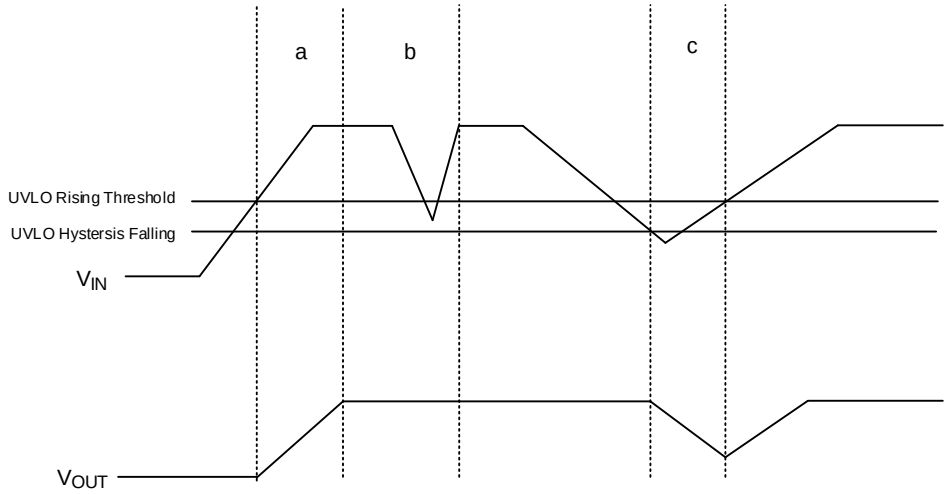


Figure 5. Undervoltage Lockout Trigging Conditions and Output Variation

18.8 Power-Good (PGOOD) Function

The power-good function monitors the voltage level at the feedback pin to indicate whether the output voltage status is normal or not. This function enables other devices to receive the RTQ2537E's power-good signal as a logic signal that can be used for the sequence design of the system application. The PGOOD pin is an open-drain structure and an external pull-up resistor connected to an external supply is necessary. A pull-up resistor value between 10kΩ to 100kΩ is recommended for proper operation. The lower limit of 10kΩ results from the maximum pull-down strength of the power-good transistor, and the upper limit of 100kΩ results from the maximum leakage

current at the power-good node.

Figure 6 demonstrates some PGOOD scenarios versus VIN, EN, and protection status. During “a”, V_{EN} is higher than the V_{EN_H} threshold, and the device is under operation. In this period, V_{OUT} starts rising (the rising time is related to the soft-start capacitor $C_{NR/SS}$). When V_{OUT} is over the PGOOD hysteresis threshold, the reflected feedback voltage V_{FB} exceeds V_{PGOOD_HYS} threshold. Consequently, the PGOOD pin becomes a high impedance node. The duration “b” indicates some unpredictable operation (for example, OTP, OCP, or a severe output voltage drop caused by a very fast load variation). When V_{FB} is lower than the V_{PGOOD} threshold, V_{PGOOD} is pulled to GND, which indicates that the output voltage is not ready. In duration “c”, V_{OUT} has a small drop which is not lower than the PGOOD falling threshold; the PGOOD pin remains in high impedance. After V_{EN} becomes logic “0”, V_{PGOOD} is pulled to GND, as shown in duration “d”.

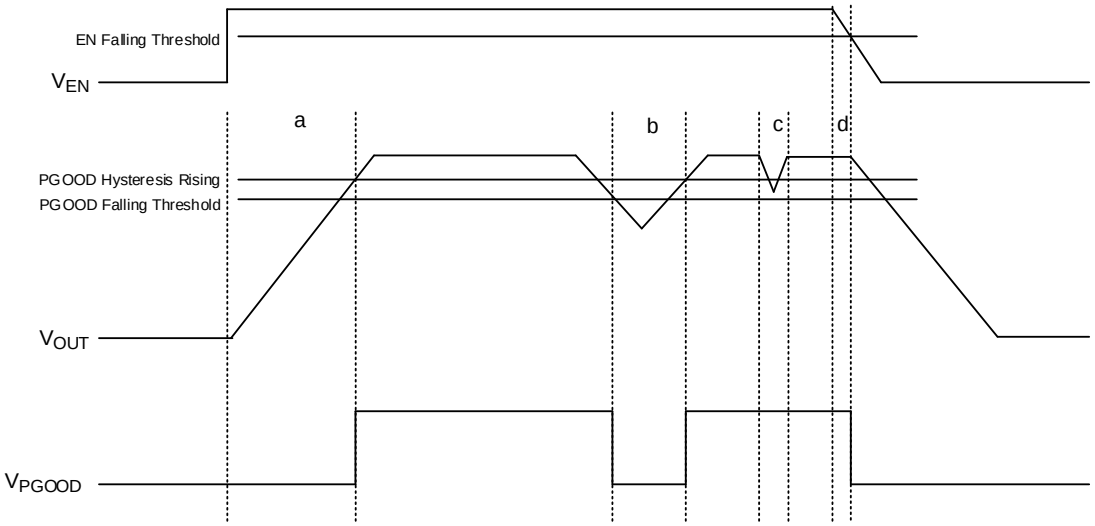


Figure 6. PGOOD Trigger Scenario with Different Operating Status

18.9 Reverse Current Protection

The reverse current from V_{OUT} to V_{IN} that flows through the body diode of the pass element instead of the normal conducting channel can happen if the maximum V_{OUT} exceeds V_{IN} + 0.3V; in this case, the pass element may be damaged.

For example, if the output is biased above the input supply voltage level or the input supply has an instant drop at light load operation that makes $V_{IN} < V_{OUT}$. As shown in Figure 7, an external Schottky diode can be added to prevent the pass element from being damaged by the reverse current.

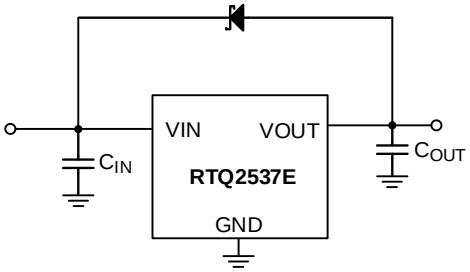


Figure 7. Application Circuit for Reverse Current Protection

18.10 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated

using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a VQFN-20L 3.5x3.5 package, the thermal resistance, $\theta_{JA(EVB)}$, is 39.33°C/W on a standard high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (39.33°C/W) = 2.54W for a VQFN-20L 3.5x3.5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curve in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

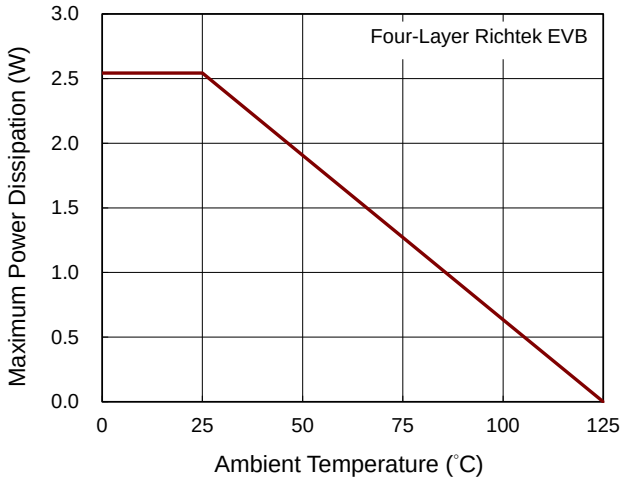


Figure 8. Derating Curve of Maximum Power Dissipation

18.11 Layout Considerations

For the best performance of the RTQ2537E, the PCB layout suggestions below are highly recommended.

1. All circuit components should be placed on the same side and as close to the respective LDO pins as possible.
2. Place the ground return path connection to the input and output capacitor.
3. Connect the ground plane with a wide copper surface for good thermal dissipation.
4. Using vias and long power traces for the input and output capacitors connections is not recommended and has negative effects on performance.
5. Figure 9 show a layout example that reduces conduction trace loops, helping to minimize inductive parasitic and load transient effects while improving the circuit stability.

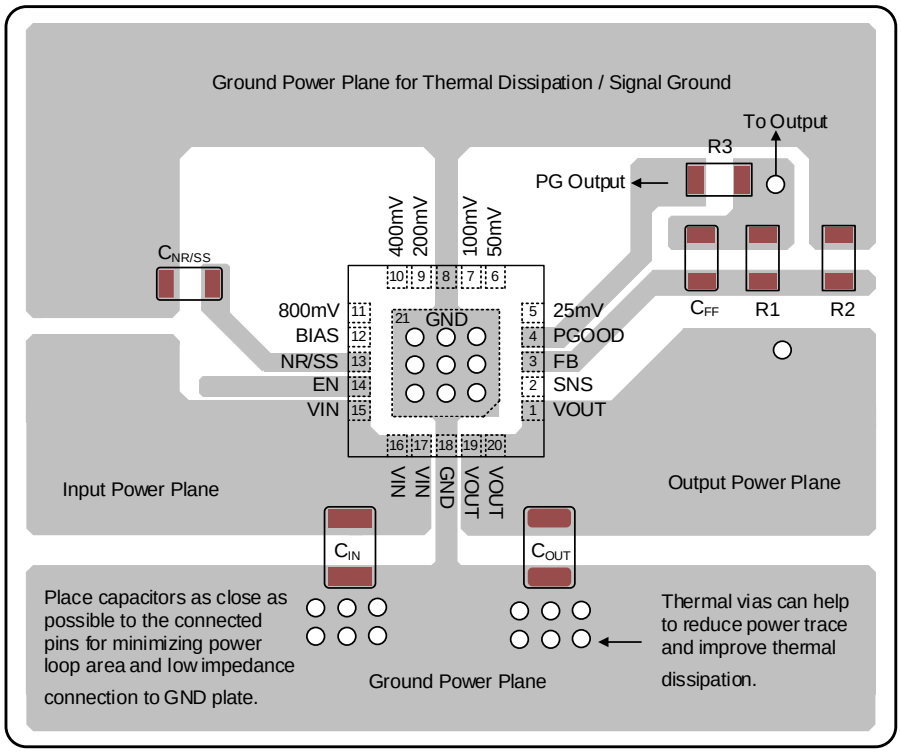
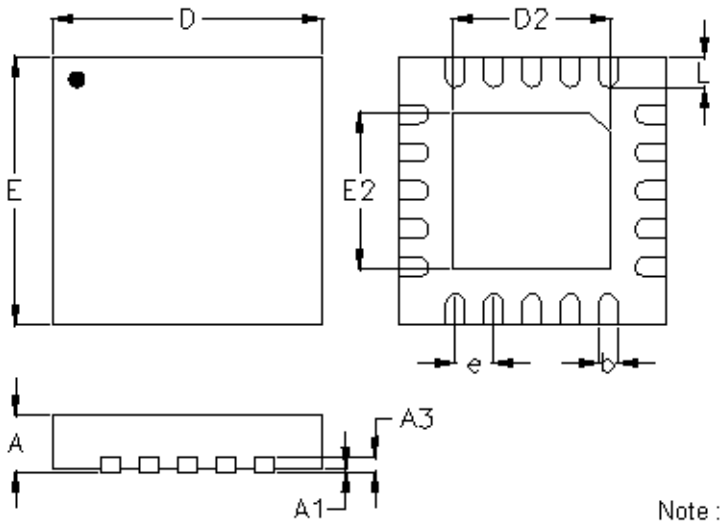
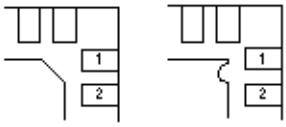


Figure 9. PCB Layout Guide for VQFN-20L 3.5x3.5 Package

19 Outline Dimension





DETAIL A

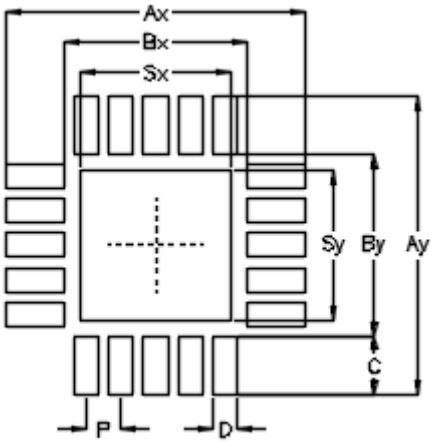
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	3.400	3.600	0.134	0.142
D2	2.000	2.100	0.079	0.083
E	3.400	3.600	0.134	0.142
E2	2.000	2.100	0.079	0.083
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 20L QFN 3.5x3.5 Package

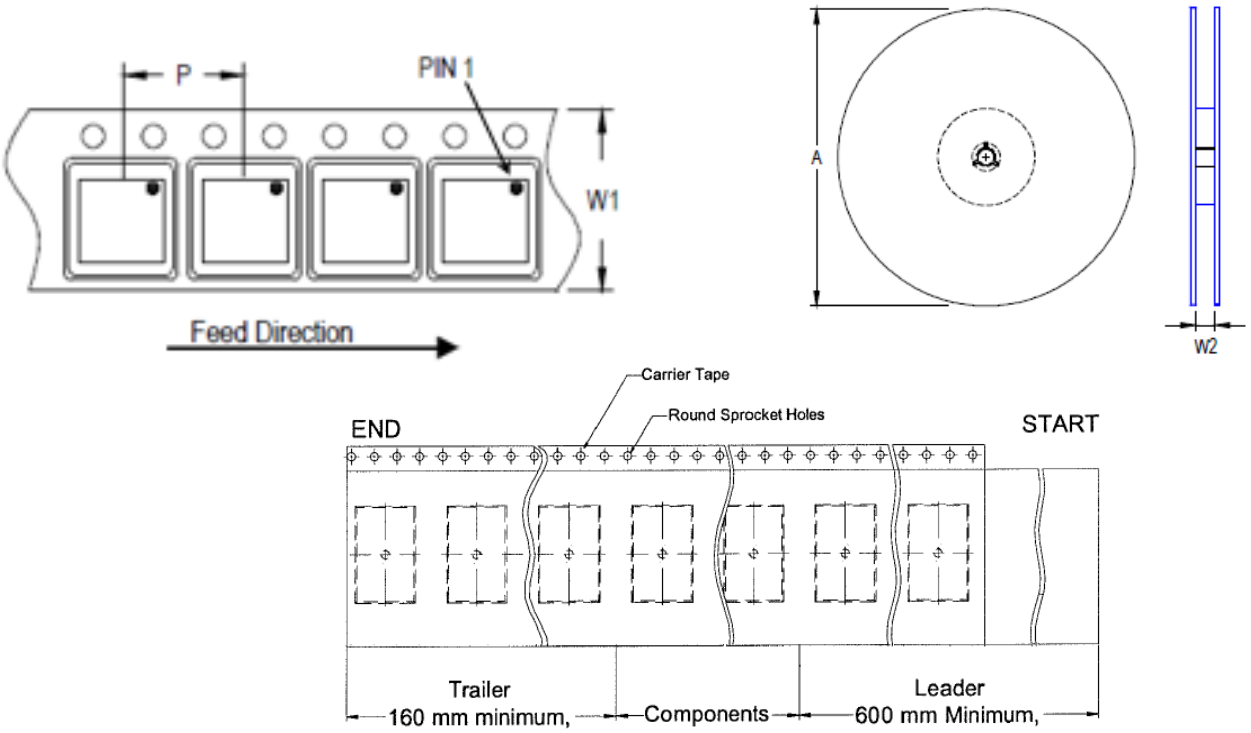
20 Footprint Information



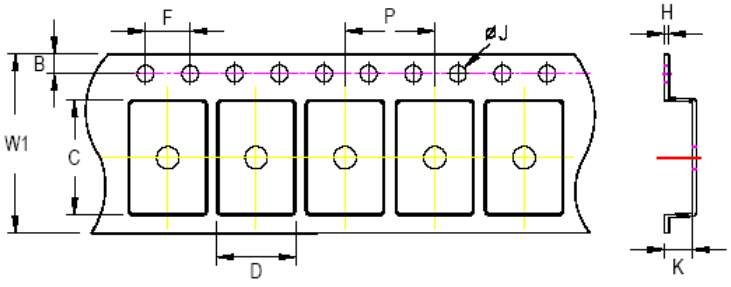
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3.5*3.5-20	20	0.50	4.30	4.30	2.60	2.60	0.85	0.35	2.15	2.15	±0.05

21 Packing Information

21.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3.5x3.5	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box					Carton			
	Size	Units	Item	Size(cm)	Weight(Kg)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN/DFN 3.5x3.5	7”	1,500	Box A	18.3*18.3*8.0	0.1	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	0.03	1	1,500	For Combined or Partial Reel.			

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description	Item
00	2024/3/7	Final	