DDR5 VR on DIMM PMIC

General Description

The RTQ5119A is an integrated solution for DDR5 R/LRDIMM and NVDIMM power management IC. This device provides 4 single Buck voltage regulators (SWA, SWB, SWC and SWD) and 3 LDOs (VLDO_1.0V, VLDO_1.8V and V_{BIAS}). Among the four voltage regulators, the SWA and SWB can operate either in single phase mode or dual phase mode. Moreover, the RTQ5119A supports selectable interface (I^2C or I^3C Basic) to fit various application environment. A complete protection mechanism is also embedded for safe power distribution and the corresponding fault events can be recorded by the registers as well as CAMP and GSI_n open-drain indicators. The RTQ5119A is available in a VQFN-35L.5x5-FC package.

Ordering Information

RTQ5119A□□-□□

- MTP
- Version
- Package Type
  QVF : VQFN-35L 5x5 (FC)
- Lead Plating System
  G : Green
  (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

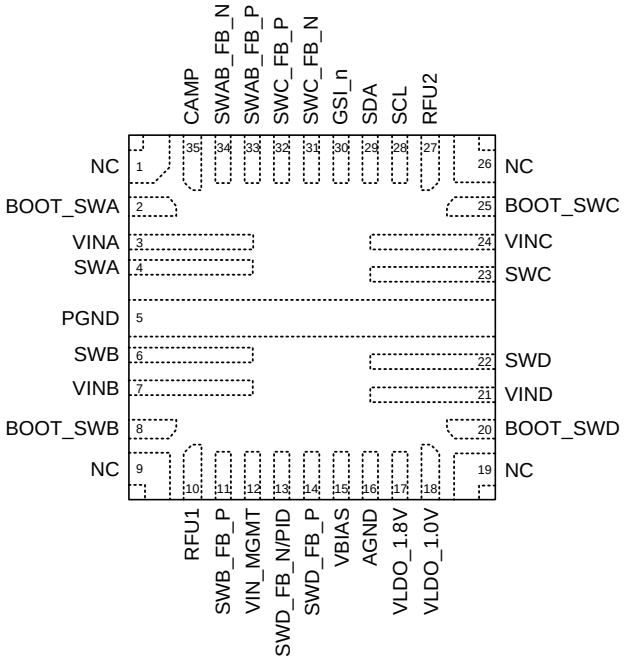
- **Efficiency Up to 91.5% for Each Buck Converter**
- **Smart Protection Unit Provides Best Protection Shutdown Sequence Control**
- **Dual-Phase DEM Operation Implements Good Light Load Efficiency and Good Transient Response**
- **Output Valley Current Limit for Bucks**
- **Meet JEDEC DDR5 PMIC5010 Specification**
  - **PMIC50x0 Compatible Package: VQFN-35L 5x5 (FC)**
  - **Wide Input Supply Range: 4.25V to 15V**
  - **VIN_MGMT Input Supply Range: 3V to 3.6V**
  - **High Integration: 4 x Bucks (3.5A) and 3 LDOs**
    - **Configurable Dual-Phase or Single-Phase Converters (SWA, SWB)**
    - **Single-Phase Converters (SWC, SWD)**
    - **LDOs (V_{BIAS}, VLDO_1.8V, VLDO_1.0V)**
  - **Automatic Input Supply Switch-over for LDOs**
  - **MTP Registers with Secured R/W Access**
  - **Support I^2C / I^3C Basic Slave Control**
  - **0.75% Converter Output Accuracy**
  - **Support Pure MLCC Output Capacitor Stable**
  - **Telemetry for Output Current, Voltage and Power**
  - **Error Log Counter & Data Storage (NVM)**
  - **Complete Protection Mechanisms**

Applications

- DDR5 LR-/RDIMM, NVDIMM

Pin Configuration

(TOP VIEW)



VQFN-35L 5x5 (FC)

Marking Information

RTQ5119AQVF-XX : Product Number
YMDNN : Date Code

Simplified Application Circuit

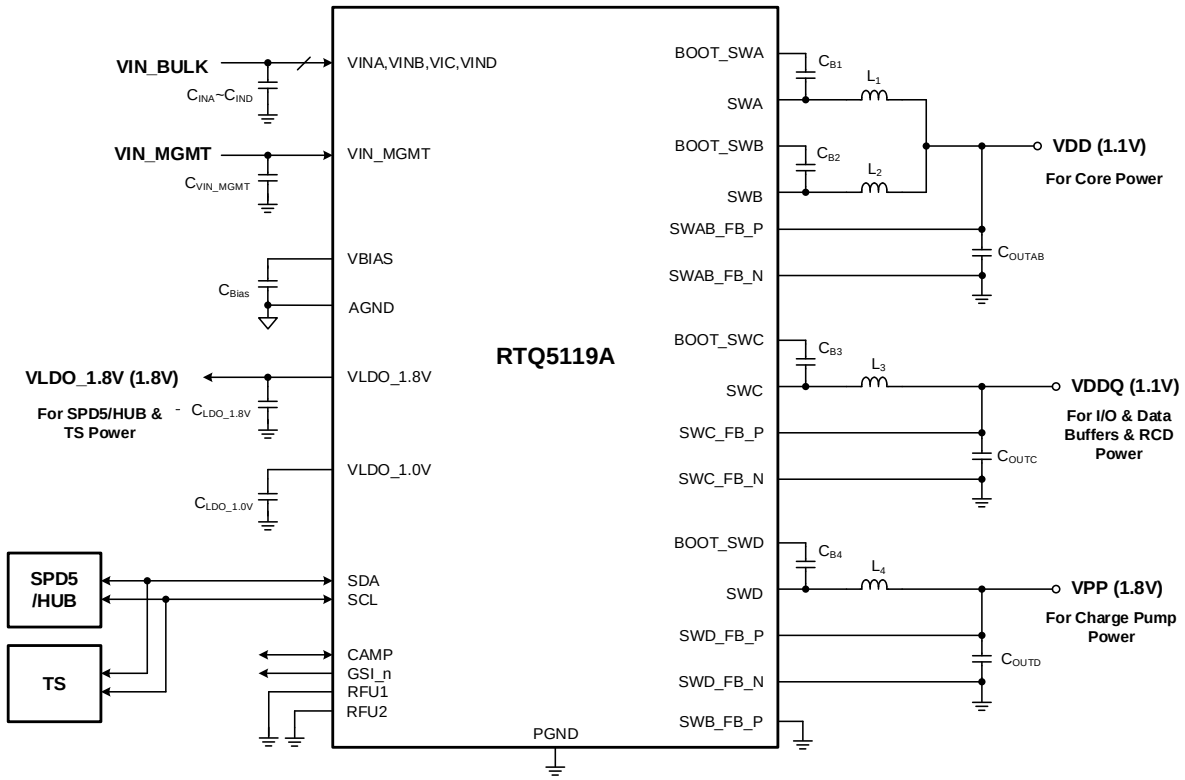


Figure 1. SWA and SWB are Combined as Dual-Phase Mode

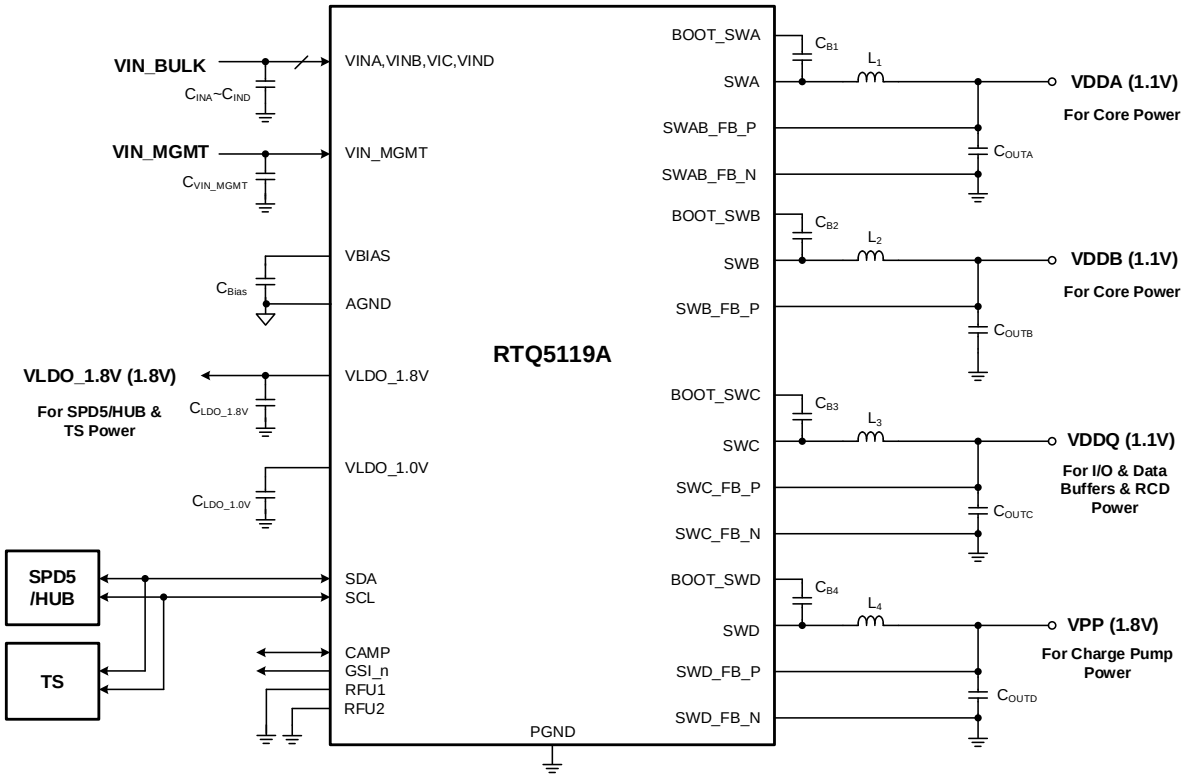


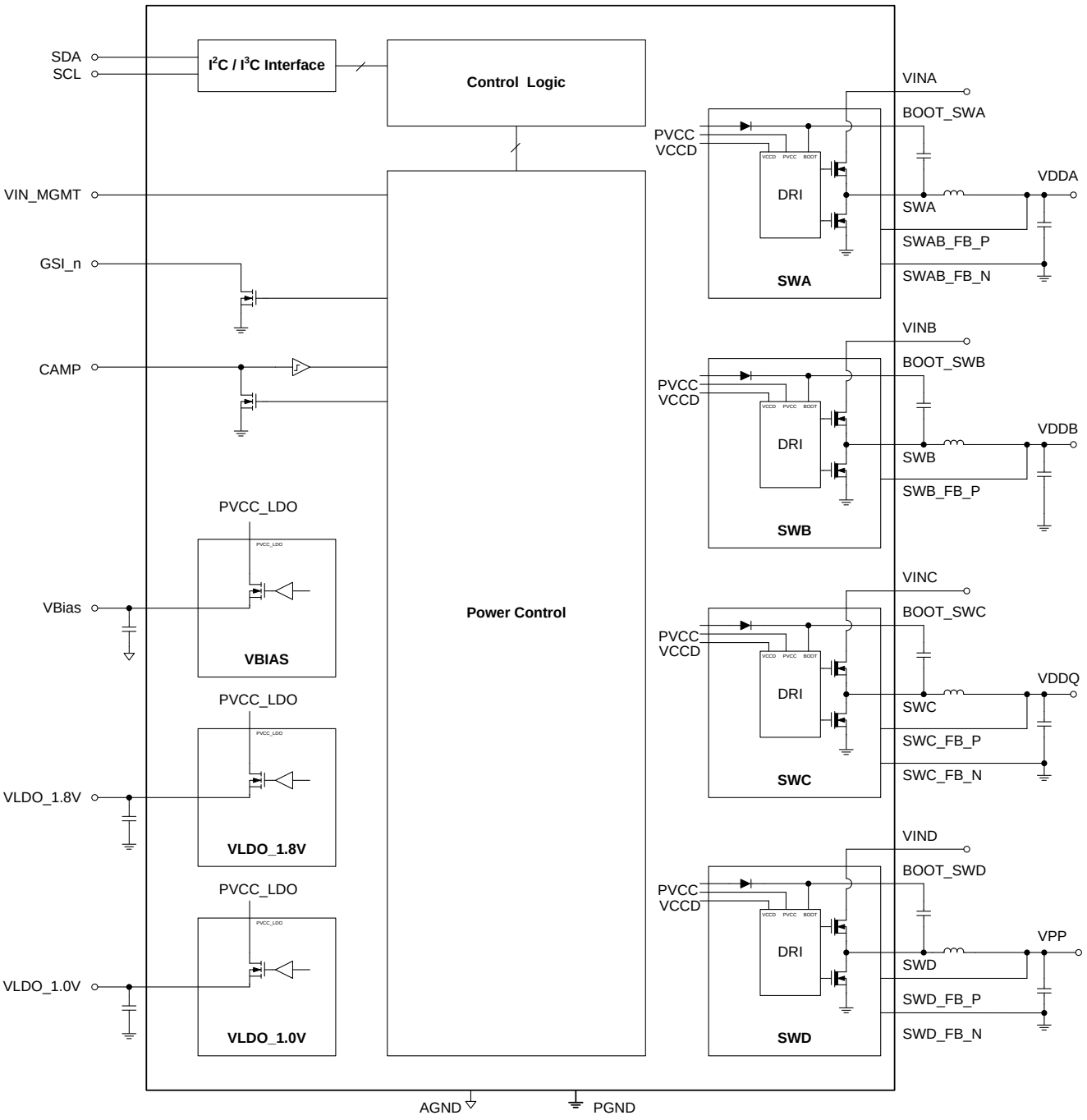
Figure 2. SWA and SWB are Operating in Single-Phase Mode

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 9, 19, 26	NC	Leave these pins floating don't affect the chip functionality. By connecting these pins to GND, design engineers can extend the GND copper coverage on the PCB top layer to enhance the thermal convection.
2	BOOT_SWA	Buck A bootstrap. Bootstrap node for switch node SWA high-side NMOS driver. Connect a capacitor between SWA and BOOT_SWA to form a floating supply across the high-side switch driver of Buck A. The recommended value of C_{BOOT} is 0.1μF/0201/6.3V/X5R.
3	VINA	Input supply of Buck A. VINA is connected to 12V power plane on the DIMM. VINA must be connected to 12V power plane on the DIMM, even if this rail is not intended to be used.
4	SWA	Output switch node of SWA regulator. This pin is connected to an external inductor (L1). Note: In single phase mode of operation, SWA output must not be connected to SWB or SWC output, even if this switch node is configured for the same output voltage as the others.
5	PGND	Common Power ground. Connect PGND to DIMM ground plane. For better thermal convection, adding some thermal vias is recommended.
6	SWB	Output switch node of SWB regulator. This pin is connected to an external inductor (L2). Note: In single phase mode of operation, SWB output must not be connected to SWA or SWC output, even if this switch node is configured for the same output voltage as the others.
7	VINB	Input supply of Buck B. VINB is connected to 12V power plane on the DIMM. VINB must be connected to 12V power plane on the DIMM, even if this rail is not intended to be used.
8	BOOT_SWB	Buck B bootstrap. Bootstrap node for switch node SWB high-side NMOS driver. Connect a capacitor between SWB and BOOT_SWB to form a floating supply across the high-side switch driver of Buck B. The recommended value of C_{BOOT} is 0.1μF/0201/6.3V/X5R.
10	RFU1	Internally connected for testing purpose. Application must connect this pin to GND.
11	SWB_FB_P	Positive feedback of Buck B. In single-phase output regular configuration, this pin is connected to the SWB remote positive sense feedback. Otherwise, it must be connected to AGND.
12	VIN_MGMT	3.3V supply input to the PMIC. Connect a 4.7μF decoupling capacitor near this pin.
13	SWD_FB_N/PID	Remote sense ground of Buck D. SWD remote negative sense feedback and/or PMIC device ID. (The PMIC AGND pin is used for the negative sense feedback if PID is taken.)
14	SWD_FB_P	Positive feedback of Buck D. SWD remote positive sense feedback.
15	VBIAS	Internal 5V LDO output. The driver and control circuits are powered from the V_{BIAS} voltage. Connect a 4.7μF decoupling capacitor near this pin.
16	AGND	Analog ground. Connect AGND to the power ground pin with a single point.
17	VLDO_1.8V	PMIC 1.8V LDO supply. Connect a 4.7μF decoupling capacitor near this pin.
18	VLDO_1.0V	PMIC 1.0V LDO supply for I^3C push-pull driver. For PMIC internal use only. Connect a 4.7μF decoupling capacitor near this pin.

Pin No.	Pin Name	Pin Function
20	BOOT_SWD	Buck D bootstrap. Bootstrap node for switch node SWD high-side NMOS driver. Connect a capacitor between SWD and BOOT_SWD to form a floating supply across the high-side switch driver of Buck D. The recommended value of C_{BOOT} is 0.1μF/0201/6.3V/X5R.
21	VIND	Input supply of Buck D. VIND is connected to 12V power plane on the DIMM. VIND must be connected to 12V power plane on the DIMM, even if this rail is not intended to be used.
22	SWD	Output switch node of SWD regulator. This pin is connected to an external inductor (L4).
23	SWC	Output switch node of SWC regulator. This pin is connected to an external inductor (L3). The output of SWC must not be connected to the output of SWA or SWB, or (SWA + SWB) even if they configure for exact same output voltage.
24	VINC	Input supply of Buck C. VINC is connected to 12V power plane on the DIMM. VINC must be connected to 12V power plane on the DIMM, even if this rail is not intended to be used.
25	BOOT_SWC	Buck C bootstrap. Bootstrap node for switch node SWC high-side NMOS driver. Connect a capacitor between SWC and BOOT_SWC to form a floating supply across the high-side switch driver of Buck C. The recommended value of C_{BOOT} is 0.1μF/0201/6.3V/X5R.
27	RFU2	Reserved pin. It must be connected to GND.
28	SCL	Bus clock of I^2C and I^3C.
29	SDA	Bus data of I^2C and I^3C.
30	GSI_n	General status interrupt. Optional PMIC debug function pin (not required) for DDR5 RDIMM/LRDIMM application.
31	SWC_FB_N	Remote sense ground of Buck C. SWC remote negative sense feedback.
32	SWC_FB_P	Positive feedback of Buck C. SWC remote positive sense feedback.
33	SWAB_FB_P	Feedback of Buck A and Buck B. SWA/B rail remote sense feedback when SWA and SWB are combined as dual-phase, single output rail. When SWA and SWB are separated for two independent rails, this pin is used as SWA remote positive sense feedback (+).
34	SWAB_FB_N	Remote sense ground of Buck A and Buck B. SWA/B rail remote sense feedback when SWA and SWB are combined as dual-phase, single output rail. When SWA and SWB are separated for two independent rails, this pin is used as SWA and SWB remote negative sense feedback return (-). (For SWB, it is recommended to internally connect to AGND on package)
35	CAMP	Control and monitor port. Open-drain output. The PMIC floats this pin when VIN_BULK input supply, as well as all enabled output buck regulators and all LDO regulators tolerance thresholds are maintained as configured in the appropriate register. The PMIC drives this pin low when VIN_BULK input goes below the threshold or when any of the enabled output buck regulator exceeds the thresholds configured in the appropriate register. Input : The PMIC disables its output regulator when this pin transitions from high to low. The LDO outputs remain on. Input : The PMIC enters write protect mode when it is high and configuration mode when it is low.

Functional Block Diagram



Operation

Power Up Initialization and Start-up Sequence

There are two input supplies, VIN_BULK and VIN_MGMT, from the platform to provide RTQ5119A for power on.

The VIN_BULK supply is used by the RTQ5119A for all output regulators except for the VLDO_1.8V & VLDO_1.0V LDO outputs regulators when not in switchover mode. The internal bias voltage, V_{BIAS}, is also generated by the VIN_BULK input supply. At first power on, the VIN_BULK input supply shall reach a minimum threshold voltage value per “Register 0x1A” [7:5] plus 1.0V offset before it can be detected as a valid input supply to the PMIC.

The VIN_MGMT supply is used to read out its internal non-volatile memory content and to supply VLDO_1.8V & VLDO_1.0V to other devices such as SPD, TS and RCD on the DIMM. At first power on, the VIN_MGMT supply shall reach a minimum of 2.8V before it can be detected as a valid input supply to the PMIC.

At power on, the RTQ5119A floats CAMP signal and then drives CAMP output signal low only when VIN_MGMT input supply reaches minimum of 2.8V & VLDO_1.8V and VLDO_1.0V outputs are valid. VIN_BULK input supply doesn’t trigger PMIC to drive CAMP output signal low at power on.

Figure 3 and Figure 4 show PMIC power up sequence when power is first applied. Note that the specific sequence of ramping up the output regulators (SWA, SWB, SWC and SWD) is for example purpose only, and the specific ramp up sequence is configurable through the registers. The platform can power up VIN_BULK and VIN_MGMT supply in any sequence. Figure 3 shows VIN_MGMT supply ramps up first prior to VIN_BULK supply. Figure 4 shows VIN_BULK supply ramps up first prior to VIN_MGMT supply. The RTQ5119A does not mandate any specific timing relationship between VIN_BULK and VIN_MGMT supply.

During power on, the user shall :

(1) Ramp up VIN_MGMT supply; Ramp up VIN_BULK supply;

(2) Hold VIN_MGMT supply stable for a minimum of tVIN_MGMT_to_Enable time (min. = 6.5ms)

(3) Hold VIN_BULK supply stable for a minimum of tVIN_BULK_to_Enable time (min. = 6.5ms)

(4) Query the status of the PMIC status register to determine if it is safe to enable VR.

(5) If it is safe to enable, send VR Enable command by setting “Register 0x32” [7] = ‘1’ or by issuing DEVCTRL CCC.

Once the VIN_MGMT supply is valid and stable, the RTQ5119A drives VLDO_1.8V & VLDO_1.0V supply within t1.8V_Ready (typ. = 500us) & t1.1V_Ready time (typ. = 500μs) and enables I^2C/I^3C Basic bus interface function within tManagement_Ready (max. = 3ms). The user can’t access the RTQ5119A’s memory registers until tManagement_Ready timing requirement is satisfied. Further, the user shall not attempt to issue VR Enable command until tVIN_MGMT_to_Enable and tVIN_BULK_to_Enable timing requirement is satisfied. In Figure 3, the RTQ5119A allows access to its memory registers for indefinite period of time as long as VIN_MGMT input supply is valid without the requirement of VIN_BULK input supply.

The user, prior to issuing VR Enable command, must keep VIN_MGMT input supply valid as long as VLDO_1.8V & VLDO_1.0V LDO outputs are required. If VIN_MGMT input supply is removed or drops below 2.8V, the RTQ5119A does not guarantee any operation including VLDO_1.8V & VLDO_1.0V LDO output as well as access to its I^2C/I^3C Basic interface regardless of VIN_BULK input supply status.

After user issues VR Enable command to the RTQ5119A, the RTQ5119A offers the input supply switchover function. The RTQ5119A has an automatic internal input supply switchover function from VIN_MGMT input supply to VIN_BULK input supply. The RTQ5119A triggers the switchover to VIN_BULK input supply when VIN_MGMT input supply drops below the threshold set in “Register 0x2F” [7]. The internal input supply switchover is for RTQ5119A’s VLDO_1.8V & VLDO_1.0V LDO output. The RTQ5119A’s I^2C/I^3C Basic interfaces (SCL/SDA) are kept alive when RTQ5119A switches over to VIN_BULK input supply.

Figure 5 shows automatic internal switchover function when VIN_MGMT input supply drops below the threshold while maintaining its LDO outputs as well as I^2C/I^3C Basic interfaces. While RTQ5119A is in switchover mode to VIN_BULK, the VIN_MGMT input supply can re-power backup at any time and RTQ5119A switches back to VIN_MGMT input supply for its LDO outputs and I^2C/I^3C Basic interface continues to operate as normal.

After VR Enable command is registered, the RTQ5119A completes the following steps within tPMIC_PWR_GOOD_OUT :

(1) Check VIN_BULK, VIN_MGMT and V_{BIAS} Power Good status is valid.

(2) Power up itself – RTQ5119A executes Power on Sequence Config0 to Power on Sequence Config3 registers and configures RTQ5119A internal registers as programmed in DIMM vendor memory space registers.

(3) Power up all enabled output switch regulators and ready for normal operation.

(4) Update status registers “Register 0x08” [5:2] and floats CAMP signal.

If CAMP signal is not pulled as High within tPMIC_PWR_GOOD_OUT time, the user can access the RTQ5119A status registers for detailed information after tPMIC_PWR_GOOD_OUT time.

Once output regulators are running, the RTQ5119A allows VIN_BULK input supply to vary. Figure 6 shows that VIN_BULK can go as low as VIN_BULK Min. value (4.25 V) and the output regulators will continue to operate as normal. The VIN_MGMT input supply can drop and may re-power back up at any time. It should be noticed that the VIN_BULK power good threshold is set to 4.25V in “Register 0x1A” [7:5], and hence the CAMP signal remains at valid High level.

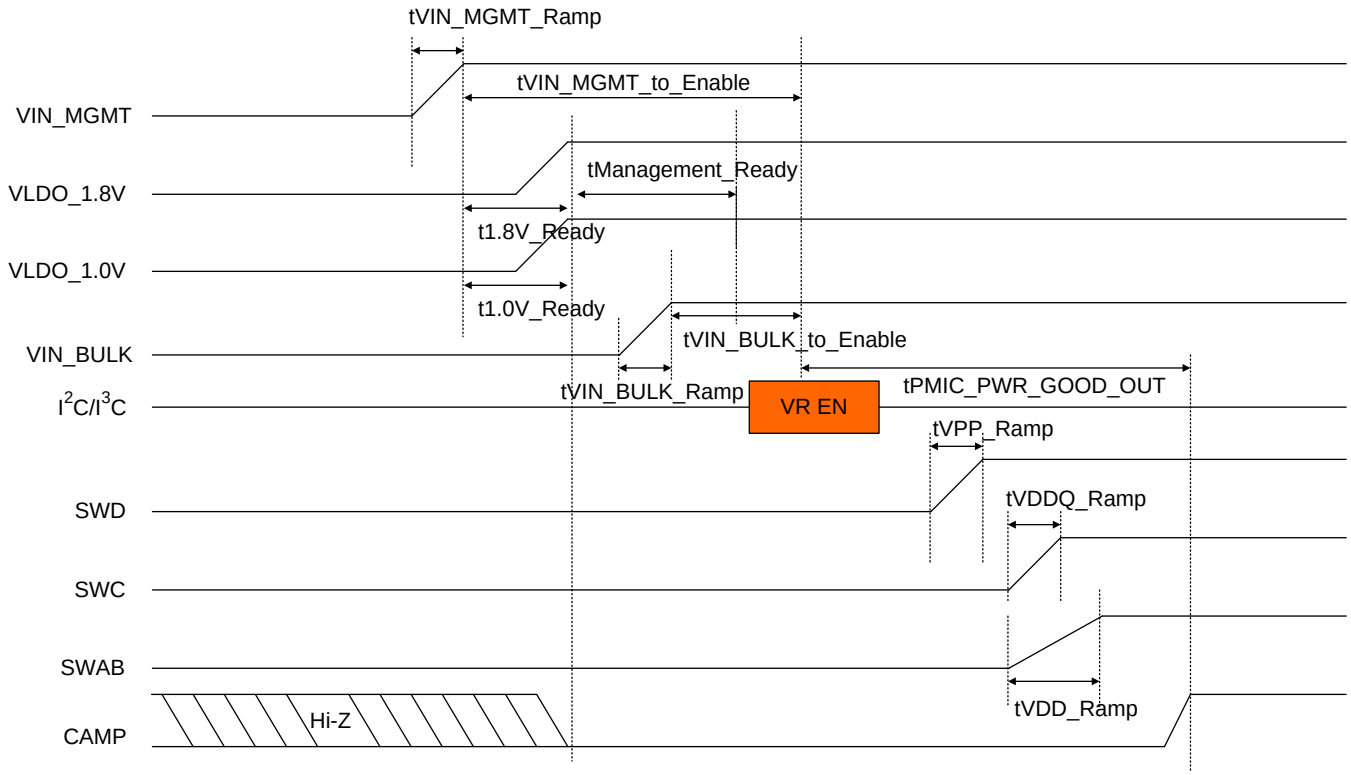


Figure 3. RTQ5119A Power-on Sequence: apply VIN_MGMT then VIN_BULK

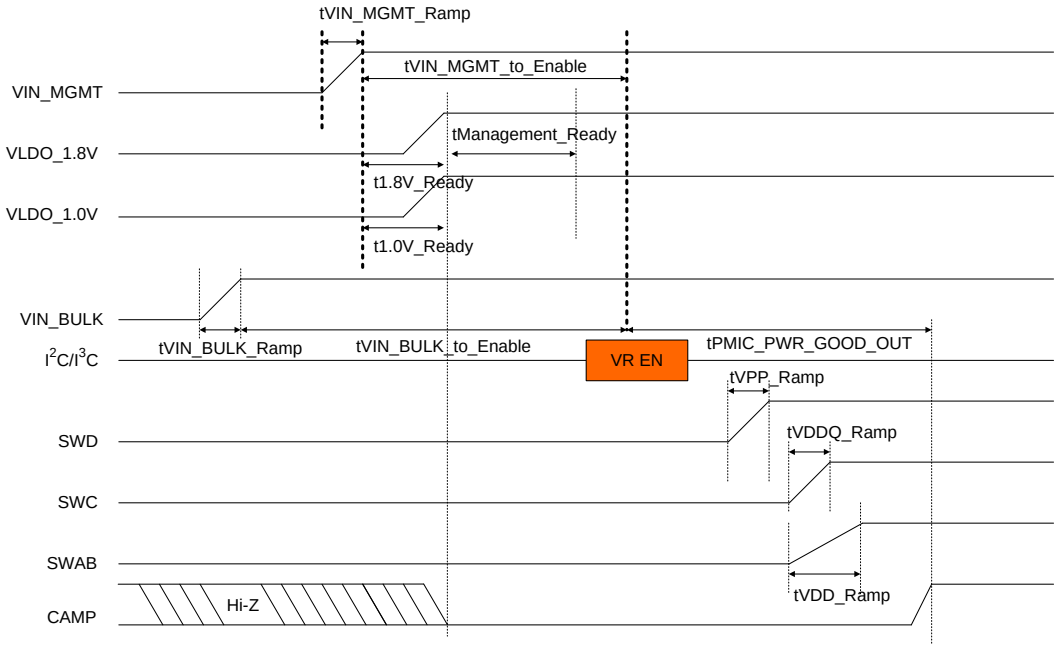


Figure 4. RTQ5119A Power-on Sequence: apply VIN_BULK then VIN_MGMT

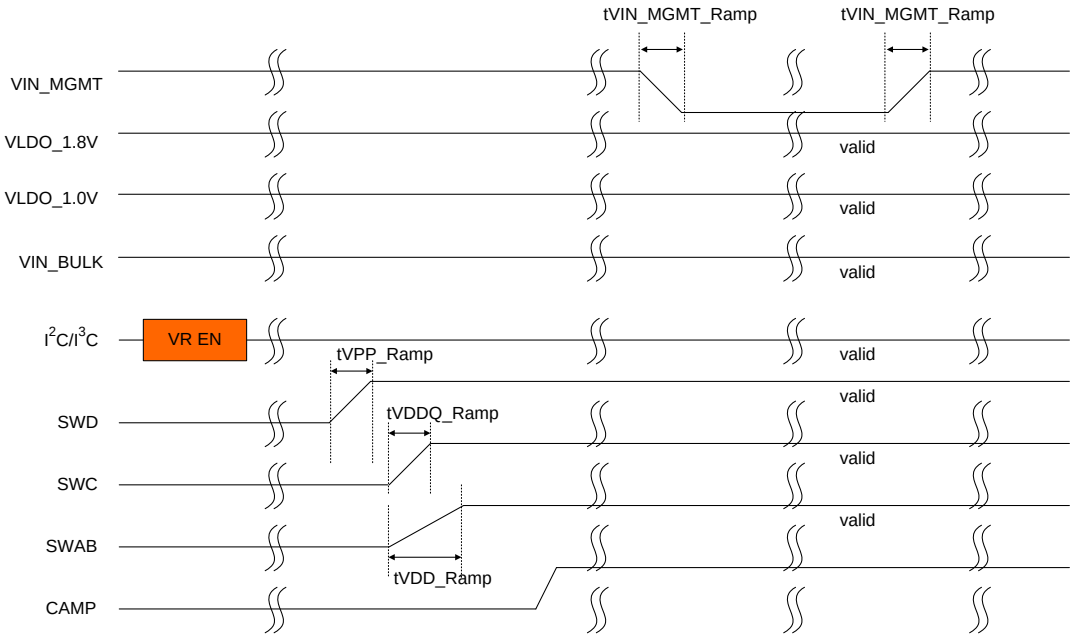


Figure 5. VIN_MGMT Switch-over to VIN_BULK

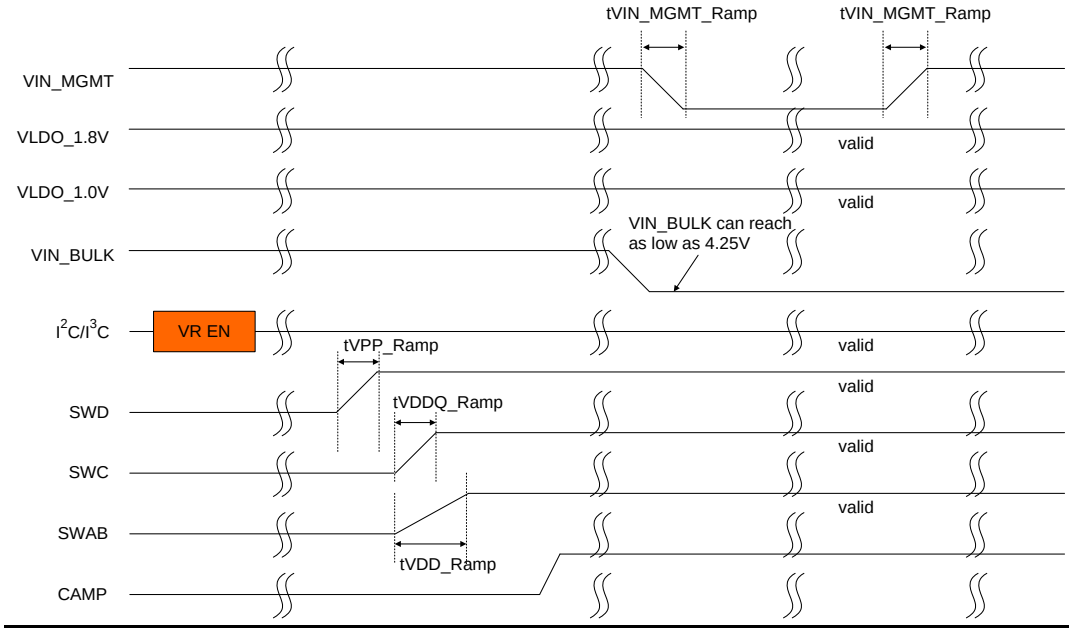


Figure 6. VIN_BULK Supply Transition

Enabling PMIC Output Switch Voltage Regulators

The Figure 7 below shows the timing relationship once the RTQ5119A receives VR Enable command and when it floats CAMP output signal; timing parameter tPMIC_PWR_GOOD_OUT applies. This timing parameter is a sum of maximum soft-start time and configured delay for each power-on sequence configuration registers that are executed plus additional 5ms timing margin error. The waveform shows each buck regulator output soft-start time and delay time once the soft-start time expires for each power-on sequence config0 to power-on sequence config3 registers. Note that if multiple regulators are enabled in a power-on sequence configuration register, and if those regulators have different soft-start time programmed, then the larger value of that soft-start time is used as a reference for delay timer to start. Each regulator will still follow different soft-start time to turn on the buck regulator.

The specific example in Figure 7 uses only three power-on sequence config0 to config2 registers and only one buck regulator is enabled in power-on sequence config0 register and power-on sequence config1 register. The power-on sequence config2 register enables dual phase regulator for SWA and SWB.

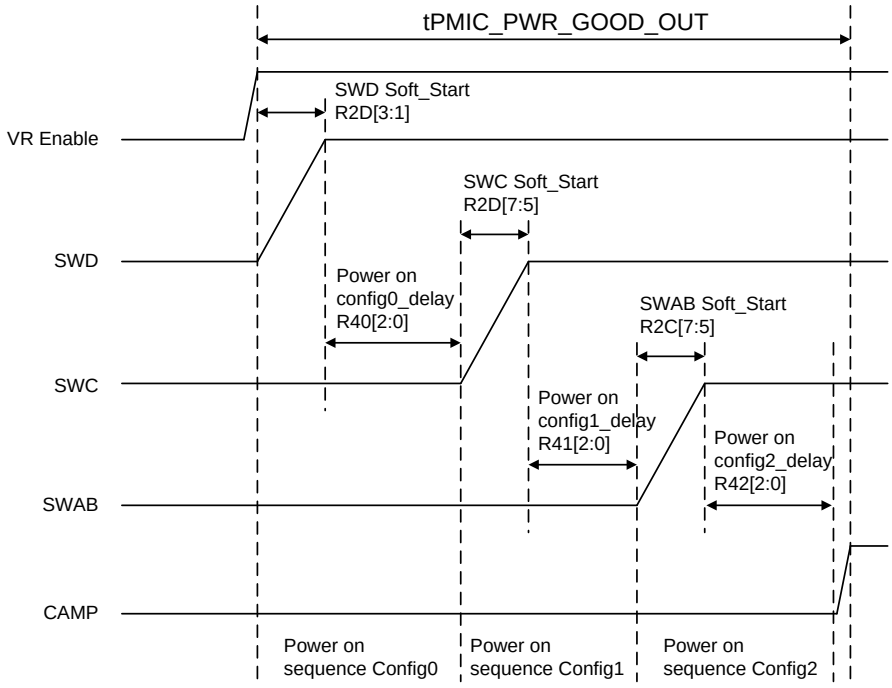


Figure 7. RTQ5119A Rails Power On Timing

Power Down Output Regulators

Regardless of how PMIC's output regulators are turned on, the PMIC's output regulators are powered down as described below depending on mode of operation.

In non-write protect of operation, users can power down any or all output regulators by any of the three methods below.

(1) The VR Disable command ("Register 0x32" [7] = '0'). The RTQ5119A executes power-off sequence config0 to power-off sequence config3 to preserve the appropriate voltage relationship as configured by the DIMM vendors. The RTQ5119A keeps the CAMP signal floating (i.e. it remains High) because this is an intentional command from the user and not a fault condition. Note that user can re-enable the RTQ5119A's output regulator by issuing VR Enable command.

(2) Configuring one or more bits in "Register 0x2F" [6:3] to '0' in any specific sequence that is desired by the user. The RTQ5119A does not execute power-off sequence config0 to power-off sequence config3 on its own. The RTQ5119A keeps the CAMP signal floating (i.e it remains High) because this is intentional command from the host and not a fault condition. Note that user can re-enable any of disabled output regulators by configuring one or more bits in "Register 0x2F" [6:3] to '1' in any specific sequence that is desired by the user.

(3) By driving CAMP input low. The PMIC executes power-off sequence config0 to power-off sequence config3 to preserve the appropriate voltage relationship as configured by the DIMM vendors.

In write protect mode of operation, the user can disable RTQ5119A's all enabled output regulators by any of the two methods below.

(1) Power cycle the VIN_BULK.

(2) By driving CAMP input low. The RTQ5119A executes power-off sequence config0 to power-off sequence config3 to preserve the appropriate voltage relationship as configured by the DIMM vendors.

Regardless of the either mode of the operation, the RTQ5119A can generate VR Disable command at any time due to one or more events listed in Table 3 under column "Trigger VR Disable" on its own. The PMIC executes power-off sequence config0 to power-off sequence config3 to preserve the appropriate voltage relationship as configured by the DIMM vendors. Moreover, during power-on sequence, it is possible that RTQ5119A can trigger VR Disable command on its own due to fault events when one or more regulators are

already turned on even while other remaining output regulators are not yet turned on because RTQ5119A has not completed the power on sequence configuration registers. For these types of cases, the RTQ5119A will not execute the remaining power-on sequence configuration registers and will immediately jump to execute the power-off sequence config0 to power-off sequence config3 registers. The RTQ5119A will update the status registers and error log registers appropriately as normal because it generated VR Disable command on its own. The CAMP output signal will remain low.

The Figure 8 below shows the timing relationship once the RTQ5119A registers VR Disable command internally due to a fault event. The waveform shows each buck regulator output soft-stop time and delay time once the soft-stop time expires from each power-off sequence config0 to power-off sequence config3 registers. Note that if multiple regulators are disabled in a power-off sequence configuration register, and if those regulators have different soft-stop time programmed, then the larger value of that soft-stop time is used as a reference for delay timer to start. Each regulator will still follow different soft-stop time to turn off the buck regulator.

The specific example in Figure 8 uses only three power-off sequence config0 to config2 registers and only one buck regulator is disabled in power-off sequence config1 register and power-off sequence config2 register. The power-off sequence config0 register disables dual phase regulator for SWA and SWB.

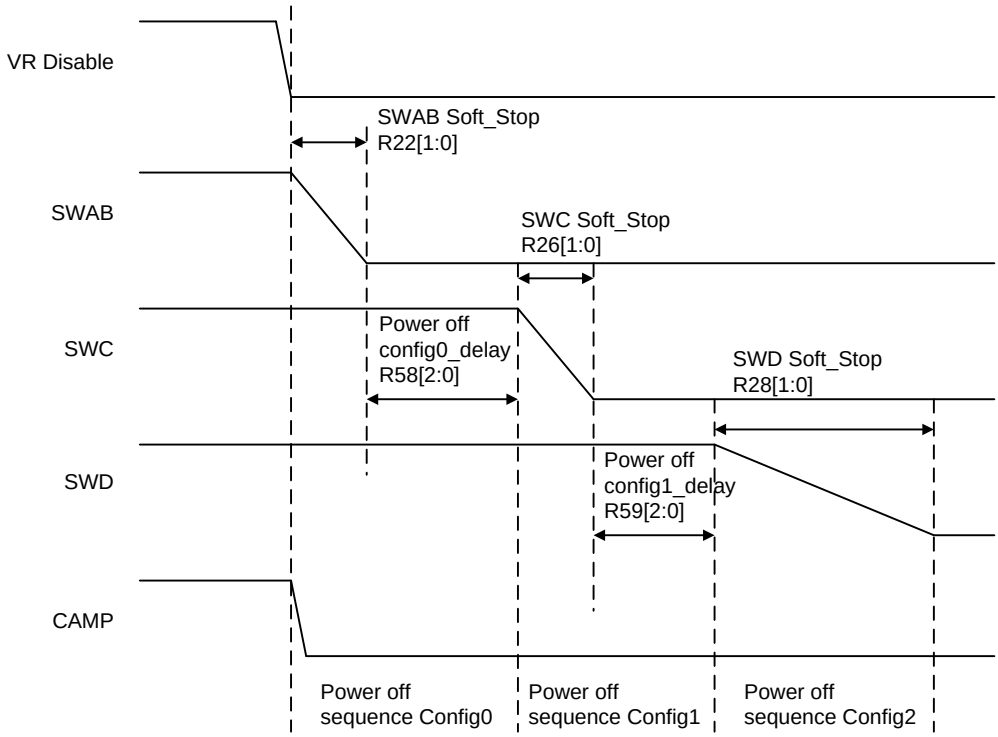


Figure 8. RTQ5119A Power-Off Timing Due to Internal Fault Condition

CAMP Signal

The CAMP (Control AND Monitor Port) signal provides three different functions.

i. Register write protect function

ii. Fail_n function

iii. Status function

(1) Register Write Protect Function

By default, PMIC register write protect function is enabled (i.e. “Register 0x2F” [2] = ‘0’). The CAMP input signal level determines when PMIC will enter or exit the write protect mode. The PMIC enters the write protect mode when CAMP signal is at logic level High. PMIC exits the write protect mode when CAMP signal is at logic level Low. When PMIC is in write protect mode, the PMIC does not allow to modify “Register 0x15” to “Register 0x2F”, “Register 0x32” in the host region as well as “Register 0x40” to “Register 0x6F” in the DIMM vendor region. These registers are write protected denoted with “WP” in “Register” column in Section A-4.1 “Register Map (Host Region Map)”. The PMIC simply ignores the host request for write operation in write protect mode. PMIC allows all register read access in write protect mode.

Once PMIC is in write protect mode, there are three ways PMIC can exit write protect mode:

1. PMIC sees CAMP input signal Low

2. PMIC triggers internal fault event (VIN_BULK OV, VIN_BULK UV, SWx_OV, SWx_UV) and asserts CAMP signal low.

3. PMIC goes through power cycle (i.e. simultaneous removal of VIN_BULK and VIN_MGMT input supplies)

If “Register 0x2F” [2] = ‘1’, the PMIC does not enter write protect mode. The PMIC CAMP input signal has no effect on write protect function. The PMIC allows write and read access to all registers. Caution: The operation of non-write protect mode should be limited to lab and debug environment instead of normal system operation.

(2) Fail_n Function

By default, PMIC Fail_n function is enabled (“Register 0x32” [4] = ‘0’). When PMIC CAMP input signal transitions from High to Low, the PMIC executes VR Disable command (i.e. execute power off sequence config0 to config3 registers), asserts CAMP signal low (if “Register 0x32” [3] = ‘0’), exits the write protect mode and clears “Register 0x32” [7] to ‘0’.

If “Register 0x32” [4] = ‘1’, the PMIC Fail_n function is disabled. When CAMP signal transition from High to Low, the PMIC does not execute VR Disable command (i.e does not execute power off sequence config0 to config3 registers), does not assert CAMP signal low, exits the write protect mode and does not clear “Register 0x32” [7] to ‘0’. The Fail_n function is independent of PMIC’s write protect function.

(3) Status Function

The PMIC CAMP PWR_GOOD output signal indicates status of VIN_BULK input supply and all output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_D, VLDO_1.8V, VLDO_1.0V, V_{BIAS}). Once RTQ5119A receives VR Enable command, the PMIC floats CAMP pin when VIN_BULK input supply is valid and all enabled output regulator’s (VOUT_A, VOUT_B, VOUT_C, VOUT_D, VLDO_1.8V, VLDO_1.0V, V_{BIAS}) tolerances are maintained as configured in the appropriate register space. Note that CAMP pin is not affected based on VIN_MGMT input supply.

At first power up, with stable & valid input supply VIN_MGMT as well as VLDO_1.8V & VLDO_1.0V outputs, the PMIC asserts CAMP pin low. However, PMIC updates corresponding status register. Once PMIC receives VR Enable command from the host, the PMIC enables all appropriate output regulators and updates corresponding status registers and enters state called as “Regulation”. At this point, PMIC floats CAMP PWR_GOOD output and the external board pull-up resistor pulls the CAMP pin high. Once the CAMP pin is pulled high (i.e no other PMIC is driving the CAMP pin low), the PMIC enters state called “online” state.

Once the CAMP pin is high, if PMIC detects any condition either on VIN_BULK input supply or any of the output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_D, VLDO_1.8V, VLDO_1.0V, V_{BIAS}) that causes the PMIC to update status registers to indicate the power status is not good, then PMIC asserts CAMP pin low and keeps it asserted until the host explicitly takes a specific action corresponding to it. The PMIC does not automatically let the CAMP pin float even if the condition that triggered the PMIC to assert the CAMP pin no longer exists. In other words, the PMIC’s CAMP pin is

latched and once latched, it must be explicitly addressed by the host. Regardless of whether PMIC is operating in write protect mode or not, the PMIC always asserts CAMP signal low to indicate the status if there is a fault event.

GSI_n Signal

The RTQ5119A features a general purpose interrupt, GSI_n, for signaling any other event to the user. The GSI_n is an open-drain output pin which needs an external pull-up resistor (~10kΩ) to 3.3V or 1.8V.

The interrupts are active Low “latched” signal (when an interrupt event occurs in the RTQ5119A, a low level shall be output on the corresponding interrupt pin).

The interrupt pin is held low until both of the following requirements are met:

(1) The condition causing the interrupt (or others condition has occurred since) no longer persists.

(2) The register is cleared through I^2C or I^3C write to the clear bit.

All warning status bits should be latched to ‘1’ (based on their condition occurring). The latch shall remain a ‘1’ until the corresponding clear bit is written with a ‘1’. If an exception bit is cleared, but the condition continues to persist, a new interrupt will be generated (as if it is a new condition).

When GSI_n signal is asserted, the PMIC continues to operate as normal.

The user can query appropriate status registers to determine and isolate the cause of the GSI_n signal assertion.

Table 1. Summary of GSI_n Assertion Events

No	Event Description
1	Input (VIN_BULK) Power Good status.
2	Input (VIN_BULK or VIN_MGMT) Over-Voltage protection.
3	Output (SW[A:D] or VLDO_1.8V, VLDO_1.0V, V_{BIAS}) Power Good status.
4	Output (SW[A:D]) Over-Voltage protection.
5	Output (SW[A:D]) Under-Voltage Lockout protection.
6	V_{BIAS} LDO Output or VIN_BULK Input Under-Voltage Lockout protection.
7	Output (SW[A:D]) Current Limiter Warning event.
8	Output (SW[A:D]) High Current Consumption Warning event.
9	PMIC High Temperature Warning status.
10	PMIC Critical Temperature protection.
11	VIN_MGMT to VIN_BULK Input Supply Switch-over event.
12	RTQ5119A detects valid VIN_MGMT during Switch-over mode.
13	PEC Error.
14	Parity Error.

State Transition Diagram

There are four high level states in RTQ5119A, the description of states are summarized in Table 2. Figure 9 shows high level simplified state diagram. Specific transition details are function of PMIC's configuration register settings (e.g. R2F, R32, etc. as well as CAMP signal and input/output supplies). Please refer to detail functional description and configuration register definition for PMIC operation.

Table 2. High Level Finite State Description

State	Description
Offline	1. VIN_MGMT is invalid and VIN_BULK = X (valid or invalid); LDOs are invalid 2. All registers are reset to specified default values 3. CAMP is Hi-Z.
Configuration (non-write protect)	1. At initial configuration state, all registers follow the register attributes as defined. 2. The I^2C/I^3C bus interface is alive and running. 3. LDOs are valid, switch regulators are off 4. CAMP is low.
Regulation (non-write protect)	1. All registers are read/write accessible. 2. All enabled output rails are active. 3. Internal power good is floated, external CAMP is low.
Online (write protect)	1. All registers are readable. All non-protect registers are writable. 2. All enabled output rails are active. 3. CAMP is high.

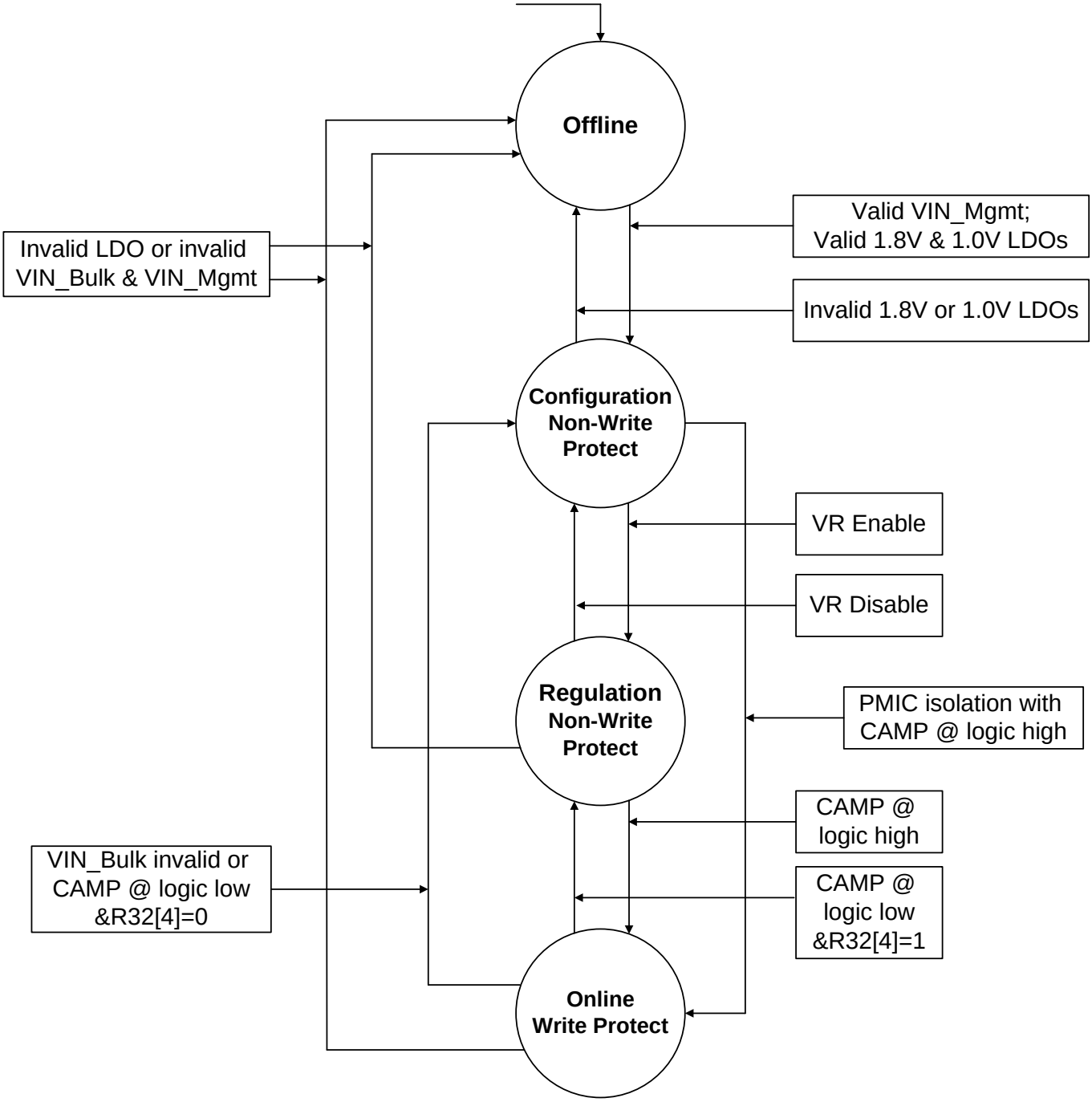


Figure 9. High Level State Transitions

Function Interrupt - CAMP and GSI_n Output Signals

This section defines the output functionality of GSI_n pin and CAMP pin.

When mask register bits are not set, the RTQ5119A asserts its GSI_n output and CAMP output signals as shown in Table 3 when any event occurs. The table also highlights 11 events that cause RTQ5119A to generate internally VR Disable command. For remaining events that does not trigger internal VR Disable command, the RTQ5119A continues to operate as normal.

Table 3. Events Interrupt Summary

Status Event	Status Bit	Clear Bit	Mask Bit	Threshold Setting	VR Disable Trigger?	CAMP Output	GSI_n
VIN_BULK Power Good	R08[7]	R10[7]	R15[7]	R1A[7:5]	No	Low	Low
VIN_BULK Over Voltage	R08[0]	R10[0]	R15[0]	R1B[7]	Yes	Low	Low
VIN_MGMT Over Voltage	R08[1]	R10[1]	R15[1]	R1B[5]	No	High	Low
SWA Output Power Good	R08[5]	R10[5]	R15[5]	R21[1:0], R22[7:6]	No	Low	Low
SWB Output Power Good	R08[4]	R10[4]	R15[4]	R23[1:0], R24[7:6]	No	Low	Low
SWC Output Power Good	R08[3]	R10[3]	R15[3]	R25[1:0], R26[7:6]	No	Low	Low
SWD Output Power Good	R08[2]	R10[2]	R15[2]	R27[1:0], R28[7:6]	No	Low	Low
1.8V LDO Power Good	R09[5]	R11[5]	R16[5]	R1A[2]	No	Low	Low
1.0V LDO Power Good	R33[2]	R14[2]	R19[2]	R1A[0]	No	Low	Low
V_{BIAS} LDO Power Good	R09[6]	R11[6]	R16[6]	R1A[3]	No	Low	Low
SWA Output Over Voltage	R0A[7]	R12[7]	R17[7]	R22[5:4]	Yes	Low	Low
SWB Output Over Voltage	R0A[6]	R12[6]	R17[6]	R24[5:4]	Yes	Low	Low
SWC Output Over Voltage	R0A[5]	R12[5]	R17[5]	R26[5:4]	Yes	Low	Low
SWD Output Over Voltage	R0A[4]	R12[4]	R17[4]	R28[5:4]	Yes	Low	Low
SWA Output Under Voltage	R0B[3]	R13[3]	R18[3]	R22[3:2]	Yes	Low	Low
SWB Output Under Voltage	R0B[2]	R13[2]	R18[2]	R24[3:2]	Yes	Low	Low
SWC Output Under Voltage	R0B[1]	R13[1]	R18[1]	R26[3:2]	Yes	Low	Low
SWD Output Under Voltage	R0B[0]	R13[0]	R18[0]	R28[3:2]	Yes	Low	Low

Status Event	Status Bit	Clear Bit	Mask Bit	Threshold Setting	VR Disable Trigger?	CAMP Output	GSI_n
V_{BIAS} LDO or VIN_BULK Under Voltage	R33[3]	R14[3]	R19[3]	4.0V	Yes	Low	Low
SWA Output Current Limit	R0B[7]	R13[7]	R18[7]	R20[7:6]	No	High	Low
SWB Output Current Limit	R0B[6]	R13[6]	R18[6]	R20[5:4]	No	High	Low
SWC Output Current Limit	R0B[5]	R13[5]	R18[5]	R20[3:2]	No	High	Low
SWD Output Current Limit	R0B[4]	R13[4]	R18[4]	R20[1:0]	No	High	Low
SWA Output High Current /Power	R09[3]	R11[3]	R16[3]	R1C[7:2]	No	High	Low
SWB Output High Current /Power	R09[2]	R11[2]	R16[2]	R1D[7:2]	No	High	Low
SWC Output High Current /Power	R09[1]	R11[1]	R16[1]	R1E[7:2]	No	High	Low
SWD Output High Current /Power	R09[0]	R11[0]	R16[0]	R1F[7:2]	No	High	Low
High Temperature Warning	R09[7]	R11[7]	R16[7]	R1B[2:0]	No	High	Low
Critical Temperature	R08[6]	N/A	N/A	R2E[2:0]	Yes	Low	Low
VIN_MGMT to VIN_BULK Switchover	R09[4]	R11[4]	R16[4]	R2F[7]	No	High	Low
Valid VIN_MGMT in Switchover	R33[4]	R14[4]	R19[4]	N/A	No	High	Low
PEC Error	R0A[3]	R12[3]	R17[3]	N/A	No	High	Low
Parity Error	R0A[2]	R12[2]	R17[2]	N/A	No	High	Low

The user can read appropriate status registers to determine and isolate the cause of the GSI_n signal assertion or CAMP signal assertion. The user may attempt to clear or mask the appropriate corresponding interrupt event. The RTQ5119A keeps the GSI_n signal asserted or CAMP signal asserted until the appropriate corresponding registers are explicitly cleared or masked by the user. Table 4 and Table 5 shows the RTQ5119A's response of GSI_n signal and CAMP output signal for each event before and after user issues the Clear command. The Table 4 and Table 5 assume that all mask bits are either '0' or '1' for simplicity.

Table 4. RTQ5119A Response for Clear Command by Host (Part I)

Event	Event Occurred; All Mask Bits = "0"		Clear Command; Event Not Present; All Mask Bits = "0"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
			R2F[1:0] = "00" or "01" or "10"		R2F[1:0] = "00"		R2F[1:0] = "00"	
	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output
VIN_BULK Power Good	Low	Low	High	High	Low	High	High	High
VIN_BULK Over Voltage	Low	Low	Low	High	Low	High	Low	High
VIN_MGMT Over Voltage	High	Low	High	High	High	High	High	High
SWA Output Power Good	Low	Low	High	High	Low	High	High	High
SWB Output Power Good	Low	Low	High	High	Low	High	High	High
SWC Output Power Good	Low	Low	High	High	Low	High	High	High
SWD Output Power Good	Low	Low	High	High	Low	High	High	High
1.8V LDO Power Good	Low	Low	High	High	Low	High	High	High
1.0V LDO Power Good	Low	Low	High	High	Low	High	High	High
V_{BIAS} LDO Power Good	Low	Low	High	High	Low	High	High	High
SWA Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWD Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWD Output Under Voltage	Low	Low	Low	High	Low	High	Low	High

Event	Event Occurred; All Mask Bits = "0"		Clear Command; Event Not Present; All Mask Bits = "0"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
			R2F[1:0] = "00" or "01" or "10"		R2F[1:0] = "00"		R2F[1:0] = "00"	
	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output
V_{BIAS} LDO or VIN_BULK Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWD Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current /Power	High	Low	High	High	High	High	High	High
SWB Output High Current /Power	High	Low	High	High	High	High	High	High
SWC Output High Current /Power	High	Low	High	High	High	High	High	High
SWD Output High Current /Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	Power Cycle	Power Cycle	Low	Low	Power Cycle	Power Cycle
VIN_MGMT to VIN_BULK Switchover	High	Low	High	High	High	High	High	High
Valid VIN_MGMT in Switchover	High	Low	High	High	High	High	High	High
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Table 5 shows the RTQ5119A's response of GSI_n signal and CAMP signal for each event before and after user issues the Clear command. The table assumes that all mask bits are '1'.

Table 5. RTQ5119A Response for Clear Command by Host (Part II)

Event	Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
	R2F[1:0] = "01"		R2F[1:0] = "01"		R2F[1:0] = "10"		R2F[1:0] = "10"	
	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output
VIN_BULK Power Good	High	Low	High	High	High	High	High	High
VIN_BULK Over Voltage	Low	Low	Low	High	Low	High	Low	High
VIN_MGMT Over Voltage	High	Low	High	High	High	High	High	High
SWA Output Power Good	High	Low	High	High	High	High	High	High
SWB Output Power Good	High	Low	High	High	High	High	High	High
SWC Output Power Good	High	Low	High	High	High	High	High	High
SWD Output Power Good	High	Low	High	High	High	High	High	High
1.8V LDO Power Good	High	Low	High	High	High	High	High	High
1.0V LDO Power Good	High	Low	High	High	High	High	High	High
V_{BIAS} LDO Power Good	High	Low	High	High	High	High	High	High
SWA Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWD Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWD Output Under Voltage	Low	Low	Low	High	Low	High	Low	High

Event	Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
	R2F[1:0] = "01"		R2F[1:0] = "01"		R2F[1:0] = "10"		R2F[1:0] = "10"	
	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output
V_{BIAS} LDO or VIN_BULK Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWD Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current /Power	High	Low	High	High	High	High	High	High
SWB Output High Current /Power	High	Low	High	High	High	High	High	High
SWC Output High Current /Power	High	Low	High	High	High	High	High	High
SWD Output High Current /Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	Power Cycle	Power Cycle	Low	Low	Power Cycle	Power Cycle
VIN_MGMT to VIN_BULK Switchover	High	Low	High	High	High	High	High	High
Valid VIN_MGMT in Switchover	High	Low	High	High	High	High	High	High
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Note that when user masks any of the event in appropriate register, it only masks the assertion of GSI_n output signal or assertion of CAMP output signal. The PMIC functional behavior remains the same as noted for each event other than assertion of GSI_n output signal and assertion of CAMP output signal.

Input Power Good Status

The RTQ5119A recognizes the input supply fail as VIN_BULK goes below the threshold set in “Register 0x1A” [7:5]. When this event occurs for a period longer than tInput_PWR_GOOD_GSI_Assertion (max. = 10μs) time then RTQ5119A sets the “Register 0x08” [7] and drives GSI_n and CAMP output signal as shown in Table 3 at the same time. The RTQ5119A allows access to all registers and PMIC continues to operate as normal as long as VIN_BULK input remains above 4.25V. The user can clear the VIN_BULK input power good status register by writing ‘1’ to “Register 0x08” [7] or by writing ‘1’ to global status clear “Register 0x14” [0]. If the input power not good condition is still present, then RTQ5119A will continue to drive GSI_n and CAMP output signal as in Table 3 and the status “Register 0x08” [7] will remain at ‘1’. If the input power not good condition persists, the host can set the appropriate mask register to remove GSI_n or CAMP output signal as shown in Table 4 and Table 5.

Note that after VR enable command, when VIN_MGMT input goes below the threshold set in “Register 0x2F” [7], it is reported as switchover event. Prior to VR Enable command, the VIN_MGMT is always required to be above 2.8V to guarantee RTQ5119A’s functionality.

Input Over-Voltage Protection

An input over-voltage protection mechanism is implemented to limit the voltages to the RTQ5119A. The RTQ5119A actively monitors the input voltage VIN_BULK and VIN_MGMT rail.

There are two conditions where RTQ5119A recognizes the input over-voltage event.

(1) VIN_MGMT input goes above the threshold set in “Register 0x1B” [5].

(2) VIN_BULK input goes above the threshold set in “Register 0x1B” [7].

When either one or both event occurs for a period longer than tInput_OV_GSI_Assertion time (max. = 10μs), then RTQ5119A sets the “Register 0x08” [1:0] accordingly and drives GSI_n output signal as shown in Table 3 at the same time. Note that at this point, the RTQ5119A does not assert CAMP output signal. The RTQ5119A allows access to all registers and continues to operate as normal. The host can clear the VIN_MGMT or VIN_BULK input over-voltage status register by writing ‘1’ to “Register 0x10” [1:0] appropriately or by writing ‘1’ to global status clear “Register 0x14” [0]. If the input over-voltage condition is still present, then RTQ5119A will continue to assert GSI_n output signal and the status “Register 0x08” [1:0] will remain at ‘1’.

In non-write protect mode, if VIN_BULK input supply over-voltage condition persists greater than tInput_OV_VR_Disable time (max. = 20μs), then RTQ5119A internally generates VR Disable command and disables all of its switching output regulators and asserts CAMP signal. The output regulators follow the power-off sequence Config0 to Config3 to discharge the output voltage by tracking the soft-stop ramping down voltage. The RTQ5119A keeps VLDO_1.8V and VLDO_1.0V LDO output regulators active. The RTQ5119A allows access to all registers. The user can query the PMIC register space to determine the cause of the CAMP signal assertion and GSI_n signal assertion. Once user determines the cause, the user must first clear the VIN_BULK input over-voltage status register as well as any other relevant status registers individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. If the input over-voltage condition is still present, then RTQ5119A will continue to assert GSI_n output signal and the status “Register 0x08” [0] will remain at ‘1’. Once the status register is cleared and GSI_n output signal is de-asserted, the user may re-enable the RTQ5119A’s output switching regulator by issuing VR Enable command. The RTQ5119A enables output switching regulators and ensures CAMP signal is floated when all of its output regulators are normal and input over-voltage condition is no longer present.

In write protect mode, if VIN_BULK input supply over-voltage condition persists greater than tInput_OV_VR_Disable time (max. = 20μs), then RTQ5119A internally generates VR Disable command and disables all of its switching output regulators by executing Power Off Sequence configuration registers, asserts CAMP signal low and returns to configuration mode. The RTQ5119A keeps its VLDO_1.8V and VLDO_1.0V output regulators active.

Output Power Good Status (SWA/B/C/D, LDO_1.8V, LDO_1.0V, V_{BIAS})

The RTQ5119A provides output power good indicators to determine that the output regulators have crossed the desired voltage tolerance from its nominal programmed setting. The nominal programmed setting for output regulator SWA, SWB, SWC and SWD is programmed in “Register 0x21” [7:1], “Register 0x23” [7:1], “Register 0x25” [7:1] and “Register 0x27” [7:1] respectively. The RTQ5119A offers the CAMP condition to be set independently for low-side threshold and high-side threshold regarding to voltage regulators (SWA, SWB, SWC and SWD). In addition, there are three LDO regulators: V_{BIAS}, VLDO_1.8V and VLDO_1.0V in the RTQ5119A.

There are five possibilities where RTQ5119A recognizes the output power good event for any output regulator.

(1) Output voltage goes below the threshold set in “Register 0x21” [0] for SWA or “Register 0x23” [0] for SWB or “Register 0x25” [0] for SWC or “Register 0x27” [0] for SWD.

(2) Output voltage goes above the threshold set in “Register 0x22” [7:6] for SWA or “Register 0x24” [7:6] for SWB or “Register 0x26” [7:6] for SWC or “Register 0x28” [7:6] for SWD.

(3) LDO output V_{BIAS} goes below the threshold set in “Register 0x1A” [3].

(4) LDO output VLDO_1.8V goes below the threshold set in “Register 0x1A” [2].

(5) LDO output VLDO_1.0V goes below the threshold set in “Register 0x1A” [0].

When either event occurs for a period longer than Output_PWR_GOOD_GSI_Assertion time (max. = 10μs), then RTQ5119A sets the “Register 0x08” [5:2] or “Register 0x09” [6:5] or “Register 0x33” [2] appropriately and drives CAMP and GSI_n output signal as shown in Table 3 at the same time. The RTQ5119A continues to operate but DDR5 DIMM functionality may not be guaranteed.

The user can query the register space to determine and identify the cause of the CAMP signal assertion and GSI_n signal assertion. Once user determines the cause, the user may clear the appropriate status register individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted and CAMP signal to be de-asserted. If the output power not good condition is still present then RTQ5119A will continue to assert GSI_n output signal and assert CAMP signal and the appropriate status “Register 0x08” [5:2] or “Register 0x09” [6:5] or “Register 0x33” [2] will remain at ‘1’. If the output power not good condition persists, the user may set the appropriate mask register to remove GSI_n or CAMP output signal as shown in Table 4 and Table 5.

Output Over-Voltage Protection (SWA/B/C/D)

An output over-voltage protection mechanism is implemented to limit the voltages on the RTQ5119A output regulators. The RTQ5119A actively monitors the output voltage on each enabled regulator.

There are four possibilities where RTQ5119A recognizes the over-voltage event.

(1) SWA output regulator goes above the threshold set in “Register 0x22” [5:4].

(2) SWB output regulator goes above the threshold set in “Register 0x24” [5:4].

(3) SWC output regulator goes above the threshold set in “Register 0x26” [5:4].

(4) SWD output regulator goes above the threshold set in “Register 0x28” [5:4].

According to different DDR5 application environments, the “Register 0x4F” [7] has different setting.

Condition1. DDR5 RDIMM/LRDIMM Environment - “Register 0x4F” [7] = ‘0’:

In non-write protect mode, if any output over-voltage condition persists longer than tOutput_OV_VR_Disable time (max. = 20μs), then RTQ5119A internally generates VR Disable command and disables all of its switching output regulators, sets “Register 0x0A” [7:4] appropriately, asserts CAMP and asserts GSI_n output signal. The output regulators stop regulation once VR disable command is issued by RTQ5119A, and following the power-off sequence Config0 to Config3 to discharge the output voltage by tracking the soft-stop ramping down voltage. The VLDO_1.8V and VLDO_1.0V LDO output regulators keep active.

The user can query the register space to determine the

cause of the CAMP signal assertion and GSI_n signal assertion. Once user determines the cause, the user must first clear the appropriate output over-voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear "Register 0x14" [0] which triggers the GSI_n signal to be de-asserted. Once the status register is cleared and GSI_n output signal is de-asserted, the user may re-enable the PMIC's output switching regulator by issuing VR Enable command. The RTQ5119A enables output switching regulators and ensures CAMP signal is floated when all of its output regulators are normal.

In write protect mode, if any output over-voltage condition persists greater than tOutput_OV_VR_Disable time (max. = 20μs) then RTQ5119A internally generates VR Disable command and disables all of its switching output regulators by executing Power Off Sequence configuration registers, asserts CAMP signal low and returns to configuration mode. The RTQ5119A keeps its VLDO_1.8V and VLDO_1.0V output regulators active.

Condition2. DDR5 NVDIMM or Other Custom Environment - "Register 0x4F" [7] = '1'

In non-write protect mode, if any output over-voltage condition persists longer than tOutput_OV_VR_Disable time (max. = 20μs), then RTQ5119A internally generates VR Disable command to disable only the affected switching output regulator, sets "Register 0x0A" [7:4] appropriately, asserts CAMP and asserts GSI_n output signal and continues to operate normal on other output regulators. Once the affected switching output regulator receives VR Disable command, the regulator stops switching and turns on the internal discharging resistor. The VLDO_1.8V and VLDO_1.0V LDO output regulators keep active.

The user may query the register space to determine the cause of the CAMP signal assertion and GSI_n signal assertion. Once user determines the cause, the user must first clear the appropriate output over voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear "Register 0x14" [0] which triggers the GSI_n signal to be de-asserted.

Once the status register is cleared and GSI_n output signal is de-asserted, the user can re-enable the RTQ5119A's output switching regulator by issuing VR Enable command. The RTQ5119A enables output switching regulator and floats CAMP signal when all of its output regulators are normal. Note that in this case, though user issues VR Enable command, it only turns on the affected regulator that was disabled, other rails keep operating normally.

It should be noticed that the write protect mode is not allowed when "Register 0x4F" [7] = '1'.

Output Under-Voltage & VIN_BULK Under-Voltage Lockout Protection

An output under-voltage lockout protection mechanism is implemented to limit the voltages on the RTQ5119A output regulators. The RTQ5119A actively monitors the output voltage on each enabled regulator.

There are five possibilities where RTQ5119A recognizes the under-voltage lockout event.

(1) SWA output regulator goes below the threshold set in "Register 0x22" [3:2].

(2) SWB output regulator goes below the threshold set in "Register 0x24" [3:2].

(3) SWC output regulator goes below the threshold set in "Register 0x26" [3:2].

(4) SWD output regulator goes below the threshold set in "Register 0x28" [3:2].

(5) V_{BIAS} LDO output regulator goes below the 3.6V(default) or VIN_BULK Input Voltage goes below 4V.

According to different DDR5 application environments, the "Register 0x4F" [7] has different settings.

Condition1. DDR5 RDIMM/LRDIMM Environment - "Register 0x4F" [7] = '0':

In non-write protect mode, if any under-voltage condition (among five possibilities listed above) persists longer than tOutput_UV_VR_Disable time (max. = 20μs), then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets "Register 0x0B" [3:0], "Register 0x33" [3] appropriately, asserts CAMP and asserts GSI_n output signal. The output regulators stop regulation once VR disable command is issued by RTQ5119A, and following the power-off sequence Config0 to Config3 to discharge the output voltage by tracking the ramping down voltage reference. For SWA/B/C/D

output under-voltage events, the regulator increases the current limit threshold to 1.34 times deserved threshold for 35us as soon as UVP event is triggered, then follows the power-off sequence to discharge output voltage. The special mechanism of UVP shutdown is to prevent the abnormal power-off sequence between VPP and VDD/VDDQ. The VLDO_1.8V and VLDO_1.0V LDO output regulators keep active.

The user can query the register space to determine the cause of the CAMP signal assertion and GSI_n signal assertion. Once user determines the cause, the user must first clear the appropriate output under- voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear "Register 0x14" [0] which triggers the GSI_n signal to be de-asserted. Once the status register is cleared and GSI_n output signal is de-asserted, the user may re-enable the RTQ5119A's output switching regulator by issuing VR Enable command assuming valid VIN_BULK input voltage. The RTQ5119A enables output switching regulators and floats CAMP signal when all of its output regulators are normal.

In write protect mode, if any output under-voltage condition (among five possibilities listed above) or VIN_BULK input voltage condition listed above persists greater than tOutput_UV_VR_Disable time (max. = 20μs) then RTQ5119A internally generates VR Disable command and disables all of its switching output regulators by executing Power Off Sequence configuration registers, asserts CAMP signal low and returns to configuration mode. The RTQ5119A keeps its VLDO_1.8V and VLDO_1.0V output regulators active.

Condition2. DDR5 NVDIMM or Other Custom Environment - "Register 0x4F" [7] = '1'

In non-write protect mode, if any output under-voltage condition (First four possibilities listed above) as listed above persists longer than tOutput_UV_VR_Disable time (max. = 20μs), then RTQ5119A internally generates VR Disable command to disable only the affected switching output regulator, sets "Register 0x0B" [3:0] appropriately, asserts CAMP and asserts GSI_n output signal and continues to operate normal on other output regulators. Once the affected switching output regulator receives VR Disable command, the regulator follows soft-stop ramp to discharge output voltage. Note that if the fifth condition (V_{BIAS} LDO output goes below 3.6V (default) or VIN_BULK input goes below 4V) listed above persists longer than tOutput_UV_VR_Disable time (max. = 20μs), then the RTQ5119A internally generates VR Disable command and disables all of its switching output regulators, sets "Register 0x0B" [3:0] and "Register 0x33" [3] appropriately, asserts CAMP and asserts GSI_n output signal. The output regulators follow the power-off sequence Config0 to Config3 to discharge the output voltage. The RTQ5119A keeps VLDO_1.8V and VLDO_1.0V LDO output regulators active.

The user can query the register space to determine the cause of the CAMP signal assertion and GSI_n signal assertion. Once user determines the cause, the user must first clear the appropriate output under voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear "Register 0x14" [0] which triggers the GSI_n signal to be de-asserted. Once the status register is cleared and GSI_n output signal is de-asserted, the user can re-enable the RTQ5119A's output switching regulator by issuing VR Enable command. The RTQ5119A enables output switching regulator and ensures CAMP signal is floated when all of its output regulators are normal. Note that in this case, though user issues VR Enable command, it only turns on the affected regulator that was disabled.

It should be noticed that the write protect mode is not allowed when "Register 0x4F" [7] = '1'.

Output Current Limiter Warning Event

The RTQ5119A has output current limiter mechanism to limit the current on the output voltage regulators. The inductor current is actively monitored through low-side MOSFET during conduction. The voltage drop across phase node to PGND is compared with current limit threshold, which is set in "Register 0x20" [7:0], and the valley point of inductor current is limited cycle-by-cycle. When output voltage regulators operate in current limit mode, the PWM on-time one-shot should wait inductor current discharging below current limit threshold to trigger next on-time output even the output voltage has been below the reference feedback voltage. Hence, the output voltage starts dropping in current limit condition

due to insufficient energy to output load. The output under-voltage event will occur after that if output voltage is lower than under-voltage threshold as describes in previous section. The protection mechanism of output current limit is shown in Figure 10.

There are four possibilities where RTQ5119A recognizes the current limiter event.

(1) SWA output regulator current goes above the threshold set in “Register 0x20” [7:6].

(2) SWB output regulator current goes above the threshold set in “Register 0x20” [5:4].

(3) SWC output regulator current goes above the threshold set in “Register 0x20” [3:2].

(4) SWD output regulator current goes above the threshold set in “Register 0x20” [1:0].

When either event occurs for a period longer than tOutput_Current_Limiter time (max. = 10μs) then RTQ5119A sets the “Register 0x0B” [7:4] appropriately, drives GSI_n output signal as shown in Table 3 at the same time. The RTQ5119A continues to operate as normal.

The user can query the register space to determine the cause of the GSI_n signal assertion. Once user determine the cause, the user may clear the appropriate output current limiter status register as well as any other status registers individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. If the output current limiter condition is still present, then RTQ5119A will continue to assert GSI_n output signal and the appropriate status “Register 0x0B” [7:4] will remain at ‘1’. If the output current limiter condition persists, the user can set the appropriate mask register to remove the GSI_n output signal as shown in Table 4 and Table 5.

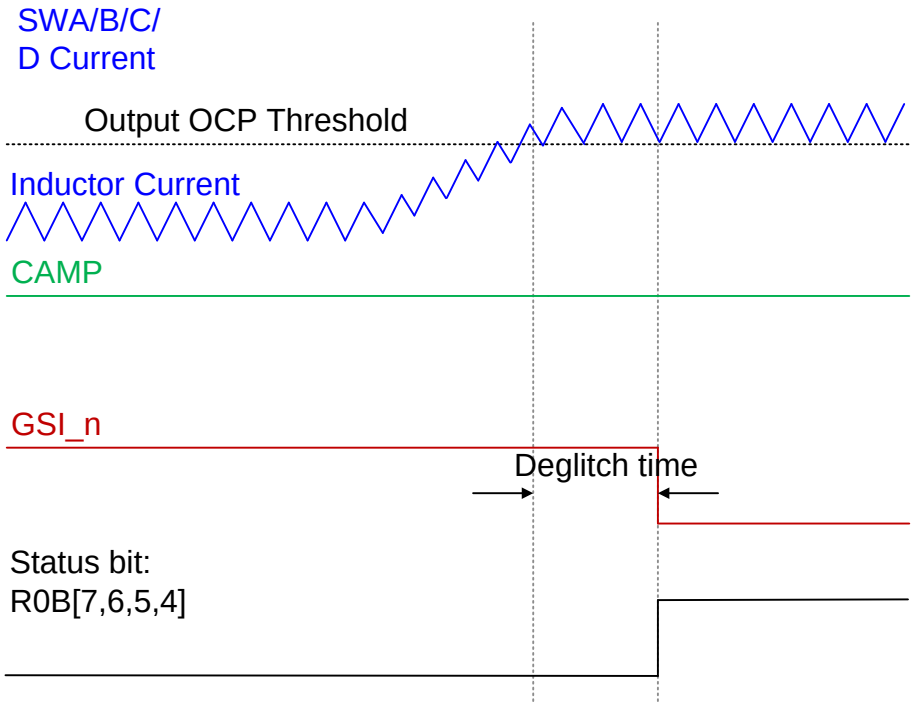


Figure 10. Output Current Limiter Protection

Output High Current Consumption Warning Event

The RTQ5119A supports high output current consumption warning mechanism for each of its regulator output. Through sensing the voltage drop across low-side MOSFET during conduction, the inductor current can be detected. If ADC function is enabled, the RTQ5119A actively monitors the average output current of the regulator.

There are four possibilities where RTQ5119A recognizes the high output current consumption.

(1) SWA output regulator average current goes above the threshold set in “Register 0x1C” [7:2].

(2) SWB output regulator average current goes above the threshold set in “Register 0x1D” [7:2].

(3) SWC output regulator average current goes above the threshold set in “Register 0x1E” [7:2].

(4) SWD output regulator average current goes above the threshold set in “Register 0x1F” [7:2].

When either event occurs, then RTQ5119A sets the “Register 0x09” [3:0] appropriately, and drives GSI_n output signal as shown in Table 3 at the same time. The RTQ5119A continues to operate as normal.

The user can query the register space to determine the cause of the GSI_n signal assertion. Once user determines the cause, the user can clear the appropriate output current consumption warning status register as well as any other status registers individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. If the output current consumption warning condition is still present then RTQ5119A will continue to assert GSI_n output signal and the appropriate status “Register 0x09” [3:0] will remain at ‘1’. If the output current consumption warning condition persists, the user can set the appropriate mask register to remove GSI_n output signal as shown in Table 4 and Table 5.

PMIC LDO Output Failure

In the event where RTQ5119A LDO outputs (VLDO_1.8V or VLDO_1.0V) failure occurs and RTQ5119A cannot reliably support external communication, the RTQ5119A has no control of CAMP signal and it is floated. The RTQ5119A returns to “offline” state.

PMIC High Temperature Warning and Critical Temperature Protection

The RTQ5119A provides a high temperature warning mechanism as well as critical temperature shutdown. An internal temperature sensor is placed near the heating MOSFET to detect the die temperature and protects RTQ5119A from over-heat operation. There are two registers associated with RTQ5119A’s die temperature : The high temperature warning threshold “Register 0x1B” [2:0] and shutdown temperature threshold “Register 0x2E” [2:0]. The value programmed in the shutdown temperature register must be equal or greater than value programmed in a warning threshold register.

If the die temperature goes above the threshold set in “Register 0x1B” [2:0] for a period longer than tHigh_Temp_Warning time (max. = 10μs), the RTQ5119A sets the “Register 0x09” [7] and drives GSI_n output signal as shown in Table 3 at the same time.

The user can query the register space to determine the cause of the GSI_n signal assertion. Once user determines the cause, the user can clear the temperature warning status register as well as any other status registers individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. If the high temperature warning condition is still present, then RTQ5119A will continue to assert GSI_n output signal and the appropriate status “Register 0x09” [7] will remain at ‘1’. If the high temperature warning condition persists, the user can set the appropriate mask register to remove GSI_n output signal as shown in Table 4 and Table 5.

If the die temperature goes above the threshold set in “Register 0x2E” [2:0] for a period longer than tShut_Down_Temp time (max.=10μs), the RTQ5119A internally generates VR Disable command and disables all of its switching output regulators, sets the code in “Register 0x05” [2:0], updates “Register 0x08” [6], and drives GSI_n and CAMP output signal as shown in Table 3 at the same time. The VLDO_1.8V and VLDO_1.0V output regulator keep active.

The user is expected to monitor the temperature status registers. When the temperature drops below the

threshold, the user must re-start the RTQ5119A by going through the power cycle of the VIN_MGMT input supply. If the RTQ5119A is in VIN_BULK input supply switchover state, the user must re-start the RTQ5119A by going through the power cycle of the VIN_BULK input supply.

Input Supply Switchover Event

There are two conditions of input supply switchover between VIN_MGMT and VIN_BULK.

(1) VIN_MGMT to VIN_BULK Switchover

After VR Enable command is registered, the RTQ5119A automatically switches over from VIN_MGMT to VIN_BULK input supply as VIN_MGMT goes below the threshold set in “Register 0x2F” [7].

When the above event occurs for a period longer than tInput_PWR_GOOD_GSI_Assertion time (max. = 10μs), then RTQ5119A sets the “Register 0x09” [4] and drives GSI_n output signal as shown in Table 3 at the same time. The RTQ5119A continues to operate as normal.

The user can query the register space to determine the cause of the GSI_n signal assertion. Once user determines the cause, the user can clear the status register individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. No further action is needed by the user or the RTQ5119A at this point.

Note that this event is treated differently by the RTQ5119A. When user clears this event, the RTQ5119A removes the GSI_n signal assertion even though there is no valid VIN_MGMT. This is to simplify user because user knows that there is no VIN_MGMT and yet user expects the RTQ5119A (as well as system) to continue to run normally and user should not have to worry about masking this event.

It is assumed that at some point VIN_MGMT supply will come back up again, RTQ5119A will detect it and assert GSI_n output signal as described below. At this point, RTQ5119A will be ready to assert GSI_n output signal again if VIN_MGMT input supply goes below the threshold set in “Register 0x2F” [7].

(2) Valid VIN_MGMT Supply Detection in Switchover Mode

When RTQ5119A is in switchover mode as described above, the VIN_MGMT input supply can power back up at any time. When VIN_MGMT input supply re-powers backup, the RTQ5119A sets the “Register 0x33” [4] and drives GSI_n output signal as shown in Table 3 at the same time. The RTQ5119A continues to operate as normal and automatically switches back to VIN_MGMT input supply.

The user can query the register space to determine the cause of the GSI_n signal assertion. Once user determines the cause, the user can clear the status register individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. No further action is needed by the user or the RTQ5119A at this point.

Note that this event is treated differently by the RTQ5119A. When user clears this event, the RTQ5119A removes the GSI_n signal assertion even though there is valid VIN_MGMT. This is to simplify user because user knows that VIN_MGMT input supply is back and so user expects the RTQ5119A (as well as system) to continue to run normally and user should not have to worry about masking this event.

It is assumed that if at some point VIN_MGMT supply goes below the threshold again, RTQ5119A will detect it and assert GSI_n output signal as described above. At this point, RTQ5119A will be ready to assert GSI_n output signal again if VIN_MGMT input supply re-powers back up again.

Packet Error Code (PEC) & Parity Error Event

In I^3C Basic mode, on RTQ5119A’s primary management interface, PEC function and parity function can be enabled. If enabled, when RTQ5119A detects either PEC error or parity error, the RTQ5119A sets the “Register 0x0A” [3:2] appropriately, drives GSI_n output signal as shown in Table 3, continues to operate as normal, and allows access to all registers.

The user can query the register space to determine the cause of the GSI_n signal assertion. Once user determines the cause, the user can clear the status register individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. No further action is needed by the user at this point.

(1) Parity Error Check Function

In I^2C mode, parity error checking is not supported except for supported CCCs. Only I^3C Basic mode supports parity error checking. By default, when RTQ5119A is put in I^3C Basic mode, parity function is automatically enabled. The user can disable the function after it is enabled. User can also disable the parity function with DEVCTRL CCC or by directly writing '1' to "Register 0x34" [5]. When parity function is disabled, the RTQ5119A simply ignores the "T" bit information from the master. The RTQ5119A implements ODD parity. If an odd number of bits in the byte are '1', the parity bit value is '0'. If even number of bits in the byte are '1', the parity bit value is '1'. The master computes the parity and sends during "T" bit.

(2) Packet Error Check (PEC) Function

In I^2C mode, packet error checking is not supported. Only I^3C Basic mode supports packet error checking. The RTQ5119A implements an 8-bit Packet Error Code (PEC) which is appended at the end of all transactions if PECs is enabled through DEVCTRL CCC or by directly writing '1' to "Register 0x34" [7]. The PEC is a CRC-8 value calculated on all the messages bytes except for START, STOP, REPEATED START conditions or Tbits, ACK and NACK and IBI header (7'h7E followed W=0) bits.

The polynomial for CRC-8 calculations is :

- $C(X) = X^8 + X^2 + X^1 + 1$

The seed value for PEC function is all zero.

When master calculates PEC for RTQ5119A, it includes LID and HID bits followed by R/W bit.

RTQ5119A Output Regulator Control Topology

The RTQ5119A applies A^2RCOT (Accurate Adaptive Ramp COT) to regulate the output voltage of VDD, VDDQ and VPP. The SWA and SWB can operate in either single phase mode or dual-phase mode. When operating as dual-phase mode, the interleaving PWM control is applied to balance the output current.

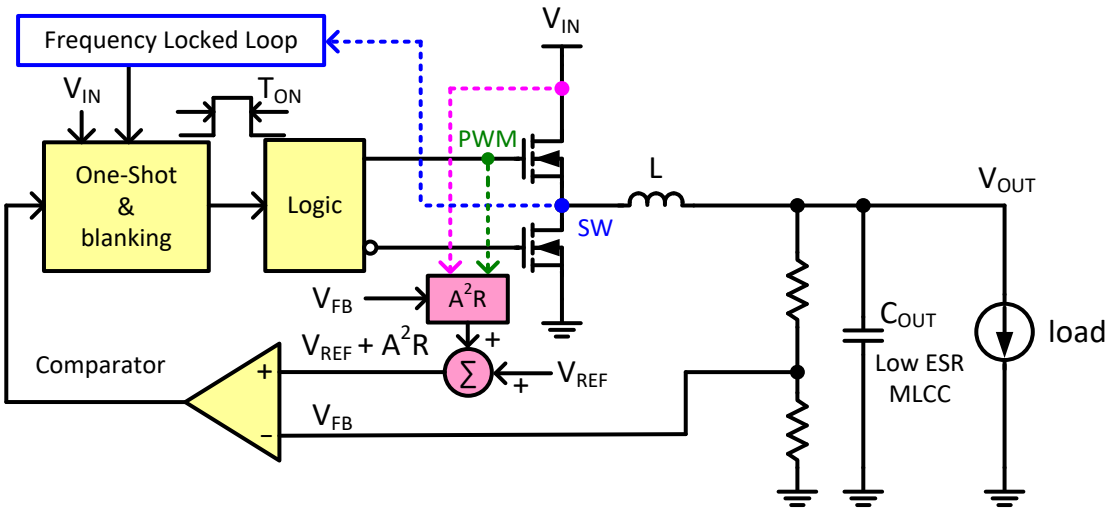


Figure 11. A^2RCOT Control Mechanism

Figure 11 illustrates a standard A^2RCOT control Buck converter. In order to achieve good stability with low-ESR ceramic capacitors, A^2RCOT generates an internal ramp by sensing V_{IN}, V_{FB} and PWM signal. The internal ramp is in phase with PWM signal and its magnitude is proportional to V_{IN}. Moreover, the average of V_{FB} can be well regulated at V_{REF} which makes good output load and line regulation. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

However, making the on-time proportional to V_{OUT} and inversely proportional to V_{IN} is not sufficient to achieve good constant-frequency behavior for following reasons. The voltage drops across MOSFET and inductor make equivalent conversion ratio to be smaller than ideal duty ratio. That is, the switching frequency is not fixed at

different output load conditions. Frequency is increasing at higher loading and junction temperature as compared to smaller loading and junction temperature.

One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. The A^{2}RCOT uses the frequency locked loop, measuring the actual switching frequency and modifying the on-time with a feedback loop to make the average switching frequency in the desired range.

The RTQ5119A control algorithm is simple to understand as depicted in Figure 12. The feedback voltage is compared to the reference voltage, V_{REF}, with the accurate adaptive ramp (A^{2}R) added. When the feedback signal is less than the combined reference, the on-time one-shot is triggered as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

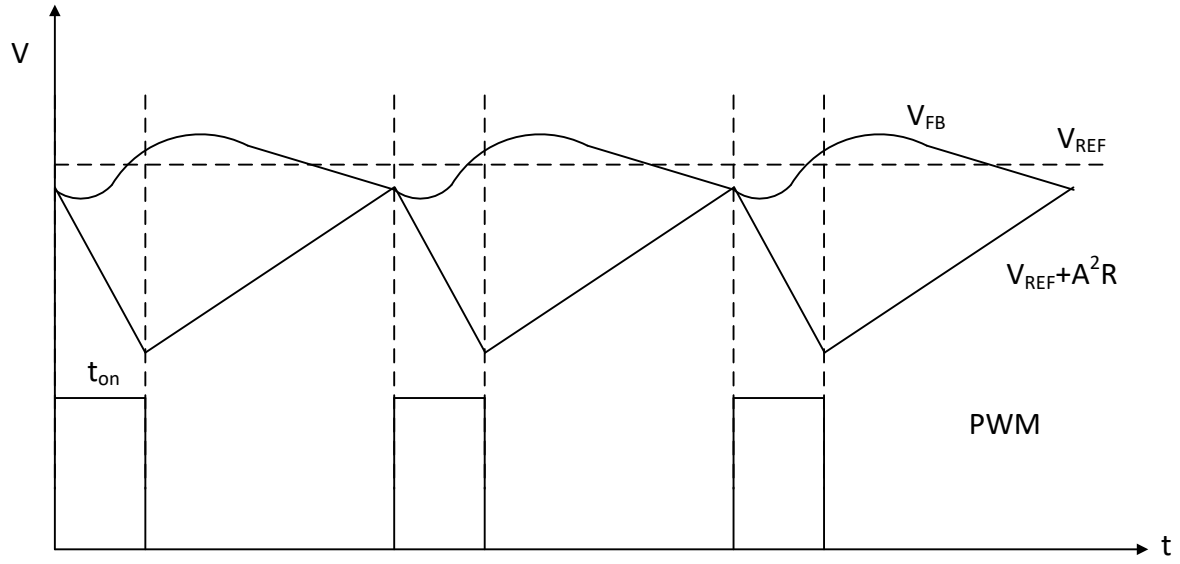


Figure 12. A^{2}RCOT PWM Control Diagram

Regulator Operating Mode Selection

The RTQ5119A offers two kinds of PWM operation in the light load. One is diode emulation mode (DEM), and another is forced continuous conduction mode (FCCM). The user can switch between DEM and FCCM by the “Register 0x29” [7:6], “Register 0x29” [3:2], “Register 0x2A” [7:6] and “Register 0x2A” [3:2] in diagnostic mode or in the configuration state of FSM before issuing the VR_EN command. The details of the two operation modes are described below.

(1) DEM (Diode Emulation Mode)

In diode emulation mode, the RTQ5119A automatically reduces switching frequency at light load conditions to maintain high efficiency. The reduction of frequency is achieved smoothly. As the output current decreases from heavy load conditions, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative current to flow when the inductor free-wheeling current becomes negative. As the load current is further decreased, it takes longer and longer time to discharge the output capacitor to the level that requires the next “ON” cycle. Contrarily, when the output current increases from light load to heavy load, the switching frequency increases to the pre-set value as the inductor

current reaches the continuous conduction. The transition load point between DEM and CCM operation is shown in Figure 13 and can be calculated as follows :

$$I_{LOAD\_BCM} = \frac{V_{IN} - V_{OUT}}{2L} \times t_{ON}$$

, where t_{ON} is the on-time of high-side MOSFET.

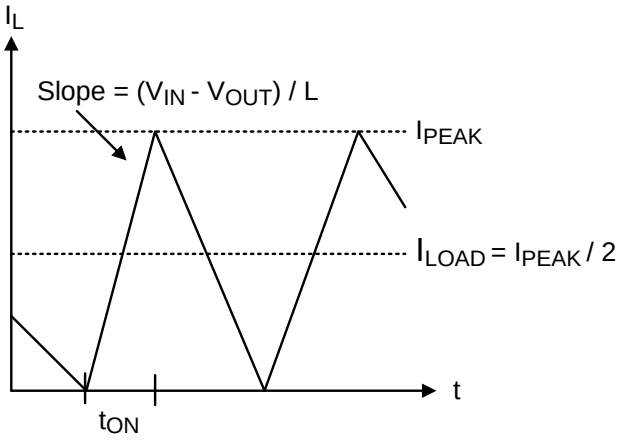


Figure 13. Boundary Condition of DEM/CCM

The switching frequency in DEM can be calculated as follows :

$$f_{SW}(I_{LOAD}) = \frac{2LI_{LOAD}}{V_{IN}t_{ON}^2\left(\frac{V_{IN}}{V_{OUT}} - 1\right)}$$

, where I_{LOAD} is smaller than I_{LOAD_BCM}.

As can be shown in the equation, switching frequency is a function of output load current, I_{LOAD}, and it is proportional to I_{LOAD}, which means it becomes higher at heavy load and reduces to almost zero at a very light load. Besides, inductor selection can also change the switching frequency in DEM. Choosing large inductance makes more switching loss as compared to small inductance. However, the core loss of inductor increases with larger inductor current ripple for a given inductor. That is, proper selection of inductor based on efficiency target is important.

Moreover, in order to achieve smooth transition from DEM to CCM or backward, during discontinuous switching, the on-time is immediately increased to add “hysteresis” to discourage the IC from switching back to continuous switching unless the load increases substantially. The RTQ5119A returns to continuous conduction as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced back to the length needed for presetting switching frequency and encouraging the circuit to remain in continuous conduction, preventing repetitive mode transitions between continuous switching and discontinuous switching.

(2) FCCM (Forced Continuous Conduction Mode)

Unlike diode emulation mode (DEM) that enables zero current detection (ZDC) to reject negative inductor current during low-side MOSFET turns on. The inductor current can be negative until next on-time is generated in FCCM. The switching frequency is fixed from no load to full load. Therefore, benefits like better transient response from light load to heavy load and smaller EMI/EMC come along with FCCM. Nevertheless, poor efficiency in light load is a tradeoff.

Analog-to-Digital Converter (ADC)

The RTQ5119A supports analog to digital converter (ADC) to monitor input supply voltages (VIN_BULK and VIN_MGMT) as well as output voltage regulator voltage (SWA, SWB, SWC, SWD, V_{BIAS}, VLDO_1.8V and VLDO_1.0V). The “Register 0x30” [7:3] allows to enable the ADC and select the desire input supply voltage or output supply voltage. It should be noticed that the ADC circuitry stops converting the SWA~SWD output voltage when VR_EN is programmed as "0". Only input supply voltages (VIN_BULK and VIN_MGMT) and output voltages (V_{BIAS}, VLDO_1.8V and VLDO_1.0V) are available for ADC reporting as VR_EN=0. The “Register 0x31” [7:0] provides the actual voltage measurement. The accuracy of the voltage measurement is as follows :

Table 6. RTQ5119A ADC Accuracy Table

Input Rail	ADC Range	ADC Accuracy
SWA, SWB, SWC Output Voltage	1050mV to 1160mV	± 1 LSB
	Outside of 1050mV to 1160mV	± 3 LSB
SWD Output Voltage	1750mV to 1850mV	± 1 LSB
	Outside of 1750 mV to 1850mV	± 3 LSB
VLDO_1.8V, VLDO_1.0V Output Voltage, VIN_BULK, VIN_MGMT Input Voltage	--	± 3 LSB
V_{BIAS} Output Voltage	--	± 6 LSB

The RTQ5119A also monitors output voltage regulator current or power (SWA, SWB, SWC and SWD) and updates "Register 0x0C" [7:0] for SWA, "Register 0x0D" [5:0] for SWB, "Register 0x0E" [5:0] for SWC and "Register 0x0F" [5:0] for SWD. The "Register 0x1B" [6] allows user to select whether RTQ5119A should report current measurements or power measurements. The current or power measurement reported in these registers are an average measurement over time period defined in "Register 0x30" [1:0]. If "Register 0x1B" [6] = '1', the "Register 0x1A" [1] allows user to select whether RTQ5119A should report individual rail power or total power in "Register 0x0C" [7:0]. The register update frequency of this register is configured in "Register 0x30" [1:0]. The accuracy of the current (> 0.5 A) or corresponding power measurement is ± 3 LSB or ± 6 LSB respectively. The accuracy of the current measurement (< 0.5 A) is ± 4 LSB or corresponding power measurement is ± 7 LSB respectively.

If "Register 0x1A" [1] = '1', the accuracy of total power reported in "Register 0x0C" = ± 12 LSB

Besides, the RTQ5119A die temperature is also monitored and converted to ADC value, the temperature is reported in "Register 0x33" [7:5]. The ADC for temperature automatically works as die temperature is higher than 85°C.

Table 7. General Purpose of ADC Units

Default Monitoring (5-channel) ± User Selection (1-channel)			
Channel Sensor	**Type**	**Monitor Register**	**Current/Power Measurement Selector**
SWA Output Current or Power	Default monitor	R0C[7:0]	R1B[6]=0 Set for current R1B[6]=1 Set for power R1A[1]=0 Report power for single switcher output R1A[1]=1 Report the sum of power for all switcher outputs (SWA,SWB,SWC,SWD)
SWB Output Current or Power		R0D[5:0]	
SWC Output Current or Power		R0E[5:0]	
SWD Output Current or Power		R0F[5:0]	
PMIC die Temperature		R33[7:5]	
SWA Output voltage	User selection R30[6:3]	R31[7:0]	
SWB Output voltage			
SWC Output voltage			
SWD Output voltage			
VIN_BULK Input voltage			
VIN_MGMT Input voltage			
VLDO_1.8V Output voltage			
VLDO_1.0V Output voltage			
V_{BIAS} Output Voltage			

PMIC Address ID (PID)

The RTQ5119A has PID input pin which allows assigning up to three different unique ID for I^2C and I^3C Basic protocol. The PID input pin is shared with SWD_FB_N pin.

At first power on, when VIN_MGMT input is applied, the RTQ5119A automatically senses its ID as well as checks the configuration “Register 0x4F” [1].

If SWD output regulator is enabled and intended to operate in a single ended remote sensing mode, the RTQ5119A offers three different ID as shown in Table 8. If SWD output regulator is not enabled, the RTQ5119A still offers three different ID as shown in Table 8.

If SWD output regulator is enabled and intended to operate in a differential remote sensing mode, there is only one default ID for the RTQ5119A as shown in Table 8 which means there can be only one PMIC on the DIMM (or I^2C and I^3C Basic bus).

Table 8. PMIC ID

R4F[1] =	PID Pin Connection on DIMM Board	PMIC ID	Comment
0	Short to GND	PID = 1001	PMIC can be configured
	Floating	PID = 1000	
	Short to 1.8V	PID = 1100	Connected to RTQ5119A’s VLDO_1.8V
1	Connect to differential sensing GND	PID = 1001	SWD differential sensing

Serial Address of PMIC Device

The 7-bit serial address of the RTQ5119A applies to both I^2C and I^3C Basic mode of operation identically. The 7-bit serial address composed of 4-bit LID and 3-bit HID as shown in Table 9. The RTQ5119A 4-bit LID can be configured as introduced in the section of PMIC Address ID (PID). The 3-bit HID can be set via CCC code SETHID.

Table 9. 7-bit Address of PMIC Device

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	X	0	X	1	1	1	R/W
PMIC Device Type ID (LID)				Host ID (HID)			Read/Write

Error Injection

The RTQ5119A offers error injection capability for the purpose of debug, test and validation at various stages as well as to isolate and map out faulty PMIC in memory subsystem for normal application environment. There are two conditions for error injection test.

(1) Error Injection Function Usage prior to VR Enable:

Prior to VR Enable command, the Error injection function can be invoked by setting error injection enable bit “Register 0x35” [7] = ‘1’ during the configuration state. If any of either VIN_BULK UV/OV or SWx OV/UV or Critical Temp Shutdown error is injected prior to VR Enable command, the RTQ5119A will not execute power on sequence and will not enable output regulators when receiving VR Enable command. The RTQ5119A will not update error log registers (“Register 0x04” to “Register 0x06”). The RTQ5119A updates appropriate status registers accordingly when error is injected.

(2) Error Injection Function Usage after VR Enable:

After RTQ5119A output regulators are enabled with VR Enable command and RTQ5119A is in programmable mode, the error injection function can be invoked by setting error injection enable bit “Register 0x35” [7] = ‘1’. If any of either

VIN_BULK UV/OV or SWx OV/UV or Critical Temp Shutdown error is injected, the RTQ5119A executes power-off sequence to disable output regulators and updates the error log registers (“Register 0x04” to “Register 0x06”) as well as status registers accordingly.

On the other hand, after RTQ5119A output regulators are enabled with VR Enable command and RTQ5119A is in secure mode, the error injection enabling “Register 0x35” [7] = ‘1’ is disallowed. The RTQ5119A ignores any attempts to inject any error and will not execute power-off sequence to disable output regulators and will not update any error log or status registers.

To exit error injection mode of operation, the RTQ5119A requires power cycle of VIN_BULK and VIN_MGMT input supply.

Absolute Maximum Ratings (Note1)

- Supply Input Voltage, VINA, VINB, VINC, VIND ---------- –0.3V to 17V
- Supply Input Voltage, VIN_MGNT ---------- –0.3V to 6V
- AGND to PGND ---------- –0.3V to 0.3V
- Switching PIN, SWA, SWB, SWC, SWD
  - DC ---------- –0.3V to 17V
  - < 50ns ---------- –4.5V to 20V
- Boot Voltage
  - BOOT to SWA (BOOT-SWA) ---------- –0.3V to 6V
  - BOOT_SWB (BOOT-SWB) ---------- –0.3V to 6V
  - BOOT_SWC (BOOT-SWC) ---------- –0.3V to 6V
  - BOOT_SWD (BOOT-SWD) ---------- –0.3V to 6V
- Remote GND Pin (SWAB_FB_N, SWC_FB_N) ---------- –0.3V to 2.2V
- Other I/O ---------- –0.3V to +6V
- Power Dissipation, P_D @ T_A = 25°C
  - VQFN-35L 5x5 (FC) ---------- 4.05W
- Package Thermal Resistance (Note 2)
  - WQFN-35L 5x5, θ_{JA} ---------- 24.7°C/W
  - WQFN-35L 5x5, θ_{JC} ---------- 0.1°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- –40°C to 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM ---------- 2kV
  - CDM ---------- 500V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{INA}, V_{INB}, V_{INC}, V_{IND} ---------- 4.25V to 15V
- Supply Input Voltage, V_{IN_MGMT} ---------- 3V to 3.6V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN_SWA} = V_{IN_SWB} = V_{IN_SWC} = V_{IN_SWD} = 12V, V_{IN_MGMT} = 3.3V, T_J = –40°C to 125°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
VIN_MGMT Supply Current	I_{Q_VMGMT}	VIN_MGMT = 3.3V, VIN_BULK = 0V	--	780	--	μA
		VIN_MGMT = 3.3V, VIN_BULK = 12V	--	330	--	μA
VIN Supply Current	I_{Q_VIN}	VR_EN = 0	--	430	--	μA
		Io = 0mA, not switching	--	3	--	mA
VIN_MGMT Power Good and Switch-over and OVP Threshold						
VIN_MGMT Power Good High Threshold		Setting by reg_0x2F"[7] = "0"	--	2.8	--	V
		Setting by reg_0x2F"[7] = "1"	--	2.85	--	V
VIN_MGMT Switch Over Threshold		Setting by reg_0x2F"[7] = "0"	--	2.7	--	V
		Setting by reg_0x2F"[7] = "1"	--	2.75	--	V
VIN_MGMT Over-Voltage Threshold		Setting by reg_0x1B"[5] = "0"	--	3.8	--	V
		Setting by reg_0x1B"[5] = "1"	--	3.7	--	V
VIN _Bulk Power Good and OVP Protection						
VIN_BULK Power Good Falling Threshold		Setting by reg_0x1A"[7:5] = "001"	--	9.5	--	V
		Setting by reg_0x1A"[7:5] = "010"	--	8.5	--	V
		Setting by reg_0x1A"[7:5] = "011"	--	7.5	-	V
		Setting by reg_0x1A"[7:5] = "100"	--	6.5	-	V
		Setting by reg_0x1A"[7:5] = "101"	--	5.5	--	V
		Setting by reg_0x1A"[7:5] = "110"	--	4.25	--	V
VIN_BULK Power Good Rising Threshold		Setting by reg_0x1A"[7:5] = "001"	--	10.25	--	V
		Setting by reg_0x1A"[7:5] = "010"	--	9.25	--	V
		Setting by reg_0x1A"[7:5] = "011"	--	8.25	--	V
		Setting by reg_0x1A"[7:5] = "100"	--	7.25	--	V
		Setting by reg_0x1A"[7:5] = "101"	--	6.25	--	V
		Setting by reg_0x1A"[7:5] = "110"	--	4.75	--	V
VIN_BULK Over-Voltage Rising Threshold	$V_{IN\_BULK\_OVH}$	Setting by reg_0x1B"[7] = "0"	--	14.5	--	V
		Setting by reg_0x1B"[7] = "1"	--	16	--	V
VIN_BULK Over-Voltage Hysteresis	$V_{IN\_BULK\_HYS}$	OVP release hysteresis, OVL= $V_{IN\_BULK\_OVH}$ – $V_{IN\_BULK\_HYS}$	--	1	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I²C, I³C and Interface DC Electrical Specification						
SDA, SCL Operate Frequency	f_{SCL}		0.01	--	12.5	MHz
SDA, SCL Input High Voltage	$V_{IH\_SDA\_SCL}$		0.7	--	3.6	V
SDA, SCL Input Low Voltage	$V_{IL\_SDA\_SCL}$		–0.3	--	0.3	V
Input High Voltage (CAMP)			1.2	--	3.6	V
Input Low Voltage (CAMP)		Setting by reg_0x32"[5] = "1"	–0.3	--	0.3	V
Output Low Voltage (SDA, GSI_n, CAMP)	V_{OL}	Io = 3mA	--	--	0.3	V
Output High Voltage (SDA)	V_{OH}	Io = -3mA	0.75	--	--	V
SDA Output Pull-Up Driver Impedance	R_{ON}		--	40	100	Ω
SDA Output Pull-Down Driver Impedance	R_{ON}		--	20	100	Ω
GSI_n Output Pull-Down Driver Impedance	R_{ON}		--	10	100	Ω
CAMP Output Pull-Down Driver Impedance	R_{ON}		--	45	100	Ω
Input Current (SDA, SCL)	I_i	–100mV < Vi < VDD_pull high	–10	--	10	µA
PID High Voltage	P_{ID_VIH}		1.2	--	--	V
PID Low Voltage	P_{ID_VIL}		--	--	0.23	V
SWA, SWB Rail – VDD (1.1V) - Dual Phase Regulator (0.8V to 1.435V or 0.6V to 1.235V, I_{MAX} = 3.5A for each rail)						
Output Voltage Setting	V_{setAB}	SWA(single phase) or SWA+SWB(dual phase) setting by reg_0x21"[7:1], reg_0x2B[5]= "0"	0.8	--	1.435	V
		SWB(single phase) setting by reg_0x23"[7:1], reg_0x2B[4]= "0"				
		SWA(single phase) or SWA+SWB(dual phase) setting by reg_0x21"[7:1], reg_0x2B[5]= "1"	0.6	--	1.235	V
		SWB(single phase) setting by reg_0x23"[7:1], reg_0x2B[4]= "1"				
Output Voltage Accuracy	$V_{out\_SWA/B}$	Io = 0A, operating at CCM	–0.75	--	+0.75	% of V_{setAB}
Dynamic Voltage Scale Slew Rate			0.9	1	1.1	mV/µs
SWA/B Soft-Start/Stop Time						
Soft-Start Time		t_{set} = 1ms ~ 14ms	–15	--	+15	% of T_{set}

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Soft-Stop Time		t_{set} = 0.5ms ~ 4ms	–20	--	+20	% of T_{set}
SWA/B Switching Frequency (Note 5)						
Switching Frequency	$f_{SW\_SWA/B}$	Setting by reg_0x29"[5:4] = "00"	0.38	0.45	0.52	MHz
		Setting by reg_0x29"[5:4] = "01" (default)	0.57	0.67	0.77	MHz
		Setting by reg_0x29"[5:4] = "10"	0.76	0.89	1.02	MHz
		Setting by reg_0x29"[5:4] = "11"	0.94	1.11	1.28	MHz
SWA/B Power Good Indicator						
Power Good Threshold Low-Side Voltage		Setting by reg_0x21"[0] = "0"	--	–5	--	% of V_{setAB}
		Setting by reg_0x21"[0] = "1" (default)	--	–7.5	--	% of V_{setAB}
PG_L Propagation Delay	$t_{PGLDLY\_SWA/B}$		--	5	--	µs
Power Good Threshold High-Side Voltage		Setting by reg_0x22"[7:6] = "00"	--	+5	--	% of V_{setAB}
		Setting by reg_0x22"[7:6] = "01" (default)	+5	+7.5	+10	% of V_{setAB}
		Setting by reg_0x22"[7:6] = "10"	--	+10	--	% of V_{setAB}
		Setting by reg_0x22"[7:6] = "11"	--	+3	--	% of V_{setAB}
PG_H Propagation Delay	$t_{PGHDLY\_SWA/B}$		--	5	--	µs
SWA/B Protections						
OVP Threshold		Setting by reg_0x22"[5:4] = "00" (default)	--	+7.5	--	% of V_{setAB}
		Setting by reg_0x22"[5:4] = "01"	--	+10	--	% of V_{setAB}
		Setting by reg_0x22"[5:4] = "10"	--	+12.5	--	% of V_{setAB}
		Setting by reg_0x22"[5:4] = "11"	--	+5	-	% of V_{setAB}
OVP Propagation Delay	$t_{Output\_OV\_VR\_Disable\_SWA/B}$		--	5	--	µs
UVP Threshold		Setting by reg_0x22"[3:2] = "00" (default)	--	–10	--	% of V_{setAB}
		Setting by reg_0x22"[3:2] = "01"	--	–12.5	-	% of V_{setAB}
		Setting by reg_0x22"[3:2] = "10"	--	–5	--	% of V_{setAB}
		Setting by reg_0x22"[3:2] = "11"	--	–7.5	--	% of V_{setAB}

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UVP Propagation Delay	$t_{Output\_UV\_VR\_Disable\_SWA/B}$		--	5	--	µs
SWA/B Current Limit						
Current Limit	$I_{LIM\_SWA/B\_LOW\ Current}$	For Low Current, valley current limited Setting by reg_0x20"[7:6] = "00"	--	2.5	--	A
		Setting by reg_0x20"[7:6] = "01"	--	3	--	A
		Setting by reg_0x20"[7:6] = "10" (default)	--	3.5	--	A
		Setting by reg_0x20"[7:6] = "11"	--	4	--	A
SWC Rail – VDDQ (1.1V) – Single Phase Regulator (0.8V to 1.435V or 0.6V to 1.235V, I_{MAX} = 3.5A)						
Output Voltage Setting	V_{setC}	Setting by reg_0x25"[7:1], reg_0x2B[3]= "0"	0.8	--	1.435	V
		Setting by reg_0x25"[7:1], reg_0x2B[3]= "1"	0.6	--	1.235	V
Output Voltage Accuracy	V_{out_SWC}	Io = 0A, operating at CCM	–0.75	--	+0.75	% of V_{setC}
Dynamic Voltage Scale Slew Rate			0.9	1	1.1	mV/µs
SWC Soft-Start/Stop Time						
Soft-Start Time		t_{set} = 1ms ~ 14ms	–15	--	+15	% of T_{set}
Soft-Stop Time		t_{set} = 0.5ms ~ 4ms	–20	--	+20	% of T_{set}
SWC Switching Frequency (Note 5)						
Switching Frequency	f_{SW_SWC}	Setting by reg_0x2A"[5:4] = "00"	0.38	0.45	0.52	MHz
		Setting by reg_0x2A"[5:4] = "01" (default)	0.57	0.67	0.77	MHz
		Setting by reg_0x2A"[5:4] = "10"	0.76	0.89	1.02	MHz
		Setting by reg_0x2A"[5:4] = "11"	0.94	1.11	1.28	MHz
SWC Power Good Indicator						
Power Good Threshold Low-Side Voltage		Setting by reg_0x25"[0] = "0"	--	–5	--	% of V_{setC}
		Setting by reg_0x25"[0] = "1"	--	–7.5	--	% of V_{setC}
PG_L Propagation Delay	t_{PGLDLY_SWC}		--	5	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Good Threshold High-Side Voltage		Setting by reg_0x26"[7:6] = "00" (default)	--	+5	--	% of V_{setC}
		Setting by reg_0x26"[7:6] = "01"	--	+7.5	--	% of V_{setC}
		Setting by reg_0x26"[7:6] = "10"	--	+10	--	% of V_{setC}
		Setting by reg_0x26"[7:6] = "11"	--	+3	--	% of V_{setC}
PG_H Propagation Delay	t_{PGHDLY_SWC}		--	5	--	µs
SWC Protections						
OVP Threshold		Setting by reg_0x26"[5:4] = "00" (default)	--	+7.5	--	% of V_{setC}
		Setting by reg_0x26"[5:4] = "01"	--	+10	--	% of V_{setC}
		Setting by reg_0x26"[5:4] = "10"	--	+12.5	--	% of V_{setC}
		Setting by reg_0x26"[5:4] = "11"	--	+5	--	% of V_{setC}
OVP Propagation Delay	$t_{Output\_OV\_VR\_Disable\_SWC}$		--	5	--	µs
UVP Threshold		Setting by reg_0x26"[3:2] = "00" (default)	--	–10	--	% of V_{setC}
		Setting by reg_0x26"[3:2] = "01"	--	–12.5	--	% of V_{setC}
		Setting by reg_0x26"[3:2] = "10"	--	–5	--	% of V_{setC}
		Setting by reg_0x26"[3:2] = "11"	--	–7.5	--	% of V_{setC}
UVP Propagation Delay	$t_{Output\_UV\_VR\_Disable\_SWC}$		--	5	--	µs
SWC Current Limit						
Current Limit	$I_{LIM\_SWC\_LOW}$ Current	For Low Current, valley current limited Setting by reg_0x20"[3:2] = "00"	--	2.5	--	A
		Setting by reg_0x20"[3:2] = "01"	--	3	--	A
		Setting by reg_0x20"[3:2] = "10" (default)	--	3.5	--	A
		Setting by reg_0x20"[3:2] = "11"	--	4	--	A
SWD Rail – VPP (1.8V) – Single Phase Regulator (1.5V to 2.135V or 2.2V to 2.835V, I_{MAX} = 3.5A)						
Output Voltage Setting	V_{setD}	Setting by reg_0x27"[7:1], 5mV/Step, reg_0x2B"[0] =”0”	1.5	--	2.135	V
		Setting by reg_0x27"[7:1], 5mV/Step, reg_0x2B"[0] =”1”	2.2	--	2.835	V
Output Voltage Accuracy	V_{out_SWD}	Io = 0A, operating at CCM	–0.75	--	+0.75	% of V_{setD}

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Dynamic Voltage Scale Slew Rate			0.9	1	1.1	mV/μs
SWD Soft-Start/Stop Time						
Soft-Start Time		t_{set} = 1ms ~ 14ms	–15	--	+15	% of T_{set}
Soft-Stop Time		t_{set} = 1ms ~ 8ms	–20	--	+20	% of T_{set}
SWD Switching Frequency						
Switching Frequency	f_{SW_SWD}	Setting by reg_0x2A"[1:0] = "00"	0.425	0.5	0.575	MHz
		Setting by reg_0x2A"[1:0] = "01"	0.6375	0.75	0.8635	MHz
		Setting by reg_0x2A"[1:0] = "10" (default)	0.85	1	1.15	MHz
		Setting by reg_0x2A"[1:0] = "11"	1.0625	1.25	1.4375	MHz
SWD Power Good Indicator						
Power Good Threshold Low-Side Voltage		Setting by reg_0x27"[0] = "0" (default)	--	–5	--	% of V_{setD}
		Setting by reg_0x27"[0] = "1"	--	–7.5	--	% of V_{setD}
PG_L Propagation Delay	t_{PGLDLY_SWD}		--	5	--	μs
Power Good Threshold High-Side Voltage		Setting by reg_0x28"[7:6] = "00"	--	+5	--	% of V_{setD}
		Setting by reg_0x28"[7:6] = "01" (default)	+5	+7.5	+10	% of V_{setD}
		Setting by reg_0x28"[7:6] = "10"	--	+10	--	% of V_{setD}
		Setting by reg_0x28"[7:6] = "11"	--	+3	--	% of V_{setD}
PG_H Propagation Delay	t_{PGHDLY_SWD}		--	5	--	μs
SWD Protections						
OVP Threshold		Setting by reg_0x28"[5:4] = "00"	--	+7.5	--	% of V_{setD}
		Setting by reg_0x28"[5:4] = "01"	--	+10	--	% of V_{setD}
		Setting by reg_0x28"[5:4] = "10" (default)	--	+12.5	--	% of V_{setD}
		Setting by reg_0x28"[5:4] = "11"	--	+5	--	% of V_{setD}
OVP Propagation Delay	$t_{Output\_OV\_VR\_Disable\_SWD}$		--	5	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UVP Threshold		Setting by reg_0x28"[3:2] = "00" (default)	--	–10	--	% of V_{setD}
		Setting by reg_0x28"[3:2] = "01"	--	–12.5	-	% of V_{setD}
		Setting by reg_0x28"[3:2] = "10"	--	–5	--	% of V_{setD}
		Setting by reg_0x28"[3:2] = "11"	--	–7.5	--	% of V_{setD}
UVP Propagation Delay	$t_{Output\_UV\_VR\_Disable\_SWD}$		--	5	--	µs
SWD Current Limit						
Current Limit	$I_{LIM\_SWD\_LOW\ Current}$	For Low Current, valley current limited Setting by reg_0x20"[1:0] = "00"	--	2.5	--	A
		Setting by reg_0x20"[1:0] = "01"	--	3	--	A
		Setting by reg_0x20"[1:0] = "10" (default)	--	3.5	--	A
		Setting by reg_0x20"[1:0] = "11"	--	4	--	A
VLDO_1.8V (1.8V, I_{MAX} = 25mA)						
Output Voltage	$V_{LDO\_1.8V}$	Setting by reg_0x2B"[7:6] = "00"	--	1.7	--	V
		Setting by reg_0x2B"[7:6] = "01" (default)	--	1.8	--	V
		Setting by reg_0x2B"[7:6] = "10"	--	1.9	--	V
Output Voltage Accuracy		$V_{LDO\_1.8V}$ = 1.8V	–30	--	30	mV
		DC + AC	–100	--	100	mV
Soft-Start Time			--	0.17	--	ms
Power Good Threshold		Setting by reg_0x1A"[2] = "0"	--	1.55	--	V
PG Propagation Delay	$t_{PGLDLY\_LDO1.8}$		--	5	--	µs
Current Limit			30	--	--	mA
CREG/VLDO_1.0V (1.0V, I_{MAX} = 20mA)						
Output Voltage	V_{CREG}	Setting by reg_0x2B"[2:1] = "00"	--	0.9	--	V
		Setting by reg_0x2B"[2:1] = "01" (default)	--	1.0	--	V
		Setting by reg_0x2B"[2:1] = "10"	--	1.1	--	V
		Setting by reg_0x2B"[2:1] = "11"	--	1.2	--	V
Output Voltage Accuracy		V_{CREG} = 1.1V	–20	--	+20	mV
		DC + AC	–50	--	+50	mV
Soft-Start Time			--	0.17	--	ms
Power Good Threshold		Setting by reg_0x1A"[0] = "0" (default)	--	–10	--	% of V_{CREG}
		Setting by reg_0x1A"[0] = "1"	--	–15	--	% of V_{CREG}

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PG Propagation Delay	tPGLDLY_CREG		--	5	--	μs
Current Limit			25	--	--	mA
VBIAS (5V, IMAX = 40mA, Internal use only)						
Output Voltage	VBIAS		--	5	-	V
Power Good High Threshold		Setting by reg_0x1A"[3] = "0" (default)	--	4	--	V
		Setting by reg_0x1A"[3] = "1"	--	3.6	--	V
Power Good Low Threshold		Setting by reg_0x1A"[3] = "0" (default)	--	3.6	--	V
		Setting by reg_0x1A"[3] = "1"	--	3.2	--	V
PG Propagation Delay	tPGLDLY_VBIAS		--	5	--	μs

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on Richtek twelve layers EVB with DIMM card size. The design of trace area and vias is based on layout guide.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. The typical switching frequency defined in JESD301-1A are summarized as below :

For SWA :

0x29"[5:4] = "00" → Typ. f_{SW} = 500kHz

0x29"[5:4] = "01" → Typ. f_{SW} = 750kHz

0x29"[5:4] = "10" → Typ. f_{SW} = 1000kHz

0x29"[5:4] = "11" → Typ. f_{SW} = 1250kHz

For SWB :

0x29"[1:0] = "00" → Typ. f_{SW} = 500kHz

0x29"[1:0] = "01" → Typ. f_{SW} = 750kHz

0x29"[1:0] = "10" → Typ. f_{SW} = 1000kHz

0x29"[1:0] = "11" → Typ. f_{SW} = 1250kHz

For SWC :

0x2A"[5:4] = "00" → Typ. f_{SW} = 500kHz

0x2A"[5:4] = "01" → Typ. f_{SW} = 750kHz

0x2A"[5:4] = "10" → Typ. f_{SW} = 1000kHz

0x2A"[5:4] = "11" → Typ. f_{SW} = 1250kHz

Typical Application Circuit

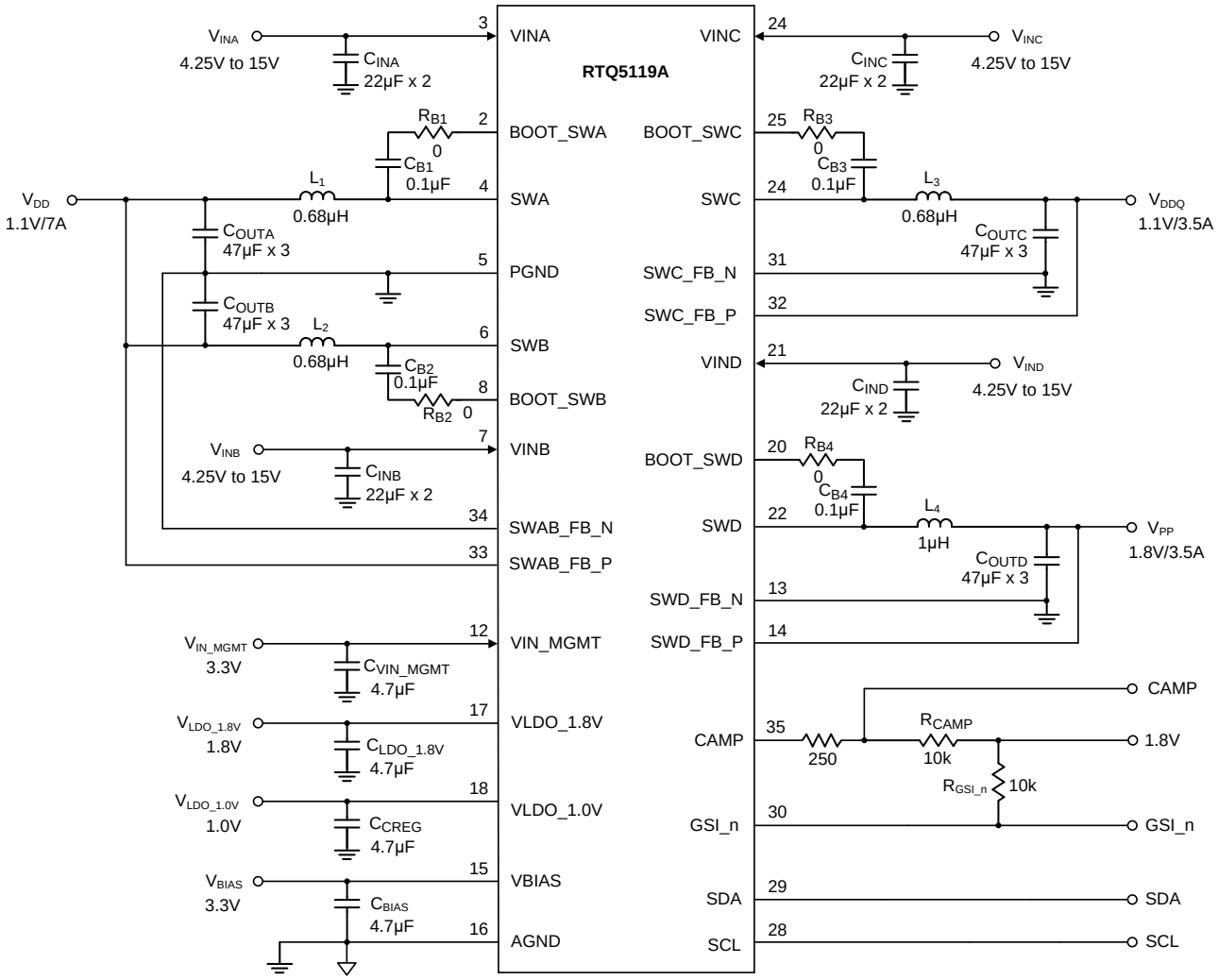


Figure 14. Typical application circuit when SWA and SWB are combined as two phase, single output rail.

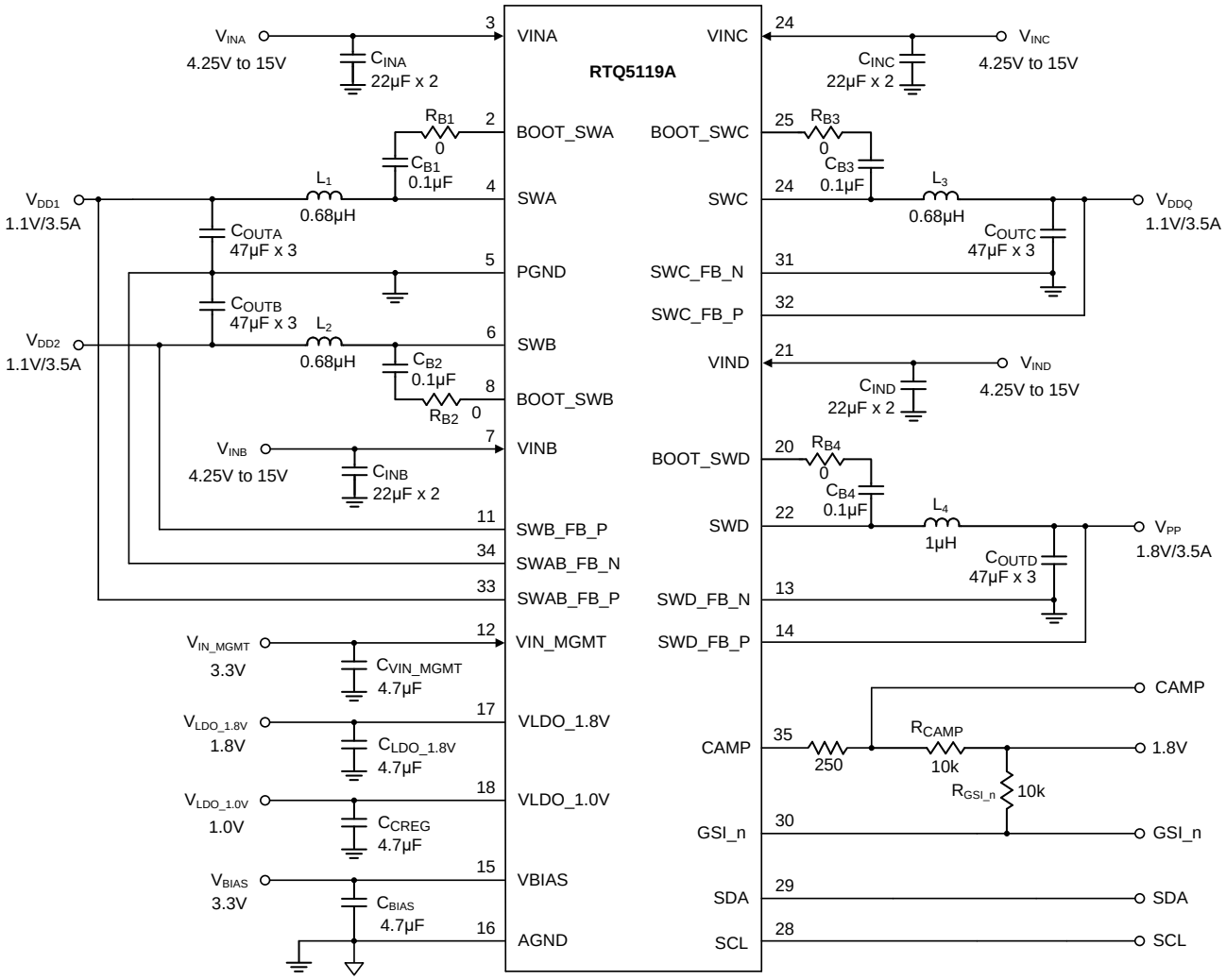
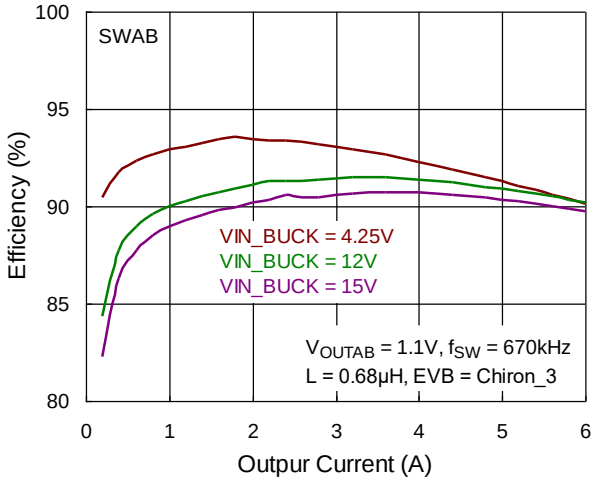


Figure 15. Typical application circuit when SWA and SWB are separated for 2-outputs.

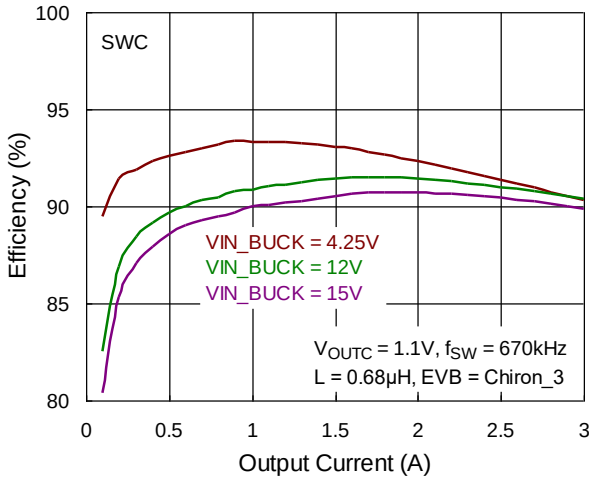
Typical Operating Characteristics

Performance waveforms are tested on the evaluation board of the Typical Application Circuit, VIN_BULK = 12V, VIN_MGMT = 3.3V, V_{OUTAB} = V_{DD}= 1.1V, V_{OUTC} = V_{DDQ} = 1.1V, V_{OUTD} = V_{PP} = 1.8V, L_1 = L_2 = L_3 = 0.68µH, L_4 = 1µH, T_J = 25°C, unless otherwise noted.

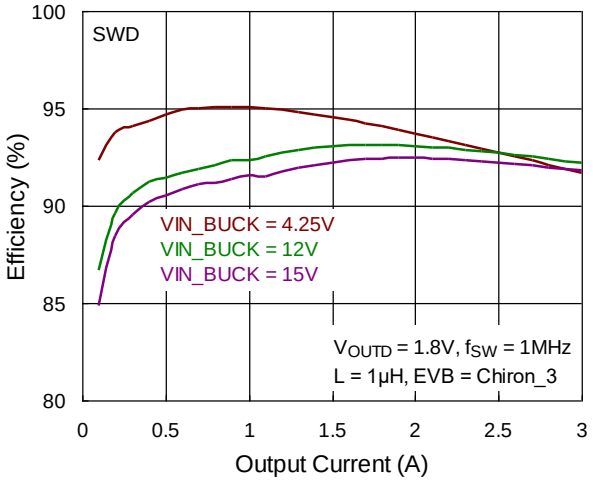
Efficiency vs. Ouptut Current



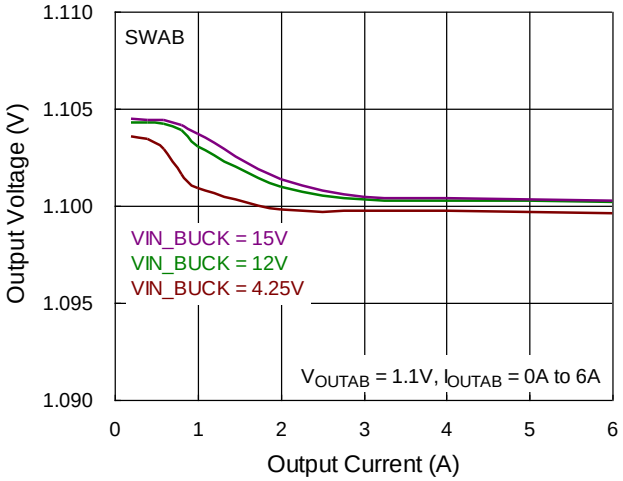
Efficiecny vs. Output Current



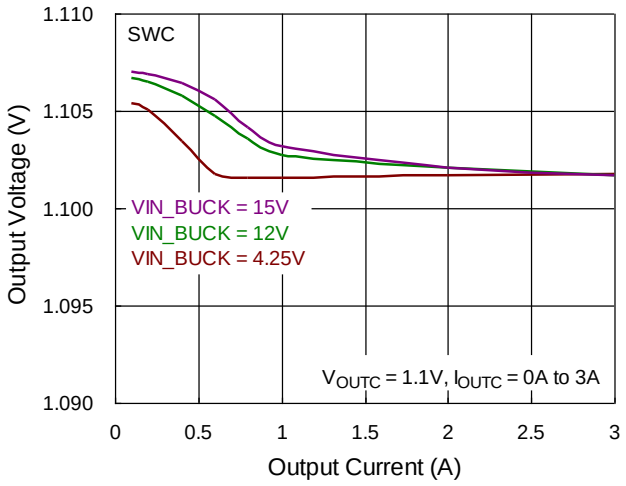
Efficiecny vs. Output Current



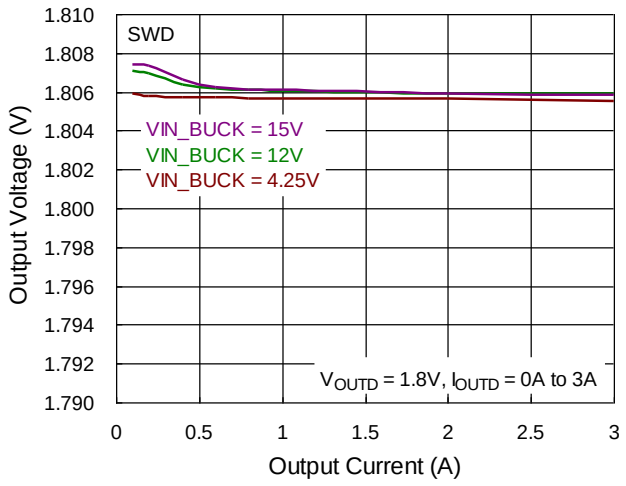
Output Voltage vs. Output Current



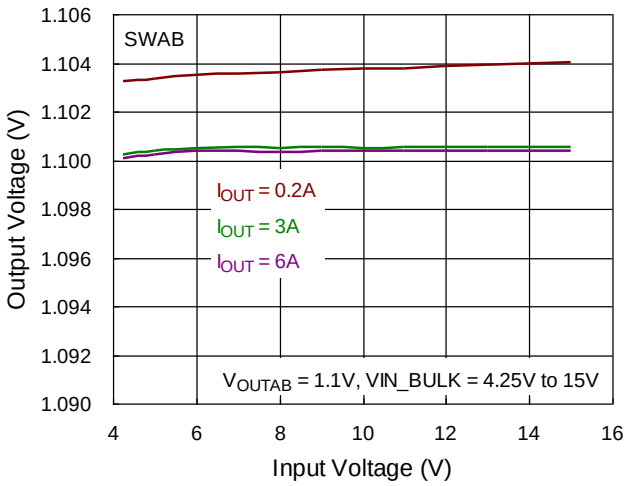
Output Voltage vs. Output Current



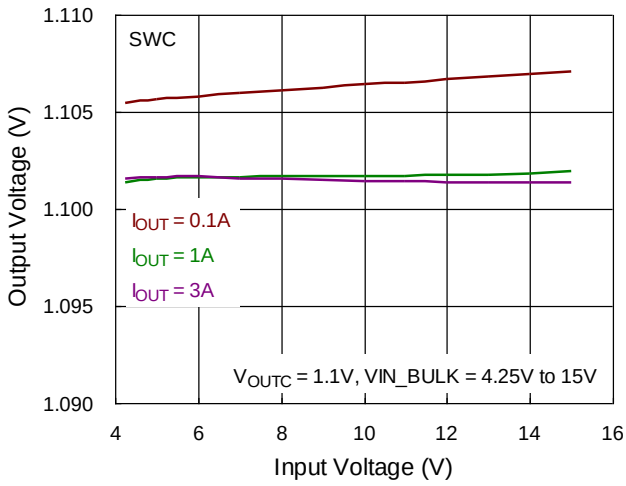
Output Voltage vs. Output Current



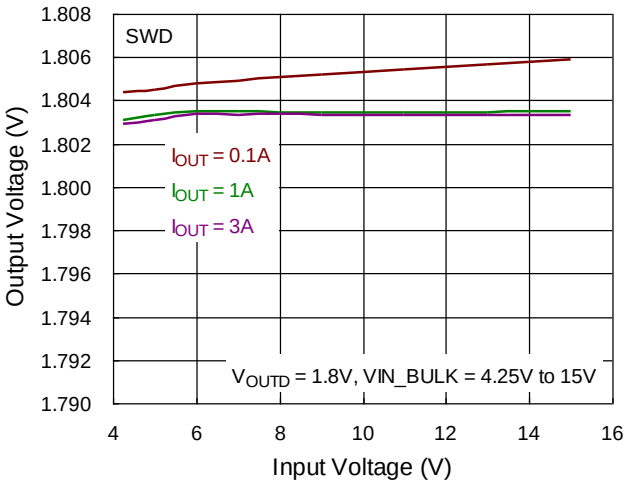
Output Voltage vs. Input Voltage



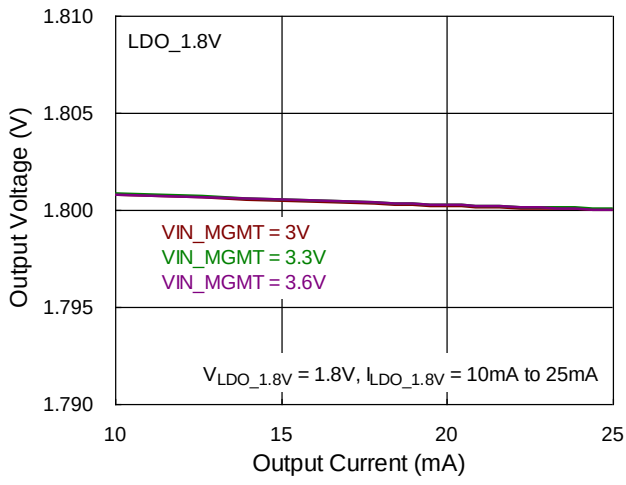
Output Voltage vs. Input Voltage



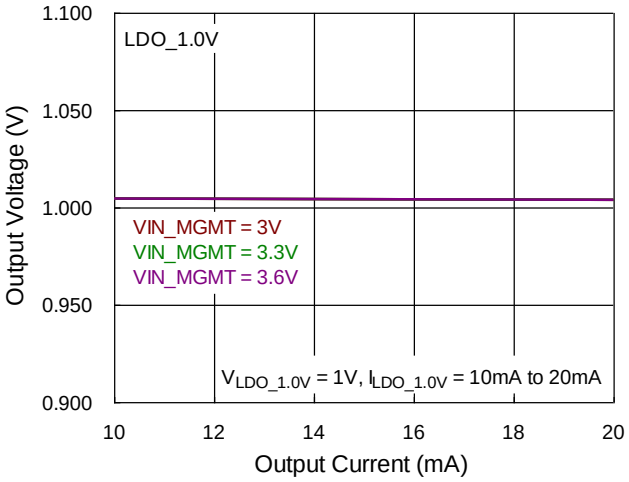
Output Voltage vs. Input Voltage



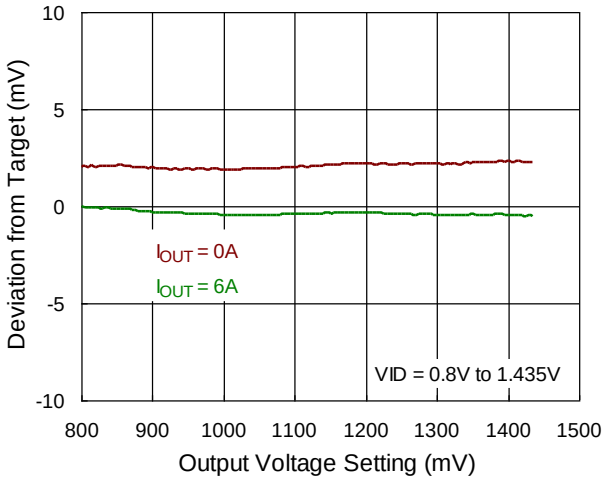
Output Voltage vs. Output Current



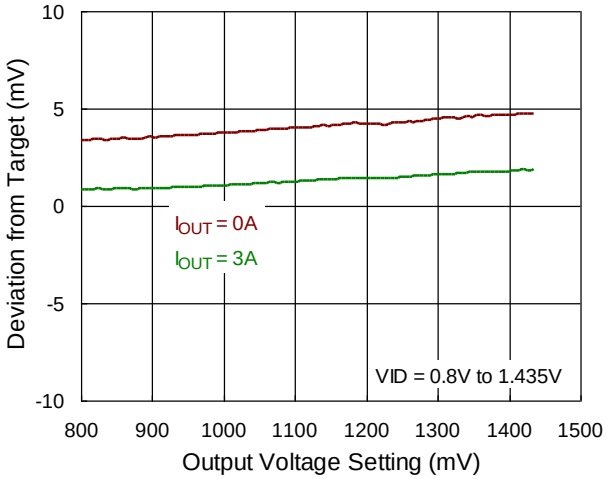
Output Voltage vs. Output Current



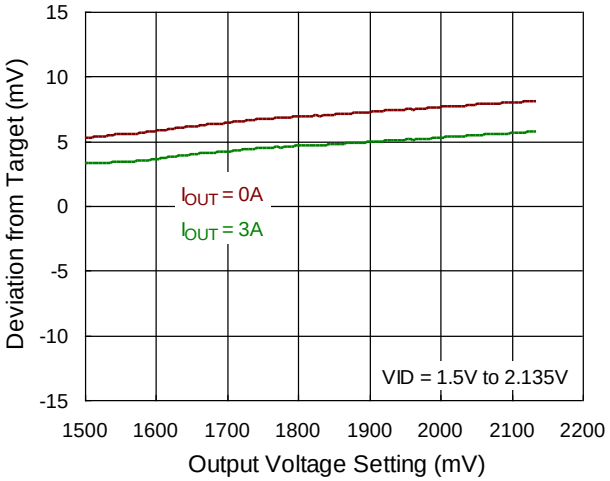
SWAB VID Setting Deviation



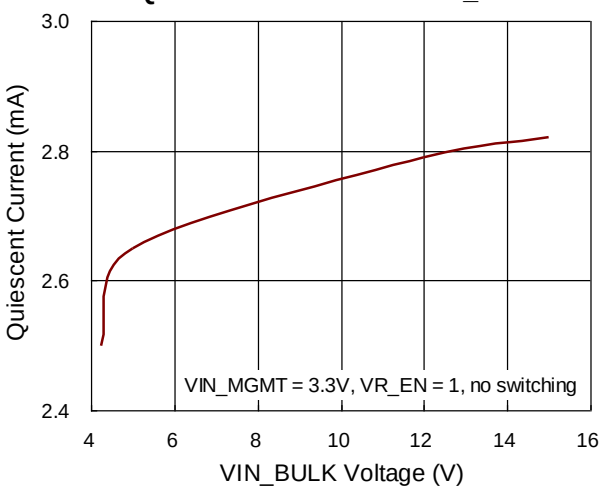
SWC VID Setting Deviation



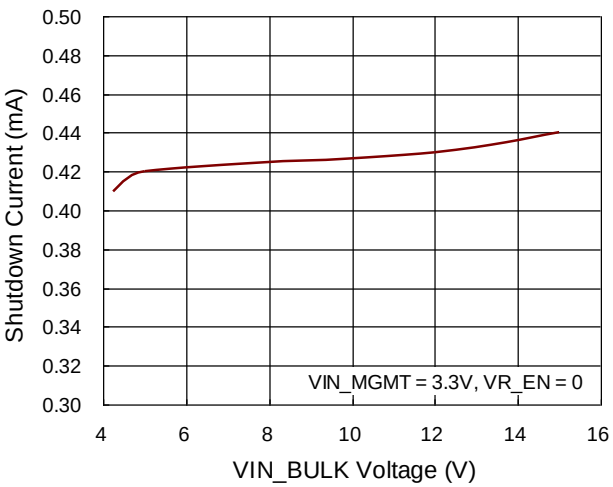
SWD VID Setting Deviation



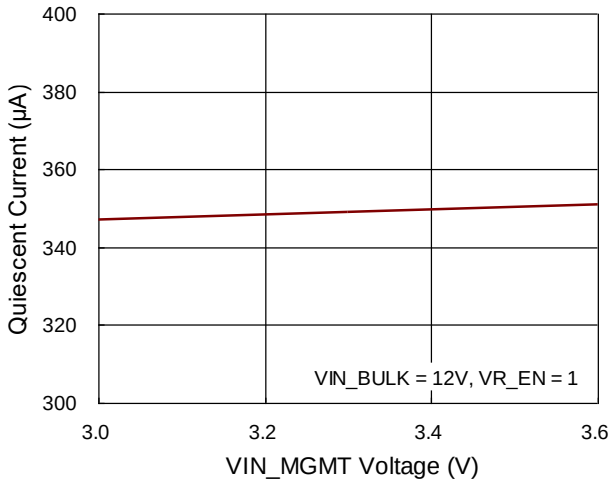
Quiescent Current vs. VIN_BULK



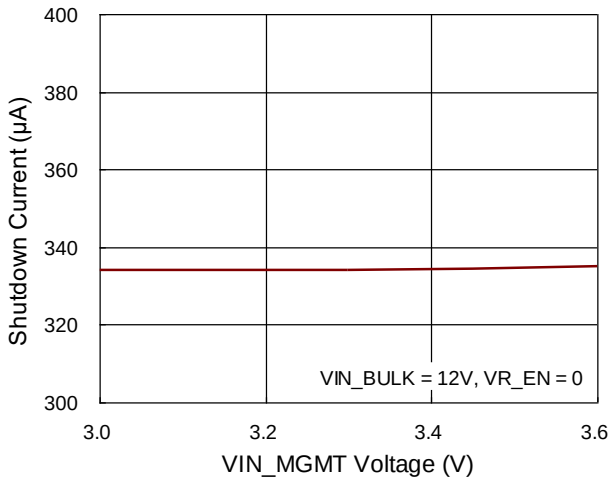
Shutdown Current vs. VIN_BULK



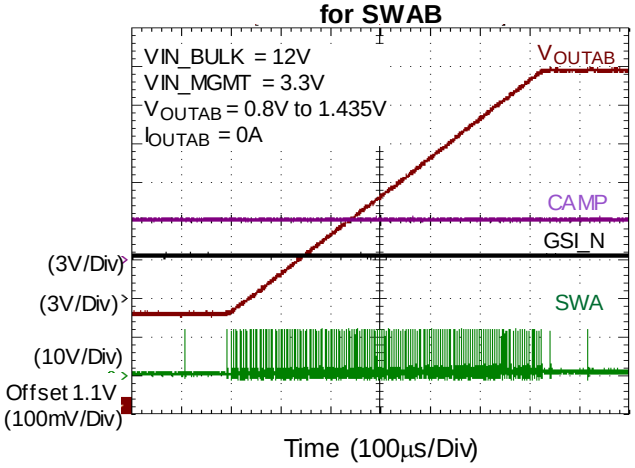
Quiescent Current vs. VIN_MGMT



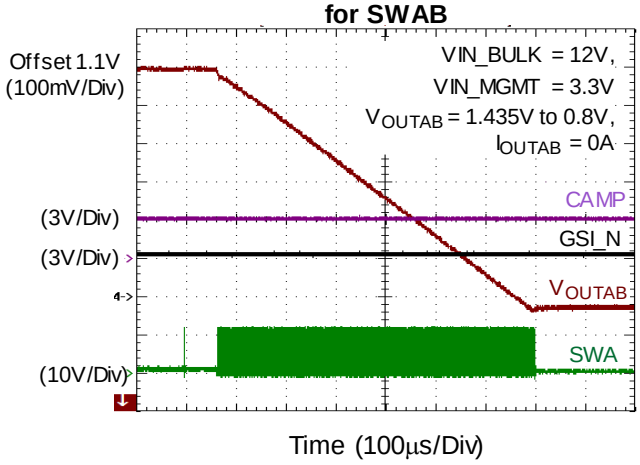
Shutdown Current vs. VIN_MGMT



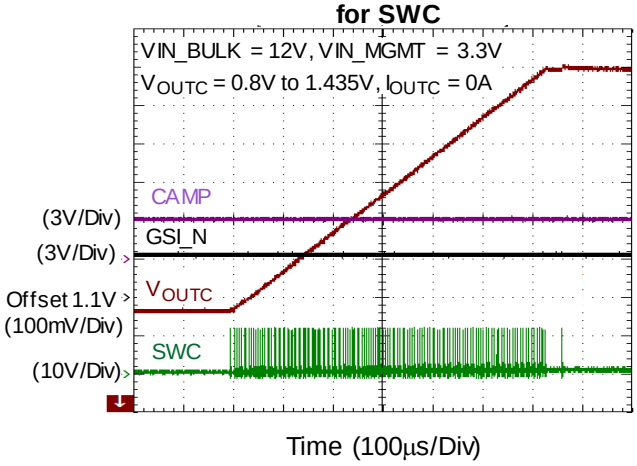
VID Output Voltage Margining Up for SWAB



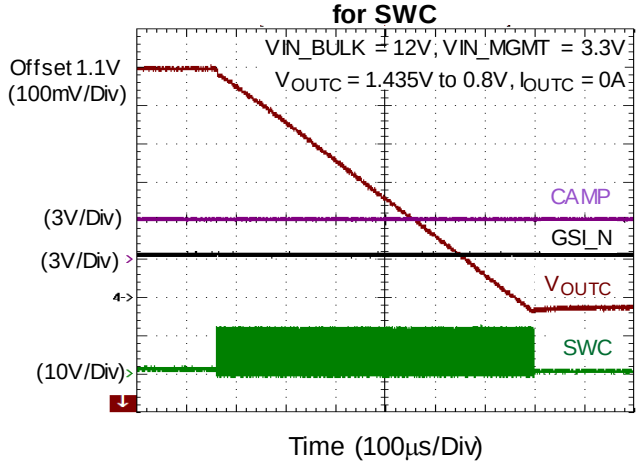
VID Output Voltage Margining Down for SWAB



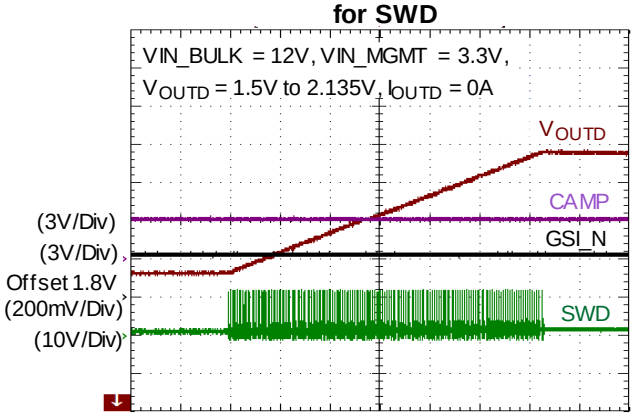
VID Output Voltage Margining Up for SWC



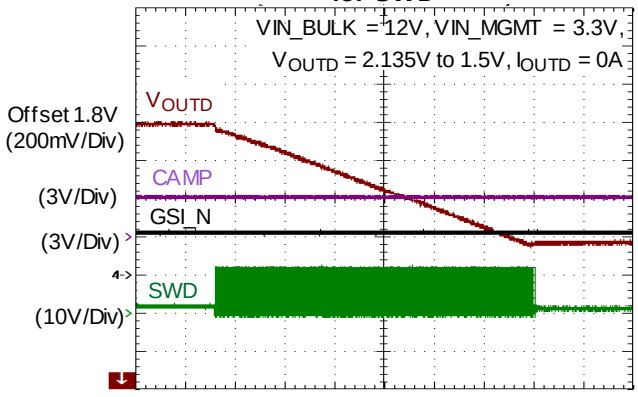
VID Output Voltage Margining Down for SWC



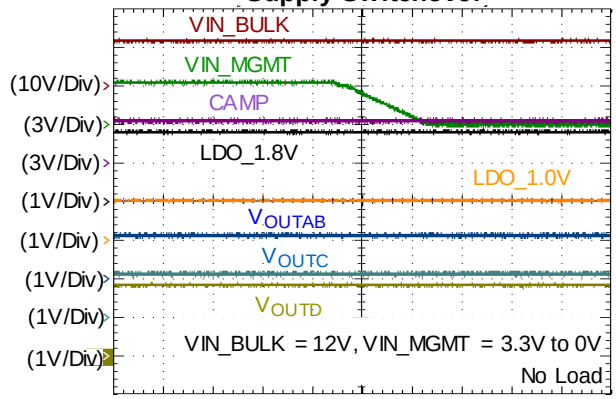
VID Output Voltage Margining Up for SWD



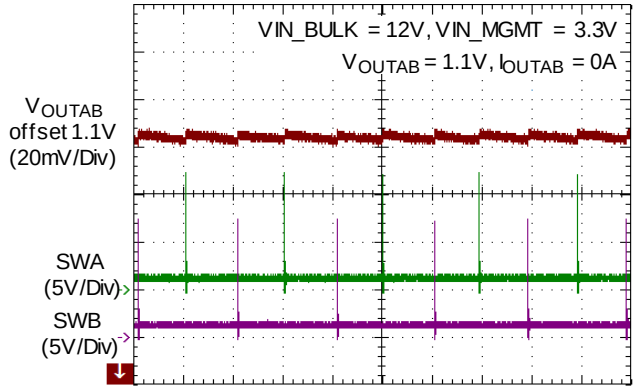
VID Output Voltage Margining Down for SWD



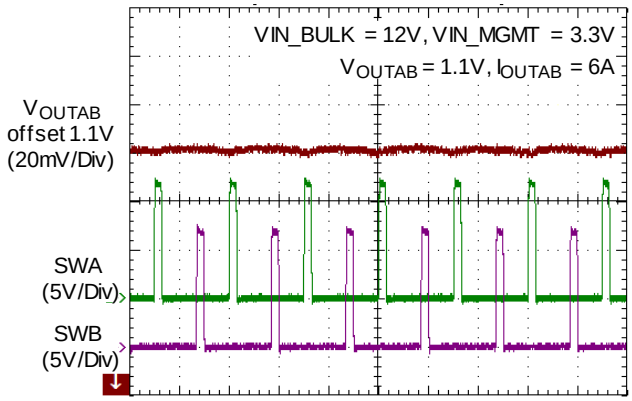
VIN_MGMT to VIN_BULK Input Supply Switchover



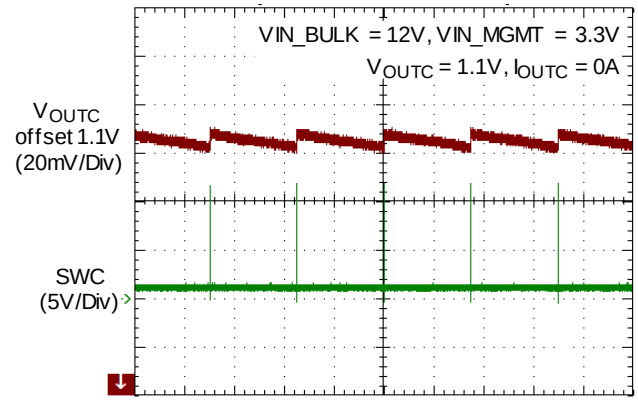
SWAB Stability in DEM



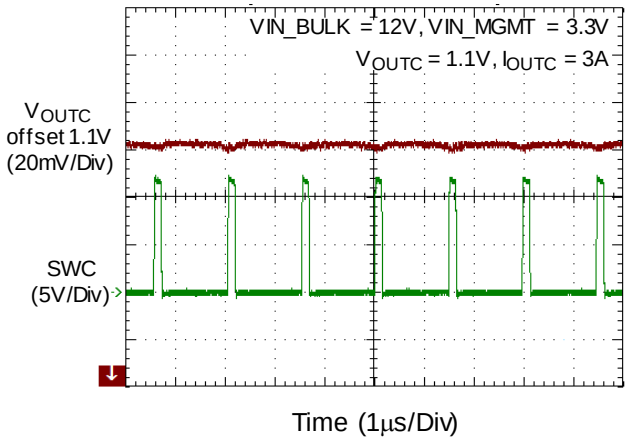
SWAB Stability in CCM



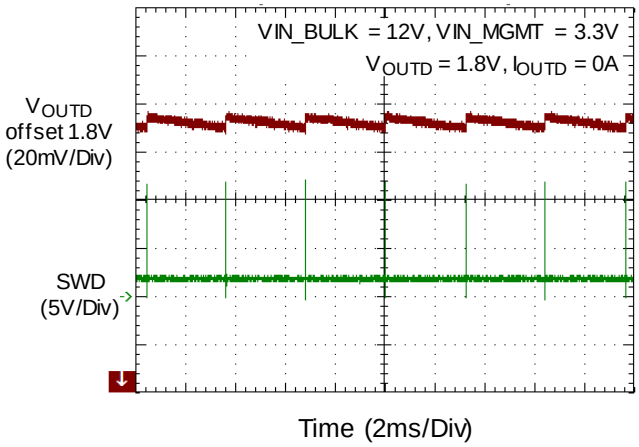
SWC Stability in DEM



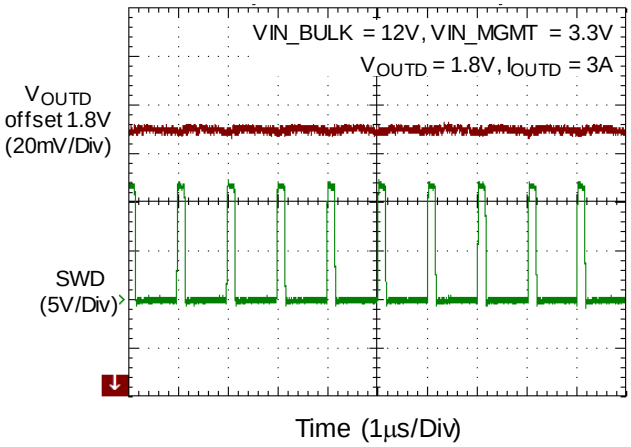
SWC Stability in CCM



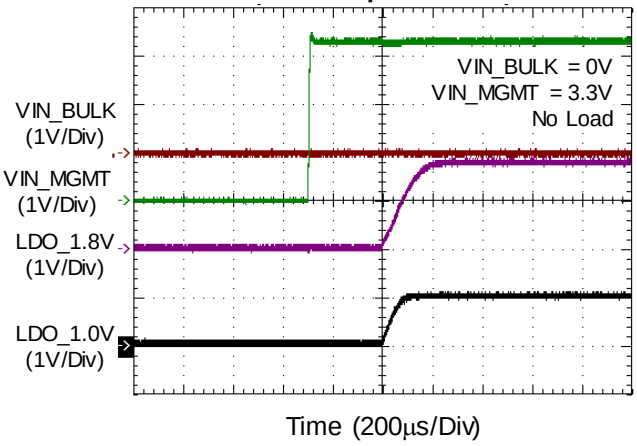
SWD Stability in DEM



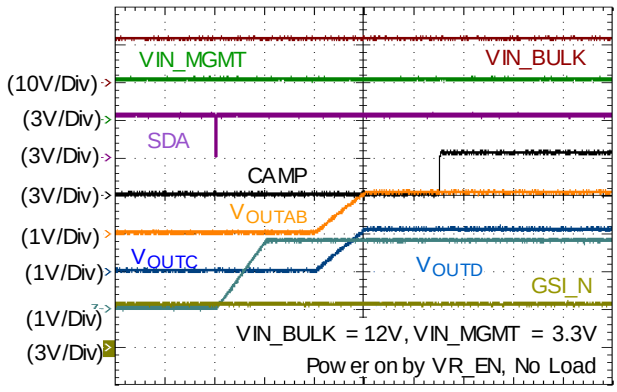
SWD Stability in CCM



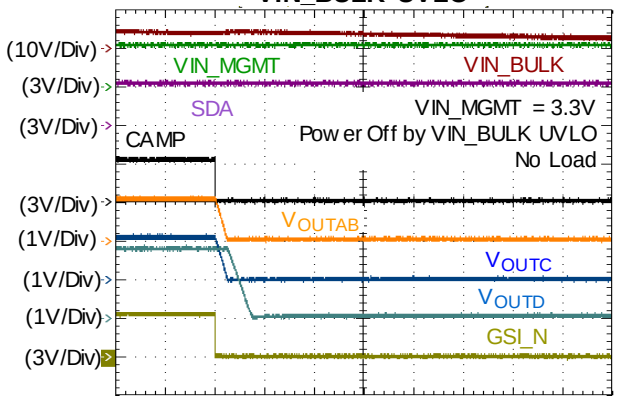
LDO_1.8V and LDO_1.0V Power On Sequence



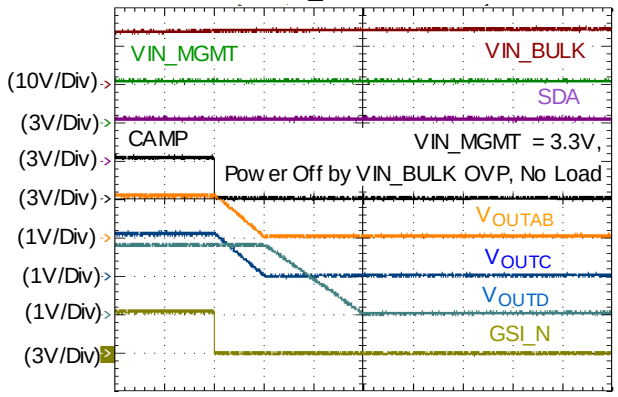
PMIC Power On Sequence



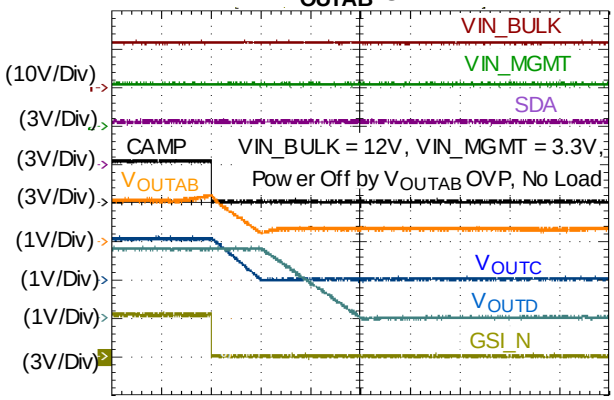
PMIC Power Off Sequence by VIN_BULK UVLO



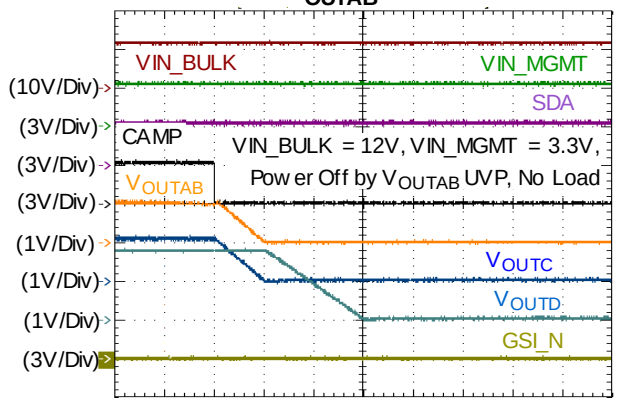
PMIC Power Off Sequence by VIN_BULK OVP



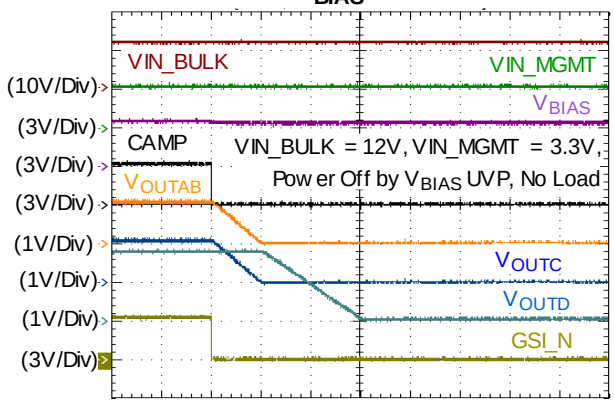
PMIC Power Off Sequence by V_{OUTAB} OVP



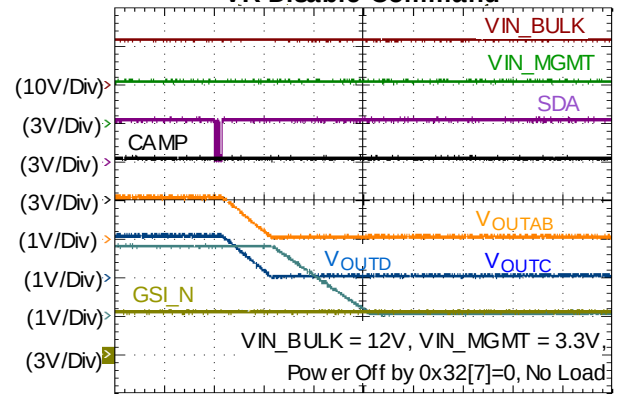
PMIC Power Off Sequence by V_{OUTAB} UVP



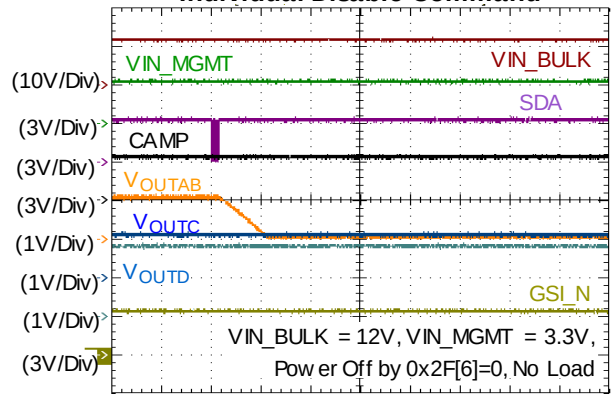
PMIC Power Off Sequence by V_{BIAS} UVP



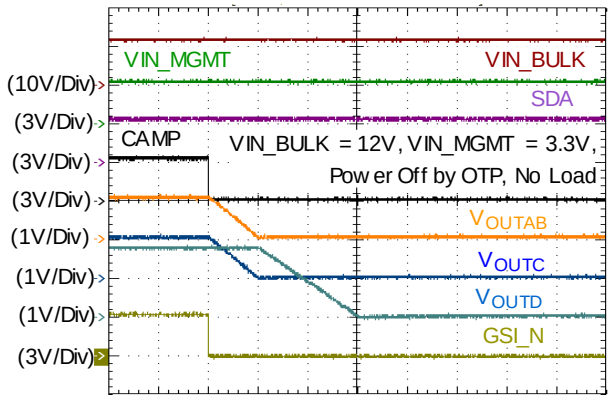
PMIC Power Off Sequence by VR Disable Command



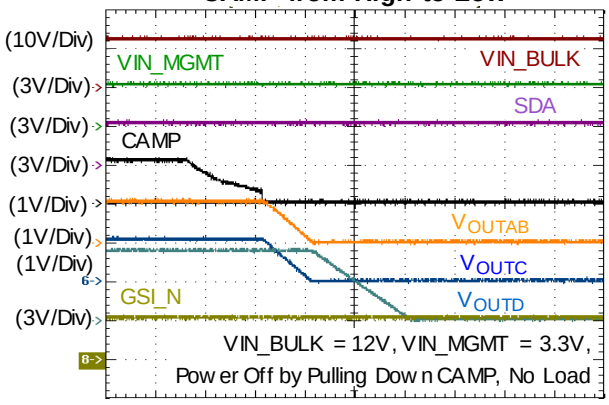
PMIC Power Off Sequence by Individual Disable Command



PMIC Power Off Sequence by OTP



PMIC Power Off Sequence by CAMP from High to Low



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response; however, they increase the inductor ripple current and output voltage ripple, and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required. Also, transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) about 20-50% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \quad \text{and}$$

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short-circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output under-voltage shutdown feature makes this unnecessary for most applications.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For low inductor core losses, some types of shielded ferrite core are usually better. Although they are possibly larger or more expensive, they will probably give fewer EMI and other noise problems.

Since DDR5 on DIMM has layout space limitation to power management IC on DIMM as well as the surrounding components like inductors and input/output capacitors, a standard inductor mechanical specification is defined in Table 10. Moreover, the electrical specification of inductor is also defined in Table 11. The electrical specifications include inductance, maximum DCR, maximum ACR and the minimum inductance requirement after de-rating at a specified operating current. The DIMM vendors can select an inductor based on the Table 11. Because the inductor size is fixed, the tradeoff between efficiency and transient response is the main concern on selection. Generally, the inductance for SWA, SWB and SWC, which are 1.1V output rails, is recommended to choose between 0.47μH and 0.68uH. The transient performance with L = 0.47μH is better than that with L = 0.68μH. However, the efficiency performance with L = 0.68μH is better than that with L = 0.47μH. On the other hand, the output rail with V_{OUT} = 1.8V, which is SWD or VPP rail, is suggested to apply inductance between 0.68uH to 1μH.

Table 10. Inductor Mechanical Specifications

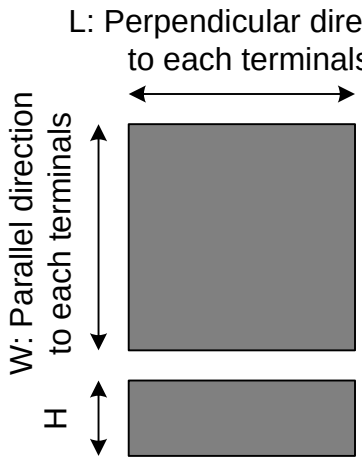
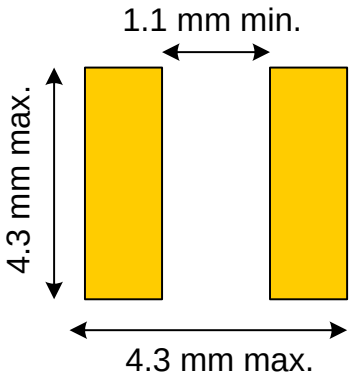
Package Size		Reference Drawings	Recommended Land Pattern
L [mm]	4.3max		
W [mm]	4.3max		
H [mm]	2.0max		

Table 11. Inductor Electrical Specifications

Package Height	L @ 0.5-1MHz / 0bias ± 20% [µH]	Max DCR [mΩ]	Max ACR @ 1MHz [mΩ]	Min. L @ 3.5A [µH]
2.0 Max [mm]	0.47	6.9	90	0.30
	0.68	8.4	145	0.38
	1.0	15.5	250	0.56
	1.2	16.5	300	0.67

Output Cap. Selection

The Buck output regulators of RTQ5119A are optimized for ceramic output capacitors, and the best performance will be obtained by using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR, ESL and stored charge. These three ripple components are called ESR ripple, ESL ripple, and capacitive ripple. Since ceramic capacitors have extremely low ESR, ESL and relatively little capacitance, all these components should be considered if ripple is critical. The decomposition of output ripple is shown in Figure 16. The formulas to describe each component are listed below.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(ESL)} = \frac{d}{dt} I_L \times ESL$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

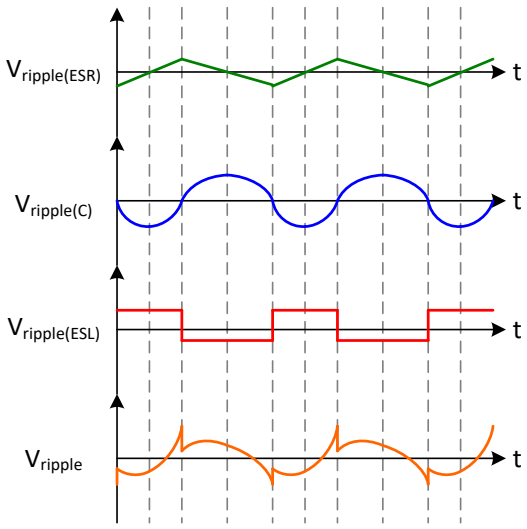


Figure 16. Output Ripple Decomposition

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The A^{2}RCOT transient response is very quick and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's switching frequency. But some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the A^{2}RCOT control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. The behavior diagram of output voltage drop is depicted as Figure 17. Calculate the approximate on-time (neglecting parasitic) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ ,and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF(MIN)}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but it can be neglected both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

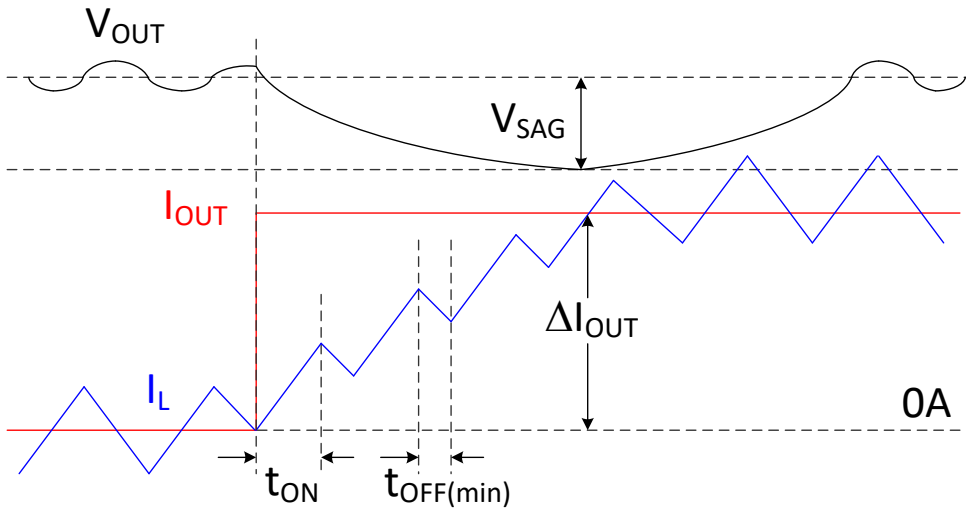


Figure 17. Output Voltage Drop (V_{SAG}) Estimation as Output Load Current Step Up

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

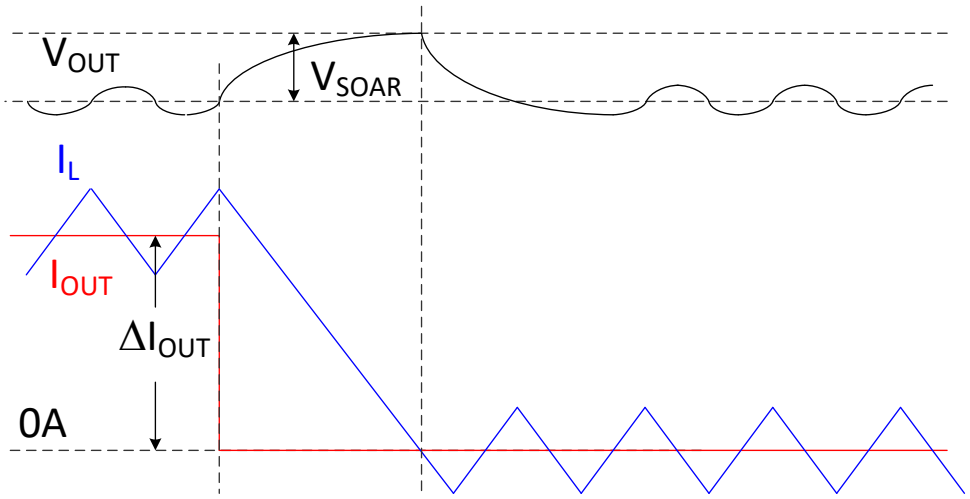


Figure 18. Output Voltage Soar (V_{SOAR}) Estimation as Output Load Current Step Down

Most applications never experience instantaneous full load steps and the RTQ5119A's high switching frequency and fast transient response can easily control voltage regulation at all times. Therefore, sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitor (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

In any application with large quick transients, it should calculate soar and sag to make sure that over-voltage protection and under-voltage protection will not be triggered.

In addition, the recommended dielectric type of the capacitor is X7R which has the best performance among temperature and DC and AC bias voltage variations. The variation of the capacitance value with temperature, DC bias voltage and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Input Cap. Selection

A buck converter generates a pulsating ripple current with high di/dt at the input. Without input capacitors, ripple current is supplied by the upper power source. Printed circuit board (PCB) resistance and inductance cause high-voltage ripple that disrupts electronic devices. The circulating ripple current results in increased conducted and radiated EMI. Input capacitors provide a short bypass path for ripple current and stabilize bus voltage during a transient event.

The capacitor voltage rating should meet reliability and safety requirements. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design. Among the different types of capacitors, the multilayer ceramic capacitor (MLCC) is particularly good regarding allowable ripple current due to low ESR and ESL. Following equation is used to estimate the required effective capacitance that will meet the ripple requirement.

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1-D)}{\Delta V_{IN\_PP} \times f_{SW}}$$

where D is calculated as below :

$$D = \frac{V_O}{V_{IN} \times \eta}$$

Besides the ripple-voltage requirement, the ceramic capacitors should meet the thermal stress requirement as well. The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left[(1 - \frac{V_{OUT}}{V_{IN}}) \times {I_{OUT}}^2 + \frac{\Delta {I_L}^2}{12} \right]}$$

Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Besides, since the ESL of ceramic capacitors plays a significant role on voltage spike at input and phase node, it is desirable to add a small capacitor with low ESL near VIN pin.

While the MLCC is excellent regarding allowable ripple current, it is well-known regarding effective capacitance that is necessary to meet transient response requirements. There could be two VIN spikes during the transient: the first spike is related to the ESR; and the second spike is caused by the difference between the buck-converter input current (i_{IN_B}) and the bus-converter output current (i_{PS}) as depicted in Figure 19.

Both spikes should be lower than the VIN undershoot or overshoot requirement (VIN_tran). First, since the MLCCs have very small ESR, the component of ESR drop can almost be ignored. The second spike is related to the response of the bus converter. The converter output-current rise time during a transient event, T_{R_PS}, can be approximated by the following equation:

$$T_{R\_PS} \cong \frac{0.35}{f_{BW\_PS}}$$

, where f_{BW_PS} is the control loop bandwidth of Buck converter.

The equivalent capacitance of the input capacitors should be greater than that calculated with following equation :

$$C_{IN} \geq \frac{\frac{1}{2} \times I_{Step} \times D_{max} \times T_{R\_PS}}{V_{IN\_Tran}}$$

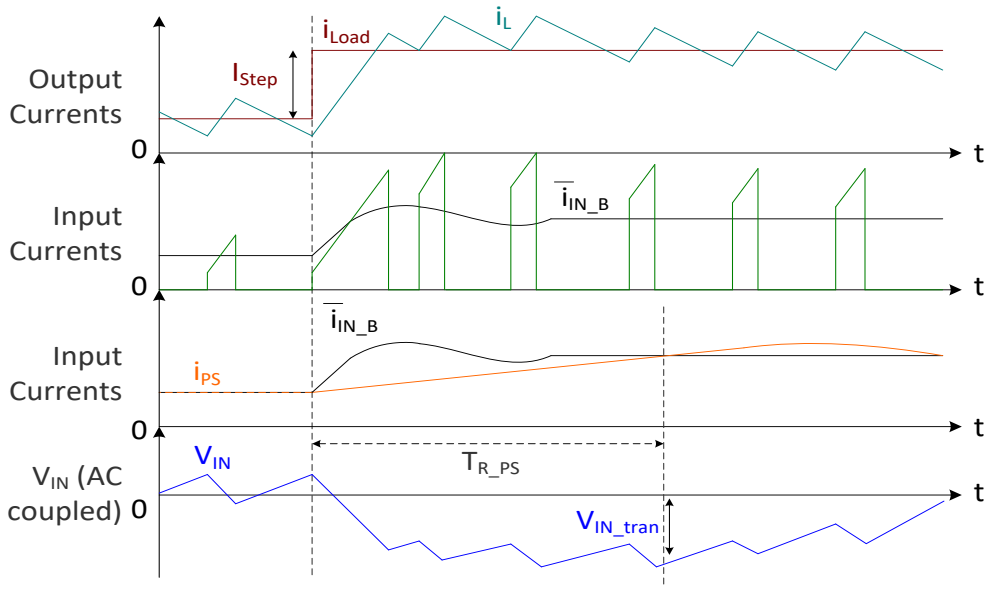


Figure 19. VIN Transient Current Diagram

Either VIN ripple (ΔV_{IN_PP}) or Vin transient ripple (V_{IN_Tran}) should meet the design requirements. For RTQ5119A, the input voltage should be always higher than VIN_UVLO threshold to confirm the PMIC's functionality. Moreover, it should be noticed that many de-rating factors, including V_{BIAS} dc voltage, ac voltage and operating temperature, make equivalent capacitance smaller than the capacitance without bias.

Bootstrap Circuit

The bootstrap circuit is useful in a high-voltage gate driver and operates as follows. When the SW node goes below the IC supply voltage V_{CC} (V_{DD}) or is pulled down to ground (the low-side MOSFET is turned on and the high-side MOSFET is turned off), the bootstrap

capacitor, C_{BOOT}, charges through the bootstrap resistor, R_{BOOT}, and bootstrap diode, D_{BOOT}, from the VCC power supply, as shown in Figure 20. On the other hand, the voltage across V_{BOOT} and SW can supply gate charge to high-side MOSFET when low-side MOSFET is turned off and SW node goes to a higher voltage, VOUT. In the meantime, the bootstrap diode reverses bias and blocks the rail voltage from the IC supply voltage, V_{CC}.

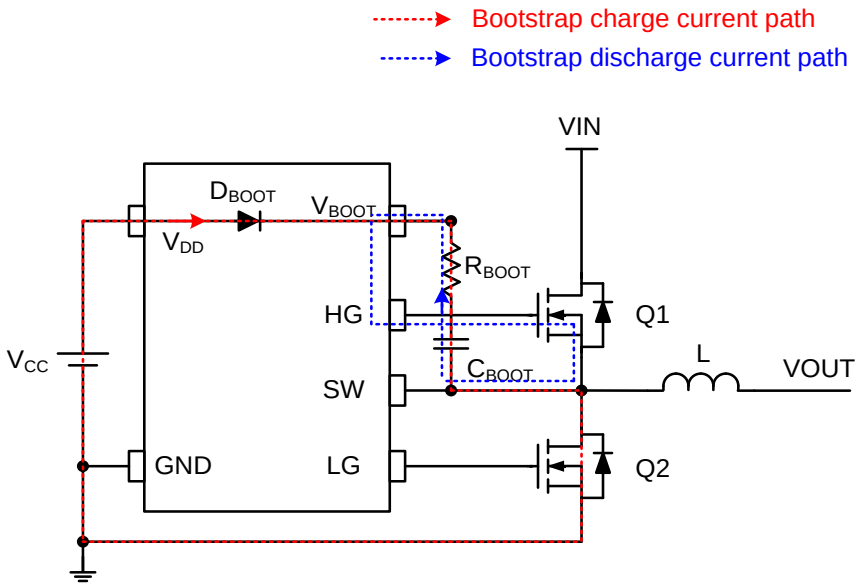


Figure 20. Bootstrap Power Supply Circuit

There are some design considerations for a bootstrap circuit. First, the selection of bootstrap capacitor (C_{BOOT}) is based on the maximum voltage drop across C_{BOOT} to guarantee the high-side MOSFET has enough charge to turn on periodically. The maximum allowable voltage drop (ΔV_{BOOT}) depends on the minimum gate drive voltage (for the high-side MOSFET) to maintain. If V_{GSMIN} is the minimum gate-source voltage, the capacitor drop must be:

$$\Delta V_{BOOT} = V_{CC} - V_F - V_{GSMIN}$$

where V_{CC} is the supply voltage of gate driver, and VF is the forward voltage drop of bootstrap diode.

Therefore, the value of bootstrap capacitor is calculated as :

$$C_{BOOT} = \frac{Q_{Total}}{\Delta V_{BOOT}}$$

where Q_{Total} is the total amount of the charge required for driving the high-side MOSFET and some leakage charge in the chip.

Second, when the external bootstrap resistor is used, the resistance, R_{BOOT}, introduces an additional voltage drop :

$$V_{RBOOT} = \frac{Q_{Total}}{t_{Charge}} \times R_{BOOT}$$

where t_{Charge} is the bootstrap charging time (the low-side MOSFET turn-on time).

The power dissipation on R_{BOOT} should be considered when choosing the package size of resistor. When estimating the maximum allowable voltage drop, the value of voltage drop of bootstrap resistor should be taken into account.

For example, assume V_{CC} = 5V, VF = 0.7V, R_{BOOT} = 1Ω, V_{GSMIN} = 2.5V and Q_{Total} = 5nC. The ΔV_{BOOT} can be calculated as 1.8V. The estimated C_{BOOT} is 2.8nF. Generally, the ΔVBOOT is not suggested to be too large and also need to consider the additional voltage drop on R_{BOOT}. Moreover, the de-rating factors, including V_{BIAS} dc voltage, ac voltage and operating temperature, make equivalent capacitance be smaller. The common selection value of C_{BOOT} is 100nF~220nF, that makes the ΔV_{BOOT} to be 50mV and 25mV separately. If choosing the bias capacitor with 0201 package and

6.3V voltage rating, the de-rating factor is about 0.5. Therefore, the ΔV_{BOOT} increases to 100mV and 50mV. In addition, the voltage drop on R_{BOOT} = 1Ω is 25mV as t_{Charge} is 200nsec. Adding the R_{BOOT} can reduce the EMI noise as well as voltage spike on phase node. However, the additional power loss will reduce the system efficiency.

VLDO_1.8V, VLDO_1.0V and V_{BIAS} LDO Decoupling Capacitor

The RTQ5119A integrates three LDO regulators (VLDO_1.8V, VLDO_1.0V and V_{BIAS}). V_{BIAS} is supplied by VIN_BULK and provides power to the internal circuitry. The V_{BIAS} can be used as the PGOOD pull-up supply, but it can't be a power source to external loads. A decoupling capacitor is necessary to place near VBIAS pin and the equivalent minimum capacitance should be at least 2.2μF. In many applications, a 4.7μF/6.3V/X5R/0402 capacitor is recommended and the layout placement should be as close as possible to VBIAS pin and AGND pin, in order to reduce the parasitic inductance and impedance. When choosing the package size and voltage rating of a capacitor, the de-rating coefficient versus voltage and temperature is important for taking account of equivalent capacitance under actual operating condition.

The VLDO_1.8V and VLDO_1.0V LDOs are supplied by VIN_MGMT. They provide power to system devices such as SPD, TS and RCD on the DIMM. After VR_EN is pulled high, the VIN_MGMT will switch-over to VIN_BULK supply when VIN_MGMT is lower than switch-over threshold. Both VLDO_1.8V and VLDO_1.0V need a decoupling capacitor placed near output pin and the equivalent minimum capacitance should be at least 2.2μF. In many applications, a 4.7μF/6.3V/X5R/0402 capacitor is recommended. When choosing the package size and voltage rating of a capacitor, the de-rating coefficient versus voltage and temperature is important for taking account of equivalent capacitance under actual operating condition.

Thermal Consideration

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a VQFN-35L 5x5 (FC) package, the thermal resistance, θ_{JA}, is 24.7°C/W on a twelve layers DIMM card size PCB. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)} = (125°C - 25°C) / (24.7°C/W) = 4.05W$ for a VQFN-35L 5x5 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 21 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

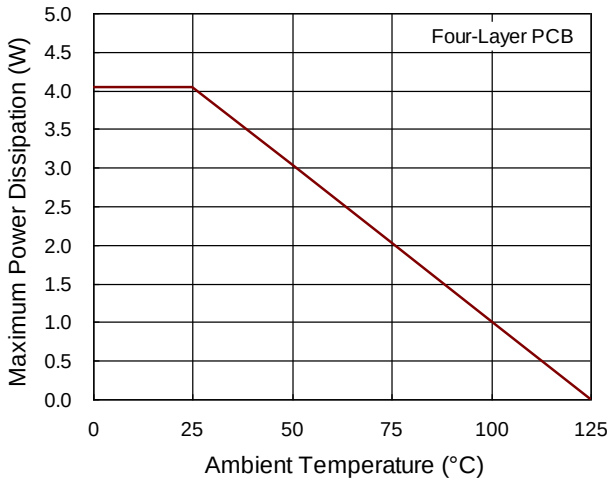


Figure 21. Derating Curve of Maximum Power Dissipation

Layout Consideration

Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. Certain points must be considered before starting a layout for RTQ5119A. Figure 22, Figure 23 and Figure 24 show the recommended layout guide for reference. In Figure 22, the top layer layout of RTQ5119A's EVB is demonstrated. It should be noticed that the components' size is considered and drawn in real relating size. Four inductors and one PMIC are on the same layer to avoid the necessary of phase node vias which can induce large phase ringing and EMI noise. In Figure 24, the bottom layer layout of RTQ5119A's EVB is demonstrated. The input caps and output caps are placed at this plane because there is a layout area limitation of PMIC on DIMM, that is 15.75mmX12.4mm. Moreover, the input caps have been divided into two parts. A small decoupling capacitor with smaller package size and capacitance is mounted under the one side of VIN pin for each rail. Two bulk capacitors are placed at the other side right beneath the VIN pin for each rail. Place the small decoupling capacitor can help to filter out the high frequency voltage spike, reduce the phase ringing on phase pin. Bulk capacitors can provide prompt energy during output load transient. At last, in Figure 23, an inner layer of RTQ5119A's EVB is demonstrated. The differential feedback sensing for each rail are undertaken. Most important thing is to keep away the noisy signal, like switching node, output caps' vias. Below are the key items of RTQ5119A's EVB layout.

- Make traces of the high current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VINA, VINB, VINC and VIND).
- The SW node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the SW node to prevent noise couple.
- The PGND pin should be connected to a strong ground plane for heat sinking and noise protection. For better power dissipation, adding thermal vias near PGND pin to connect between different layers is recommended.
- The ground of VBIAS is recommended to connect to AGND then connect to PGND layer through via.
- Place the decoupling capacitors as close as possible to the device pins (VBIAS and AGND).
- Differential routing the feedback traces for each rail and keep away from noisy signal on the EVB.
- The NC pins at the four corners are recommended to connect to PGND for better heat dissipation.

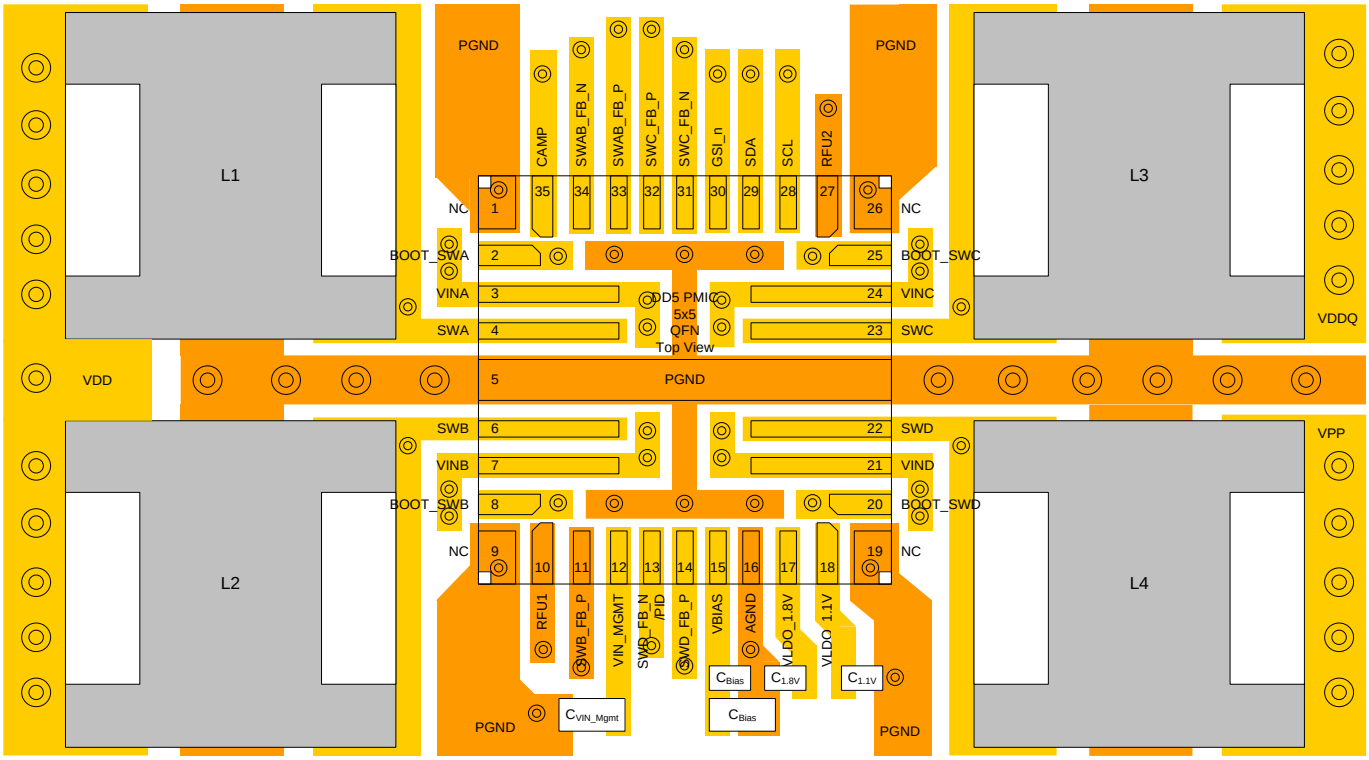


Figure 22. RTQ5119A Layout Guide (Top Layer)

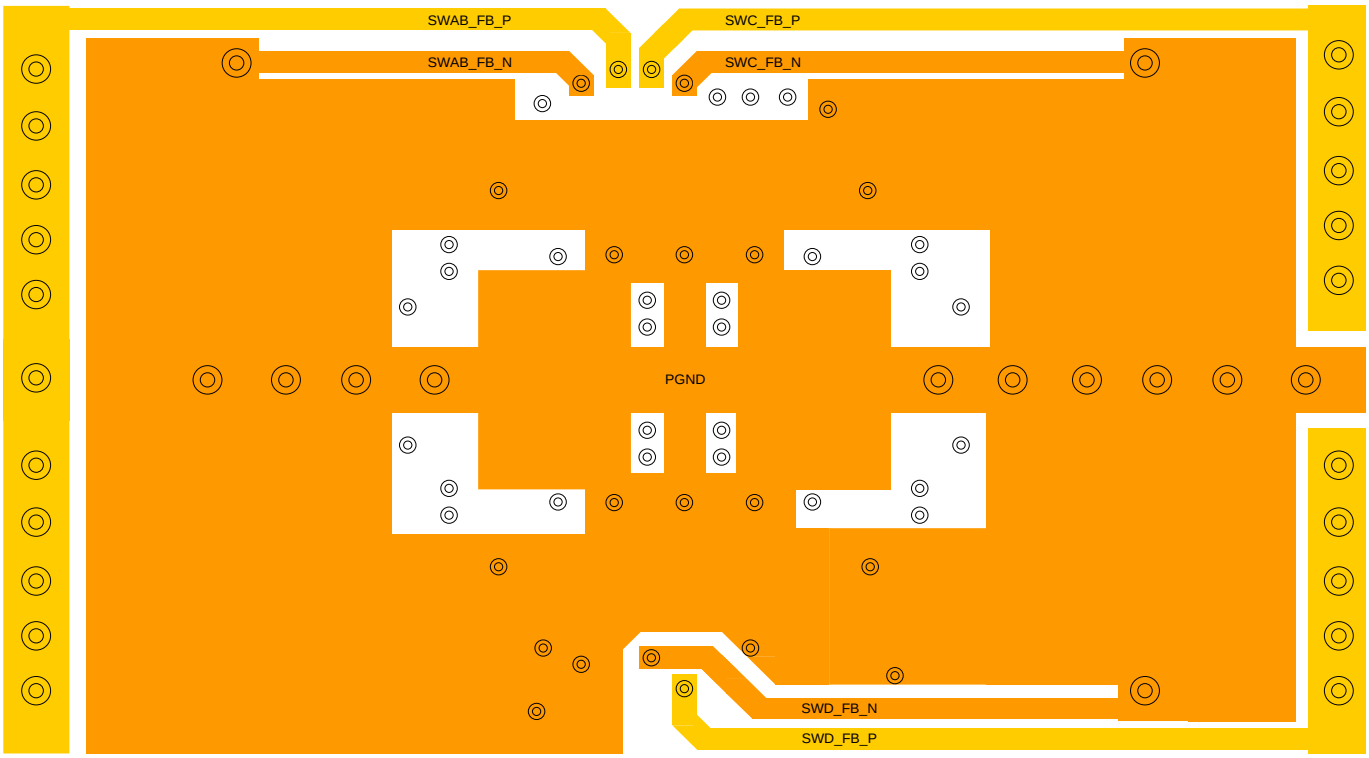


Figure 23. RTQ5119A Layout Guide (Inner Layer)

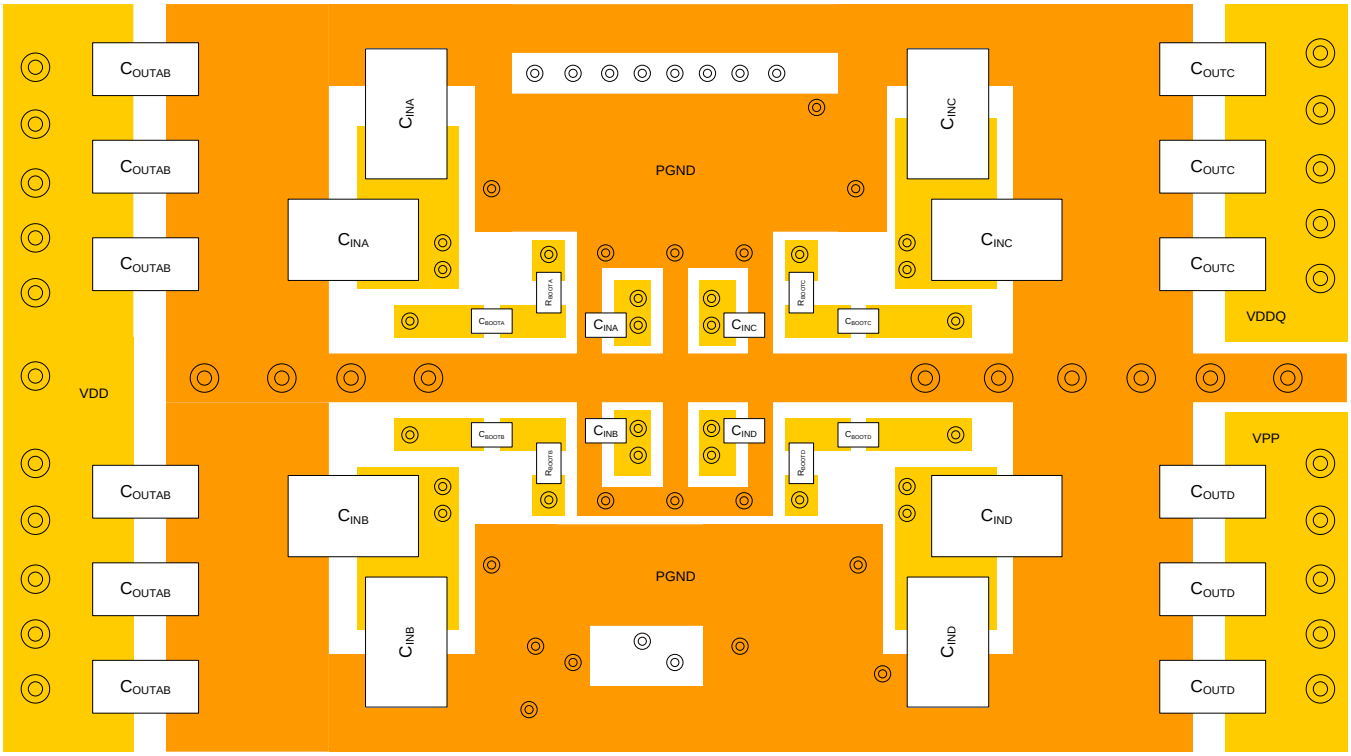


Figure 24. RTQ5119A Layout Guide (Bottom Layer)

A. Register Description

A-1 Register Attribute Definition

Attribute	Abbreviation	Description
Read Only	RO	This bit can be read by host. Write has no effect.
Read/Write	RW	This bit can be read or written by host.
Write Only	WO	This bit can only be written by host. Read from this bit return ‘0’.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by host. The bit will return ‘0’ when read. Write has no effect.
Write ‘1’ Only	1O	This bit can only be set (i.e. write ‘1’) but not reset (i.e. write ‘0’). Write ‘0’ has no effect.
Persistent	E	This bit is persistent during power cycle
Protected	P	This bit is protected by the password registers. This bit cannot be read to or written unless the password code has been written into the password registers.

A-2 Register Map Breakdown

Region	Register Range	Restriction
Host User (NVM and VM)	R00 – R14, [R30 - R31, R32[6], R33 - R3F]	Read/Write accessible in both WP or WE mode
	[R15 - R2F, R32[7,5:0], R35	Restricted access in WP mode
DIMM Vendor (NVM)	[R40 - R6F]	Restricted access in WP mode
PMIC Vendor (NVM)	[R70 - RFF]	Restricted access in WP mode

A-3 Register Memory Protection

The PMIC DIMM vendors registers (0x40 - 0x6F) are password protected registers. Both Read and Write access to DIMM vendor registers are blocked unless it is unlocked by providing the correct password. The default password for DIMM vendor registers is (Register_0x37 = 0x73) and (Register_0x38 = 0x94). The PMIC offers DIMM vendors to select their own password for DIMM vendor registers.

A-3.1 Steps to Access DIMM Vendor Region Registers

The steps to access the DIMM vendor registers are as following:

1. Write to “Register 0x37” = 8 bit password LSB code.
2. Write to “Register 0x38” = 8 bit password MSB code.
3. Write to “Register 0x39” = 0x40.
4. Perform Read operations to DIMM vendor registers as desired.
5. Write to “Register 0x39” = 0x00 (Lock).

A-3.2 Steps to Change DIMM Vendor Region Password

By default, the DIMM vendor region register password is 0x9473. The steps to change the password from default password are as following:

1. Write to “Register 0x37” = 0x73. (default)
2. Write to “Register 0x38” = 0x94. (default)
3. Write to “Register 0x39” = 0x40.
4. Write to “Register 0x37” = New 8 bit password LSB code as desired by DIMM vendor.
5. Write to “Register 0x38” = New 8 bit password MSB code as desired by DIMM vendor.
6. Write to “Register 0x39” = 0x80.
7. Wait 100ms.
8. Write to “Register 0x39” = 0x00 (Lock).
9. Power cycle the PMIC. Remove VIN_BULK and VIN_MGMT supply from the PMIC. The new password is in effect after the power cycle.

To change the password again from this point on, repeat steps 1 to 8 but note that in steps 1 and 2 current password is required.

A-3.3 Steps to Burn or Program DIMM Vendor Region Registers

The steps to burn or to program the DIMM vendor registers are as following:

1. Write to “Register 0x37” = 8 bit password LSB code.
2. Write to “Register 0x38” = 8 bit password MSB code.
3. Write to “Register 0x39” = 0x40.
4. Programming DIMM vendor registers are done at block level.

Block 40 addresses: 0x40 - 0x4F;

Block 50 addresses: 0x50 - 0x5F;

Block 60 addresses: 0x60 - 0x6F.

Perform write operation to each block as desired.

5. Burn each block one at a time:

Block 40 addresses: Write “Register 0x39” = 0x81.

Block 50 addresses: Write “Register 0x39” = 0x82.

Block 60 addresses: Write Register 0x39” = 0x85.

6. Wait time 100ms.
7. To check if programming is complete:

Perform read from “Register 0x39”. The code 0x5A indicates it is complete. It takes 60ms per page to program.

8. To verify if programming is done correctly:

Perform read operation from appropriate block addresses.

9. Write to “Register 0x39” = 0x00. (Lock)

A-4.1 Register Map (Host Region Map)

Register	Attribute	Description
R00	RV	R00 [7:0] - Reserved
R01	RV	R01 [7:0] - Reserved
R02	RV	R02 [7:0] - Reserved
R03	RV	R03 [7:0] - Reserved
R04	ROE	R04 [7] - Global Error Count R04 [6:4] Global Error History Log of High Level Status Code R04 [3:0] Reserved
R05	ROE	R05 [7] Reserved R05 [6:3] SWA, SWB, SWC & SWD Power Not Good Status (Power on reset) R05 [2:0] High Level Status Code (Power on reset)
R06	ROE	R06 [7:4] SWA, SWB, SWC & SWD Under Voltage Lockout (Power on reset) R06 [3:0] SWA, SWB, SWC & SWD Over Voltage Status (Power on reset)
R07	ROE	R07 [7:0] Reserved
R08	RO	R08 [7] VIN_BULK Input Power Good Status R08 [6] Critical Temperature Shutdown Status R08 [5:2] SWA, SWB, SWC, SWD Output Power Good Status R08 [1] VIN_MGMT Input Over Voltage Status R08 [0] VIN_BULK Input Over Voltage Status
R09	RO	R09 [7] PMIC High Temperature Warning Status R09 [6] V_{BIAS} Power Good Status R09 [5] VLDO_1.8V Output Power Good Status R09 [4] VIN_MGMT to VIN_BULK Input Supply Switchover Status R09 [3:0] SWA, SWB, SWC & SWD High Output Current Consumption Warning Status
R0A	RO	R0A [7:4] SWA, SWB, SWC, SWD Output Over Voltage Status R0A [3] PEC Error Status R0A [2] Parity Error Status R0A [1] IBI Status R0A [0] Reserved
R0B	RO	R0B [7:4] SWA, SWB, SWC and SWD Output Current Limiter Warning Status R0B [3:0] SWA, SWB, SWC and SWD Output Under-Voltage Lockout Status
R0C	RO	R0C [7:0] SWA Output Current or Power Measurement (Single rail only or All rails SWA, SWB, SWC, SWD)
R0D	RO	R0D [7:6] Reserved R0D [5:0] SWB Output Current or Power Measurement
R0E	RO	R0E [7:6] Reserved R0E [5:0] SWC Output Current or Power Measurement
R0F	RO	R0F [7:6] Reserved R0F [5:0] SWD Output Current or Power Measurement
R10	1O	R10 [7] Clear VIN_BULK Input Power Good Status R10 [6] Reserved R10 [5:2] Clear SWA, SWB, SWC & SWD Output Power Good Status R10 [1] Clear VIN_MGMT Input Over Voltage Status R10 [0] Clear VIN_BULK Input Over Voltage Status

Register	Attribute	Description
R11	1O	R11 [7] Clear PMIC High Temperature Warning Status R11 [6] Clear V_{BIAS} Power Good Status R11 [5] Clear VLDO_1.8V Output Power Good Status R11 [4] Clear VIN_MGMT to VIN_BULK Input Supply Switchover Status R11 [3:0] Clear SWA, SWB, SWC & SWD High Output Current Consumption Warning Status
R12	1O	R12 [7:4] Clear SWA, SWB, SWC, SWD Output Over Voltage Status R12 [3] Clear PEC Error R12 [2] Clear Parity Error R12 [1:0] Reserved
R13	1O	R13 [7:4] Clear SWA, SWB, SWC and SWD Output Current Limiter Warning Status R13 [3:0] Clear SWA, SWB, SWC and SWD Output Under-Voltage Lockout Status
R14	RW	R14 [7:5] Reserved R14 [4] Clear VIN_MGMT Power Good Status in Switchover Mode R14 [3] Clear V_{BIAS} Output or VIN_BULK Input Under Voltage Lockout Status R14 [2] Clear VLDO_1.0V Output Power Good Status R14 [1] Reserved R14 [0] Clear Global Status
R15 (WP)	RW	R15 [7] Mask VIN_BULK Input Power Good Status R15 [6] Reserved R15 [5:2] Mask SWA, SWB,SWC & SWD Output Power Good Status R15 [1] Mask VIN_MGMT Input Over Voltage Status R15 [0] Mask VIN_BULK Input Over Voltage Status
R16 (WP)	RW	R16 [7] Mask PMIC High Temperature Warning Status R16 [6] Mask V_{BIAS} Power Good Status R16 [5] Mask VLDO_1.8V Output Power Good Status R16 [4] Mask VIN_MGMT to VIN_BULK Input Supply Switchover Status R16 [3:0] Mask SWA, SWB, SWC & SWD High Output Current Consumption Warning Status
R17 (WP)	RW	R17 [7:4] Mask SWA, SWB, SWC, SWD Output Over Voltage R17 [3] Mask PEC Error Status R17 [2] Mask Parity Error Status R17 [1:0] Reserved
R18 (WP)	RW	R18 [7:4] Mask SWA, SWB, SWC & SWD Output Current Limiter Warning Status R18 [3:0] Mask SWA, SWB, SWC & SWD Output Under Voltage Lockout Status
R19 (WP)	RW	R19 [7:5] Reserved R19 [4] Mask VIN_MGMT Power Good Status Switchover Mode R19 [3] Mask V_{BIAS} Output Under Voltage Lockout Status R19 [2] Mask VLDO_1.0V Output Power Good Status R19 [1:0] Reserved
R1A (WP)	RW	R1A [7:5] VIN_BULK Falling Input Power Good Threshold Voltage R1A [4] Reserved R1A [3] V_{BIAS} Power Good Threshold Voltage R1A [2] VLDO_1.8 V Power Good Threshold Voltage R1A [1] Output Power Measurement Select R1A [0] VLDO_1.0V Power Good Threshold Voltage

Register	Attribute	Description
R1B (WP)	RW	R1B [7] VIN_BULK Input Over Voltage Threshold R1B [6] Current or Power Meter Select R1B [5] VIN_MGMT Input Over Voltage Threshold R1B [4] Global Mask Control for CAMP Output Pin R1B [3] GSI_n Output Pin Enable R1B [2:0] PMIC High Temperature Warning Threshold
R1C (WP)	RW	R1C [7:2] SWA Output High Current Threshold R1C [1:0] Reserved
R1D (WP)	RW	R1D [7:2] SWB Output High Current Threshold R1D [1:0] Reserved
R1E (WP)	RW	R1E [7:2] SWC Output High Current Threshold R1E [1:0] Reserved
R1F (WP)	RW	R1F [7:2] SWD Output High Current Threshold R1F [1:0] Reserved
R20 (WP)	RW	R20 [7:6] SWA Output Current Limiter Warning Threshold R20 [5:4] SWB Output Current Limiter Warning Threshold R20 [3:2] SWC Output Current Limiter Warning Threshold R20 [1:0] SWD Output Current Limiter Warning Threshold
R21 (WP)	RW	R21 [7:1] SWA Voltage Setting R21 [0] SWA Power Good Low-Side Threshold
R22 (WP)	RW	R22 [7:6] SWA Power Good High-Side Threshold R22 [5:4] SWA Over Voltage Threshold R22 [3:2] SWA Under Voltage Lockout Threshold R22 [1:0] SWA Soft-Stop Time
R23 (WP)	RW	R23 [7:1] SWB Voltage Setting R23 [0] SWB Power Good Low-Side Threshold
R24 (WP)	RW	R24 [7:6] SWB Power Good High-Side Threshold R24 [5:4] SWB Over Voltage Threshold R24 [3:2] SWB Under Voltage Lockout Threshold R24 [1:0] SWB Soft-Stop Time
R25 (WP)	RW	R25 [7:1] SWC Voltage Setting R25 [0] SWC Power Good Low-Side Threshold
R26 (WP)	RW	R26 [7:6] SWC Power Good High-Side Threshold R26 [5:4] SWC Over Voltage Threshold R26 [3:2] SWC Under Voltage Lockout Threshold R26 [1:0] SWC Soft-Stop Time
R27 (WP)	RW	R27 [7:1] SWD Voltage Setting R27 [0] SWD Power Good Low-Side Threshold
R28 (WP)	RW	R28 [7:6] SWD Power Good High-Side Threshold R28 [5:4] SWD Over Voltage Threshold R28 [3:2] SWD Under Voltage Lockout Threshold R28 [1:0] SWD Soft-Stop Time
R29 (WP)	RW	R29 [7:6] SWA Mode Select R29 [5:4] SWA Switching Frequency R29 [3:2] SWB Mode Select R29 [1:0] SWB Switching Frequency
R2A (WP)	RW	R2A [7:6] SWC Mode Select R2A [5:4] SWC Switching Frequency R2A [3:2] SWD Mode Select R2A [1:0] SWD Switching Frequency

Register	Attribute	Description
R2B (WP)	RW	R2B [7:6] VLDO_1.8V Voltage Setting R2B [5:3] Voltage Range Selection for SWA, SWB and SWC R2B [2:1] VLDO_1.0V Voltage Setting R2B [0] Voltage Range Selection for SWD
R2C (WP)	RW	R2C [7:5] SWA Soft-Start Time R2C [4] Reserved R2C [3:1] SWB Soft-Start Time R2C [0] Reserved
R2D (WP)	RW	R2D [7:5] SWC Soft-Start Time R2D [4] Reserved R2D [3:1] SWD Soft-Start Time R2D [0] Reserved
R2E (WP)	RW	R2E [7:3] Reserved R2E [2:0] PMIC Shutdown temperature threshold
R2F (WP)	RW	R2F [7] VIN_MGMT Input Supply Switchover Threshold Voltage R2F [6:3] SWA, SWB, SWC & SWD Enable R2F [2] Write Protect Function Control R2F [1:0] Mask Bits Register Control
R30	RW	R30 [7] ADC Enable R30 [6:3] ADC Select R30 [2] Reserved R30 [1:0] ADC Register Update Frequency
R31	RO	R31 [7:0] ADC Read Out
R32 (WP)	RW, RO	R32 [7] VR Enable R32 [6] Management Interface Selection R32[5] Execute VR Enable Control R32[4] Execute CAMP Fail_n Function Control R32[3] PMIC CAMP Power Good Output Signal Control R32 [2:0] Reserved
R33	RO	R33 [7:5] Temperature Measurement R33 [4] VIN_MGMT Power Good Status in Switchover Mode Only R33 [3] V_{BIAS} Output or VIN_BULK Input Under Voltage Lockout Status R33 [2] VLDO_1.0V Output Power Good Status R33 [1:0] Reserved
R34	RW, RO	R34 [7] PEC Enable R34 [6] IBI Enable R34 [5] Parity Disable R34 [4] Reserved R34 [3:1] HID_CODE R34 [0] Reserved
R35 (WP)	RW	R35 [7] Error Injection Enable R35 [6:4] Output Rail Selection R35 [3] Over and Under Voltage Select R35 [2:0] Misc. Error Injection Type
R36	RV	R36 [7:0] Reserved
R37	WO	R37 [7:0] Password Lower Byte 0
R38	WO	R38 [7:0] Password Upper Byte 1
R39	RW	R39 [7:0] Command Codes

Register	Attribute	Description
R3A	RW	R3A [7] Reserved R3A [6] Default Read Address Pointer Enable R3A [5:4] Default Read Address Pointer Selection R3A [3:2] Burst Length for Default Read Address Pointer Mode in PEC Enabled Mode R3A [1:0] Reserved
R3B	ROE	R3B [7:6] Reserved R3B [5:4] Major Revision ID R3B [3:1] Minor Revision ID R3B [0] PMIC Current Capability
R3C	ROE	R3C [7:0] VENDOR_ID_BYTE0
R3D	ROE	R3D [7:0] VENDOR_ID_BYTE1
R3E	RV	R3E [7:0] Reserved
R3F	RV	R3F [7:0] Reserved

Note: R15 to R2F, R32 registers are read-only in write protection mode as CAMP signal is at logic high level. Denoted "WP" in "Register" column for clarification.

A-4.2 Register Map (DIMM Region Map)

Register	Attribute	Description
R40	RWPE	R40 [7:0] Power-On Sequence - Configuration 0
R41	RWPE	R41 [7:0] Power-On Sequence - Configuration 1
R42	RWPE	R42 [7:0] Power-On Sequence - Configuration 2
R43	RWPE	R43 [7:0] Power-On Sequence - Configuration 3
R44	RV	R44 [7:0] Reserved
R45	RWPE	R45 [7:1] SWA Voltage Setting R45 [0] SWA Power Good Low-Side Threshold
R46	RWPE	R46 [7:6] SWA Power Good High-Side Threshold R46 [5:4] SWA Over-Voltage Threshold R46 [3:2] SWA Under-Voltage Lockout Threshold R46 [1:0] SWA Soft-Stop Time
R47	RWPE	R47 [7:1] SWB Voltage Setting R47 [0] SWB Power Good Low-Side Threshold
R48	RWPE	R48 [7:6] SWB Power Good High-Side Threshold R48 [5:4] SWB Over-Voltage Threshold R48 [3:2] SWB Under-Voltage Lockout Threshold R48 [1:0] SWB Soft-Stop Time
R49	RWPE	R49 [7:1] SWC Voltage Setting R49 [0] SWC Power Good Low-Side Threshold
R4A	RWPE	R4A [7:6] SWC Power Good High-Side Threshold R4A [5:4] SWC Over-Voltage Threshold R4A [3:2] SWC Under-Voltage Lockout Threshold R4A [1:0] SWC Soft-Stop Time
R4B	RWPE	R4B [7:1] SWD Voltage Setting R4B [0] SWD Power Good Low-Side Threshold
R4C	RWPE	R4C [7:6] SWD Power Good High-Side Threshold R4C [5:4] SWD Over-Voltage Threshold R4C [3:2] SWD Under-Voltage Lockout Threshold R4C [1:0] SWD Soft-Stop Time
R4D	RWPE	R4D [7:6] SWA Mode Select R4D [5:4] SWA Switching Frequency R4D [3:2] SWB Mode Select R4D [1:0] SWB Switching Frequency
R4E	RWPE	R4E [7:6] SWC Mode Select R4E [5:4] SWC Switching Frequency R4E [3:2] SWD Mode Select R4E [1:0] SWD Switching Frequency
R4F	RWPE	R4F [7] Output Regulators Disable Control R4F [6:5] Reserved R4F [4] SWA Regulator Remote Sensing Scheme R4F [3] Reserved R4F [2] SWC Regulator Remote Sensing Scheme R4F [1] SWD Regulator Remote Sensing Scheme R4F [0] SWA and SWB Single or Dual Phase Regulator Mode Select
R50	RWPE	R50 [7:6] SWA Output Current Limiter Warning Threshold R50 [5:4] SWB Output Current Limiter Warning Threshold R50 [3:2] SWC Output Current Limiter Warning Threshold R50 [1:0] SWD Output Current Limiter Warning Threshold

Register	Attribute	Description
R51	RWPE	R51 [7:6] VLDO_1.8V LDO Output Voltage Setting R51 [5:3] Voltage Range Selection for SWA, SWB and SWC R51 [2:1] VLDO_1.0V LDO Voltage Setting R51 [0] Voltage Range Selection for SWD
R52-R57	RV	R52 [7:0] - R57 [7:0] Reserved
R58	RWPE	R58 [7:0] Power-Off Sequence - Configuration 0
R59	RWPE	R59 [7:0] Power-Off Sequence - Configuration 1
R5A	RWPE	R5A [7:0] Power-Off Sequence - Configuration 2
R5B	RWPE	R5B [7:0] Power-Off Sequence - Configuration 3
R5C	RV	R5C [7:0] Reserved
R5D	RWPE	R5D [7:5] SWA Soft-Start Time R5D [4] Reserved R5D [3:1] SWB Soft-Start Time R5D [0] Reserved
R5E	RWPE	R5E [7:5] SWC Soft-Start Time R5E [4] Reserved R5E [3:1] SWD Soft-Start Time R5E [0] Reserved
R5F-R6F	RV	R5F [7:0] to R6F [7:0] Reserved

A-5 Host Region Registers

R00 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R00 [7:0] : Reserved

R01 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R01 [7:0] : Reserved

R02 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R02 [7:0] : Reserved

R03 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R03 [7:0] : Reserved

R04 - Global Error Log			
Bits	**Attribute**	**Default**	**Description**
7	ROE	0	R04 [7] : GLOBAL_ERROR_COUNT Global Error Count Since Last Erase Operation 0 = No Error or Only 1 Error Since Last Erase Operation 1 = > 1 Error Count since last Erase Operation
6	ROE	0	R04 [6] : GLOBAL_ERROR_LOG_BUCK_OV_OR_UV Global Error Buck Regulator Output Over-Voltage or Under-Voltage 0 = No Error 1 = Error
5	ROE	0	R04 [5] : GLOBAL_ERROR_LOG_VIN_BULK_OVER_VOTLAGE Global Error VIN_BULK Over-Voltage 0 = No Error 1 = Error
4	ROE	0	R04 [4] : GLOBAL_ERROR_LOG_CRITICAL_TEMPERATURE Global Error Critical Temperature 0 = No Error 1 = Error
3:0	RV	0	R04 [3:0] : Reserved

R05 - PG-on-Reset ERR Log			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R05 [7] : Reserved
6	ROE	0	R05 [6] : SWA_CONDITION_FROM_PREVIOUS_POWER_CYCLE 0 = Normal 1 = Failed
5	ROE	0	R05 [5] : SWB_CONDITION_FROM_PREVIOUS_POWER_CYCLE 0 = Normal 1 = Failed
4	ROE	0	R05 [4] : SWC_CONDITION_FROM_PREVIOUS_POWER_CYCLE 0 = Normal 1 = Failed
3	ROE	0	R05 [3] : SWD_CONDITION_FROM_PREVIOUS_POWER_CYCLE 0 = Normal 1 = Failed
2:0	ROE	0	R05 [2:0] : PMIC_ERROR_LOG PMIC Power On - High Level Status Bit to Indicate previous power down cycle 000 = Normal Power Down 001 = Reserved 010 = Buck Regulator Output Over or Under-Voltage Lockout 011 = Critical Temperature 100 = VIN_BULK Input Over Voltage 101 = Reserved 110 = Reserved 111 = Reserved

R06 - UVLO/OV ERR Log			
Bits	**Attribute**	**Default**	**Description**
7	ROE	0	R06 [7] : SWA_UNDER_VOLTAGE_LOCKOUT 0 = Normal Power On 1 = SWA Under-Voltage Lockout
6	ROE	0	R06 [6] : SWB_UNDER_VOLTAGE_LOCKOUT 0 = Normal Power On 1 = SWB Under-Voltage Lockout
5	ROE	0	R06 [5] : SWC_UNDER_VOLTAGE_LOCKOUT 0 = Normal Power On 1 = SWC Under-Voltage Lockout
4	ROE	0	R06 [4] : SWD_UNDER_VOLTAGE_LOCKOUT 0 = Normal Power On 1 = SWD Under-Voltage Lockout
3	ROE	0	R06 [3] : SWA_OVER_VOLTAGE 0 = Normal Power On 1 = SWA Over-Voltage
2	ROE	0	R06 [2]: SWB_OVER_VOLTAGE 0 = Normal Power On 1 = SWB Over-Voltage
1	ROE	0	R06 [1] : SWC_OVER_VOLTAGE 0 = Normal Power On 1 = SWC Over-Voltage
0	ROE	0	R06 [0] : SWD_OVER_VOLTAGE 0 = Normal Power On 1 = SWD Over-Voltage

R07 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R07 [7:0] : Reserved

R08 - Power Good Status			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R08 [7] : VIN_BULK_INPUT_POWER_GOOD_STATUS VIN_BULK Input Power Good Status 0 = Power Good 1 = Not Good
6	RO	0	R08 [6]: CRITICAL_TEMP_SHUTDOWN_STATUS Critical Temperature Shutdown Status 0 = No Critical Temperature Shutdown 1 = Critical Temperature Shutdown
5	RO	0	R08 [5] : SWA_OUTPUT_POWER_GOOD_STATUS Switch Node A Output Power Good Status 0 = Power Good 1 = Not Good
4	RO	0	R08 [4] : SWB_OUTPUT_POWER_GOOD_STATUS Switch Node B Output Power Good Status 0 = Power Good 1 = Not Good
3	RO	0	R08 [3] : SWC_OUTPUT_POWER_GOOD_STATUS Switch Node C Output Power Good Status 0 = Power Good 1 = Not Good
2	RO	0	R08 [2] : SWD_OUTPUT_POWER_GOOD_STATUS Switch Node D Output Power Good Status 0 = Power Good 1 = Not Good
1	RO	0	R08 [1] : VIN_MGMT_INPUT_OVER_VOLTAGE_STATUS VIN_MGMT Input Supply Over Voltage Status 0 = No Over-Voltage 1 = Over-Voltage
0	RO	0	R08 [0] : VIN_BULK_INPUT_OVER_VOLTAGE_STATUS VIN_BULK Input Supply Over Voltage Status 0 = No Over-Voltage 1 = Over-Voltage

R09 - HT, PG, Switch Over, High Current Warning			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R09 [7] : PMIC_HIGH_TEMP_WARNING_STATUS PMIC High Temperature Warning Status 0 = Temperature Below the Warning Threshold 1 = Temperature Exceeded the Warning Threshold
6	RO	0	R09 [6] : V_{BIAS}_POWER_GOOD_STATUS V_{BIAS} Power Good Status 0 = Power Good 1 = Power Not Good
5	RO	0	R09 [5] : VLDO_1.8V_OUTPUT_POWER_GOOD_STATUS VLDO_1.8V Output Power Good Status 0 = Power Good 1 = Power Not Good
4	RO	0	R09 [4]: VIN_MGMT_TO_VIN_BULK_INPUT_SUPPLY_SWITCHOVER_STATUS VIN_MGMT to VIN_BULK Input Supply Automatic Switchover Status 0 = VIN_MGMT Input Supply is Present 1 = VIN_MGMT Input Supply is Removed (i.e using VIN_BULK Input Supply)
3	RO	0	R09[3] : SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node A High Output Current Consumption Warning Status 0 = Normal 1 = High Current
2	RO	0	R09 [2] : SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node B High Output Current Consumption Warning Status 0 = Normal 1 = High Current
1	RO	0	R09 [1] : SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node C High Output Current Consumption Warning Status 0 = Normal 1 = High Current
0	RO	0	R09 [0] : SWD_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node D High Output Current Consumption Warning Status 0 = Normal 1 = High Current

R0A - SW[A:D] OV Status & PEC/Parity/IBI Status			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R0A [7] : SWA_OUTPUT_OVER_VOLTAGE_STATUS Switch Node A Output Over-Voltage Status 0 = No Over-Voltage 1 = Over-Voltage
6	RO	0	R0A [6] : SWB_OUTPUT_OVER_VOLTAGE_STATUS Switch Node B Output Over-Voltage Status 0 = No Over-Voltage 1 = Over-Voltage
5	RO	0	R0A [5] : SWC_OUTPUT_OVER_VOLTAGE_STATUS Switch Node C Output Over-Voltage Status 0 = No Over-Voltage 1 = Over-Voltage
4	RO	0	R0A [4] : SWD_OUTPUT_OVER_VOLTAGE_STATUS Switch Node D Output Over-Voltage Status 0 = No Over-Voltage 1 = Over-Voltage
3	RO	0	R0A [3]: PEC_ERROR_STATUS Packet Error Code Status 0 = No PEC Error 1 = PEC Error
2	RO	0	R0A [2]: PARITY_ERROR_STATUS T Bit Parity Error Status 0 = No Parity Error 1 = Parity Error
1	RO	0	R0A [1]: IBI_STATUS In Band Interrupt Status 0 = No Pending IBI 1 = Pending IBI
0	RV	0	R0A [0]: Reserved

R0B - SW[A:D] Current Limited and UVLO			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R0B [7] : SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node A Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
6	RO	0	R0B [6] : SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node B Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
5	RO	0	R0B [5] : SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node C Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
4	RO	0	R0B [4] : SWD_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node D Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
3	RO	0	R0B [3] : SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node A Output Under-Voltage Lockout Status 0 = No Under Voltage Lockout 1 = Under Voltage Lockout
2	RO	0	R0B [2] : SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node B Output Under-Voltage Lockout Status 0 = No Under-Voltage Lockout 1 = Under-Voltage Lockout
1	RO	0	R0B [1] : SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node C Output Under-Voltage Lockout Status 0 = No Under-Voltage Lockout 1 = Under-Voltage Lockout
0	RO	0	R0B [0] : SWD_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node D Output Under-Voltage Lockout Status 0 = No Under-Voltage Lockout 1 = Under-Voltage Lockout

R0C - SWA Current and Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	0	R0C [7:0] : SWA_OUTPUT_CURRENT_POWER_MEASUREMENT If Register R1A [1] = 0, Switch Node A Output Current or Output Power Measurement 0000 0000 = Un-defined 0000 0001 = 0.125A or 125mW 0000 0010 = 0.25A or 250mW 0000 0011 = 0.375A or 375mW 0000 0100 = 0.5A or 500mW 0000 0101 = 0.625A or 625mW 0000 0110 = 0.75A or 750mW 0000 0111 = 0.875A or 875mW 0000 1000 = 1.0A or 1000mW 0000 1001 = 1.125A or 1125mW .. 0011 0111 = 6.875A or 6875mW 0011 1000 = 7.0A or 7000mW 0011 1001 = 7.125A or 7125mW 0011 1010 = 7.25A or 7250mW 0011 1011 = 7.375A or 7375mW 0011 1100 = 7.5Aor 7500mW 0011 1101 = 7.625A or 7625mW 0011 1110 = 7.75A or 7750mW 0011 1111 >= 7.875A or 7875mW All other encodings are reserved If Register R1A [1] = 1, Sum of power measurement for Switch Outputs SW[A..D] 0000 0000 = Un-defined 0000 0001 = 125mW 0000 0010 = 250mW 0000 0011 = 375mW 0000 0100 = 500mW ... 1111 1100 = 31500mW 1111 1101 = 31625mW 1111 1110 = 31750mW 1111 1111 >= 31875mW

R0D - SWB Current and Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R0D [7:6]: Reserved
5:0	RO	0	R0D [5:0]: SWB_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node B Output Current or Output Power Measurement 000000 = Un-defined 000001 = 0.125A or 125mW 000010 = 0.25A or 250mW 000011 = 0.375A or 375mW 000100 = 0.5A or 500mW 000101 = 0.625A or 625mW 000110 = 0.75A or 750mW 000111 = 0.875A or 875mW 001000 = 1.0A or 1000mW 001001 = 1.125A or 1125mW ... 110111 = 6.875A or 6875mW 111000 = 7.0A or 7000mW 111001 = 7.125A or 7125mW 111010 = 7.25A or 7250mW 111011 = 7.375A or 7375mW 111100 = 7.5A or 7500mW 111101 = 7.625A or 7625mW 111110 = 7.75A or 7750mW 111111 >= 7.875A or 7875mW

R0E - SWC Current and Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R0E [7:6]: Reserved
5:0	RO	0	R0E [5:0]: SWC_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node C Output Current or Output Power Measurement 000000 = Un-defined 000001 = 0.125A or 125mW 000010 = 0.25A or 250mW 000011 = 0.375A or 375mW 000100 = 0.5A or 500mW 000101 = 0.625A or 625mW 000110 = 0.75A or 750mW 000111 = 0.875A or 875mW 001000 = 1.0A or 1000mW 001001 = 1.125A or 1125mW 001010 = 1.25A or 1250mW ... 110111 = 6.875A or 6875mW 111000 = 7.0A or 7000mW 111001 = 7.125A or 7125mW 111010 = 7.25A or 7250mW 111011 = 7.375A or 7375mW 111100 = 7.5A or 7500mW 111101 = 7.625A or 7625mW 111110 = 7.75A or 7750mW 111111 >= 7.875A or 7875mW

R0F - SWD Current and Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R0F [7:6]: Reserved
5:0	RO	0	R0F [5:0]: SWD_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node D Output Current or Output Power Measurement 000000 = Un-defined 000001 = 0.125A or 125mW 000010 = 0.25A or 250mW 000011 = 0.375A or 375mW 000100 = 0.5A or 500mW 000101 = 0.625A or 625mW 000110 = 0.75A or 750mW 000111 = 0.875A or 875mW 001000 = 1.0A or 1000mW 001001 = 1.125A or 1125mW ... 110111 = 6.875A or 6875mW 111000 = 7.0A or 7000mW 111001 = 7.125A or 7125mW 111010 = 7.25A or 7250mW 111011 = 7.375A or 7375mW 111100 = 7.5A or 7500mW 111101 = 7.625A or 7625mW 111110 = 7.75A or 7750mW 111111 >= 7.875A or 7875mW

R10 - Clear Status Bits_0			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	R10 [7] : CLEAR_VIN_BULK_INPUT_POWER_GOOD_STATUS Clear VIN_BULK Input Power Good Status. 1 = Clear “Register R08” [7]
6	RV	0	R10 [6]: Reserved
5	1O	0	R10 [5] : CLEAR_SWA_OUTPUT_POWER_GOOD_STATUS Clear SWA Output Power Good Status. 1 = Clear “Register R08” [5]
4	1O	0	R10 [4] : CLEAR_SWB_OUTPUT_POWER_GOOD_STATUS Clear SWB Output Power Good Status. 1 = Clear “Register R08” [4]
3	1O	0	R10 [3] : CLEAR_SWC_OUTPUT_POWER_GOOD_STATUS Clear SWC Output Power Good Status. 1 = Clear “Register R08” [3]
2	1O	0	R10 [2] : CLEAR_SWD_OUTPUT_POWER_GOOD_STATUS Clear SWD Output Power Good Status. 1 = Clear “Register R08” [2]
1	1O	0	R10 [1] : CLEAR_VIN_MGMT_INPUT_OVER_VOLTAGE_STATUS Clear 3.3V Input Supply Over-Voltage Status. 1 = Clear “Register R08” [1]
0	1O	0	R10 [0] : CLEAR_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Clear 12V Input Supply Over-Voltage Status. 1 = Clear “Register R08” [0]

R11 - Clear Status Bits_1			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	R11 [7] : CLEAR_PMIC_HIGH_TEMP_WARNING_STATUS 1 = Clear “Register R09” [7]
6	1O	0	R11 [6] : CLEAR_V_{BIAS}_POWER_GOOD_STATUS 1 = Clear “Register R09” [6]
5	1O	0	R11 [5] : CLEAR_VLDO_1.8V_OUTPUT_POWER_GOOD_STATUS 1 = Clear “Register R09” [5]
4	1O	0	R11 [4] : CLEAR_VIN_MGMT_TO_VIN_BULK_INPUT_SWITCHOVER_STATUS 1 = Clear “Register R09” [4]
3	1O	0	R11 [3] : CLEAR_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS 1 = Clear “Register R09” [3]
2	1O	0	R11 [2] : CLEAR_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS 1 = Clear “Register R09” [2]
1	1O	0	R11 [1] : CLEAR_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS 1 = Clear “Register R09” [1]
0	1O	0	R11 [0] : CLEAR_SWD_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS 1 = Clear “Register R09” [0]

R12 - Clear Status Bits_2			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	R12 [7] : CLEAR_SWA_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node A Output Over-Voltage Status. 1 = Clear “Register R0A” [7]
6	1O	0	R12 [6] : CLEAR_SWB_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node B Output Over-Voltage Status. 1 = Clear “Register R0A” [6]
5	1O	0	R12 [5] : CLEAR_SWC_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node C Output Over-Voltage Status. 1 = Clear “Register R0A” [5]
4	1O	0	R12 [4] : CLEAR_SWD_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node D Output Over-Voltage Status. 1 = Clear “Register R0A” [4]
3	1O	0	R12 [3]: CLEAR_PEC_ERROR_STATUS Clear PEC Error Status. 1 = Clear “Register R0A” [3]
2	1O	0	R12 [2]: CLEAR_PARITY_ERROR_STATUS Clear Parity Error Status. 1 = Clear “Register R0A” [2]
1:0	RV	0	R12 [1:0]: Reserved

R13 - Clear Status Bits_3			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	R13 [7]: CLEAR_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS 1 = Clear “Register R0B” [7]
6	1O	0	R13 [6]: CLEAR_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS 1 = Clear “Register R0B” [6]
5	1O	0	R13 [5]: CLEAR_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS 1 = Clear “Register R0B” [5]
4	1O	0	R13 [4]: CLEAR_SWD_OUTPUT_CURRENT_LIMITER_WARNING_STATUS 1 = Clear “Register R0B” [4]
3	1O	0	R13 [3]: CLEAR_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS 1 = Clear “Register R0B” [3]
2	1O	0	R13 [2]: CLEAR_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS 1 = Clear “Register R0B” [2]
1	1O	0	R13 [1]: CLEAR_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS 1 = Clear “Register R0B” [1]
0	1O	0	R13 [0]: CLEAR_SWD_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS 1 = Clear “Register R0B” [0]

R14 - Clear Status Bits_4			
Bits	**Attribute**	**Default**	**Description**
7:5	RV	0	R14 [7:5] : Reserved
4	1O	0	R14 [4] : CLEAR_VIN_MGMT_POWER_GOOD_STATUS_SWITCHOVER_MODE 1 = Clear “Register R33” [4]
3	1O	0	R14 [3] : CLEAR_V_{BIAS}_OUTPUT_OR_VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS 1 = Clear “Register R33” [3]
2	1O	0	R14 [2] : CLEAR_VLDO_1.0V_OUTPUT_POWER_GOOD_STATUS 1 = Clear “Register R33” [2]
1	RV	0	R14 [1] : Reserved
0	1O	0	R14 [0] : GLOBAL_CLEAR_STATUS Clear all4 status bits. 1 = Clear all status bits

R15 - Mask Status_0			
Bits	**Attribute**	**Default**	**Description**
7	RW	1	R15 [7] : MASK_VIN_BULK_INPUT_POWER_GOOD_STATUS 0 = Do Not Mask 1 = Mask Event
6	RV	0	R15 [6]: Reserved
5	RW	1	R15 [5] : MASK_SWA_OUTPUT_POWER_GOOD_STATUS 0 = Do Not Mask 1 = Mask Event
4	RW	1	R15 [4] : MASK_SWB_OUTPUT_POWER_GOOD_STATUS 0 = Do Not Mask 1 = Mask Event
3	RW	1	R15 [3] : MASK_SWC_OUTPUT_POWER_GOOD_STATUS 0 = Do Not Mask 1 = Mask Event
2	RW	1	R15 [2] : MASK_SWD_OUTPUT_POWER_GOOD_STATUS 0 = Do Not Mask 1 = Mask Event
1	RW	0	R15 [1] : MASK_VIN_MGMT_INPUT_OVER_VOLTAGE_STATUS 0 = Do Not Mask 1 = Mask Event
0	RW	0	R15 [0] : MASK_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS 0 = Do Not Mask 1 = Mask Event

R16 - Mask Status_1			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R16 [7] : MASK_PMIC_HIGH_TEMP_WARNING_STATUS 0 = Do Not Mask 1 = Mask Event
6	RW	0	R16 [6] : MASK_V_{BIAS}_POWER_GOOD_STATUS 0 = Do Not Mask 1 = Mask Event
5	RW	1	R16 [5] : MASK_VLDO_1.8V_OUTPUT_POWER_GOOD_STATUS 0 = Do Not Mask 1 = Mask Event
4	RW	0	R16 [4] : MASK_VIN_MGMT_TO_VIN_BULK_SWITCHOVER_STATUS 0 = Do Not Mask Event 1 = Mask Event
3	RW	0	R16 [3] : MASK_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS 0 = Do Not Mask 1 = Mask Event
2	RW	0	R16 [2] : MASK_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS 0 = Do Not Mask 1 = Mask Event
1	RW	0	R16 [1] : MASK_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS 0 = Do Not Mask 1 = Mask Event
0	RW	0	R16 [0] : MASK_SWD_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS 0 = Do Not Mask 1 = Mask Event

R17 - Mask Status_2			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R17 [7] : MASK_SWA_OUTPUT_OVER_VOLTAGE_STATUS 0 = Do Not Mask 1 = Mask Event
6	RW	0	R17 [6] : MASK_SWB_OUTPUT_OVER_VOLTAGE_STATUS 0 = Do Not Mask 1 = Mask Event
5	RW	0	R17 [5] : MASK_SWC_OUTPUT_OVER_VOLTAGE_STATUS 0 = Do Not Mask 1 = Mask Event
4	RW	0	R17 [4] : MASK_SWD_OUTPUT_OVER_VOLTAGE_STATUS 0 = Do Not Mask 1 = Mask Event
3	RW	0	R17 [3]: MASK_PEC_ERROR_STATUS Mask PEC Error Event for GSI_n output Only 0 = Do Not Mask PEC Error Status Event 1 = Mask PEC Error Status
2	RW	0	R17 [2]: MASK_PARITY_ERROR_STATUS Mask Parity Error Event for GSI_n output Only 0 = Do Not Mask Parity Error Status Event 1 = Mask Parity Error Status
1:0	RV	0	R17 [1:0]: Reserved

R18 - Mask Status_3			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R18 [7] : MASK_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS 0 = Do Not Mask 1 = Mask Event
6	RW	0	R18 [6] : MASK_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS 0 = Do Not Mask 1 = Mask Event
5	RW	0	R18 [5] : MASK_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS 0 = Do Not Mask 1 = Mask Event
4	RW	0	R18 [4] : MASK_SWD_OUTPUT_CURRENT_LIMITER_WARNING_STATUS 0 = Do Not Mask 1 = Mask Event
3	RW	0	R18 [3] : MASK_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS 0 = Do Not Mask 1 = Mask Event
2	RW	0	R18 [2] : MASK_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS 0 = Do Not Mask 1 = Mask Event
1	RW	0	R18 [1] : MASK_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS 0 = Do Not Mask 1 = Mask Event
0	RW	0	R18 [0] : MASK_SWD_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS 0 = Do Not Mask 1 = Mask Event

R19 - Mask Status_4			
Bits	**Attribute**	**Default**	**Description**
7:5	RV	0	R19 [7:5] : Reserved
4	RW	0	R19 [4] : MASK_VIN_MGMT_POWER_GOOD_STATUS_SWITCHOVER_MODE 0 = Do Not Mask 1 = Mask Event
3	RW	0	R19 [3] : MASK_V_{BIAS}_OUTPUT_OR_VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS 0 = Do Not Mask 1 = Mask Event
2	RW	1	R19 [2] : MASK_VLDO_1.0V_OUTPUT_POWER_GOOD_STATUS 0 = Do Not Mask 1 = Mask Event
1:0	RV	0	R19 [1:0] : Reserved

R1A - IN/OUT PG/UVLO TH			
Bits	**Attribute**	**Default**	**Description**
7:5	RW	110	R1A [7:5] : VIN_BULK_POWER_GOOD_THRESHOLD_VOLTAGE VIN Bulk Input Threshold Voltage level for Input Power Good Falling Status 000 = Reserved (9.5V) 001 = 9.5V 010 = 8.5V 011 = 7.5V 100 = 6.5V 101 = 5.5V 110 = 4.25V 111 = Reserved (4.25V)
4	RV	0	R1A [4]: Reserved
3	RW	0	R1A [3] : V_{BIAS}_POWER_GOOD_THRESHOLD_VOLTAGE V_{BIAS} LDO Output Threshold Voltage for Power Good Status 0 = Power Good Low Threshold (3.6V) 1 = Power Good Low Threshold (3.2V)
2	RW	0	R1A [2] : VLDO_1.8V_POWER_GOOD_THRESHOLD_VOLTAGE VOUT 1.8V LDO Output Threshold Voltage for Power Good Status 0 = 1.6V 1 = Reserved
1	RW	0	R1A [1]: OUTPUT_POWER_SELECT Switch Regulator Output Power Select 0 = Report Power Measurement for Each Rail in R0C, R0D, R0E & R0F 1 = Report Total Power Measurement of Each Rail in R0C
0	RW	0	R1A [0] : VLDO_1.0V_POWER_GOOD_THRESHOLD_VOLTAGE VOUT 1.0V LDO Output Threshold Voltage for Power Good Status 0 = –10% from the setting in “Register R51” [2:1] 1 = –15% from the setting in “Register R51” [2:1]

R1B - OV/OT_TH; GSI EN; Global PG MASK			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R1B [7]: VIN_BULK_OVER_VOLTAGE_THRESHOLD VIN_BULK Input Over Voltage Threshold Setting For GSI_n Assertion 0 = OVH(14.5V), OVL(13.5V) 1 = OVH(16.0V), OVL(15V)
6	RW	0	R1B [6] : CURRENT_OR_POWER_METER_SELECT PMIC Output Regulator Measurement - Current or Power Meter 0 = Report Current Measurements in registers 1 = Report Power Measurements in registers
5	RW	0	R1B [5]: VIN_MGMT_OVER_VOLTAGE_THRESHOLD VIN_MGMT Input Over Voltage Threshold 0 = 3.8 V 1 = 3.7 V
4	RW	0	R1B [4]: GLOBAL_CAMP_PIN_STATUS_MASK Global Mask CAMP Output Pin 0 = Not Masked 1 = Masked
3	RW	0	R1B [3] : GSI_N_OUTPUT_PIN_ENABLE Enable GSI_n Output Pin 0 = Disable GSI_n Output Pin 1 = Enable GSI_n Output Pin
2:0	RW	101	R1B [2:0] : PMIC_HIGH_TEMPERATURE_WARNING_THRESHOLD PMIC High Temperature Warning Threshold 000 = Reserved 001 = PMIC temperature > 85°C 010 = PMIC temperature > 95°C 011 = PMIC temperature > 105°C 100 = PMIC temperature > 115°C 101 = PMIC temperature > 125°C 110 = PMIC temperature > 135°C 111 = Reserved

R1C - SWA High Current Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:2	RW	011000	R1C [7:2] : SWA_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node A Output High Current Consumption Warning Threshold 000000 = Un-defined 000001 = >0.125A 000010 = >0.25A 000011 = >0.375A 000100 = >0.5A 000101 = >0.625A 000110 = >0.75A 000111 = >0.875A 001000 = >1.0A 001001 = >1.125A ... ... 010111 = >2.875A 011000 = >3.0A 011001 = >3.125A ... 110111 = >6.875A 111000 = >7.0A 111001 = >7.125A 111010 = >7.25A 111011 = >7.375A 111100 = >7.5A 111101 = >7.625A 111110 = >7.75A 111111 = >7.875A
1:0	RV	0	R1C [1:0] : Reserved

R1D - SWB High Current Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:2	RW	011000	R1D [7:2] : SWB_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node B Output High Current Consumption Warning Threshold 000000 = Un-defined 000001 = >0.125A 000010 = >0.25A 000011 = >0.375A 000100 = >0.5A 000101 = >0.625A 000110 = >0.75A 000111 = >0.875A 001000 = >1.0A 001001 = >1.125A ... 010111 = >2.875A 011000 = >3.0A ... 110111 = >6.875A 111000 = >7.0A 111001 = >7.125A 111010 = >7.25A 111011 = >7.375A 111100 = >7.5A 111101 = >7.625A 111110 = >7.75A 111111 = >7.875A
1:0	RV	0	R1D [1:0] : Reserved

R1E - SWC High Current Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:2	RW	011000	R1E [7:2] : SWC_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node C Output High Current Consumption Warning Threshold 000000 = Un-defined 000001 = >0.125A 000010 = >0.25A 000011 = >0.375A 000100 = >0.5A 000101 = >0.625A 000110 = >0.75A 000111 = >0.875A 001000 = >1.0A 001001 = >1.125A ... 010111 = >2.875A 011000 = >3.0A 011001 = >3.125A ... 110111 = >6.875A 111000 = >7.0A 111001 = >7.125A 111010 = >7.25A 111011 = >7.375A 111100 = >7.5A 111101 = >7.625A 111110 = >7.75A 111111 = >7.875A
1:0	RV	0	R1E [1:0] : Reserved

R1F - SWD High Current Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:2	RW	011000	R1F [7:2] : SWD_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node D Output High Current Consumption Warning Threshold 000000 = Un-defined 000001 = >0.125A 000010 = >0.25A 000011 = >0.375A 000100 = >0.5A 000101 = >0.625A 000110 = >0.75A 000111 = >0.875A 001000 = >1.0A 001001 = >1.125A ... 010111 = >2.875A 011000 = >3.0A 011001 = >3.125A ... 110111 = >6.875A 111000 = >7.0A 111001 = >7.125A 111010 = >7.25A 111011 = >7.375A 111100 = >7.5A 111101 = >7.625A 111110 = >7.75A 111111 = >7.875A
1:0	RV	0	R1F [1:0] : Reserved

R20 - SW[A:D] Current Limited Warning TH			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	10	R20 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Low Current PMIC Encoding Definition For Constant On Time (COT) Mode, Ivalley_limit: 00 = 2.5A 01 = 3.0A 10 = 3.5A 11 = 4.0A
5:4	RW	10	R20 [5:4]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Low Current PMIC Encoding Definition For Constant On Time (COT) Mode, Ivalley_limit: 00 = 2.5A 01 = 3.0A 10 = 3.5A 11 = 4.0A
3:2	RW	10	R20 [3:2]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Low Current PMIC Encoding Definition For Constant On Time (COT) Mode, Ivalley_limit: 00 = 2.5A 01 = 3.0A 10 = 3.5A 11 = 4.0A
1:0	RW	10	R20 [1:0]: SWD_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Low Current PMIC Encoding Definition For Constant On Time (COT) Mode, Ivalley_limit: 00 = 2.5A 01 = 3.0A 10 = 3.5A 11 = 4.0A

R21 - SWA Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	R21 [7:1]: SWA_VOLTAGE_SETTING Switch Node A Output Regulator Voltage Setting 000 0000 = 800mV or 600mV 000 0001 = 805mV or 605mV 000 0010 = 810mV or 610mV ... 011 1100 = 1100mV or 900mV ... 111 1101 = 1425mV or 1225mV 111 1110 = 1430mV or 1230mV 111 1111 = 1435mV or 1235mV
0	RW	0	R21 [0] : SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register R21,” [7:1] 1 = –7.5% from the setting in “Register R21,” [7:1]

R22 - SWA Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R22 [7:6] : SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High-Side Voltage “Upper bound level” For Power Good Status 00 = +5% from the setting in “Register R21,” [7:1] 01 = +7.5% from the setting in “Register R21,” [7:1] 10 = +10% from the setting in “Register R21,” [7:1] 11 = +3% from the setting in “Register R21,” [7:1]
5:4	RW	10	R22 [5:4] : SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Over-Voltage Status 00 = +7.5% from the setting in “Register R21,” [7:1] 01 = +10% from the setting in “Register R21,” [7:1] 10 = +12.5% from the setting in “Register R21,” [7:1] 11 = +5% from the setting in “Register R21,” [7:1]
3:2	RW	00	R22 [3:2] : SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Under-Voltage Lockout Status 00 = –10% from the setting in “Register R21,” [7:1] 01 = –12.5% from the setting in “Register R21,” [7:1] 10 = –5% from the setting in “Register R21,” [7:1] 11 = –7.5% from the setting in “Register R21,” [7:1]
1:0	RW	00	R22 [1:0] : SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

R23 - SWB Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	R23 [7:1]: SWB_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting 000 0000 = 800mV or 600mV 000 0001 = 805mV or 605mV 000 0010 = 810mV or 610mV ... 011 1100 = 1100mV or 900mV ... 111 1101 = 1425mV or 1225mV 111 1110 = 1430mV or 1230mV 111 1111 = 1435mV or 1235mV
0	RW	0	R23 [0] : SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register R23,” [7:1] 1 = –7.5% from the setting in “Register R23,” [7:1]

R24 - SWB Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R24 [7:6] : SWB_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R23,” [7:1] 01 = +7.5% from the setting in “Register R23,” [7:1] 10 = +10% from the setting in “Register R23,” [7:1] 11 = +3% from the setting in “Register R23,” [7:1]
5:4	RW	10	R24 [5:4] : SWB_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Over-Voltage Status 00 = +7.5% from the setting in “Register R23,” [7:1] 01 = +10% from the setting in “Register R23,” [7:1] 10 = +12.5% from the setting in “Register R23,” [7:1] 11 = +5% from the setting in “Register R23,” [7:1]
3:2	RW	00	R24 [3:2] : SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Under-Voltage Lockout Status 00 = –10% from the setting in “Register R23,” [7:1] 01 = –12.5% from the setting in “Register R23,” [7:1] 10 = –5% from the setting in “Register R23,” [7:1] 11 = –7.5% from the setting in “Register R23,” [7:1]
1:0	RW	00	R24 [1:0] : SWB_OUTPUT_SOFT_STOP_TIME SWB Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

R25 - SWC Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	R25 [7:1]: SWC_VOLTAGE_SETTING Switch Node C Output Regulator Voltage Setting 000 0000 = 800 mV or 600 mV 000 0001 = 805 mV or 605 mV 000 0010 = 810 mV or 610 mV ... 011 1100 = 1100 mV or 900 mV ... 111 1101 = 1425 mV or 1225 mV 111 1110 = 1430 mV or 1230 mV 111 1111 = 1435 mV or 1235 mV
0	RW	0	R25 [0] : SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register R25,” [7:1] 1 = –7.5% from the setting in “Register R25,” [7:1]

R26 - SWC Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R26 [7:6] : SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R25” [7:1] 01 = +7.5% from the setting in “Register R25” [7:1] 10 = +10% from the setting in “Register R25” [7:1] 11 = +3% from the setting in “Register R25” [7:1]
5:4	RW	10	R26 [5:4] : SWC_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Over-Voltage Status 00 = +7.5% from the setting in “Register R25” [7:1] 01 = +10% from the setting in “Register R25” [7:1] 10 = +12.5% from the setting in “Register R25” [7:1] 11 = +5% from the setting in “Register R25” [7:1]
3:2	RW	00	R26 [3:2] : SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Under-Voltage Lockout Status 00 = –10% from the setting in “Register R25” [7:1] 01 = –12.5% from the setting in “Register R25” [7:1] 10 = –5% from the setting in “Register R25” [7:1] 11 = –7.5% from the setting in “Register R25” [7:1]
1:0	RW	00	R26 [1:0] : SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

R27 - SWD Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	R27 [7:1] : SWD_VOLTAGE_SETTING Switch Node D Output Regulator Voltage Setting 000 0000 = 1500mV or 2200mV 000 0001 = 1505mV 2205mV 000 0010 = 1510mV 2210mV ... 011 1100 = 1800mV 2500mV ... 111 1101 = 2125mV 2825mV 111 1110 = 2130mV 2830mV 111 1111 = 2135mV 2835mV
0	RW	0	R27 [0] : SWD_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node D Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register R27” [7:1] 1 = –7.5% from the setting in “Register R27” [7:1]

R28 - SWD Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R28 [7:6] : SWD_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node D Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R27” [7:1] 01 = +7.5% from the setting in “Register R27” [7:1] 10 = +10% from the setting in “Register R27” [7:1] 11 = +3% from the setting in “Register R27” [7:1]
5:4	RW	10	R28 [5:4] : SWD_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node D Output Regulator Threshold For Over-Voltage Status 00 = +7.5% from the setting in “Register R27” [7:1] 01 = +10% from the setting in “Register R27” [7:1] 10 = +12.5% from the setting in “Register R27” [7:1] 11 = +5% from the setting in “Register R27” [7:1]
3:2	RW	00	R28 [3:2] : SWD_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node D Output Regulator Threshold For Under-Voltage Lockout Status 00 = –10% from the setting in “Register R27” [7:1] 01 = –12.5% from the setting in “Register R27” [7:1] 10 = –5% from the setting in “Register R27” [7:1] 11 = –7.5% from the setting in “Register R27” [7:1]
1:0	RW	00	R28 [1:0] : SWD_OUTPUT_SOFT_STOP_TIME SWD Output Regulator Soft-Stop Time After VR Disable 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

R29 - SW[A:B] FSW and Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	10	R29 [7:6] : SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RW	01	R29 [5:4]: SWA_SWITCHING_FREQ [1] Switch Node A Output Regulator Switching Frequency 00 = 500kHz 01 = 750kHz 10 = 1000kHz 11 = 1250kHz
3:2	RW	10	R29 [3:2] : SWB_MODE_SELECT Switch Node B Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
1:0	RW	01	R29 [1:0]: SWB_SWITCHING_FREQ [2] Switch Node B Output Regulator Switching Frequency 00 = 500kHz 01 = 750kHz 10 = 1000kHz 11 = 1250kHz

[1] The typical switching frequency for RTQ5119A's SWA are summarized as below :

as 0x29"[5:4] = "00" → Typ. f_{SW} = 450kHz; as 0x29"[5:4] = "01" → Typ. f_{SW} = 670kHz;

as 0x29"[5:4] = "10" → Typ. f_{SW} = 890kHz; as 0x29"[5:4] = "11" → Typ. f_{SW} = 1110kHz

[2] The typical switching frequency for RTQ5119A's SWB are summarized as below :

as 0x29"[1:0] = "00" → Typ. f_{SW} = 450kHz; as 0x29"[1:0] = "01" → Typ. f_{SW} = 670kHz;

as 0x29"[1:0] = "10" → Typ. f_{SW} = 890kHz; as 0x29"[1:0] = "11" → Typ. f_{SW} = 1110kHz

R2A - SW[C:D] FSW and Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	10	R2A [7:6] : SWC_MODE_SELECT Switch Node C Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RW	01	R2A [5:4]: SWC_SWITCHING_FREQ [1] Switch Node C Output Regulator Switching Frequency 00 = 500kHz 01 = 750kHz 10 = 1000kHz 11 = 1250kHz
3:2	RW	10	R2A [3:2] : SWD_MODE_SELECT Switch Node D Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
1:0	RW	10	R2A [1:0]: SWD_SWITCHING_FREQ Switch Node D Output Regulator Switching Frequency 00 = 500kHz 01 = 750kHz 10 = 1000kHz 11 = 1250kHz

[1] The typical switching frequency for RTQ5119A's SWC are summarized as below :

as 0x2A"[5:4] = "00" → Typ. f_{SW} = 450kHz; as 0x2A"[5:4] = "01" → Typ. f_{SW} = 670kHz;

as 0x2A"[5:4] = "10" → Typ. f_{SW} = 890kHz; as 0x2A"[5:4] = "11" → Typ. f_{SW} = 1110kHz

R2B – Voltage Setting for LDO_1.8V & LDO_1.0V & SW[A:D] Output Voltage Range			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R2B [7:6] : VLDO_1.8V_VOLTAGE_SETTING VOUT 1.8V LDO Output Voltage Setting 00 = 1.7V 01 = 1.8V 10 = 1.9V 11 = Reserved
5	RW	0	R2B [5]: SWA_VOLTAGE_RANGE SWA Output Voltage Range Selection 0 = Range: 800mV to 1435mV for SWA; 5mV step size 1 = Range: 600mV to 1235mV for SWA; 5mV step size
4	RW	0	R2B [4]: SWB_VOLTAGE_RANGE SWB Output Voltage Range Selection 0 = Range: 800mV to 1435mV for SWB; 5mV step size 1 = Range: 600mV to 1235mV for SWB; 5mV step size
3	RW	0	R2B [3]: SWC_VOLTAGE_RANGE SWC Output Voltage Range Selection 0 = Range: 800mV to 1435mV for SWC; 5mV step size 1 = Range: 600mV to 1235mV for SWC; 5mV step size
2:1	RW	01	R2B [2:1]: VLDO_1.0V_VOLTAGE_SETTING VOUT 1.0V LDO Voltage Setting 00 = 0.9V 01 = 1.0V 10 = 1.1V 11 = 1.2V
0	RW	0	R2B [0]:SWD_VOLTAGE_RANGE SWD Output Voltage Range Selection 0 = Range: 1500mV to 2135mV for SWD; 5mV step size 1 = Range: 2200mV to 2835mV for SWD; 5mV step size

R2C - SW[A:B] Soft-Start			
Bits	**Attribute**	**Default**	**Description**
7:5	RW	001	R2C [7:5] : SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
4	RV	0	R2C [4] : Reserved
3:1	RW	001	R2C [3:1] : SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
0	RV	0	R2C [0] : Reserved

R2D - SW[C:D] Soft-Start			
Bits	**Attribute**	**Default**	**Description**
7:5	RW	001	R2D [7:5] : SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
4	RV	0	R2D [4]: Reserved
3:1	RW	001	R2D [3:1] : SWD_OUTPUT_SOFT_START_TIME SWD Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
0	RV	0	R2D [0] : Reserved

R2E - Shutdown Temp. Threshold			
Bits	**Attribute**	**Default**	**Description**
7:3	RV	0	R2E [7:3] : Reserved
2:0	RW	100	R2E [2:0] : PMIC_SHUTDOWN_TEMPERATURE_THRESHOLD PMIC Shutdown Temperature Threshold 000 = PMIC Temperature > 105°C 001 = PMIC Temperature > 115°C 010 = PMIC Temperature > 125°C 011 = PMIC Temperature > 135°C 100 = PMIC Temperature > 145°C 101 = Reserved 110 = Reserved 111 = Reserved

R2F PMIC Configuration			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R2F [7]: VIN_MGMT_INPUT_SUPPLY_SWITCHOVER_THRESHOLD VIN_MGMT Input Supply Switchover Voltage Threshold to VIN_BULK Supply 0 = 2.7V 1 = 2.75V
6	RW	0	R2F [6] : SWA_REGULATOR_CONTROL Disable SWA Regulator Output 0 = Disable SWA Output 1 = Enable SWA Output
5	RW	0	R2F [5] : SWB_REGULATOR_CONTROL Disable SWB Regulator Output 0 = Disable SWB Output 1 = Enable SWB Output
4	RW	0	R2F [4] : SWC_REGULATOR_CONTROL Disable SWC Regulator Output 0 = Disable SWC Output 1 = Enable SWC Output
3	RW	0	R2F [3] : SWD_REGULATOR_CONTROL Disable SWD Regulator Output 0 = Disable SWD Output 1 = Enable SWD Output
2	RW	0	R2F [2]: WRITE_PROTECT_FUNCTION_CONTROL PMIC Write Protect Function Control 0 = CAMP input signal determines the Write Protect Function 1 = Write Protect Function is disabled; All register write access is allowed independent of CAMP input signal
1:0	RW	10	R2F [1:0] : MASK_BITS_REGISTER_CONTROL Mask Bits Register Control 00 = Mask GSI_n Signal Only (PWR_GOOD Signal will assert) 01 = Mask PWR_GOOD Only (GSI_n signal will assert) 10 = Mask GSI_n and PWR_GOOD Signals (neither PWR_GOOD assert or GSI_n signal will assert) 11 = Reserved

R30 - ADC Enable			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R30 [7] : ADC_ENABLE Enable ADC (Analog to Digital Conversion) 0 = Disable 1 = Enable
6:3	RW	0	R30 [6:3] : ADC_SELECT Input Selection for ADC Readout 0000 = SWA Output Voltage 0001 = SWB Output Voltage 0010 = SWC Output Voltage 0011 = SWD Output Voltage 0100 = Reserved 0101 = VIN_BULK Input Voltage 0110 = VIN_MGMT Input Voltage 0111 = V_{BIAS} Output Voltage 1000 = VLDO_1.8V Output Voltage 1001 = VLDO_1.0V Output Voltage All other encodings are reserved.
2	RV	0	R30[2] : Reserved
1:0	RW	0	R30 [1:0] : ADC_REGISTER_UPDATE_FREQUENCY ADC Current or Power Measurement Update Frequency 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

R31 - ADC Read			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	0	R31 [7:0]: ADC_READ ADC Output Voltage Reading (Applies to SW[A:D], VLDO_1.8V, VLDO_1.0V, VIN_MGMT) 0000 0000 = Undefined 0000 0001 = 15mV 0000 0010 = 30mV .. 1111 1111 >= 3825mV ADC Output Voltage Reading (Applies to VIN_BULK Input Voltage) 0000 0000 = Undefined 0000 0001 = 70mV 0000 0010 = 140mV .. 1111 1111 >= 17850mV ADC Output Voltage Reading (Applies to V_{BIAS} Output Voltage) 0000 0000 = Undefined 0000 0001 = 25mV 0000 0010 = 50mV .. 1111 1111 >= 6375mV

R32 - PMIC_EN & MGMT Interface Selection			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R32 [7] : VR_ENABLE PMIC Enable 0 = PMIC Disable 1 = PMIC Enable
6	RO	0	R32 [6]: MANAGEMENT_INTERFACE_SELECTION PMIC Management Bus Interface Protocol Selection 0 = I^2C Interface (Max speed 1MHz) 1 = I^3C Basic Protocol
5	RW	1	R32 [5]: EXECUTE_VR_ENABLE_CONTROL PMIC VR Enable Command Execution Control over I^2C/I^3C Bus 0 = Do Not Execute VR Enable Command; i.e. ignore bit [7] = ‘1’ and keep it as ‘0’. 1 = Execute VR Enable Command
4	RW	0	R32 [4]: EXECUTE_CAMP_FAIL_N_FUNCTION_CONTROL PMIC CAMP Fail_n function (Transition from High to Low) Control 0 = Execute VR Disable Command 1 = Do Not Execute VR Disable Command
3	RW	0	R32 [3]: CAMP_PWR_GOOD_OUTPUT_SIGNAL_CONTROL PMIC CAMP PWR_GOOD Output Signal Control 0 = PMIC controls PWR_GOOD output on its own based on internal status 1 = PWR_GOOD Output Float
2:0	RV	0	R32 [2:0]: Reserved

R33 - Temp_Meas and LDO Status			
Bits	**Attribute**	**Default**	**Description**
7:5	RO	0	R33 [7:5]: TEMPERATURE_MEASUREMENT PMIC Temperature 000 = ≤ 80˚C (± 5ºC) 001 = 85˚C (± 5ºC) 010 = 95˚C (± 5ºC) 011 = 105˚C (± 5ºC) 100 = 115˚C (± 5ºC) 101 = 125˚C (± 5ºC) 110 = 135˚C (± 5ºC) 111 = ≥135˚C (± 5ºC)
4	RO	0	R33 [4] : VIN_MGMT_POWER_GOOD_STATUS_SWITCHOVER_MODE VIN_MGMT Input Supply Power Good Status in Switchover Mode Only 0 = Power Not Good 1 = Power Good
3	RO	0	R33 [3] : V_{BIAS}_OR_VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS V_{BIAS} or VIN_BULK Under Voltage Lockout Status 0 = No Under Voltage Lockout 1 = Under Voltage Lockout
2	RO	0	R33 [2] : VLDO_1.0V_OUTPUT_POWER_GOOD_STATUS VLDO_1.0V LDO Output Power Good Status 0 = Power Good 1 = Power Not Good
1:0	RV	0	R33 [1:0]: Reserved

R34 – PEC/IBI/PARITY/HID_CODE			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R34 [7]: PEC_ENABLE Packet Error Code Enable (Applicable Only if R32 [6] = ‘1’) 0 = Disable 1 = Enable
6	RO	0	R34 [6]: IBI_ENABLE In Band Interrupt Enable (Applicable Only if R32 [6] = ‘1’) 0 = Disable 1 = Enable
5	RO	0	R34 [5]: PARITY_DISABLE T Bit Parity Code Disable (Applicable Only if R32 [6] = ‘1’.) 0 = Enable 1 = Disable
4	RV	0	R34 [4]: Reserved
3:1	RO	111	R34 [3:1]: HID_CODE PMIC’s 3-bit HID Code 000 001 010 011 100 101 110 111
0	RV	0	R34 [0]: Reserved

R35 – Error Injection			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R35 [7] : Error_Injection_Enable 0 = Disable 1 = Enable
6:4	RW	0	R35 [6:4]: Error_Injection_Rail_Selection 000 = Undefined 001 = SWA Output only 010 = SWB Output only 011 = SWC Output only 100 = SWD Output only 101 = VIN_BULK Input only 110 = VIN_MGMT Input only 111 = Don't use.
3	RW	0	R35 [3]: Over Voltage or Under Voltage Selection for R35[6:4] 0 = Over-Voltage 1 = Under-Voltage
2:0	RW	0	R35 [2:0]: Misc_Error_Injection_Type 000 = Undefined 001 = VIN_MGMT to VIN_BULK Switchover 010 = Critical Temperature Shutdown 011 = High Temperature Warning 100 = VLDO_1.8V LDO Power Good 101 = High Current Consumption Warning 110 = Reserved 111 = Current Limiter Warning

R36 – Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R36 [7:0] : Reserved

R37 – DIMM Vendor Region Password Lower Byte			
Bits	**Attribute**	**Default**	**Description**
7:0	WO	01110011	R37 [7:0] : DIMM_VENDOR_MEMORY_REGION_PASSWORD_LOWER_BYTE DIMM Vendor Memory Region (R40 to R6F) Password – Lower Byte [7:0] = Code

R38 – DIMM Vendor Region Password Upper Byte			
Bits	**Attribute**	**Default**	**Description**
7:0	WO	10010100	R38 [7:0] : DIMM_VENDOR_MEMORY_REGION_PASSWORD_UPPER_BYTE DIMM Vendor Memory Region (R40 to R6F) Password – Upper Byte [7:0] = Code

R39 – DIMM Vendor Password Control			
Bits	**Attribute**	**Default**	**Description**
7:0	RW	0	Host Region Codes: 0x74: Clear Registers R04 to R07, Erase MTP memory for R04 Register. DIMM Vendor Region (R40 to R6F) Write Codes: 0x00: Lock DIMM Vendor Region. 0x40: Unlock DIMM Vendor Region. Password needs to be present in R37 & R38 registers. 0x80: Burn DIMM Vendor Region Password. New password needs to be present in R37 & R38. 0x81: Burn DIMM Vendor Region – R40 to R4F 0x82: Burn DIMM Vendor Region – R50 to R5F 0x85: Burn DIMM Vendor Region – R60 to R6F DIMM Vendor Region (R40 to R6F) Read Codes: 0x5A: Burning is complete in DIMM Vendor region.

R3A – Default Address Pointer			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R3A [7]: Reserved
6	RW	0	R3A [6]: DEFAULT_READ_ADDRESS_POINTER_ENABLE Enable Default Address Read Pointer when PMIC sees STOP operation 0 = Disable Default Address Pointer (address pointer is set by Host) 1 = Enable Default Address Pointer; Address selected by register bits [5:4]
5:4	RW	0	R3A [5:4]: DEFAULT_READ_STARTING_ADDRESS Default Read Address Pointer Selection when PMIC sees STOP operation 00 = R08 01 = R0C 10 = Reserved 11 = Reserved
3:2	RW	0	R3A [3:2]: BURST_LENGTH_FOR_READ_DEFAULT_ADDR_POINTER Burst Length (# of Bytes) to be transferred for Read Default Address Pointer Mode 00 = 2 Bytes 01 = 4 Bytes 10 = Reserved 11 = 16 Bytes
1:0	RV	0	R3A [1:0]: Reserved

R3B – Revision ID, PMIC Current Capability Selection			
Bits	**Attribute**	**Default**	**Description**
7:6	ROE	0	R3B [7:6]: PMIC_PART_CAPABILITY_EXT PMIC Current Capability Extension. This register bits [7:6] and bit [0] provides 3 bit encoding as following: 000 = Small PMIC (Low Current) 001 = Big PMIC (High Current) 01x = Extreme PMIC (Highest Current) All other encodings are reserved.
5:4	ROE	10	R3B [5:4] : REVISION_ID_MAJOR_STEPPING Major Revision Stepping 00 = Revision 1 01 = Revision 2 10 = Revision 3 11 = Revision 4
3:1	ROE	101	R3B [3:1] : REVISION_ID_MINOR_STEPPING Minor Revision Stepping 000 = Revision 0 001 = Revision 1 010 = Revision 2 011 = Revision 3 All other encodings are reserved.
0	ROE	0	R3B [0] : PMIC_PART_CAPABILITY PMIC Current Capability 0 = Small PMIC (Low Current) 1 = Big PMIC (High Current)

R3C – Vendor ID			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	10001010	R3C [7:0] : VENDOR_ID_BANK_SELECTION Vendor Identification Register Bank Number. This is a fixed register. The code is a JEDEC standard for vendor.

R3D – Vendor ID			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	10001100	R3D [7:0] : VENDOR_ID_BYTE1 Vendor Identification Register Byte 1. This is a fixed register. The code is a JEDEC standard for vendor.

R3E – Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R3E [7:0] : Reserved

R3F – Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	1	R3F [7:0] : Reserved

A-6 DIMM Vendor Region Registers

R40 – Power-On Sequence Configuration 0			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R40 [7] : POWER_ON_SEQUENCE_CONFIG0 PMIC Power-On Sequence Config0 0 = Do Not Execute Config0 1 = Execute Config0
6	RWPE	0	R40 [6] : POWER_ON_SEQUENCE_CONFIG0_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable SWA Output 1 = Enable SWA Output
5	RWPE	0	R40 [5] : POWER_ON_SEQUENCE_CONFIG0_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable SWB Output 1 = Enable SWB Output
4	RWPE	0	R40 [4] : POWER_ON_SEQUENCE_CONFIG0_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable SWC Output 1 = Enable SWC Output
3	RWPE	1	R40 [3] : POWER_ON_SEQUENCE_CONFIG0_SWD_ENABLE Enable Switch Node D Output Regulator. 0 = Disable SWD Output 1 = Enable SWD Output
2:0	RWPE	001	R40 [2:0] : POWER_ON_SEQUENCE_CONFIG0_IDLE Idle time after Power-On Sequence Config0 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

R41 – Power-On Sequence Configuration 1			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R41 [7] : POWER_ON_SEQUENCE_CONFIG1 PMIC Power-On Sequence Config1 0 = Do Not Execute Config1 1 = Execute Command
6	RWPE	1	R41 [6] : POWER_ON_SEQUENCE_CONFIG1_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable SWA Output 1 = Enable SWA Output
5	RWPE	1	R41 [5] : POWER_ON_SEQUENCE_CONFIG1_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable SWB Output 1 = Enable SWB Output
4	RWPE	1	R41 [4] : POWER_ON_SEQUENCE_CONFIG1_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable SWC Output 1 = Enable SWC Output
3	RWPE	1	R41 [3] : POWER_ON_SEQUENCE_CONFIG1_SWD_ENABLE Enable Switch Node D Output Regulator. 0 = Disable SWD Output 1 = Enable SWD Output
2:0	RWPE	001	R41 [2:0] : POWER_ON_SEQUENCE_CONFIG1_IDLE Idle time after Power-On Sequence Config1 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

R42 – Power-On Sequence Configuration 2			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R42 [7] : POWER_ON_SEQUENCE_CONFIG2 PMIC Power-On Sequence Config2 0 = Do Not Execute Config2 1 = Execute Config2
6	RWPE	1	R42 [6] : POWER_ON_SEQUENCE_CONFIG2_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable SWA Output 1 = Enable SWA Output
5	RWPE	1	R42 [5] : POWER_ON_SEQUENCE_CONFIG2_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable SWB Output 1 = Enable SWB Output
4	RWPE	1	R42 [4] : POWER_ON_SEQUENCE_CONFIG2_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable SWC Output 1 = Enable SWC Output
3	RWPE	1	R42 [3] : POWER_ON_SEQUENCE_CONFIG2_SWD_ENABLE Enable Switch Node D Output Regulator. 0 = Disable SWD Output 1 = Enable SWD Output
2:0	RWPE	000	R42 [2:0] : POWER_ON_SEQUENCE_CONFIG2_IDLE Idle time after Power-On Sequence Config2 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

R43 – Power-On Sequence Configuration 3			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R43 [7] : POWER_ON_SEQUENCE_CONFIG3 PMIC Power-On Sequence Config3 0 = Do Not Execute Config3 1 = Execute Config3
6	RWPE	1	R43 [6] : POWER_ON_SEQUENCE_CONFIG3_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RWPE	1	R43 [5] : POWER_ON_SEQUENCE_CONFIG3_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
4	RWPE	1	R43 [4] : POWER_ON_SEQUENCE_CONFIG3_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
3	RWPE	1	R43 [3] : POWER_ON_SEQUENCE_CONFIG3_SWD_ENABLE Enable Switch Node D Output Regulator. 0 = Disable Switch Node D Output Regulator 1 = Enable Switch Node D Output Regulator
2:0	RWPE	000	R43 [2:0] : POWER_ON_SEQUENCE_CONFIG3_IDLE Idle time after Power-On Sequence Config3 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

R44 – Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R44 [7:0]: Reserved

R45 – SWA Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	R45 [7:1]: SWA_VOLTAGE_SETTING Switch Node A Output Regulator Voltage Setting 000 0000 = 800mV or 600mV 000 0001 = 805mV or 605mV 000 0010 = 810mV or 610mV … 011 1100 = 1100mV or 900mV … 111 1101 = 1425mV or 1225mV 111 1110 = 1430mV or 1230mV 111 1111 = 1435mV or 1235mV
0	RWPE	0	R45 [0] : SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register R45” [7:1] 1 = –7.5% from the setting in “Register R45” [7:1]

R46 – SWA Threshold, Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R46 [7:6] : SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R45” [7:1] 01 = +7.5% from the setting in “Register R45” [7:1] 10 = +10% from the setting in “Register R45” [7:1] 11 = +3% from the setting in “Register R45” [7:1]
5:4	RWPE	10	R46 [5:4] : SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Over-Voltage Status 00 = +7.5% from the setting in “Register R45” [7:1] 01 = +10% from the setting in “Register R45” [7:1] 10 = +12.5% from the setting in “Register R45” [7:1] 11 = +5% from the setting in “Register R45” [7:1]
3:2	RWPE	00	R46 [3:2] : SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Under-Voltage Lockout Status 00 = –10% from the setting in “Register R45” [7:1] 01 = –12.5% from the setting in “Register R45” [7:1] 10 = –5% from the setting in “Register R45” [7:1] 11 = –7.5% from the setting in “Register R45” [7:1]
1:0	RWPE	00	R46 [1:0] : SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

R47 – SWB Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	R47 [7:1]: SWB_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting 000 0000 = 800mV or 600mV 000 0001 = 805mV or 605mV 000 0010 = 810mV or 610mV … 011 1100 = 1100mV or 900mV … 111 1101 = 1425mV or 1225mV 111 1110 = 1430mV or 1230mV 111 1111 = 1435mV or 1235mV
0	RWPE	0	R47 [0] : SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register R47” [7:1] 1 = –7.5% from the setting in “Register R47” [7:1]

R48 – SWB Threshold, Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R48 [7:6] : SWB_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R47” [7:1] 01 = +7.5% from the setting in “Register R47” [7:1] 10 = +10% from the setting in “Register R47” [7:1] 11 = +3% from the setting in “Register R47” [7:1]
5:4	RWPE	10	R48 [5:4] : SWB_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Over-Voltage Status 00 = +7.5% from the setting in “Register R47” [7:1] 01 = +10% from the setting in “Register R47” [7:1] 10 = +12.5% from the setting in “Register R47” [7:1] 11 = +5% from the setting in “Register R47” [7:1]
3:2	RWPE	00	R48 [3:2] : SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Under-Voltage Lockout Status 00 = –10% from the setting in “Register R47” [7:1] 01 = –12.5% from the setting in “Register R47” [7:1] 10 = –5% from the setting in “Register R47” [7:1] 11 = –7.5% from the setting in “Register R47” [7:1]
1:0	RWPE	00	R48 [1:0] : SWB_OUTPUT_SOFT_STOP_TIME SWB Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

R49 – SWC Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	R49 [7:1]: SWC_VOLTAGE_SETTING Switch Node C Output Regulator Voltage Setting 000 0000 = 800mV or 600mV 000 0001 = 805mV or 605mV 000 0010 = 810mV or 610mV … 011 1100 = 1100mV or 900mV … 111 1101 = 1425mV or 1225mV 111 1110 = 1430mV or 1230mV 111 1111 = 1435mV or 1235mV
0	RWPE	0	R49 [0] : SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register R49” [7:1] 1 = –7.5% from the setting in “Register R49” [7:1]

R4A – SWC Threshold, Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R4A [7:6] : SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R49” [7:1] 01 = +7.5% from the setting in “Register R49” [7:1] 10 = +10% from the setting in “Register R49” [7:1] 11 = +3% from the setting in “Register R49” [7:1]
5:4	RWPE	10	R4A [5:4] : SWC_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Over-Voltage Status 00 = +7.5% from the setting in “Register R49” [7:2] 01 = +10% from the setting in “Register R49” [7:1] 10 = +12.5% from the setting in “Register R49” [7:1] 11 = +5% from the setting in “Register R49” [7:1]
3:2	RWPE	00	R4A [3:2] : SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Under-Voltage Lockout Status 00 = –10% from the setting in “Register R49” [7:1] 01 = –12.5% from the setting in “Register R49” [7:1] 10 = –5% from the setting in “Register R49” [7:1] 11 = –7.5% from the setting in “Register R49” [7:1]
1:0	RWPE	00	R4A [1:0] : SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

R4B – SWD Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	R4B [7:1] : SWD_VOLTAGE_SETTING Switch Node D Output Regulator Voltage Setting 000 0000 = 1500mV 2200mV 000 0001 = 1505mV 2205mV 000 0010 = 1510mV 2210mV … … 011 1100 = 1800mV 2500mV … … 111 1101 = 2125mV 2825mV 111 1110 = 2130mV 2830mV 111 1111 = 2135mV 2835mV
0	RWPE	0	R4B [0]: SWD_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node D Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register R4B” [7:1] 1 = –7.5% from the setting in “Register R4B” [7:1]

R4C – SWD Threshold, Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R4C [7:6] : SWD_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node D Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R4B” [7:1] 01 = +7.5% from the setting in “Register R4B” [7:1] 10 = +10% from the setting in “Register R4B” [7:1] 11 = +3% from the setting in “Register R4B” [7:1]
5:4	RWPE	10	R4C [5:4] : SWD_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node D Output Regulator Threshold For Over-Voltage Status 00 =+7.5% from the setting in “Register R4B” [7:1] 01 = +10% from the setting in “Register R4B” [7:1] 10 = +12.5% from the setting in “Register R4B” [7:1] 11 = +5% from the setting in “Register R4B” [7:1]
3:2	RWPE	00	R4C [3:2] : SWD_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node D Output Regulator Threshold For Under-Voltage Lockout Status 00 = –10% from the setting in “Register R4B” [7:1] 01 = –12.5% from the setting in “Register R4B” [7:1] 10 = –5% from the setting in “Register R4B” [7:1] 11 = –7.5% from the setting in “Register R4B” [7:1]
1:0	RWPE	00	R4C [1:0] : SWD_OUTPUT_SOFT_STOP_TIME SWD Output Regulator Soft-Stop Time After VR Disable 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

R4D – SW[A:B] FSW and Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	10	R4D [7:6] : SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
5:4	RWPE	01	R4D [5:4]: SWA_SWITCHING_FREQ [1] Switch Node A Output Regulator Switching Frequency 00 = 500kHz 01 = 750kHz 10 = 1000kHz 11 = 1250kHz
3:2	RWPE	10	R4D [3:2] : SWB_MODE_SELECT Switch Node B Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
1:0	RWPE	01	R4D [1:0]: SWB_SWITCHING_FREQ [2] Switch Node B Output Regulator Switching Frequency 00 = 500kHz 01 = 750kHz 10 = 1000kHz 11 = 1250kHz

[1] The typical switching frequency for RTQ5119A's SWA are summarized as below :

as 0x4D"[5:4] = "00" → Typ. f_{SW} = 450kHz; as 0x4D"[5:4] = "01" → Typ. f_{SW} = 670kHz;

as 0x4D"[5:4] = "10" → Typ. f_{SW} = 890kHz; as 0x4D"[5:4] = "11" → Typ. f_{SW} = 1110kHz

[2] The typical switching frequency for RTQ5119A's SWB are summarized as below :

as 0x4D"[1:0] = "00" → Typ. f_{SW} = 450kHz; as 0x4D"[1:0] = "01" → Typ. f_{SW} = 670kHz;

as 0x4D"[1:0] = "10" → Typ. f_{SW} = 890kHz; as 0x4D"[1:0] = "11" → Typ. f_{SW} = 1110kHz

R4E – SW[C:D] FSW and Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	10	R4E [7:6] : SWC_MODE_SELECT Switch Node C Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
5:4	RWPE	01	R4E [5:4]: SWC_SWITCHING_FREQ [1] Switch Node C Output Regulator Switching Frequency 00 = 500kHz 01 = 750kHz 10 = 1000kHz 11 = 1250kHz
3:2	RWPE	10	R4E [3:2] : SWD_MODE_SELECT Switch Node D Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
1:0	RWPE	10	R4E [1:0]: SWD_SWITCHING_FREQ Switch Node D Output Regulator Switching Frequency 00 = 500kHz 01 = 750kHz 10 = 1000kHz 11 = 1250kHz

[1] The typical switching frequency for RTQ5119A's SWC are summarized as below :

as 0x4E"[5:4] = "00" → Typ. f_{SW} = 450kHz; as 0x4E"[5:4] = "01" → Typ. f_{SW} = 670kHz;

as 0x4E"[5:4] = "10" → Typ. f_{SW} = 890kHz; as 0x4E"[5:4] = "11" → Typ. f_{SW} = 1110kHz

R4F – Switch Control and Sense			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	R4F [7] : OUTPUT_REGULATORS_DISABLE_CONTROL Output Regulator SWA, SWB, SWC and SWD Disable Control for OV, UV and OC. 0 = Disable all switching regulators of PMIC 1 = Disable only the effected switching output regulator; Rest of the PMIC's switching regulators remains operations
6:5	RWPE	0	R4F [6:5] : Reserved
4	RWPE	1	R4F [4] : SWA_OUTPUT_REGULATOR_REMOTE_SENSING SWA Output Regulator Remote Sensing Scheme on DIMM 0 = Single Ended Remote Sensing on DIMM. 1 = Differential Remote Sensing on DIMM
3	RV	0	R4F [3] : Reserved
2	RWPE	1	R4F [2] : SWC_OUTPUT_REGULATOR_REMOTE_SENSING SWC Output Regulator Remote Sensing Scheme on DIMM 0 = Single Ended Remote Sensing on DIMM. 1 = Differential Remote Sensing on DIMM
1	RWPE	1	R4F [1] : SWD_OUTPUT_REGULATOR_REMOTE_SENSING SWD Output Regulator Remote Sensing Scheme on DIMM 0 = Single Ended Remote Sensing on DIMM; Use SWD_FB_N pin as PID input pin to determine the PMIC's ID. 1 = Differential Remote Sensing on DIMM.
0	RWPE	1	R4F [0] : SWA_SWB_PHASE_MODE_SELECT Switch Node A and Switch Node B Phase Regulator Mode Selection. 0 = Single Phase Regulator Mode 1 = Dual Phase Regulator Mode

R50 – SW[A:D] Current Limited Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	10	R50 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_THRESHOLD_SETTING Switch Node A Output Current Limiter Threshold Setting Low Current PMIC Encoding Definition For COT Mode, Ivalley_limit: 00 = 2.5A 01 = 3.0A 10 = 3.5A 11 = 4.0A
5:4	RWPE	10	R50 [5:4]: SWB_OUTPUT_CURRENT_LIMITER_THRESHOLD_SETTING Switch Node B Output Current Limiter Threshold Setting Low Current PMIC Encoding Definition For COT Mode, Ivalley_limit: 00 = 2.5A 01 = 3.0A 10 = 3.5A 11 = 4.0A
3:2	RWPE	10	R50 [3:2]: SWC_OUTPUT_CURRENT_LIMITER_THRESHOLD_SETTING Switch Node C Output Current Limiter Threshold Setting Low Current PMIC Encoding Definition For COT Mode, Ivalley_limit: 00 = 2.5A 01 = 3.0A 10 = 3.5A 11 = 4.0A
1:0	RWPE	10	R50 [1:0]: SWD_OUTPUT_CURRENT_LIMITER_THRESHOLD_SETTING Switch Node D Output Current Limiter Threshold Setting Low Current PMIC Encoding Definition For COT Mode, Ivalley_limit: 00 = 2.5A 01 = 3.0A 10 = 3.5A 11 = 4.0A

R51 – Voltage Setting for LDO_1.8V & LDO_1.0V & SW[A:D] Output Voltage Range			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R51 [7:6] : VLDO_1.8V_VOLTAGE_SETTING VOUT 1.8V LDO Output Voltage Setting 00 = 1.7V 01 = 1.8V 10 = 1.9V 11 = Reserved
5	RWPE	0	R51 [5]: SWA_VOLTAGE_RANGE SWA Output Voltage Range Selection 0 = Range: 800mV to 1435mV for SWA; 5mV step size. 1 = Range: 600mV to 1235mV for SWA; 5mV step size
4	RWPE	0	R51 [4]: SWB_VOLTAGE_RANGE SWB Output Voltage Range Selection 0 = Range: 800mV to 1435mV for SWB; 5mV step size 1 = Range: 600mV to 1235mV for SWB; 5mV step size
3	RWPE	0	R51 [3]: SWC_VOLTAGE_RANGE SWC Output Voltage Range Selection 0 = Range: 800mV to 1435mV for SWC; 5mV step size 1 = Range: 600mV to 1235mV for SWC; 5mV step size
2:1	RWPE	01	R51 [2:1] : VLDO_1.0V_VOLTAGE_SETTING VOUT 1.0V LDO Voltage Setting 00 = 0.9V 01 = 1.0V 10 = 1.1V 11 = 1.2V
0	RWPE	0	R51 [0]: SWD_VOLTAGE_RANGE SWD Output Voltage Range Selection 0 = Range: 1500mV to 2135mV for SWD; 5mV step size 1 = Range: 2200mV to 2835mV for SWD; 5mV step size

R52-R57 – Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R52 [7:0] – R57 [7:0]: Reserved

R58 – Power-Off Sequence Configuration 0			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R58 [7] : POWER_OFF_SEQUENCE_CONFIG0 PMIC Power-Off Sequence Config0 0 = Do Not Execute Config0 1 = Execute Config0
6	RWPE	1	R58 [6] : POWER_OFF_SEQUENCE_CONFIG0_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RWPE	1	R58 [5] : POWER_OFF_SEQUENCE_CONFIG0_SWB_DISABLE Disable Switch Node B Output Regulator. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
4	RWPE	1	R58 [4] : POWER_OFF_SEQUENCE_CONFIG0_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
3	RWPE	0	R58 [3] : POWER_OFF_SEQUENCE_CONFIG0_SWD_DISABLE Disable Switch Node D Output Regulator. 0 = Do Not Disable Switch Node D Output Regulator 1 = Disable Switch Node D Output Regulator
2:0	RWPE	0	R58 [2:0] : POWER_OFF_SEQUENCE_CONFIG0_IDLE Idle time after Power-Off Sequence Config0 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

R59 – Power-Off Sequence Configuration 1			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R59 [7] : POWER_OFF_SEQUENCE_CONFIG1 PMIC Power-Off Sequence Config1 0 = Do Not Execute Config1 1 = Execute Config1
6	RWPE	1	R59 [6] : POWER_OFF_SEQUENCE_CONFIG1_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RWPE	1	R59 [5] : POWER_OFF_SEQUENCE_CONFIG1_SWB_DISABLE Disable Switch Node B Output Regulator. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
4	RWPE	1	R59 [4] : POWER_OFF_SEQUENCE_CONFIG1_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
3	RWPE	1	R59 [3] : POWER_OFF_SEQUENCE_CONFIG1_SWD_DISABLE Disable Switch Node D Output Regulator. 0 = Do Not Disable Switch Node D Output Regulator 1 = Disable Switch Node D Output Regulator
2:0	RWPE	0	R59 [2:0] : POWER_OFF_SEQUENCE_CONFIG1_IDLE Idle time after Power-Off Sequence Config1 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

R5A – Power-Off Sequence Configuration 2			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R5A [7] : POWER_OFF_SEQUENCE_CONFIG2 PMIC Power-Off Sequence Config2 0 = Do Not Execute Config2 1 = Execute Config2
6	RWPE	1	R5A [6] : POWER_OFF_SEQUENCE_CONFIG2_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RWPE	1	R5A [5] : POWER_OFF_SEQUENCE_CONFIG2_SWB_DISABLE Disable Switch Node B Output Regulator. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
4	RWPE	1	R5A [4] : POWER_OFF_SEQUENCE_CONFIG2_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
3	RWPE	1	R5A [3] : POWER_OFF_SEQUENCE_CONFIG2_SWD_DISABLE Disable Switch Node D Output Regulator. 0 = Do Not Disable Switch Node D Output Regulator 1 = Disable Switch Node D Output Regulator
2:0	RWPE	0	R5A [2:0] : POWER_OFF_SEQUENCE_CONFIG2_IDLE Idle time after Power-Off Sequence Config2 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

R5B – Power-Off Sequence Configuration 3			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R5B [7] : POWER_OFF_SEQUENCE_CONFIG3 PMIC Power-Off Sequence Config3 0 = Do Not Execute Config3 1 = Execute Config3
6	RWPE	1	R5B [6] : POWER_OFF_SEQUENCE_CONFIG3_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RWPE	1	R5B [5] : POWER_OFF_SEQUENCE_CONFIG3_SWB_DISABLE Disable Switch Node B Output Regulator. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
4	RWPE	1	R5B [4] : POWER_OFF_SEQUENCE_CONFIG3_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
3	RWPE	1	R5B [3] : POWER_OFF_SEQUENCE_CONFIG3_SWD_DISABLE Disable Switch Node D Output Regulator. 0 = Do Not Disable Switch Node D Output Regulator 1 = Disable Switch Node D Output Regulator
2:0	RV	0	R5B [2:0] : Reserved

R5C – Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R5C [7:0] : Reserved

R5D – SW[A:B] Soft-Start and STOP Time			
Bits	**Attribute**	**Default**	**Description**
7:5	RWPE	001	R5D [7:5] : SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms … 111 = 14ms
4	RV	0	R5D [4] : Reserved
3:1	RWPE	001	R5D [3:1] : SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms … 111 = 14ms
0	RV	0	R5D [0] : Reserved

R5E – SW[C:D] Soft-Start and STOP Time			
Bits	**Attribute**	**Default**	**Description**
7:5	RWPE	001	R5E [7:5] : SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms … 111 = 14ms
4	RV	0	R5E [4] : Reserved
3:1	RWPE	001	R5E [3:1] : SWD_OUTPUT_SOFT_START_TIME SWD Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms … 111 = 14ms
0	RV	0	R5E [0] : Reserved

B. I²C and I³C Basic Interface Operation

At power on, by default, the RTQ5119A comes up in legacy I²C mode of operation. Following applies in I²C mode:

(1) The max operation speed is limited to 1MHz.

(2) In-band interrupts are not supported.

(3) Bus reset is supported.

(4) Parity check is not supported except for supported CCCs.

(5) Packet error check is not supported.

The RTQ5119A operates in the legacy I²C mode until put into I³C Basic mode via command. The user can put the RTQ5119A in I³C Basic mode by issuing SETAASA CCC.

Following applies in I³C Basic mode:

(1) The max operation speed is up to 12.5MHz.

(2) In-band interrupts are supported.

(3) Bus reset is supported.

(4) Parity check is always enabled by default.

(5) Packet error check is supported and by default is disabled.

B-1. I²C Slave Protocol

The RTQ5119A operates on a standard I²C serial interface. Transactions where the RTQ5119A is the targeted slave device begin with the Host issuing a START condition followed by a 7-bit PMIC device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the RTQ5119A typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK.

(1) Write Operation – Data Packet

Table 12. Write Command Data Packet

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	X	0	X	HID			W=0	A	
	Address[7:0]								A	
	Data								A	
	…								A	
	Data								A	P

(2) Read Operation – Data Packet

Table 13. Read Command Data Packet

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	X	0	X	HID			W=0	A	
	Address[7:0]								A	
Sr	1	X	0	X	HID			R=1	A	
	Data								A	
	…								A	
	Data								N	P

(3) Default Read Address Pointer Mode

During normal operation of the DDR5 DIMM, the host periodically may poll critical information from the same location. An example may be the RTQ5119A's status registers or current or power measurement register readout. To help improve the efficiency of the I^2C bus protocol, the RTQ5119A offers a default read address pointer mode so that whenever the RTQ5119A sees the STOP operation on its SCL and SDA bus, its read address pointer is always reset to default address. The default read pointer address mode is enabled through "Register 0x3A" [6] and default starting address for read operation is selectable through "Register 0x3A" [5:4]. This allows host to read the read command data packet as shown in Table 14. The default read address pointer reduces the packet overhead by 2 bytes. The host typically enables this mode at last after VR Enable command when the normal operation of the DDR5 DIMM begins.

Table 14. Read Command Data Packet with Default Address Pointer Mode

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	X	0	X	HID			R=1	A	
	Data								A	
	…								A	
	Data								N	P

B-2. I^3C Basic Slave Protocol

The RTQ5119A operates on a standard I^3C Basic serial interface. Transactions where the RTQ5119A is the targeted slave device begin with the Host issuing a START condition followed by a 7-bit PMIC device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the RTQ5119A typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See Table 15. The "T" bit carries Parity information from the Host for each byte.

The Packet Error Code (PEC) function is disabled by default when the RTQ5119A is put in I^3C Basic mode. The host may optionally enable this function through DEVCTRL CCC. If enabled, the PEC is appended at the end of all transactions. If PEC is enabled, the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length pre-maturely for Write operation.

(1) Write Operation – Data Packet

Table 15. Write Command Data Packet; PEC Disabled

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A	
	Address[7:0]								T	
	Data								T	
	…								T	
	Data								T	Sr or P

Table 16. Write Command Data Packet; PEC Enabled

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A	
	Address[7:0]								T	
	CMD			W=0	0000				T	
	Data								T	
	…								T	
	Data								T	
	PEC								T	Sr or P

The host may optionally allow RTQ5119A to request IBI. For this case, the transactions to the RTQ5119A begin with the I^3C host issuing a START condition followed by 7'h7E and then write bit. If RTQ5119A has a pending IBI, it transmits its 7-bit device select code followed by R=1. If RTQ5119A has no pending IBI, there is no action taken by PMIC. The Table 17 & Table 18 shows the I^3C Basic bus write command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in Table 18 PEC calculation does not include IBI header byte (7'h7E followed by W=0).

Table 17. Write Command Data Packet with IBI Header; No Pending IBI, PEC Disabled

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A	
Sr	1	X	0	X	HID			W=0	A	
	Address[7:0]								T	
	Data								T	
	…								T	
	Data								T	Sr or P

Table 18. Write Command Data Packet with IBI Header; No Pending IBI, PEC Enabled

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A	
Sr	1	X	0	X	HID			W=0	A	
	Address[7:0]								T	
	CMD			W=0	0000				T	
	Data								T	
	…								T	
	Data								T	
	PEC								T	Sr or P

(2) Read Operation – Data Packet

Table 19. Read Command Data Packet; PEC Disabled

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A	
	Address[7:0]								T	
Sr	1	X	0	X	HID			R=1	A/N	
	Data								T=1	
	…								T=1	
	Data								T=1	Sr or P

Table 20. Read Command Data Packet; PEC Enabled

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A	
	Address[7:0]								T	
	CMD			R=1	0000				T	
	PEC								T	
Sr	1	X	0	X	HID			R=1	A/N	
	Data								T=1	
	…								T=1	
	Data								T=1	
	PEC								T=0	Sr or P

The host may optionally allow RTQ5119A to request IBI. For this case, the transactions to the RTQ5119A begin with the I^3C Basic host issuing a START condition followed by 7'h7E and then write bit. If RTQ5119A has a pending IBI, it transmits its 7-bit device select code followed by R=1. If RTQ5119A has no pending IBI, there is no action taken by PMIC. The Table 21 & Table 22 shows the I^3C Basic bus read command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in Table 22, PEC calculation does not include IBI header

byte (7'h7E followed by W=0).

Table 21. Read Command Data Packet with IBI Header; No Pending IBI, PEC Disabled

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A	
Sr	1	X	0	X	HID			W=0	A	
	Address[7:0]								T	
Sr	1	X	0	X	HID			R=1	A/N	
	Data								T=1	
	…								T=1	
	Data								T=1	Sr or P

Table 22. Read Command Data Packet with IBI Header; No Pending IBI, PEC Enabled

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A	
Sr	1	X	0	X	HID			W=0	A	
	Address[7:0]								T	
	CMD			R=1	0000				T	
	PEC								T	
Sr	1	X	0	X	HID			R=1	A/N	
	Data								T=1	
	…								T=1	
	Data								T=1	
	PEC								T=0	Sr or P

(3) Default Read Address Pointer Mode

This mode works the same exact way as explained in I^2C slave protocol section. Table 23 and Table 24 shows the read command data packet for PEC function disabled and enabled respectively. When PEC function is enabled, "Register 0x3A" [3:2] sets the number of bytes that RTA5119A sends out followed by the PEC calculation. If PEC is enabled, the host must complete the burst length as indicated in "Register 0x3A" [3:2] register. In other words, the host must not interrupt the burst length pre-maturely for default address pointer read operation.

Table 23. Read Command Data Packet with Read Address Pointer Mode; PEC Disabled

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	X	0	X	HID			R=1	A	
	Data								T=1	
	…								T=1	
	Data								T=1	Sr or P

Table 24. Read Command Data Packet with Read Address Pointer Mode; PEC Enabled

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	X	0	X	HID			R=1	A	
	Data								T=1	
	…								T=1	
	Data								T=1	
	PEC								T=0	Sr or P

Table 25. Read Command Data Packet with Read Address Pointer & IBI Header; No Pending IBI; PEC Disabled

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S	1	1	1	1	1	1	0	W=0	A	
Sr	1	X	0	X	HID			R=1	A/N	
	Data								T=1	
	…								T=1	
	Data								T=1	Sr or P

Table 26. Read Command Data Packet with Read Address Pointer & IBI Header; No Pending IBI; PEC Enabled

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S	1	1	1	1	1	1	0	W=0	A	
Sr	1	X	0	X	HID			R=1	A/N	
	Data								T=1	
	…								T=1	
	Data								T=1	
	PEC								T=0	Sr or P

B-3. In Band Interrupt (IBI)

By default, IBI function is disabled. The RTQ5119A enables the IBI when it registers ENEC CCC. Once enabled, the RTQ5119A sends an IBI when an event occurs. In I^2C mode, in band interrupt function is not supported. Only I^3C Basic mode supports in band interrupt function.

Event interrupts may be generated by the local device if IBI is enabled. When there is a pending interrupt (i.e “Register 0x0A” [1] = ‘1’) and if IBI is enabled (i.e. “Register 0x34” [6] = ‘1’) the RTQ5119A requests an interrupt after detecting START condition by transmitting its 7-bit binary address (LID bits followed by HID bits) followed by R/W = ‘1’ on the SDA bus serially (synchronized by SCL falling transitions). If RTQ5119A detects no START condition but if the I^3C bus (SDA and SCL) has been inactive (no edges seen) for tAVAL period (min. = 1μsec), then RTQ5119A asserts SDA low by tIBI_ISSUE time (max. = 15μsec) to request an interrupt. When the RTQ5119A requests an interrupt, the Host toggles the SCL. The RTQ5119A transmits its 7-bit binary address (LID bits followed by HID bits) followed by R/W bit = ‘1’ to the Host.

When the RTQ5119A requests an interrupt, the host may take one of the two actions below.

(1) The Host sends ACK on 9th bit to accept the interrupt request.

At this point, if the RTQ5119A confirms that it has won the arbitration, the RTQ5119A transmits the IBI payload as shown in Table 27 and Table 28 for PEC disabled and PEC enabled configuration respectively. The interrupt payload contains MDB followed by “Register 0x08”, “Register 0x09”, “Register 0x0A”, “Register 0x0B” & “Register 0x33” bytes. The host then issues the STOP command. The host can interrupt the IBI payload at T bit. If host stops the IBI payload at T bit in the middle of payload, the RTQ5119A retains the IBI status flag (“Register 0x0A” [1]) and Pending Interrupt Bits [3:0] internally and waits for the next opportunity to request an interrupt. If the RTQ5119A successfully transmits the entire IBI payload, it then clears IBI status flag (“Register 0x0A” [1] = ‘0’) and Pending Interrupt Bits [3:0] = ‘0000’ on its own and does not request for an IBI again unless there is another different event occurs; for another same event, the device does not request for an IBI.

(2) The Host sends NACK on the 9th bit followed by a STOP command.

In this case, the RTQ5119A does not transmit the IBI payload and waits for the next opportunity to request an interrupt. At this point, though Host sent an NACK, it does have a knowledge of which RTQ5119A sent the IBI request. The RTQ5119A retains the IBI status flag (“Register 0x0A” [1] = ‘1’) and Pending Interrupt Bits [3:0] = ‘0001’.

Table 27. Slave Device (RTQ5119A) IBI Payload Packet; PEC Disabled

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S	1	X	0	X	HID			R=1	A/N	
	MDB = 0x00								T=1	
	R08 [7:0]								T=1	
	R09 [7:0]								T=1	
	R0A [7:0]								T=1	
	R0B [7:0]								T=1	
	R33 [7:0]								T=0	P

Table 28. Slave Device (RTQ5119A) IBI Payload Packet; PEC Enabled

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S	1	X	0	X	HID			R=1	A/N	
	MDB = 0x00								T=1	
	R08 [7:0]								T=1	
	R09 [7:0]								T=1	
	R0A [7:0]								T=1	
	R0B [7:0]								T=1	
	R33 [7:0]								T=1	
	PEC								T=0	P

B-4. I3C Basic Common Command Codes (CCC)

The RTQ5119A supports CCC as listed in Table 29 below. The RTQ5119A NACKs for all unsupported CCC.

Table 29. RTQ5119A Supported CCC

CCC	Mode	Code	I2C / I3C Mode	Description
ENEC	Broadcast	0x00	I3C	Enable Event Interrupts
	Direct	0x80	I3C	
DISEC	Broadcast	0x01	I3C	Disable Event Interrupts
	Direct	0x81	I3C	
RSTDAA	Broadcast	0x06	I3C	Put the device in I2C Mode
SETAASA	Broadcast	0x29	I2C	Put the device in I3C Basic Mode
GETSTATUS	Direct	0x90	I3C	Get Device Status
DEVCAP	Direct	0xE0	I3C	Get Device Capability
SETHID	Broadcast	0x61	I2C	Set the device HID
DEVCTRL	Broadcast	0x62	I2C/I3C	Set the device configuration

(1) ENEC CCC

The ENEC CCC is only supported after RTQ5119A is put in I3C Basic mode. In I2C mode, it is illegal for host to issue this CCC. When ENEC CCC is registered by the RTQ5119A, it updates “Register 0x34” [6] = ‘1’ and it takes in effect at the next Start operation (i.e. after STOP operation). Table 30 to Table 33 shows an example of a single ENEC CCC. Table 34 shows the encoding definition for ENEC CCC. If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7’h7E with W=0 byte in PEC calculation.

Table 30. ENEC CCC – Broadcast

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x00 (Broadcast)								T	
	0x00							ENINT	T	Sr or P

Table 31. ENEC CCC – Broadcast with PEC

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x00 (Broadcast)								T	
	0x00							ENINT	T	
	PEC								T	Sr or P

Table 32. ENEC CCC – Direct

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x80 (Direct)								T	
Sr	DevID [6:0]							W=0	A	
	0x00							ENINT	T	Sr or P

Table 33. ENEC CCC – Direct with PEC

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x80 (Direct)								T	
	PEC								T	
Sr	DevID [6:0]							W=0	A	
	0x00							ENINT	T	
	PEC								T	Sr or P

Table 34. ENEC CCC Byte Encoding

Bit	Encoding	Notes
ENINT	0 = No Action 1 = Enable IBI Interrupt	It is illegal for Host to issue ENEC CCC with ENINT bit = ‘0’

(2) DISEC CCC

The DISEC CCC is only supported after RTQ5119A is put in I^3C Basic mode. In I^2C mode, it is illegal for host to issue this CCC. When DISEC CCC is registered by the RTQ5119A, it updates “Register 0x34” [6] = ‘0’ and it takes in effect at the next Start operation (i.e. after STOP operation). Table 35 to Table 38 shows an example of a single DISEC CCC. Table 39 shows the encoding definition for DISEC CCC. If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7’h7E with W=0 byte in PEC calculation.

Table 35. DISEC CCC – Broadcast

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x01 (Broadcast)								T	
	0x00							DISINT	T	Sr or P

Table 36. DISEC CCC – Broadcast with PEC

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x01 (Broadcast)								T	
	0x00							DISINT	T	
	PEC								T	Sr or P

Table 37. DISEC CCC – Direct

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x81 (Direct)								T	
Sr	DevID [6:0]							W=0	A	
	0x00							DISINT	T	Sr or P

Table 38. DISEC CCC – Direct with PEC

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x81 (Direct)								T	
	PEC								T	
Sr	DevID [6:0]							W=0	A	
	0x00							DISINT	T	
	PEC								T	Sr or P

Table 39. DISEC CCC Byte Encoding

Bit	Encoding	Notes
DISINT	0 = No Action 1 = Disable IBI Interrupt	It is illegal for Host to issue DISEC CCC with DISINT bit = ‘0’

(3) RSTDAA CCC

RSTDAA CCC is registered by the RTQ5119A, it updates “Register 0x32” [6] = ‘0’ and it takes in effect at the next Start operation (i.e. after STOP operation). Further it disables IBI & PEC function (“Register 0x34” [7:6] = ‘00’) and clears parity function (“Register 0x34” [5] = ‘0’). Table 40 to Table 41 shows an example of a single RSTDAA CCC. If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7’h7E with W=0 byte in PEC calculation.

Table 40. RSTDAA CCC – Broadcast

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x06 (Broadcast)								T	P

Table 41. RSTDAA CCC – Broadcast with PEC

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x06 (Broadcast)								T	
	PEC								T	P

(4) SETAASA CCC

The SETAASA CCC is only supported when RTQ5119A is in I^2C mode. In I^2C mode, when host issues this CCC, to guarantee that this CCC is registered by the RTQ5119A without any error, the host should limit the maximum speed operation for this CCC to 1 MHz. In I^3C Basic mode, this CCC is ignored. When SETAASA CCC is registered by the RTQ5119A, it updates “Register 0x32” [6] = ‘1’ and it takes in effect at the next Start operation (i.e. after STOP operation). Table 42 shows an example of a single SETAASA CCC. SETAASA CCC does not support PEC function as device is in I^2C mode and there is no PEC function in I^2C mode.

Table 42. SETAASA CCC – Broadcast

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x29 (Broadcast)								T	P

(5) GETSTATUS CCC

The GETSTATUS CCC is supported in I^3C Basic mode. In I^2C mode, this CCC is ignored (i.e. it is not executed internally and the Repeat Start byte arriving after the 0x90 GETSTATUS CCC code is not acknowledged and host must do STOP operation). Table 43 to Table 44 shows an example of a single GETSTATUS CCC. If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7’h7E with W=0 byte in PEC calculation.

Table 43. GETSTATUS CCC – Direct

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x90 (Direct)								T	
Sr	DevID [6:0]							R=1	A	
	PEC_Err	0	0	0	0	0	0	0	T	
	0	**0**	**P_Err**	**R32[3]**	**Pending Interrupt**				**T**	**Sr or P**

Table 44. GETSTATUS CCC – Direct with PEC

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x90 (Direct)								T	
	PEC								T	
Sr	DevID [6:0]							R=1	A	
	PEC_Err	0	0	0	0	0	0	0	T	
	0	0	P_Err	R32[3]	Pending Interrupt				T	
	PEC								T	Sr or P

Table 45. GETSTATUS CCC Byte Encoding

Bit	Encoding	Notes
PEC_Err	0 = No Error 1 = PEC Error Occurred	This register is cleared when Host issues clear command to “Register 0x12” [3] for PEC error.
P_Err	0 = No Error 1 = Protocol Error; Parity Error occurred	This register is cleared when Host issues clear command to “Register 0x12” [2] for Parity error.
R32[3]	See “Register 0x32” for encoding.	PMIC reflects the register status of R32[3] in this bit.
Pending Interrupt	0000 = No Pending Interrupt or No New Global Status Event. 0001 = Pending Interrupt or New Global Status Event. All other encodings are reserved.	This register is cleared when Host issues clear command to any appropriate device status register that causes IBI status register to get cleared.

(6) DEVCAP CCC

The DEVCAP CCC is only supported after RTQ5119A is put in I^3C Basic mode. In I^2C mode, it is illegal for host to issue this CCC. Table 46 to Table 47 shows an example of a single DEVCAP CCC. Table 48 defines the encoding for DEVCAP CCC. If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7’h7E with W=0 byte in PEC calculation.

Table 46. DEVCAP CCC – Direct

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0xE0 (Direct)								T	
Sr	DevID [6:0]							R=1	A	
	MSB (Each bit defines capability)								T	
	LSB (Each bit defines capability)								T	Sr or P

Table 47. DEVCAP CCC – Direct with PEC

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0xE0 (Direct)								T	
	PEC								T	
Sr	DevID [6:0]							R=1	A	
	MSB (Each bit defines capability)								T	
	LSB (Each bit defines capability)								T	
	PEC								T	Sr or P

Table 48. DEVCAP CCC Byte Encoding

Bit	Encoding	Notes
MSB[7]	RFU	Coded as ‘0’
MSB[6]	RFU	Coded as ‘0’
MSB[5]	RFU	Coded as ‘0’
MSB[4]	RFU	Coded as ‘0’
MSB[3]	RFU	Coded as ‘0’
MSB[2]	0 = No Support for Timer based Reset 1 = Supports Timer based Reset	Coded as ‘1’
MSB[1:0]	RFU	Coded as ‘00’
LSB[7:0]	RFU	Coded as ‘0x00’

(7) SETHID CCC

The SETHID CCC is supported only when RTQ5119A is in I^2C mode. In I^2C mode, when host issues this CCC, to guarantee that this CCC is registered by the RTQ5119A without any error, the host should limit the maximum speed operation for this CCC to 1 MHz. In I^3C Basic mode, it is illegal for host to issue this CCC. When SETHID CCC is registered by the RTQ5119A, it updates “Register 0x34” [3:1] with the HID code received by the RTQ5119A and it takes in effect at the next Start operation (i.e. after STOP operation). Table 49 shows an example of a single SETHID CCC. As the RTQ5119A is in I^2C mode when SETHID CCC is issued, the PEC function is not supported. Once RTQ5119A receives SETHID CCC and updates its 3-bit HID code, after the Stop operation, RTQ5119A only responds to the updated 7-bit address. The 4-bit LID code of the RTQ5119A remains no change.

Table 49. SETHID CCC – Broadcast

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x61 (Broadcast)								T	
	0	0	0	0	HID[2:0]			0	T	P

(8) DEVCTRL CCC

On a typical I^3C Basic bus there can be up to 120 devices. For DDR5 DIMM application environment, there are up to 8 SPD5 Hub devices and behind each SPD5 Hub devices, there are 4 local slave devices totaling up to 40 or more devices on I^3C Basic bus. For certain operation such as enable or disable functions that are common to all devices (i.e. Packet Error Check), the host must go through one device at a time which takes significant amount of time at initial power up. Further, it requires additional complexity on the host because it must speak different protocol depending on how it may access the device until all devices are configured identically.

To help expedite this configuration operation and to simplify the host complexity, the RTQ5119A supports the DEVCTRL CCC. The DEVCTRL CCC is supported either in I^2C mode or I^3C Basic mode of operation. In I^2C mode, when host issues this CCC, to guarantee that this CCC is registered by the RTQ5119A without any error, the host should limit the maximum speed operation for this CCC to 1 MHz. Table 50 to Table 51 shows an example of a single DEVCTRL CCC. In I^3C mode only, if PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7’h7E with W=0 byte in PEC calculation.

The host should pay attention to DEVCTRL CCC. If DEVCTRL CCC is used to access device specific registers (e.g.

RegMod = ‘1’), the host should still follow any device specific register restriction. For example, if device specific register requires STOP operation for device to take in the effect of the setting, the host must also use STOP operation when using DEVCTRL CCC to access device specific register.

Table 50. DEVCTRL CCC – Broadcast

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	Sr or P

Table 51. DEVCTRL CCC – Broadcast with PEC

Start	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A/N	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	
	PEC								T	Sr or P

Table 52. DEVCTRL CCC Command Definition

Parameter	Definition
AddrMask[2:0]	Broadcast, Unicast or Multicast Command Selection 000 = Unicast Command; PMIC device responds if DevID[6:0] field matches with PMIC device's own 7-bit address (4-bit LID + 3-bit HID). 011 = Multicast Command; PMIC device and possible other device responds if DevID[6:3] field matches with PMIC device's own 4-bit LID address. 111 = Broadcast Command; All devices responds to this command All other encodings are reserved.
StartOffset[1:0]	Only applicable if RegMod = '0' Identifies the starting Byte (Byte 0 or Byte 1 or Byte 2 or Byte 3) for DEVCTRL CCC. Host can start at any Byte (from Byte 0 to Byte 3) and has continuous access to next byte until STOP operation. If Byte 3 is reached, the host is responsible for applying STOP operation. 00 = Byte 0 01 = Byte 1 10 = Byte 2 11 = Byte 3
PEC BL[1:0]	Only applicable if RegMod = '0' and PEC function is enabled. Identifies the burst length just for this DEVCTRL CCC. The RTQ5119A uses the setting in this field to know when the PEC byte is expected after the data bytes. 00 = 1 Byte 01 = 2 Byte 10 = 3 Byte 11 = 4 Byte
RegMod	Identifies if DEVCTRL is going to be used for General Registers as identified in Byte 0 to Byte 3 or device specific address offset register. 0 = Access to General Registers in Byte 0 to Byte 3 (i.e. StartOffset[1:0] = Valid). 1 = Device Specific Offset Address (i.e StartOffset[1:0] & PECBL[1:0] is a don't care and does not apply). The Host shall NOT use RegMod = '1' with Broadcast Command if there are different types of devices on the I^3C Basic bus.
DevID[6:0]	Identifies 7-bit device address. RTQ5119A responds to DEVCTRL CCC data packet depending on AddrMask[2:0]. If AddrMask[2:0] = '111', DevID[6:0] is a don't care and device always responds. If AddrMask[2:0] = '000', DevID[6:0] must match for device to respond. If AddrMask[2:0] = '011', DevID[6:3] must match for device to respond. DevID[2:0] is don't care. For any other codes for AddrMask[2:0], the RTQ5119A always NACKs.

Table 53. DEVCTRL CCC Data Payload Definition

Byte#	Bit#	Function	Definition	Comment
Byte0	[7]	PEC Enable	0 = Disable 1 = Enable	“Register 0x34” [7] is updated.
	[6]	Parity Disable	0 = Enable 1 = Disable	“Register 0x34” [5] is updated.
	[5:2]	RFU	RFU	
	[1]	VR Enable	0 = VR Disable 1 = VR Enable	“Register 0x32” [7] is updated.
	[0]	RFU	RFU	
Byte1	[7:4]	RFU	RFU	
	[3]	Global & IBI Clear	0 = No Action 1 = Clear All Event and pending IBI	“Register 0x14” [0] is updated.
	[2:0]	RFU	RFU	
Byte2	[7:0]	RFU	RFU	
Byte3	[7:0]	RFU	RFU	

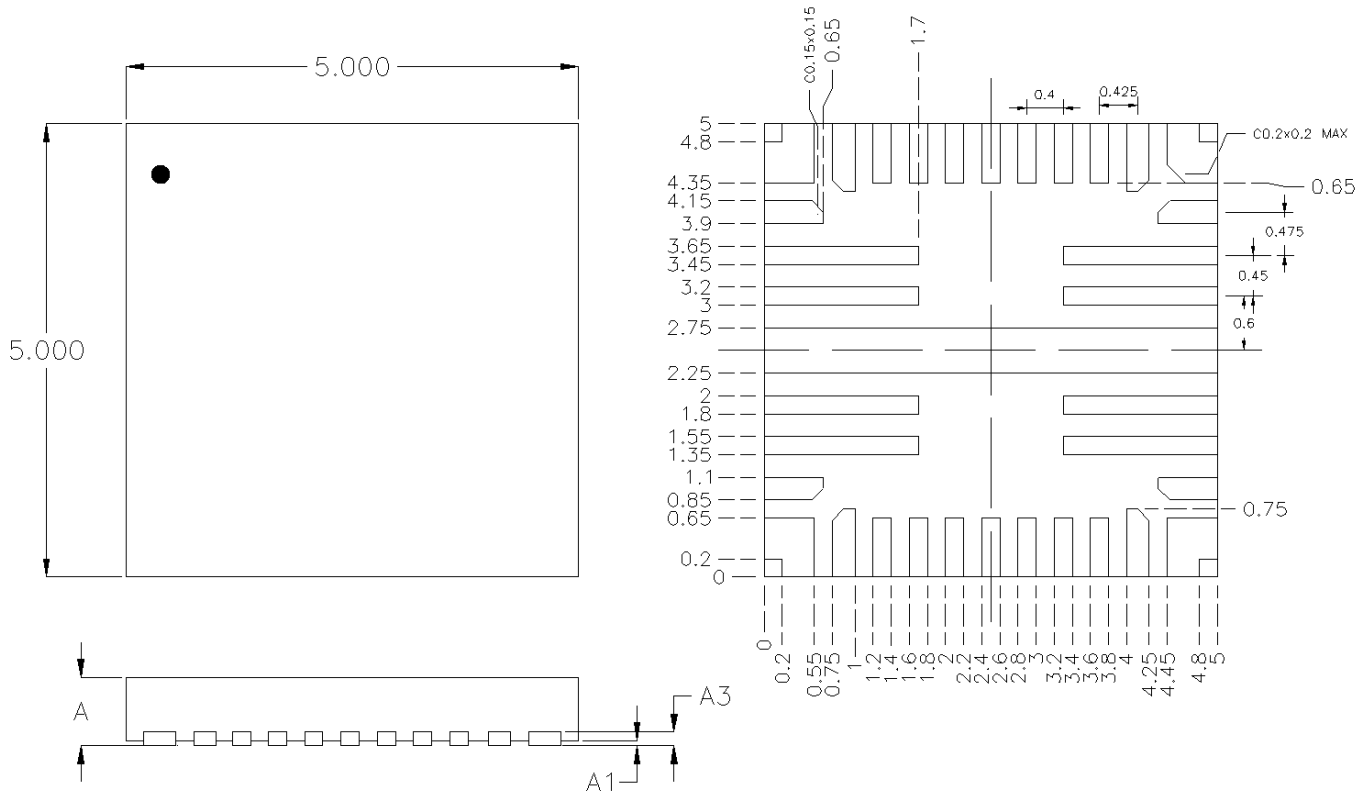
Command Truth Table

The command truth table as shown in Table 54 only applies in I^3C Basic mode with PEC enabled. In I^2C mode and I^3C Basic mode with PEC disabled, the command truth table does not apply.

Table 54. For I^3C Mode Only with PEC Enabled - Command Truth Table

TS5 Command	Command Name	CMD Code	RW	Address
		2nd Byte Bits [7:5]	2nd Byte Bit [4]	1st Byte Bits [7:0]
Write 1 Byte to Register	W1R	000	0	V
Read 1 Byte from Register	R1R		1	V
Write 2 Byte to Register	W2R	001	0	V
Read 2 Byte from Register	R2R		1	V
Write 4 Byte to Register	W4R	010	0	V
Read 4 Byte from Register	R4R		1	V
Write 16 Byte to Register	W16R	011	0	V
Read 16 Byte from Register	R16R		1	V
Reserved	RSVD	100 to 111	RSVD	RSVD

Outline Dimension

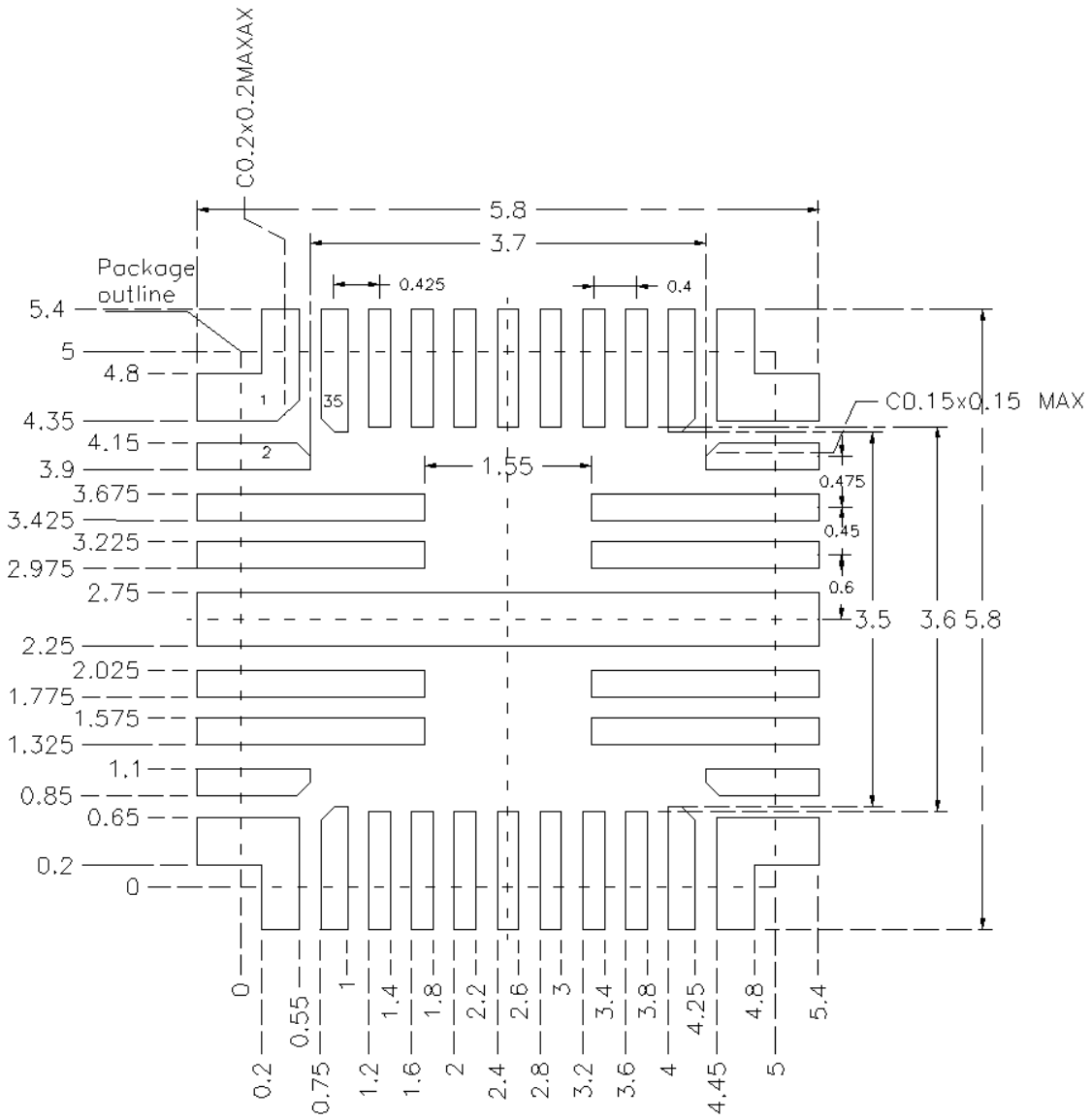


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050

V-Type 35L QFN 5x5 (FC) Package

Footprint Information



Package	Number of Pin	Tolerance
V/W/U/XQFN5x5-35(FC)	35	±0.05

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Datasheet Revision History

Version	Date	Description	Item
02	2023/3/17	Modify	Features on P1 Simplified Application Circuit on P3 Register Map on P91, 111, 121, 122 Application Information on P55