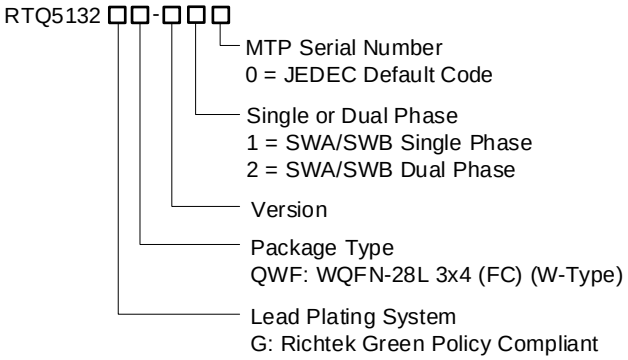
DDR5 Client VR on DIMM PMIC

General Description

The RTQ5132 is an integrated solution for DDR5 SODIMM and UDIMM power management IC. This device provides 1 dual-phase converter, 1 single phase converter and 2 LDOs. The RTQ5132 is available in a WQFN-28L 3x4 (FC) package.

The Recommended junction temperature range is –10°C to 125°C and ambient temperature range is 0°C to 85°C.

Ordering Information

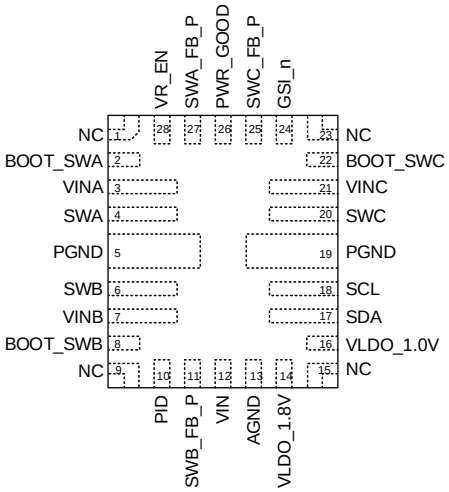


Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

Pin Configuration

(TOP VIEW)



WQFN-28L 3x4 (FC)

Features

- **VIN_Bulk with Wide Input Supply Range: 4.25V to 5.5V**
- **High Integration:**
  - **1 Configurable Dual-Phase or Single-Phase Converters (SWA, SWB),**
  - **1 Single-Phase Converters (SWC)**
  - **2 LDOs (VLDO_1.8V, VLDO_1.0V)**
- **Support I^2C and I^3C Slave Control**
- **Automatic Input Supply for LDOs**
- **MTP Registers with Secured R/W Access**
- **0.75% Converter Output Accuracy**
- **Integrated Sequencing Control for DDR5 VR on DIMM Platform**
- **Support Pure MLCC Output Capacitor Stable**
- **Common ADC Channels (5 Default and 1 User Selectable)**
- **Output Current, Voltage and Power Measurement and Reporting Mechanism**
- **Error Log Counter and Data Storage (NVM)**
- **Programmable and DIMM Specific Registers for Customization**
- **Programmable-Diagnostic Mode for Debug and Validation**
- **Complete Protection Mechanisms**
- **VIN_Bulk Input Supply OVP**
- **OTP, OVP, UVP, OCP for Each Rails**
- **General Status Interrupt Function**
- **Power Good Indicator**

Applications

- DDR5 SO-DIMM/ UDIMM

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Simplified Application Circuit

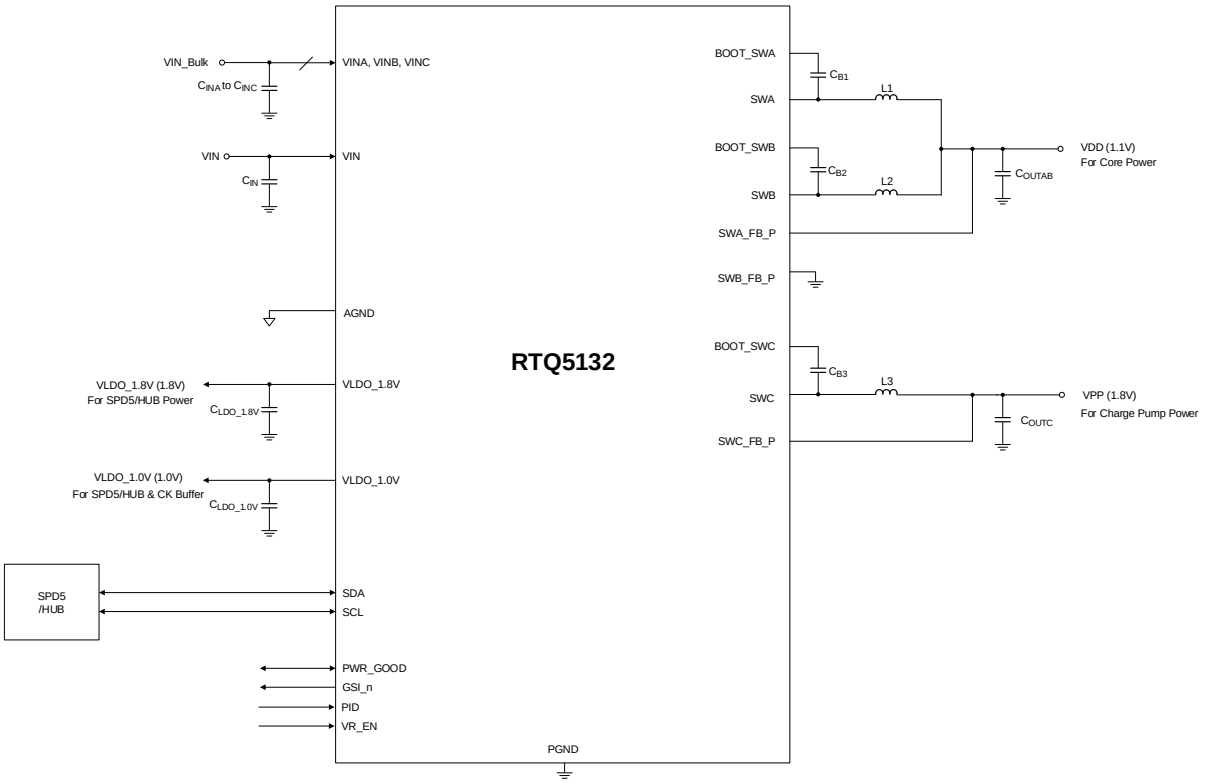


Figure 1. SWA and SWB are combined as Dual-Phase Mode

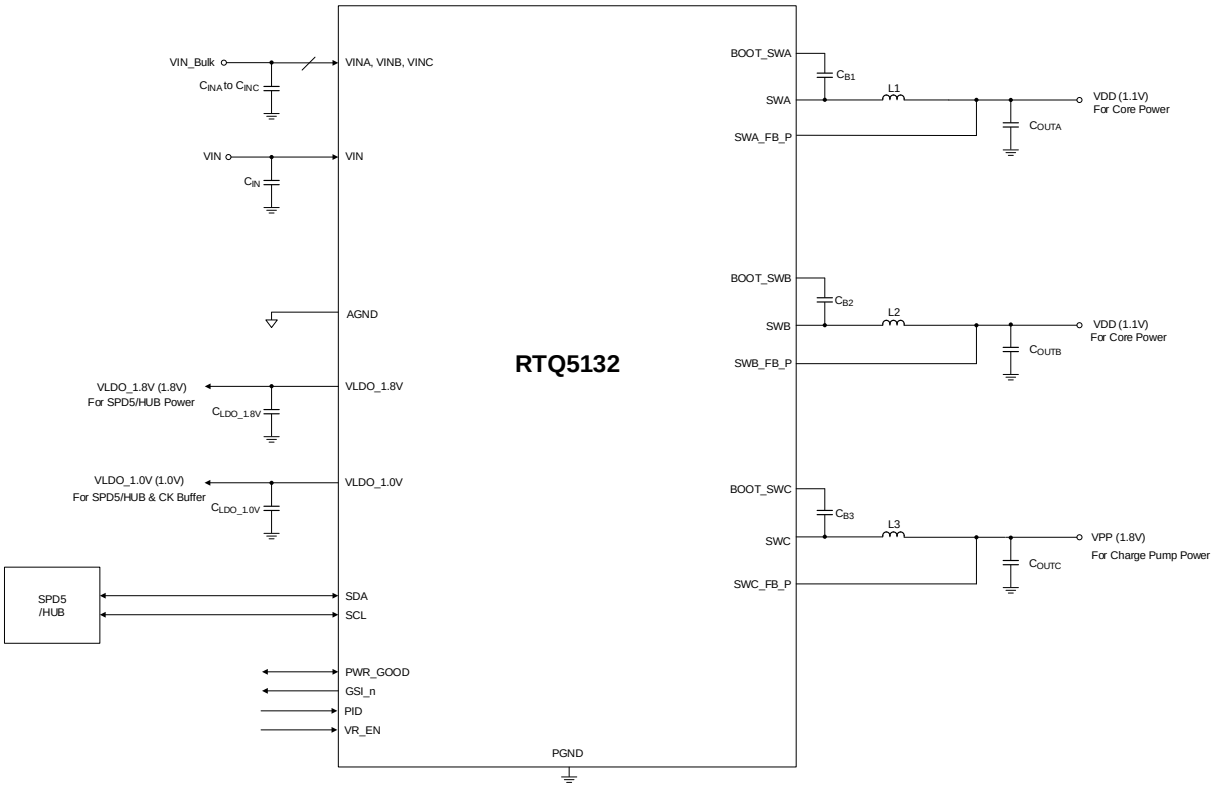


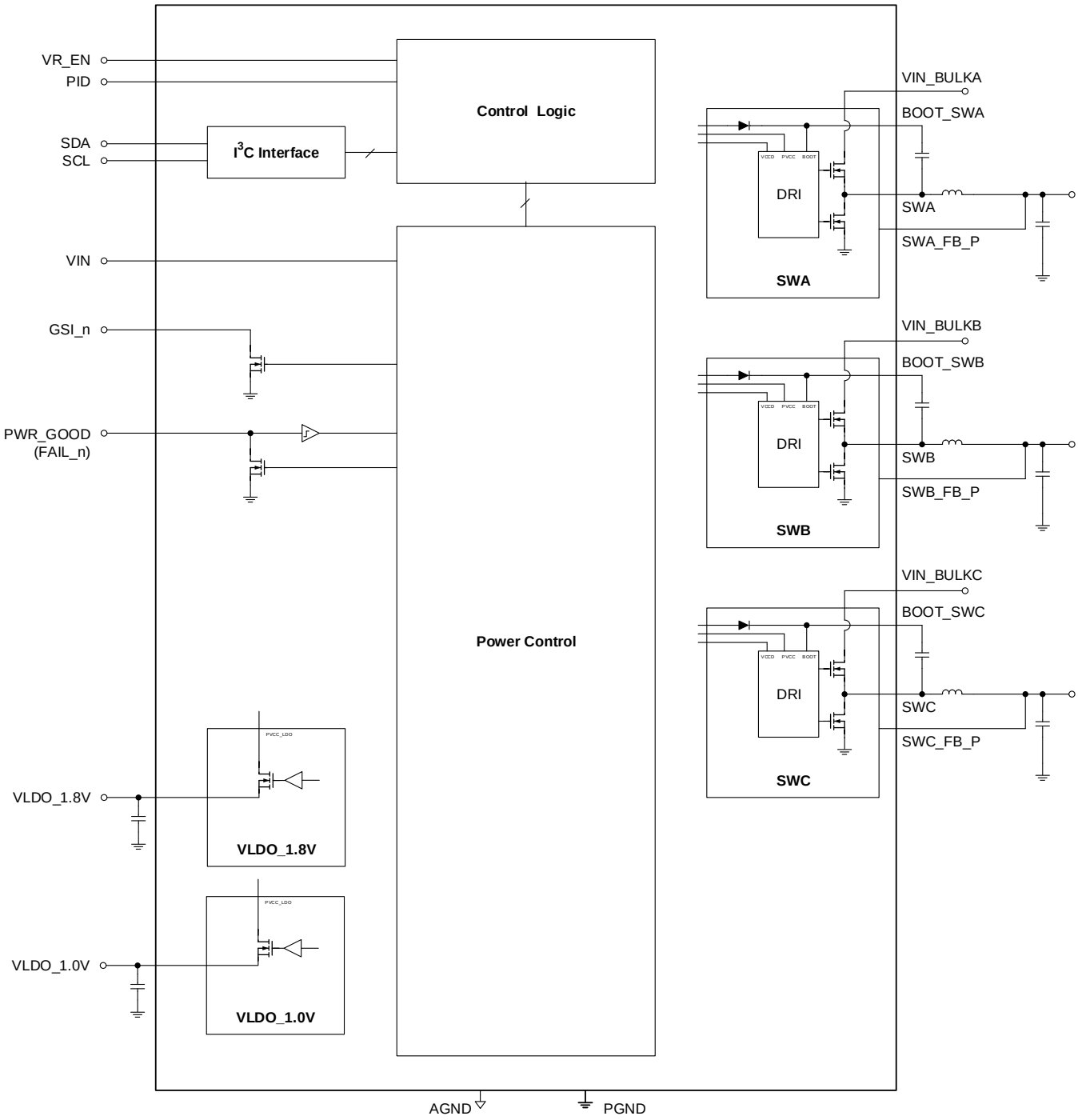
Figure 2. SWA and SWB are operating in Single-Phase Mode

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 9, 15, 23	NC	Non-functional pins. No internal connections to the chip.
2	BOOT_SWA	Buck A bootstrap. Bootstrap node for switch node SWA high-side NMOS driver. Connect a capacitor between SWA and BOOT_SWA to form a floating supply across the high-side switch driver of Buck A.
3	VINA	Input supply of Buck A. VINA is connected to 5V power plane on the DIMM. All three VINx input pins must be connected to 5V supply, even if one or more regulators are not intended to be used.
4	SWA	Buck A switch output. Output switch node SWA regulator. This pin is connected to an external inductor (L1). Note: In single phase mode of operation, SWA output must not be connected to SWB or SWC output, even if this switch node is configured for the same output voltage as the others.
5, 19	PGND	Common Power ground. Connect PGND to DIMM ground plane. PGND pins require special consideration during PCB layout.
6	SWB	Buck B switch output. Output switch node SWB regulator. This pin is connected to an external inductor (L2). Note: In single phase mode of operation, SWB output must not be connected to SWA or SWC output, even if this switch node is configured for the same output voltage as the others.
7	VINB	Input supply of Buck B. VINB is connected to 5V power plane on the DIMM. All three VINx input pins must be connected to 5V supply, even if one or more regulators are not intended to be used.
8	BOOT_SWB	Buck B bootstrap. Bootstrap node for switch node SWB high-side NMOS driver. Connect a capacitor between SWB and BOOT_SWB to form a floating supply across the high-side switch driver of Buck B.
10	PID	PMIC ID pin for I^2C and I^3C Basic bus. It must be connected to GND.
11	SWB_FB_P	Positive feedback of Buck B. In single-phase output regular configuration, this pin is connected to the SWB remote positive sense feedback. Otherwise, it must be connected to AGND.
12	VIN	5V supply input to the PMIC.
13	AGND	Analog ground. Connect AGND to the power ground pin.
14	VLDO_1.8V	PMIC 1.8V LDO supply.
16	VLDO_1.0V	PMIC 1.0V LDO supply.
17	SDA	Bus data of I^2C and I^3C.
18	SCL	Bus clock of I^2C and I^3C.
20	SWC	Buck C switch output. Connect SWC using a wide PCB trace. The output of SWC must not be connected to the output of SWA or SWB, or (SWA+SWB) even if they configure for exact same output voltage.
21	VINC	Input supply of Buck C. VINC is connected to 5V power plane on the DIMM. All three VINx input pins must be connected to 5V supply, even if one or more regulators are not intended to be used.

Pin No.	Pin Name	Pin Function
22	BOOT_SWC	Buck C bootstrap. Bootstrap node for switch node SWC high-side NMOS driver. Connect a capacitor between SWC and BOOT_SWC to form a floating supply across the high-side switch driver of Buck C.
24	GSI_n	General status interrupt. Optional PMIC debug function pin (not required) for DDR5 RDIMM/LRDIMM application.
25	SWC_FB_P	Positive feedback of Buck C. Switch node SWC remote positive sense feedback.
26	PWR_GOOD	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as all enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or when any of the enabled switch output regulators exceeds the threshold configured in the appropriate register or any LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.
27	SWA_FB_P	Feedback of Buck A and Buck B. SWA/B rail remote sense feedback when SWA and SWB are combined as dual-phase, single output rail. When SWA and SWB are separated for two independent rails, this pin is used as SWA remote positive sense feedback (+).
28	VR_EN	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This pin shall not be left floating. If it is not used, it shall be tied to GND

Functional Block Diagram



Operation

PMIC Input Voltage Supply & Ramp Condition

The DDR5 PMIC has one input supply from the platform: VIN_Bulk.

The VIN_Bulk supply is used by the PMIC for all three switch (SWA, SWB and SWC) output regulators and two LDO outputs (VOUT_1.8V & VOUT_1.0V) regulators. Note that the VOUT_1.8V LDO output is separate and independent from SWC output, which is for the DRAM VPP rail. The VOUT_1.0V LDO output is separate and independent from SWA or SWB.

At first power on, the VIN_Bulk input supply shall reach a minimum threshold voltage of 4.25V before it can be detected as a valid input supply to the PMIC.

Once the VIN_Bulk supply is valid and stable, the PMIC shall assert PWR_GOOD output low, drive VOUT_1.8V & VOUT_1.0V supply within t1.8V_Ready and t1.0V_Ready time respectively. The PMIC drives PWR_GOOD output signal low only when VIN_Bulk input supply reaches minimum of 4.25 V. The PWR_GOOD output is pulled up to either 1.8 V or 3.3V on the platform or on the host controller.

The PWR_GOOD pullup voltage (either 1.8 V or 3.3V) can be available before or after VIN_Bulk is valid and stable. If PWR_GOOD pullup voltage is available before VIN_Bulk is applied, the PWR_GOOD signal is High and remains High with no leakage path or damage to the PMIC. When VIN_Bulk is applied to the PMIC, the PMIC asserts PWR_GOOD output low.

The PMIC shall enable I^2C/I^3C bus interface function within tManagement_Ready. The host shall not attempt to access the PMIC's memory registers until tManagement_Ready timing requirement is satisfied.

During power on, the user shall:

(1) Ramp up VIN_BULK supply;

(2) Hold VIN_Bulk supply stable for a minimum of tVIN_Bulk_to_VR_Enable time.

(3) Hold VR_EN pin to static low or high.

(4) During VIN_Bulk ramp, if VR_EN signal is held low, it can transition to high only once. Once high, it shall remain high. The VR_EN signal is not allowed to transition to low during VIN_Bulk ramp up.

(5) If VR_EN pin is held High during VIN_Bulk ramp up or transitions to High during VIN_Bulk ramp up, the PMIC turns on its output rails.

(6) If VR_EN pin is held Low during VIN_Bulk Ramp, assert VR_EN signal High to turn on PMIC output rails. Alternatively, host can issue VR Enable command by setting register, Register 0x32[7] = 1 via I^2C/I^3C Basic bus or via DEVCTRL CCC to turn on PMIC output rails.

Figure 3 to Figure 6 shows example of PMIC power up initialization sequence. Note that the specific sequence of ramping the output regulators (SWA, SWB and SWC) is for example purpose only. The specific ramp up sequence is configurable through power-on sequence configuration registers.

After VR Enable command is registered on the I^2C or I^3C Basic bus or VR_EN pin is registered high, the PMIC shall complete the following steps within tPMIC_PWR_GOOD_OUT:

(1) Check VIN_Bulk Power Good status is valid.

(2) Power up itself – RTQ5132 executes Power-on sequence Config0 to Power-on Sequence Config2 registers and configures RTQ5132 internal registers as programmed in DIMM vendor memory space registers.

(3) Power up all enabled output switch regulators and ready for normal operation.

(4) Update status registers "Register 0x08" [5,3:2] and floats PWR_GOOD signal within maximum of tPMIC_PWR_GOOD_OUT time.

If PMIC PWR_GOOD signal is not floated within tPMIC_PWR_GOOD_OUT time, the host can access the PMIC status registers for detailed information after tPMIC_PWR_GOOD_OUT time. The PMIC may NACK for any host request on I^2C or I^3C Basic bus after VR Enable command (either with VR_EN pin high or on I^2C/I^3C Basic Bus) until tPMIC_PWR_GOOD_OUT time expires

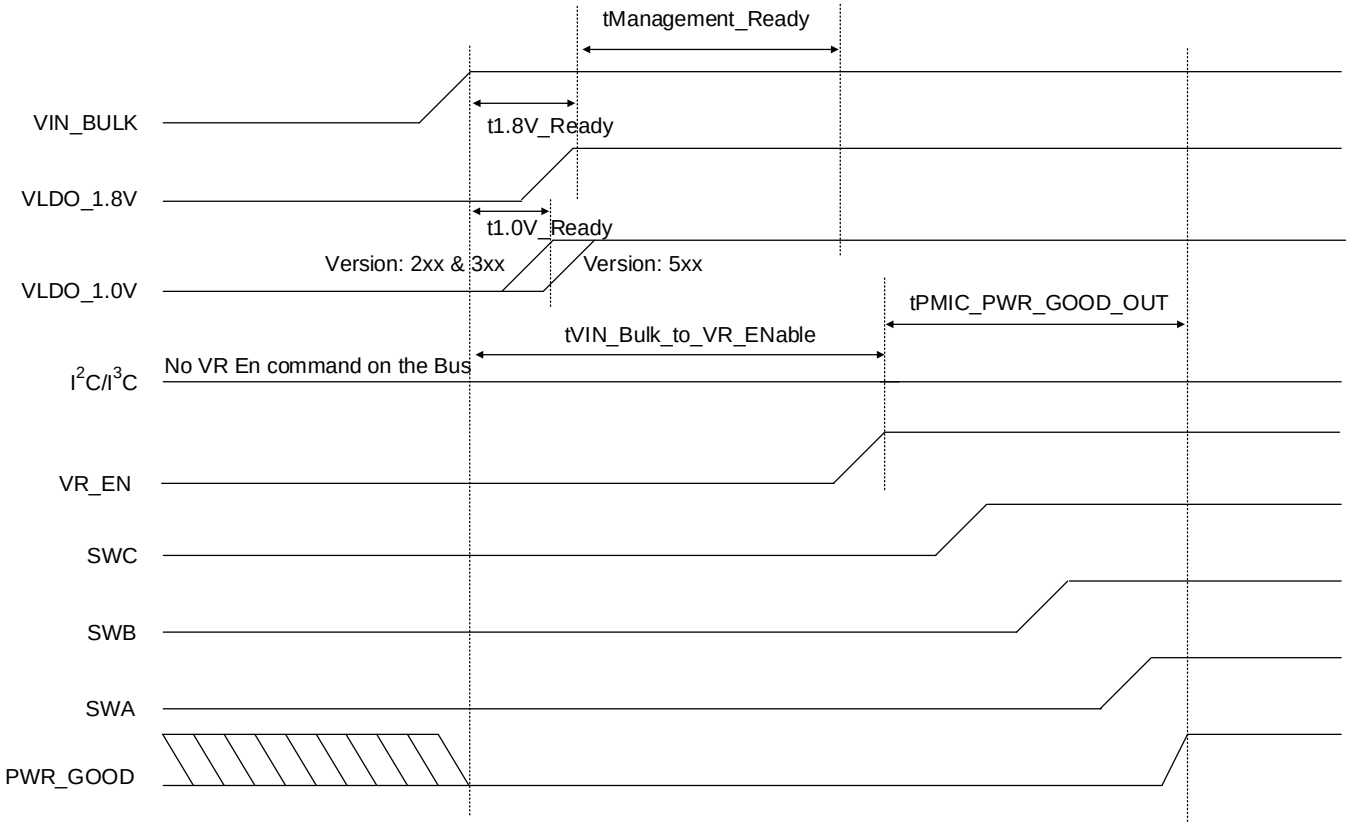


Figure 3. Power Up Sequence; VR_EN pin High after VIN_Bulk Ramp; No Bus Command

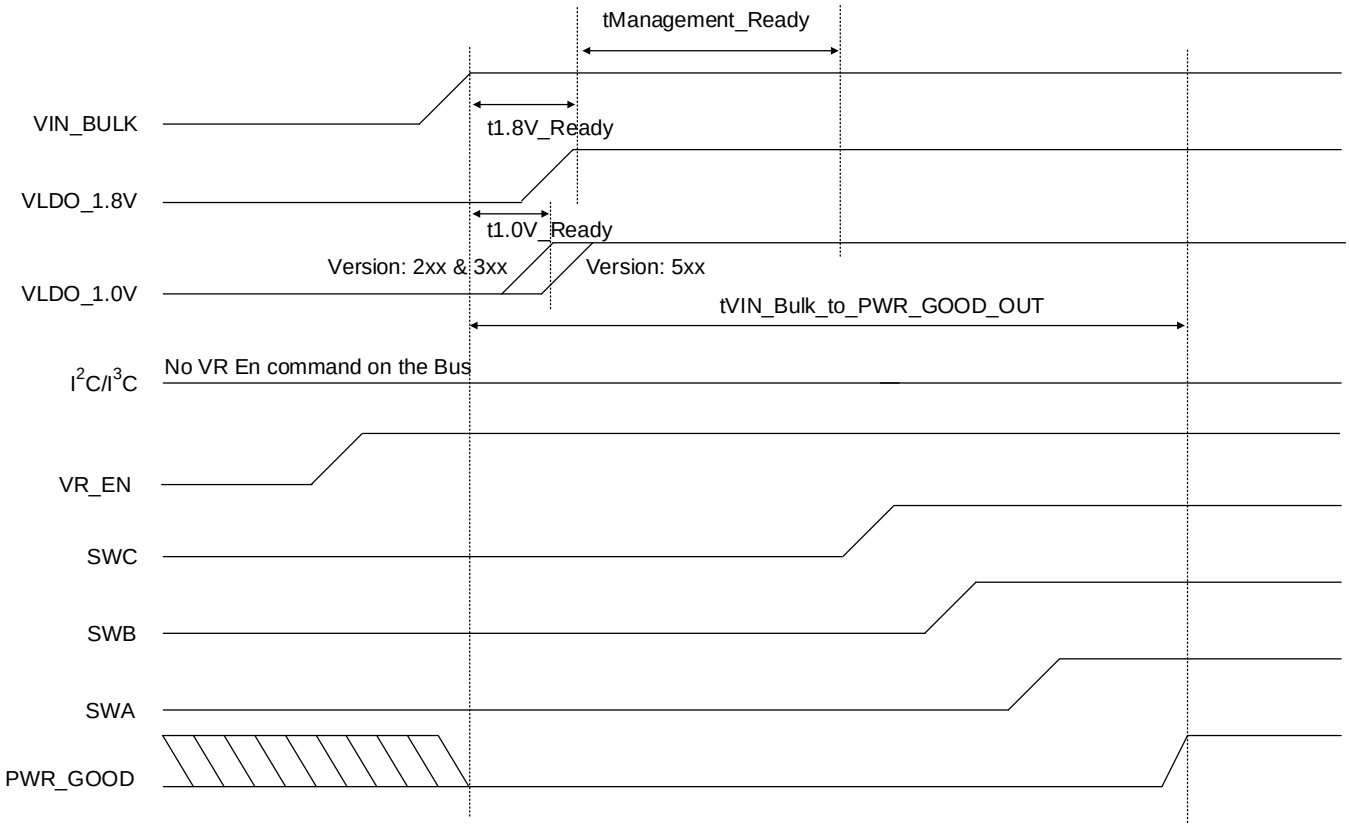


Figure 4. Power Up Sequence; VR_EN pin High before VIN_Bulk Ramp; No Bus Command

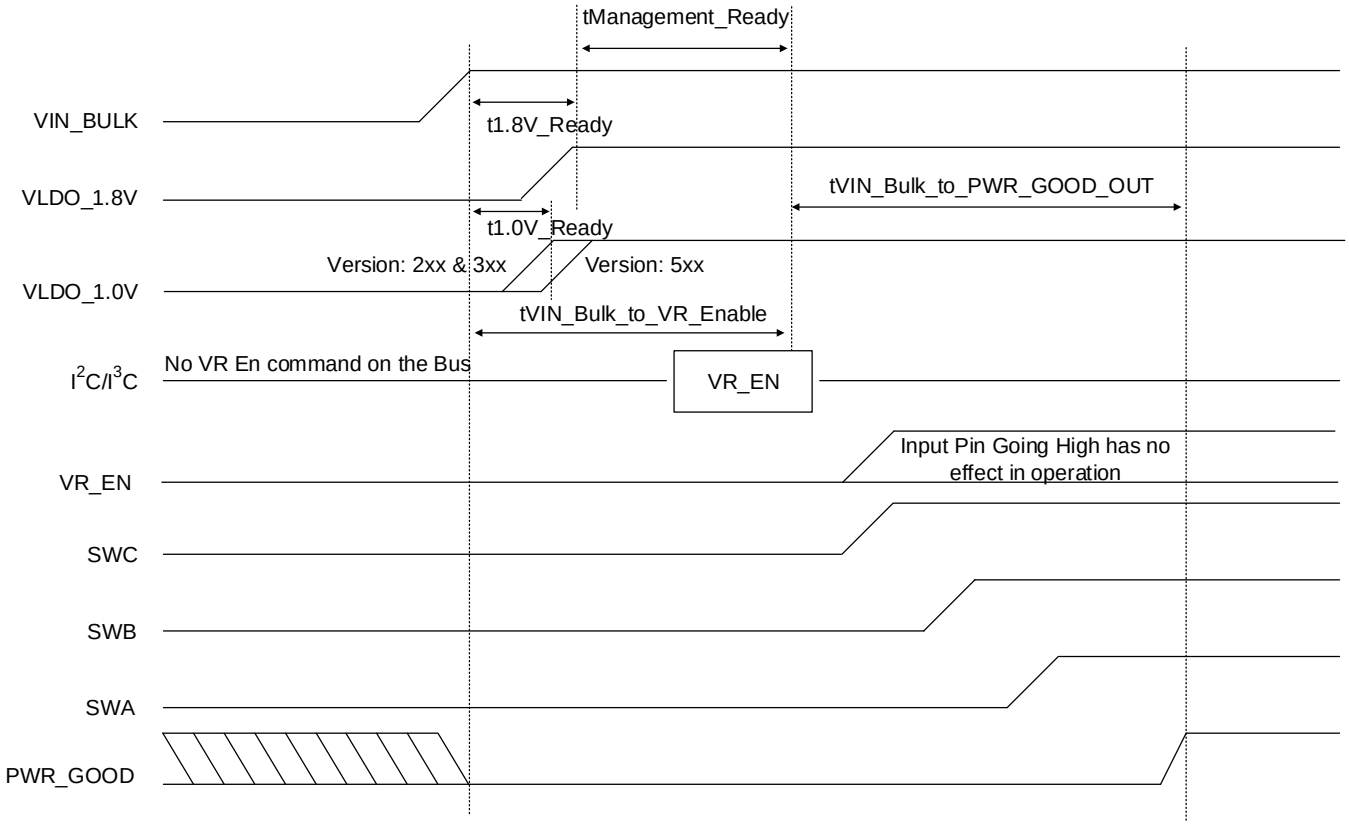


Figure 5. PMIC Power Up Sequence; w/ VR_EN Pin followed by Bus Command

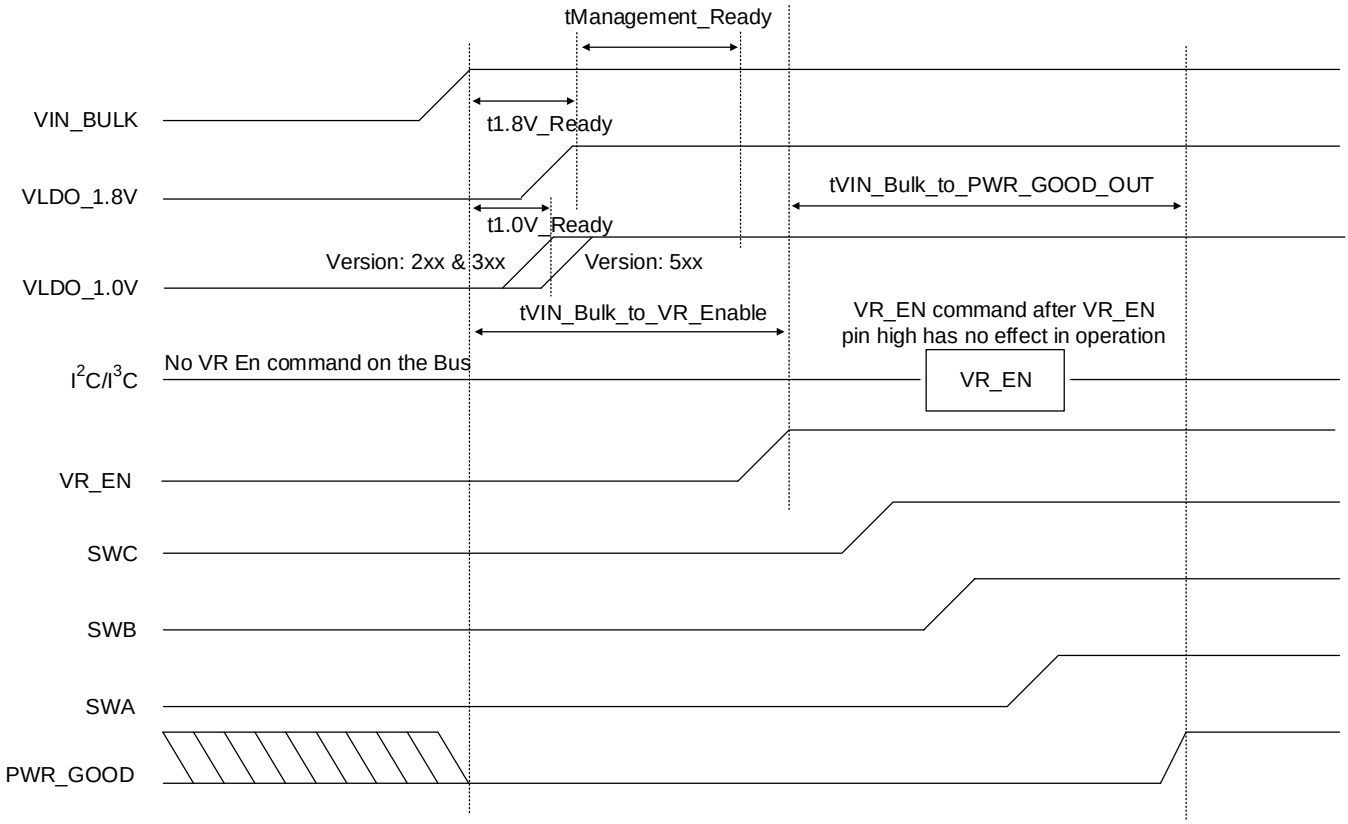


Figure 6. PMIC Power Up Sequence; w/ VR_EN Pin followed by Bus Command

Enabling PMIC Output Switch Voltage Regulators

The Figure 7 below shows the timing relationship once the PMIC receives VR Enable command (either with VR_EN pin or on I^2C/I^3C Basic bus) and when it floats PWR_GOOD output signal; timing parameter tPMIC_PWR_GOOD_OUT applies. This timing parameter is a sum of maximum soft-start time and configured delay for each power-on sequence configuration registers that are executed plus additional 5ms timing margin error. The waveform shows each buck regulator output soft-start time and delay time once the soft-start time expires for each power-on sequence config0 to power-on sequence config2 registers. Note that if more than one regulators are enabled in a power-on sequence config register and if those regulators have different soft-start time programmed, then the larger value of that soft-start time is used as a reference for delay timer to start. Each regulator will still follow different soft-start time to turn on the buck regulator.

The specific example in Figure 7 uses three power-on sequence config0 to config2 registers and only one buck regulator is enabled in each power-on sequence config 0 to config 2 register.

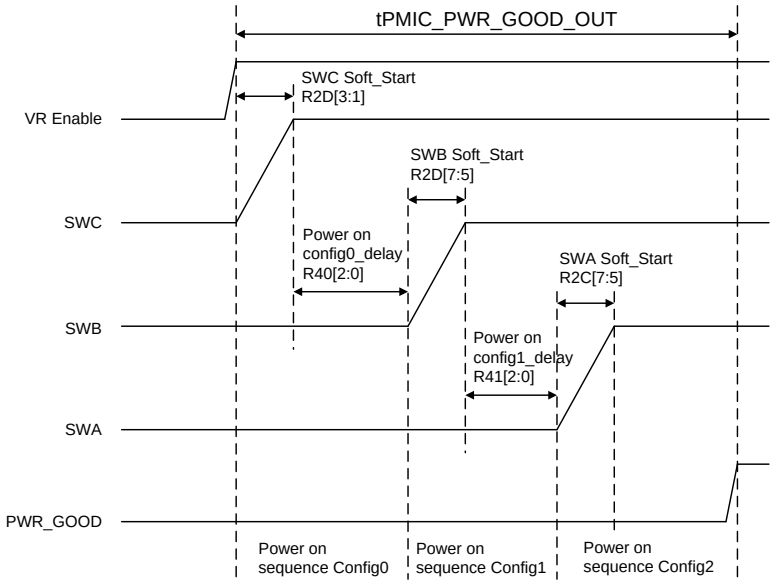


Figure 7. RTQ5132 Rails Power On Timing

Secure Mode & Programmable Mode of Operation

Prior to issuing VR Enable command (either with VR_EN pin or on I^2C/I^3C Basic bus), the host must configure the register “Register 0x2F” [2] appropriately as desired. The PMIC offers two modes of operation after VR Enable command (either with VR_EN pin or on I^2C/I^3C Basic bus) is registered.

1. Programmable Mode - In this mode, independent of when host issues VR Enable command (either with VR_EN pin or on I^2C/I^3C Basic bus), the PMIC allows modification to any register in the host region as

desired by the host and PMIC responds appropriately.

2. Secure Mode - In this mode, In this mode, after host issues VR Enable command (either with VR_EN pin or on I^2C/I^3C Basic bus), the PMIC does not allow modification to registers, “Register 0x15” to “Register 0x2F”, “Register0x32” [7,5:0] in the host region as well as “ Register 0x40” to Register 0x6F in the DIMM vendor region. These registers are write protected. The host must power cycle the PMIC to make any modification. The PMIC power cycle is defined as complete removal of VIN_Bulk input supply to the PMIC and this definition is applied to the entire specification.

The Secure Mode is only applicable once VR Enable command (either with VR_EN pin or on I^2C/I^3C Basic bus) is registered. This is important because by default, Register 0x2F”[2] = ‘0’ when PMIC is first powered up. Prior to VR Enable command (either with VR_EN pin or on I^2C/I^3C Basic bus), PMIC allows modification to any

registers in the host region.

Power Down Output Regulators

Regardless of how PMIC's output regulators are turned on (w/VR_EN pin or w/VR Enable command on I^2C/I^3C Basic bus), the PMIC's output regulators are powered down as described below depending on PMIC's mode of operation.

Programmable Mode Operation; R1A[4] = '0'

1. The VR Disable command ("Register 0x32" [7] ='0' or VR_EN pin transitions to low). The PMIC executes power-off sequence config0 ("Register 0x58") to power-off sequence config2 ("Register 0x5A") to preserve the appropriate voltage relationship as configured in the registers. The PMIC controls the PWR_GOOD signal as following in bullet a and bullet b:

(a) If VR Disable command with a pin (i.e. VR_EN pin transitions to Low), PMIC asserts PWR_GOOD signal Low. The host can re-enable the PMIC's output regulators by VR_EN pin transition to High. The PMIC executes power-on sequence config 0 to power-on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. See Figure 26. The PMIC does not require power cycle.

(b) If VR Disable command on a I^2C/I^3C Bus (i.e "Register 0x32" [7] = '0'), PMIC keeps the PWR_GOOD signal floating because this is an intentional command from the host and not a fault condition. The host can re-enable the PMIC's output regulators by issuing VR_EN command on the I^2C/I^3C bus ("Register 0x32" [7] = '1'). The PMIC executes power-on sequence config 0 to power-on sequence config 2 registers and continues to float the PWR_GOOD signal until tPMIC_PWR_GOOD_OUT time at which point, PMIC assumes normal control of PWR_GOOD signal.

(c) The simultaneous usage of VR_EN pin and I^2C/I^3C bus command to turn on/off the PMIC is not allowed. If the VR_EN pin transitions to Low first, the PWR_GOOD signal follows as described in bullet (a) and PWR_GOOD signal remains low even if there is a subsequent I^2C/I^3C bus command as described in bullet (b).

2. Configuring one or more bits "Register 0x2F"[6,4:3] to '0' in any specific sequence that is desired by the host. The PMIC does not execute power-off sequence config0 ("Register 0x58") to power-off sequence config2 ("Register 0x5A") on its own. The PMIC keeps the PWR_GOOD signal floating because this is intentional command from the host and not a fault condition. Note that host can re-enable any of disabled output regulators by configuring one or more bits in "Register 0x2F" [6,4:3] to '1' in any specific sequence that is desired by the host. The PMIC keeps the PWR_GOOD signal floating.
3. If "Register 0x32" [5] = '1', driving PWR_GOOD input low. The PMIC executes power-off sequence config0 ("Register 0x58") to power-off sequence config2 ("Register 0x5A") to preserve the appropriate voltage relationship as configured in the registers and drives PWR_GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. If host re-enables PMIC's output regulators by issuing VR_EN command on the I^2C/I^3C Basic bus (i.e."Register 0x32" [7] = '1'), the PMIC executes power-on sequence config 0 to power-on sequence config 2 registers and floats PWR_GOOD output signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The PMIC does not require power cycle.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in "Trigger VR Disable". The PMIC executes power-off sequence config0 ("Register 0x58") to power-off sequence config2 ("Register 0x5A") to preserve the appropriate voltage relationship as configured in the registers. The PMIC asserts PWR_GOOD signal low. The host can re-enable PMIC's output regulators with VR Enable command with either "Register 0x32" [7] ='1' or VR_EN pin transitions to high and PMIC turns on its output regulators and floats PWR_GOOD signal. The PMIC does not require power cycle.

Programmable Mode Operation; R1A[4] = ’1’

1. The VR Disable command (“Register 0x32” [7] =’0’ or VR_EN pin transitions to low). The PMIC executes power-off sequence config0 (“Register 0x58”) to power-off sequence config2 (“Register 0x5A”) to preserve the appropriate voltage relationship as configured in the registers and enters in P1 state. The PMIC controls the PWR_GOOD signal as following in bullet a and bullet b:

(a) If VR Disable command with a pin (i.e. VR_EN pin transitions to Low), PMIC asserts PWR_GOOD signal Low. The host can re-enable the PMIC’s output regulators by VR_EN pin transition to High. The PMIC exits from P1 state and executes power-on sequence config 0 to power-on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied.–

(b) If VR Disable command on a I^2C/I^3C Basic Bus (i.e “Register 0x32”[7] =’0’), PMIC keeps the PWR_GOOD signal floating because this is an intentional command from the host and not a fault condition. The PMIC exits from P1 state with only VR_EN pin transition to High. The host can re-enable the PMIC’s output regulators by VR_EN pin transition to High and PMIC executes power-on sequence config 0 to power-on sequence config 2 registers. The PMIC continues to float PWR_GOOD signal until tPMIC_PWR_GOOD_OUT timing parameter is satisfied and at that point PMIC assumes normal control of PWR_GOOD signal.

(c) The simultaneous usage of VR_EN pin and I^2C/I^3C bus command to turn on/off the PMIC is not allowed. If the VR_EN pin transitions to Low first, the PWR_GOOD signal follows as described in bullet (a) and PWR_GOOD signal remains low even if there is a subsequent I^2C/I^3C bus command as described in bullet (b).

2. Configuring one or more bits in “Register 0x2F” [6,4:3] to ‘0’ in any specific sequence that is desired by the host. The PMIC does not execute power-off sequence config0 (“Register 0x58”) to power-off sequence config2 (“Register 0x5A,”) on its own. The PMIC keeps the PWR_GOOD signal floating because this is intentional command from the host and not a fault condition. Note that host can re-enable any of disabled output regulators by configuring one or more bits in “Register 0x2F”[6,4:3] to ‘1’ in any specific sequence that is desired by the host. The PMIC keeps the PWR_GOOD signal floating.

3. If “Register 0x32” [5] = ‘1’, driving PWR_GOOD input low. The PMIC executes power-off sequence config0 (“Register 0x58”) to power-off sequence config2 (“Register 0x5A,”) to preserve the appropriate voltage relationship as configured in the registers and drives PWR_GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. The PMIC does not enter in P1 state. If host re-enables PMIC’s output regulators by issuing VR_EN command on I^2C/I^3C Basic bus (i.e. “Register 0x32” [7] = ‘1’), the PMIC executes power-on sequence config 0 to power-on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The PMIC does not require power cycle.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in “Trigger VR Disable”. The PMIC executes power-off sequence config0 (“Register 0x58”) to power-off sequence config2 (“Register 0x5A,”) to preserve the appropriate voltage relationship as configured in the registers. The PMIC does not enter in P1 state. The PMIC assert PWR_GOOD signal low. The host can re-enable PMIC’s output regulators with VR Enable command with either “Register 0x32” [7] = ‘1’ or VR_EN pin transitions to high and PMIC turns on its output regulators and floats PWR_GOOD signal. The PMIC does not require power cycle.

Secure Mode Operation; R1A[4] = ’0’

The PMIC allows host to power down any or all output regulators by any of the two methods below.

1. The VR Disable command with VR_EN pin transitions to low. The PMIC asserts PWR_GOOD signal Low. The PMIC executes power-off sequence config0 (“Register 0x58”) to power-off sequence config2 (“Register 0x5A”) to preserve the appropriate voltage relationship as configured in the registers. The host can re-enable the PMIC’s output regulators by VR_EN pin transition to High. The PMIC executes power-on sequence config 0 to power-on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. See Figure 30. The PMIC does not require power cycle. Note that VR Disable or Enable command on a I^2C/I^3C Basic Bus (i.e “Register 0x32” [7] = ‘0’ or ‘1’) has no effect on the PMIC. Also, configuring one or more bits in “Register0x2F” [6,4:3] to ‘0’ has no effect on the PMIC. See Figure 31.
2. If “Register 0x32” [5] =’1’, driving PWR_GOOD input low. The PMIC executes power-off sequence config0 (“Register 0x58”) to power-off sequence config2 (“Register 0x5A,”) to preserve the appropriate voltage relationship as configured in the registers; drives PWR_GOOD signal low and unlocks only “Register 0x32” [7]. The PMIC preserves all register contents including the MTP error log registers and keeps all write protect registers locked except for the “Register 0x32” [7]. When host issues VR Enable command by I^2C/I^3C Basic bus, the PMIC executes Power-on sequence config 0 to Power-on sequence config 2 registers, floats PWR_ GOOD output signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied and re-locks register “Register 0x32” [7]. The PMIC does not require power cycle to re-enable PMIC’s output regulators.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in “Trigger VR Disable”. The PMIC executes power-off sequence config0 (“Register 0x58”) to power-off sequence config2 (“Register 0x5A,”) to preserve the appropriate voltage relationship as configured in the registers. The PMIC assert PWR_GOOD signal low. The PMIC requires power cycle. The VR Enable command with, “Register 0x32” [7] = ‘1’ or VR_EN pin transitions to high has no effect on PMIC and PMIC keeps it PWR_GOOD signal low.

Secure Mode Operation; R1A[4] = ’1’

The PMIC allows host to power down any or all output regulators by any of the two methods below.

1. The VR Disable command with VR_EN pin transitions to low. The PMIC asserts PWR_GOOD signal Low. The PMIC executes power-off sequence config0 (“Register 0x58”) to power-off sequence config2 (“Register 0x5A”) to preserve the appropriate voltage relationship as configured in the registers and enters in P1 state. The host can re-enable the PMIC’s output regulators by VR_EN pin transition to High. The PMIC exits from P1 state and executes power-on sequence config 0 to config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. Note that VR Disable or Enable command on a I^2C/I^3C Basic Bus (i.e “Register 0x32” [7] = ‘0’ or ‘1’) has no effect on the PMIC. Also, configuring one or more bits in “Register0x2F” [6,4:3] to ‘0’ has no effect on the PMIC.
2. If “Register 0x32” [5] =’1’, driving PWR_GOOD input low. The PMIC executes power-off sequence config0 (“Register 0x58”) to power-off sequence config2 (“Register 0x5A,”) to preserve the appropriate voltage relationship as configured in the registers; drives PWR_GOOD signal low and unlocks only “Register 0x32” [7]. The PMIC preserves all register contents including the MTP error log registers and keeps all write protect registers locked except for the “Register 0x32” [7]. When host issues VR Enable command by I^2C/I^3C Basic bus, the PMIC executes Power-on sequence config 0 to Power-on sequence config 2 registers, floats PWR_ GOOD output signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied and re-locks register “Register 0x32” [7]. The PMIC does not require power cycle to re-enable PMIC’s output regulators.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in “Trigger VR Disable”. The PMIC executes power-off sequence config0 (“Register 0x58”) to power-off sequence config2 (“Register 0x5A”) to preserve the appropriate voltage relationship as configured in the registers. The PMIC does not enter in P1 state. The PMIC assert PWR_GOOD signal low. The PMIC requires power cycle. The VR Enable command with either Table 138, “Register 0x32” [7] = ‘1’ or VR_EN

pin transitions to high has no effect on PMIC and PMIC keeps it PWR_GOOD signal low.

PMIC Output Rail Off Timing

The Figure 8 below shows the timing relationship once the PMIC registers VR Disable command internally due to fault condition as listed in ”Events Interrupt Summary”. The waveform shows each buck regulator output soft-stop time and delay time once the soft-stop time expires from each power-off sequence config0 to power-off sequence config2 registers. Note that if more than one regulators are disabled in a power-off sequence config register and if those regulators have different soft-stop time programmed, then the larger value of that soft-stop time is used as a reference for delay timer to start. Each regulator will still follow different soft-stop time to turn off the buck regulator.

The specific example in Figure 8 uses only three power-off sequence config0 to config2 registers and only one buck regulator is disabled in power-off sequence config 0, config 1 and config 2 registers.

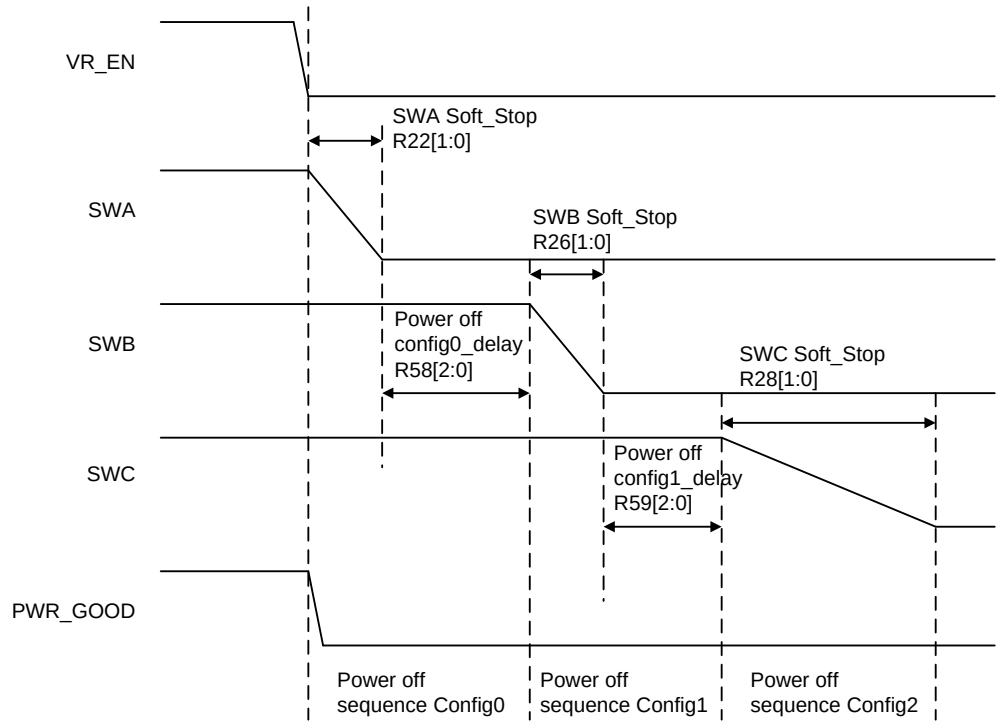


Figure 8. PMIC Power Off Timing Due to Internal Fault Condition

GSI_n Signal

The RTQ5132 features a general purpose interrupt, GSI_n, for signaling any other event to the user. The GSI_n is an open-drain output pin which needs an external pull-up resistor (~10kΩ) to 3.3V or 1.8V.

The interrupts are active Low “latched” signal (when an interrupt event occurs in the RTQ5132, a low level shall be output on the corresponding interrupt pin).

The interrupt pin is held low until both of the following requirements are met:

(1) The condition causing the interrupt (or others condition has occurred since) no longer persists.

(2) The register is cleared through I^2C or I^3C write to the clear bit.

All warning status bits should be latched to ‘1’ (based on their condition occurring). The latch shall remain a ‘1’ until the corresponding clear bit is written with a ‘1’. If an exception bit is cleared, but the condition continues to persist, a new interrupt will be generated (as if it is a new condition).

When GSI_n signal is asserted, the PMIC continues to operate as normal.

The user can query appropriate status registers to determine and isolate the cause of the GSI_n signal assertion.

Table 1. Summary of GSI_n Assertion Events

No	Event Description
1	Input (VIN_BULK) Power Good status.
2	Input (VIN_BULK) Overvoltage protection.
3	Output (SW[A:C] or VLDO_1.8V, VLDO_1.0V) Power Good status.
4	Output (SW[A:C]) Overvoltage protection.
5	Output (SW[A:C]) Undervoltage Lockout protection.
6	LDO Output or VIN_BULK Input Undervoltage Lockout protection.
7	Output (SW[A:C]) Current Limiter Warning event.
8	Output (SW[A:C]) High Current Consumption Warning event.
9	PMIC High Temperature Warning status.
10	PMIC Critical Temperature protection.
11	PEC Error.
12	Parity Error.

Idle State and Quiescent Power State

Quiescent Power State definition: VIN_Bulk nominal = 5.0V. All circuits including PMIC switch output and LDO output regulators are off. VR_EN signal is at static low or high level. I^2C or I^3C Basic interface access is not allowed and is pulled high. PID signal is at static low or high level. This state is only applicable if “Register 0x1A”[4] = ‘1’. This state is labeled as P1 state in below.

Idle Power State definition: VIN_Bulk nominal = 5.0V. All circuits including PMIC switch output and LDO output regulators are on with 0A load. VR_EN signal is at static low or high level. I^2C or I^3C Basic interface access is allowed but bus is pulled high. PID signal is at static low or high level. This state is only applicable if “Register 0x1A”[4] = ‘0’. This state is the same as P3 state but load on all switch outputs regulators and LDO output regulators is 0A.

Table 2. High Level Finite State Description

State	Description
P0	1. VIN_Bulk invalid
P1	1. R1A[4] = ‘1’ 2. Entry from P3 State Only
P2_B	1. Transient from P0 or P1 State; Before VR Enable Command 2. All Switch Regulators are Off 3. All LDOs are on 4. PWR_GOOD Output = L 5. VR_EN Input = L 6. R32[7] = ‘0’
P2_A1 (No Fault Event)	1. All registers are readable. All non-protect registers are writable. 2. All enabled output rails are active. 3. PWR_GOOD is high.
P2_A2 (Fault Event)	1. Transition from P3; After VR Enable Command 2. All Switch Regulators are Off 3. All LDOs are ON 4. PWR_GOOD Output = L 5. VR_EN Input = L or H 6. R32[7] = ‘0’
P3 (Regulation Mode or Bulk Link Monitor Mode)	1. All Switch Regulators are On 2. R32[7] = ‘1’

Function Interrupt - PWR_GOOD and GSI_n Output Signals

This section defines the output functionality of GSI_n pin and PWR_GOOD pin.

When mask register bits are not set, the RTQ5132 asserts its GSI_n output and PWR_GOOD output signals as shown in Table 3 when any event occurs. The table also highlights more events that cause RTQ5132 to generate internally VR Disable command. For remaining events that does not trigger internal VR Disable command, the RTQ5132 continues to operate as normal.

Table 3. Events Interrupt Summary

Status Event	Status Bit	Clear Bit	Mask Bit	Threshold Setting	VR Disable Trigger?	PWR_GOOD Output	GSI_n
VIN_BULK Overvoltage	R08[0]	R10[0]	R15[0]	R1B[7]	Yes	Low	Low
SWA Output Power Good	R08[5]	R10[5]	R15[5]	R21[1:0], R22[7:6]	No	Low	Low
SWB Output Power Good	R08[3]	R10[3]	R15[3]	R25[1:0], R26[7:6]	No	Low	Low
SWC Output Power Good	R08[2]	R10[2]	R15[2]	R27[1:0], R28[7:6]	No	Low	Low
1.8V LDO Power Good	R09[5]	R11[5]	R16[5]	R1A[2]	No	Low	Low
1.0V LDO Power Good	R33[2]	R14[2]	R19[2]	R1A[0]	No	Low	Low
SWA Output Overvoltage	R0A[7]	R12[7]	R17[7]	R22[5:4]	Yes	Low	Low
SWB Output Overvoltage	R0A[5]	R12[5]	R17[5]	R26[5:4]	Yes	Low	Low
SWC Output Overvoltage	R0A[4]	R12[4]	R17[4]	R28[5:4]	Yes	Low	Low
SWA Output Undervoltage	R0B[3]	R13[3]	R18[3]	R22[3:2]	Yes	Low	Low
SWB Output Undervoltage	R0B[1]	R13[1]	R18[1]	R26[3:2]	Yes	Low	Low
SWC Output Undervoltage	R0B[0]	R13[0]	R18[0]	R28[3:2]	Yes	Low	Low
SWA Output Current Limit	R0B[7]	R13[7]	R18[7]	R20[7:6]	No	High	Low
SWB Output Current Limit	R0B[5]	R13[5]	R18[5]	R20[3:2]	No	High	Low
SWC Output Current Limit	R0B[4]	R13[4]	R18[4]	R20[1:0]	No	High	Low
SWA Output High Current /Power	R09[3]	R11[3]	R16[3]	R1C[7:2]	No	High	Low
SWB Output High Current /Power	R09[1]	R11[1]	R16[1]	R1E[7:2]	No	High	Low

Status Event	Status Bit	Clear Bit	Mask Bit	Threshold Setting	VR Disable Trigger?	PWR_GOOD Output	GSI_n
SWC Output High Current /Power	R09[0]	R11[0]	R16[0]	R1F[7:2]	No	High	Low
High Temperature Warning	R09[7]	R11[7]	R16[7]	R1B[2:0]	No	High	Low
Critical Temperature	R08[6]	N/A	N/A	R2E[2:0]	Yes	Low	Low
PEC Error	R0A[3]	R12[3]	R17[3]	N/A	No	High	Low
Parity Error	R0A[2]	R12[2]	R17[2]	N/A	No	High	Low

- The host is expected to read appropriate status registers to determine and isolate the cause of the GSI_n signal assertion or PWR_GOOD signal assertion. The host may attempt to clear or mask the appropriate corresponding interrupt event. The PMIC keeps the GSI_n signal asserted or PWR_GOOD signal asserted until the appropriate corresponding registers are explicitly cleared or masked by the host. Table 3 and Table 4 shows the PMIC's response of GSI_n signal and PWR_GOOD output signal for each event before and after host issues the Clear command. The Table 3 and Table 4 assumes that all mask bits are either '0' or '1' for simplicity.

Table 4. RTQ5132 Response for Clear Command by Host (Part I)

Event	Event Occurred; All Mask Bits = "0"		Clear Command; Event Not Present; All Mask Bits = "0"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
			R2F[1:0] = "00" or "01" or "10"		R2F[1:0] = "00"		R2F[1:0] = "00"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
VIN_BULK Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Power Good	Low	Low	High	High	Low	High	High	High
SWB Output Power Good	Low	Low	High	High	Low	High	High	High
SWC Output Power Good	Low	Low	High	High	Low	High	High	High
1.8V LDO Power Good	Low	Low	High	High	Low	High	High	High
1.0V LDO Power Good	Low	Low	High	High	Low	High	High	High
SWA Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current /Power	High	Low	High	High	High	High	High	High
SWB Output High Current /Power	High	Low	High	High	High	High	High	High

Event	Event Occurred; All Mask Bits = "0"		Clear Command; Event Not Present; All Mask Bits = "0"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
			R2F[1:0] = "00" or "01" or "10"		R2F[1:0] = "00"		R2F[1:0] = "00"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
SWC Output High Current /Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	Power Cycle	Power Cycle	Low	Low	Power Cycle	Power Cycle
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Table 5 shows the RTQ5132's response of GSI_n signal and PWR_GOOD signal for each event before and after user issues the Clear command. The table assumes that all mask bits are '1'.

Table 5. RTQ5132 Response for Clear Command by Host (Part II)

Event	Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
	R2F[1:0] = "01"		R2F[1:0] = "01"		R2F[1:0] = "10"		R2F[1:0] = "10"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
VIN_BULK Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Power Good	High	Low	High	High	High	High	High	High
SWB Output Power Good	High	Low	High	High	High	High	High	High
SWC Output Power Good	High	Low	High	High	High	High	High	High
1.8V LDO Power Good	High	Low	High	High	High	High	High	High
1.0V LDO Power Good	High	Low	High	High	High	High	High	High
SWA Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current /Power	High	Low	High	High	High	High	High	High
SWB Output High Current /Power	High	Low	High	High	High	High	High	High

Event	Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
	R2F[1:0] = "01"		R2F[1:0] = "01"		R2F[1:0] = "10"		R2F[1:0] = "10"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
SWC Output High Current /Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	Power Cycle	Power Cycle	Low	Low	Power Cycle	Power Cycle
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Note that when user masks any of the event in appropriate register, it only masks the assertion of GSI_n output signal or assertion of PWR_GOOD output signal. The PMIC functional behavior remains the same as noted for each event other than assertion of GSI_n output signal and assertion of PWR_GOOD output signal.

Power Good Signal

The PWR_GOOD output signal type can be configured as either output only or input and output through register “Register 0x32”[5]. By default, PWR_GOOD is an output signal. The PWR_GOOD signal can only be configured once, at power on, before issuing VR Enable command (either with VR_EN pin or on I^2C/I^3C Basic bus).The PWR_GOOD signal configuration applies to both secure mode or programmable mode of operation.

Power Good as Output Only Signal

When “Register 0x32” [5] = ‘0’, the PWR_GOOD signal type is output only; the input of PWR_GOOD signal is ignored. The PMIC PWR_GOOD pin indicates status of VIN_Bulk input supply and all output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V). The PMIC floats PWR_GOOD pin when VIN_Bulk input supply is valid and all enabled output regulator’s (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V) tolerances are maintained as configured in the appropriate register space. At first power up, when input supply VIN_Bulk is ramped up and stable, the PMIC keeps PWR_GOOD pin asserted to low; however PMIC updates corresponding status register. By default, the register “Register 0x32”[5] = ‘0’. Once PMIC receives VR Enable command (either with VR_EN pin or on I^2C/I^3C Basic bus) from the host, the PMIC enables all appropriate output regulators and updates corresponding status registers and enters into operating state called as “Regulation”. At this point, PMIC floats PWR_GOOD pin and the external board pullup resistor pulls the pin high as there may be other PMIC on different DIMM may be driving the PWR_GOOD pin low. Once the PWR_GOOD pin is pulled high (i.e no other PMIC is driving the PWR_GOOD pin low), the PMIC remains in ”Regulation” state.

Once the PWR_GOOD pin is high, if PMIC detects any condition either on VIN_Bulk input supply or any of the output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V) that causes the PMIC to update it status registers to indicate the power status is not good, then PMIC asserts PWR_GOOD pin low and keeps it asserted until the host explicitly takes a specific action corresponding to it. The PMIC does not automatically let the PWR_GOOD pin float (i.e get High) even if the condition that triggered the PMIC to assert the PWR_GOOD pin no longer exists. In other words, the PMIC’s PWR_GOOD pin is latched and once latched, it must be explicitly addressed by the host.

PWR_GOOD as Input & Output Signal

When “Register 0x32” [5] = ‘1’, the PWR_GOOD signal type is both input and output and is only applicable after host issues VR Enable command (either with VR_EN pin or on I^2C/I^3C Basic bus). Also note that simultaneous usage of PWR_GOOD pin as IO and VR_EN pin is not allowed and considered an illegal configuration. In other words, if VR_EN pin is intended to be used to turn on and turn off output rails, the PWR_GOOD pin must be configured as output only. If PWR_GOOD pin is intended to be used as IO, the VR_EN pin must be connected to GND on the board.

The PMIC PWR_GOOD pin indicates status of VIN_Bulk input supply and all output regulators (VOUT_A,VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V). The PMIC floats PWR_GOOD pin when VIN_Bulk input supply is valid and all enabled output regulator’s (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V) tolerances are maintained as configured in the appropriate register space.

At first power up, when input supply VIN_Bulk is ramped up and stable, the PMIC keeps PWR_GOOD pin asserted to low; however PMIC updates corresponding status register. The host, prior to issuing VR Enable command on I^2C/ I^3C Basic bus, can configure the register “Register 0x32” [5] = ‘1’.When host issues VR Enable command on I^2C/I^3C Basic bus, the PMIC turns on its output regulators and updates corresponding status registers and enters into operating state called “Regulation”. At this point, the PMIC floats PWR_GOOD pin and waits for external board pullup resistor to pull the pin high as there may be other PMIC on different DIMM may be driving the PWR_GOOD pin low. Once the PWR_GOOD pin is pulled high (i.e no other PMIC is driving the PWR_GOOD pin low), the PMIC automatically enters in to operating state called “Bulk Control Link Monitor”.

Once the PWR_GOOD pin is high, if PMIC detects any condition either on VIN_Bulk input supply or any of the

output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V) that causes the PMIC to update it status registers to indicate the power status is not good, then PMIC asserts PWR_GOOD pin low and keeps it asserted until the host explicitly takes a specific action corresponding to it. The PMIC does not automatically let the PWR_GOOD pin float (i.e get High) even if the condition that triggered the PMIC to assert the PWR_GOOD pin no longer exists. In other words, the PMIC's PWR_GOOD pin is latched and once latched, it must be explicitly addressed by the host.

If PMIC is operating in Secure mode of operation, PMIC allows PWR_GOOD input signal low at any time. The host must keep the PWR_GOOD signal low for minimum tPWR_GOOD_Low_Pulse_Width to issue command to PMIC to execute VR Disable. When PMIC detects PWR_GOOD signal low, the PMIC internally triggers VR Disable command and shuts off all output regulators (the PMIC executes power-off sequence config0 ("Register 0x58") to power-off sequence config2 ("Register 0x5A"); drives PWR_GOOD signal low and unlocks only "Register 0x32" [7]. The PMIC preserves all register contents including the MTP error log registers and keeps all write protect registers locked except for the "Register 0x32" [7]. As long as there is valid VIN_Bulk input supply, the PMIC allows read access to all its configuration registers. The PMIC allows write access to non-locked configuration registers and register "Register 0x32" [7]. If host issues VR Enable command by I^2C/I^3C bus, the PMIC executes Power-on sequence config 0 to Power-on sequence config 2 registers, floats PWR_GOOD output signal and re-locks register "Register 0x32" [7].

If PMIC is in Programmable mode of operation, PMIC allows PWR_GOOD input signal low at any time. The host must keep the PWR_GOOD signal low for minimum tPWR_GOOD_Low_Pulse_Width to issue command to PMIC to execute VR Disable. When PMIC detects PWR_GOOD signal low, the PMIC internally triggers VR Disable command and shuts off all output regulators (the PMIC executes power-off sequence config0 ("Register 0x58") to power-off sequence config2 ("Register 0x5A,"); drives PWR_GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. As long as there is valid VIN_Bulk input supply, the PMIC allows read and write access to all its configuration registers. The host can issue VR Enable command with VR_EN command on I^2C/I^3C Basic bus (i.e. Register 0x32" [7] = '1') again to turn on the PMIC's output regulator and PMIC will execute Power On Config0 to Config2 registers and floats PWR_GOOD output signal.

Input Overvoltage Protection

An input overvoltage protection mechanism is implemented to limit the voltages to the RTQ5132. The RTQ5132 actively monitors the input voltage VIN_BULK rail.

There are conditions where RTQ5132 recognizes the input overvoltage event.

(1) VIN_BULK input goes above the threshold set in "Register 0x1B" [7].

When either one event occurs for a period longer than tInput_OV_GSI_Assertion time (max. = 10μs), then RTQ5132 sets the "Register 0x08" [1:0] accordingly and drives GSI_n output signal as shown in Table 3 at the same time. Note that at this point, the RTQ5132 does not assert PWR_GOOD output signal. The RTQ5132 allows access to all registers and continues to operate as normal. The host can clear the VIN_BULK input overvoltage status register by writing '1' to "Register 0x10" [1:0] appropriately or by writing '1' to global status clear "Register 0x14" [0]. If the input overvoltage condition is still present, then RTQ5132 will continue to assert GSI_n output signal and the status "Register 0x08" [1:0] will remain at '1'.

In non-write protect mode, if VIN_BULK input supply overvoltage condition persists greater than tInput_OV_VR_Disable time (max. = 20μs), then RTQ5132 internally generates VR Disable command and disables all of its switching output regulators and asserts PWR_GOOD signal. The output regulators stop switching once VR disable command is issued by RTQ5132, and following the power-off sequence Config0 to Config3 to discharge the output voltage by an internal discharging resistor. The RTQ5132 keeps VLDO_1.8V and VLDO_1.0V LDO output regulators active. The RTQ5132 allows access to all registers. The user can query the PMIC register space to determine the cause of the PWR_GOOD signal assertion and

GSI_n signal assertion. Once user determines the cause, the user must first clear the VIN_BULK input overvoltage status register as well as any other relevant status registers individually or by writing '1' to global status clear "Register 0x14" [0] which triggers the GSI_n signal to be de-asserted. If the input overvoltage condition is still present, then RTQ5132 will continue to assert GSI_n output signal and the status "Register 0x08" [0] will remain at '1'. Once the status register is cleared and GSI_n output signal is de-asserted, the user may re-enable the RTQ5132's output switching regulator by issuing VR Enable command. The RTQ5132 enables output switching regulators and ensures PWR_GOOD signal is floated when all of its output regulators are normal and input overvoltage condition is no longer present.

In write protect mode, if VIN_BULK input supply overvoltage condition persists greater than tInput_OV_VR_Disable time (max. = 20μs), then RTQ5132 internally generates VR Disable command and disables all of its switching output regulators by executing Power-off sequence configuration registers, asserts PWR_GOOD signal low and returns to configuration mode. The RTQ5132 keeps its VLDO_1.8V and VLDO_1.0V output regulators active.

Output Power Good Status (SWABC, LDO_1.8V, LDO_1.0V)

The RTQ5132 provides output power good indicators to determine that the output regulators have crossed the desired voltage tolerance from its nominal programmed setting. The nominal programmed setting for output regulator SWA, SWB and SWC is programmed in "Register 0x21" [7:1], "Register 0x25" [7:1] and "Register 0x27" [7:1] respectively. The RTQ5132 offers the PWR_GOOD condition to be set independently for low-side threshold and high-side threshold regarding to voltage regulators (SWA, SWB, and SWC). In addition, there are two LDO regulators: VLDO_1.8V and VLDO_1.0V in the RTQ5132.

There are four possibilities where RTQ5132 recognizes the output power good event for any output regulator.

(1) Output voltage goes below the threshold set in "Register 0x21" [0] for SWA or "Register 0x25" [0] for SWB or "Register 0x27" [0] for SWC.

(2) Output voltage goes above the threshold set in "Register 0x22" [7:6] for SWA or "Register 0x26" [7:6] for SWB or "Register 0x28" [7:6] for SWC.

(3) LDO output VLDO_1.8V goes below the threshold set in "Register 0x1A" [2].

(4) LDO output VLDO_1.0V goes below the threshold set in "Register 0x1A" [0].

When either event occurs for a period longer than Output_PWR_GOOD_GSI_Assertion time (max. = 10μs), then RTQ5132 sets the "Register 0x08" [5:2] or "Register 0x09" [6:5] or "Register 0x33" [2] appropriately and drives PWR_GOOD and GSI_n output signal as shown in Table 3 at the same time. The RTQ5132 continues to operate but DDR5 DIMM functionality may not be guaranteed.

The user can query the register space to determine and identify the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once user determines the cause, the user may clear the appropriate status register individually or by writing '1' to global status clear "Register 0x14" [0] which triggers the GSI_n signal to be de-asserted and PWR_GOOD signal to be de-asserted. If the output power not good condition is still present then RTQ5132 will continue to assert GSI_n output signal and assert PWR_GOOD signal and the appropriate status "Register 0x08" [5:2] or "Register 0x09" [6:5] or "Register 0x33" [2] will remain at '1'. If the output power not good condition persists, the user may set the appropriate mask register to remove GSI_n or PWR_GOOD output signal as shown in Table 4 and Table 5.

Output Overvoltage Protection (SWABC)

An output overvoltage protection mechanism is implemented to limit the voltages on the RTQ5132 output regulators. The RTQ5132 actively monitors the output voltage on each enabled regulator.

There are three possibilities where RTQ5132 recognizes the overvoltage event.

(1) SWA output regulator goes above the threshold set in "Register 0x22" [5:4].

(2) SWB output regulator goes above the threshold set in "Register 0x26" [5:4].

(3) SWC output regulator goes above the threshold set

in “Register 0x28” [5:4].

According to different DDR5 application environments, the “Register 0x4F” [7] has different setting.

Condition1. DDR5 SODIMM/UDIMM Environment - “Register 0x4F” [7] = ‘0’:

In non-write protect mode, if any output overvoltage condition persists longer than tOutput_OV_VR_Disable time (max. = 20μs), then RTQ5132 internally generates VR Disable command and disables all of its switching output regulators, sets “Register 0x0A” [7:4] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The output regulators stop regulation once VR disable command is issued by RTQ5132, and following the power-off sequence Config0 to Config3 to discharge the output voltage by tracking the soft-stop ramping down voltage. In order to prevent catastrophic condition that VPP(SWC) voltage is lower than VDD(SWA) or VDDQ(SWB) during power off, the RTQ5132 postpones the power-off sequence of VPP(SWC) until the VDD(SWA) and VDDQ(SWB) has been powered off as OVP event is detected. The VLDO_1.8V and VLDO_1.0V LDO output regulators keep active.

The user can query the register space to determine the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once user determines the cause, the user must first clear the appropriate output overvoltage status register as well as any other relevant status registers individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. Once the status register is cleared and GSI_n output signal is de-asserted, the user may re-enable the PMIC’s output switching regulator by issuing VR Enable command. The RTQ5132 enables output switching regulators and ensures PWR_GOOD signal is floated when all of its output regulators are normal.

In write protect mode, if any output overvoltage condition persists greater than tOutput_OV_VR_Disable time (max. = 20μs) then RTQ5132 internally generates VR Disable command and disables all of its switching output regulators by executing Power-off sequence configuration registers, asserts PWR_GOOD signal low and returns to configuration mode. The RTQ5132 keeps its VLDO_1.8V and VLDO_1.0V output regulators active.

Condition2. DDR5 UDIMM or Other Custom Environment - “Register 0x4F” [7] = ‘1’

In non-write protect mode, if any output overvoltage condition persists longer than tOutput_OV_VR_Disable time (max. = 20μs), then RTQ5132 internally generates VR Disable command to disable only the affected switching output regulator, sets “Register 0x0A” [7:4] appropriately, asserts PWR_GOOD and asserts GSI_n output signal and continues to operate normal on other output regulators. Once the affected switching output regulator receives VR Disable command, the regulator stops switching and turns on the internal discharging resistor. The VLDO_1.8V and VLDO_1.0V LDO output regulators keep active.

The user may query the register space to determine the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once user determines the cause, the user must first clear the appropriate output overvoltage status register as well as any other relevant status registers individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted.

Once the status register is cleared and GSI_n output signal is de-asserted, the user can re-enable the RTQ5132’s output switching regulator by issuing VR Enable command. The RTQ5132 enables output switching regulator and floats PWR_GOOD signal when all of its output regulators are normal. Note that in this case, though user issues VR Enable command, it only turns on the affected regulator that was disabled, other rails keep operating normally.

It should be noticed that the write protect mode is not allowed when “Register 0x4F” [7] = ’1’.

Output Undervoltage & VIN_BULK Undervoltage Lockout Protection

An output undervoltage lockout protection mechanism is implemented to limit the voltages on the RTQ5132 output regulators. The RTQ5132 actively monitors the output voltage on each enabled regulator.

There are four possibilities where RTQ5132 recognizes the undervoltage lockout event.

(1) SWA output regulator goes below the threshold set

in “Register 0x22” [3:2].

(2) SWB output regulator goes below the threshold set in “Register 0x26” [3:2].

(3) SWC output regulator goes below the threshold set in “Register 0x28” [3:2].

(4) LDO output regulator goes below the 3.6V (default) or VIN_BULK Input Voltage goes below 4V.

According to different DDR5 application environments, the “Register 0x4F” [7] has different settings.

Condition1. DDR5 SODIMM/UDIMM Environment - “Register 0x4F” [7] = ‘0’:

In non-write protect mode, if any undervoltage condition (among four possibilities listed above) persists longer than tOutput_UV_VR_Disable time (max. = 20μs), then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets “Register 0x0B” [3:0], “Register 0x33” [3] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The output regulators stop regulation once VR disable command is issued by RTQ5132, and following the power-off sequence Config0 to Config3 to discharge the output voltage by tracking the ramping down voltage reference. For SWA/B/C/D output undervoltage events, the regulator increases the current-limit threshold to 1.34 times deserved threshold for 35us as soon as UVP event is triggered, then follows the power-off sequence to discharge output voltage. The special mechanism of UVP shutdown is to prevent the abnormal power-off sequence between VPP and VDD/VDDQ. The VLDO_1.8V and VLDO_1.0V LDO output regulators keep active.

The user can query the register space to determine the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once user determines the cause, the user must first clear the appropriate output under-voltage status register as well as any other relevant status registers individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. Once the status register is cleared and GSI_n output signal is de-asserted, the user may re-enable the RTQ5132’s output switching regulator by issuing VR Enable command assuming valid VIN_BULK input voltage. The RTQ5132 enables output switching regulators and floats PWR_GOOD signal when all of its output regulators are normal.

In write protect mode, if any output undervoltage condition (among five possibilities listed above) or VIN_BULK input voltage condition listed above persists greater than tOutput_UV_VR_Disable time (max. = 20μs) then RTQ5132 internally generates VR Disable command and disables all of its switching output regulators by executing Power-off sequence configuration registers, asserts PWR_GOOD signal low and returns to configuration mode. The RTQ5132 keeps its VLDO_1.8V and VLDO_1.0V output regulators active.

Condition2. DDR5 UDIMM or Other Custom Environment - “Register 0x4F” [7] = ‘1’

In non-write protect mode, if any output undervoltage condition (First four possibilities listed above) as listed above persists longer than tOutput_UV_VR_Disable time (max. = 20μs), then RTQ5132 internally generates VR Disable command to disable only the affected switching output regulator, sets “Register 0x0B” [3:0] appropriately, asserts PWR_GOOD and asserts GSI_n output signal and continues to operate normal on other output regulators. Once the affected switching output regulator receives VR Disable command, the regulator turns on low-side MOSFET to discharge inductor current until zero crossing point. Note that if the fifth condition (LDO output goes below 3.6V (default) or VIN_BULK input goes below 4V) listed above persists longer than tOutput_UV_VR_Disable time (max. = 20μs), then the RTQ5132 internally generates VR Disable command and disables all of its switching output regulators, sets “Register 0x0B” [3:0] and “Register 0x33” [3] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The output regulators stop regulating once VR disable command is issued by RTQ5132, and follow the power-off sequence Config0 to Config3 to discharge the output voltage. The RTQ5132 keeps VLDO_1.8V and VLDO_1.0V LDO output regulators active.

The user can query the register space to determine the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once user determines the cause, the user must first clear the appropriate output undervoltage status register as well as any other relevant status registers individually or by writing ‘1’ to global status

clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. Once the status register is cleared and GSI_n output signal is de-asserted, the user can re-enable the RTQ5132’s output switching regulator by issuing VR Enable command. The RTQ5132 enables output switching regulator and ensures PWR_GOOD signal is floated when all of its output regulators are normal. Note that in this case, though user issues VR Enable command, it only turns on the affected regulator that was disabled.

It should be noticed that the write protect mode is not allowed when “Register 0x4F” [7] = ’1’.

Output Current Limiter Warning Event

The RTQ5132 has output current limiter mechanism to limit the current on the output voltage regulators. The inductor current is actively monitored through low-side MOSFET during conduction. The voltage drop across phase node to PGND is compared with current-limit threshold, which is set in “Register 0x20” [7:0], and the valley point of inductor current is limited cycle-by-cycle. When output voltage regulators operate in current limit mode, the PWM on-time one-shot should wait inductor current discharging below current-limit threshold to trigger next on-time output even the output voltage has been below the reference feedback voltage. Hence, the output voltage starts dropping in current limit condition due to insufficient energy to output load. The output undervoltage event will occur after that if output voltage is lower than undervoltage threshold as describes in previous section. The protection mechanism of output current limit is shown in Figure 9.

There are three possibilities where RTQ5132 recognizes the current limiter event.

(1) SWA output regulator current goes above the threshold set in “Register 0x20” [7:6].

(2) SWB output regulator current goes above the threshold set in “Register 0x20” [3:2].

(3) SWC output regulator current goes above the threshold set in “Register 0x20” [1:0].

When either event occurs for a period longer than tOutput_Current_Limiter time (max. = 10μs) then RTQ5132 sets the “Register 0x0B” [7:4] appropriately, drives GSI_n output signal as shown in Table 3 at the same time. The RTQ5132 continues to operate as normal.

The user can query the register space to determine the cause of the GSI_n signal assertion. Once user determine the cause, the user may clear the appropriate output current limiter status register as well as any other status registers individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. If the output current limiter condition is still present, then RTQ5132 will continue to assert GSI_n output signal and the appropriate status “Register 0x0B” [7:4] will remain at ‘1’. If the output current limiter condition persists, the user can set the appropriate mask register to remove the GSI_n output signal as shown in Table 4 and Table 5.

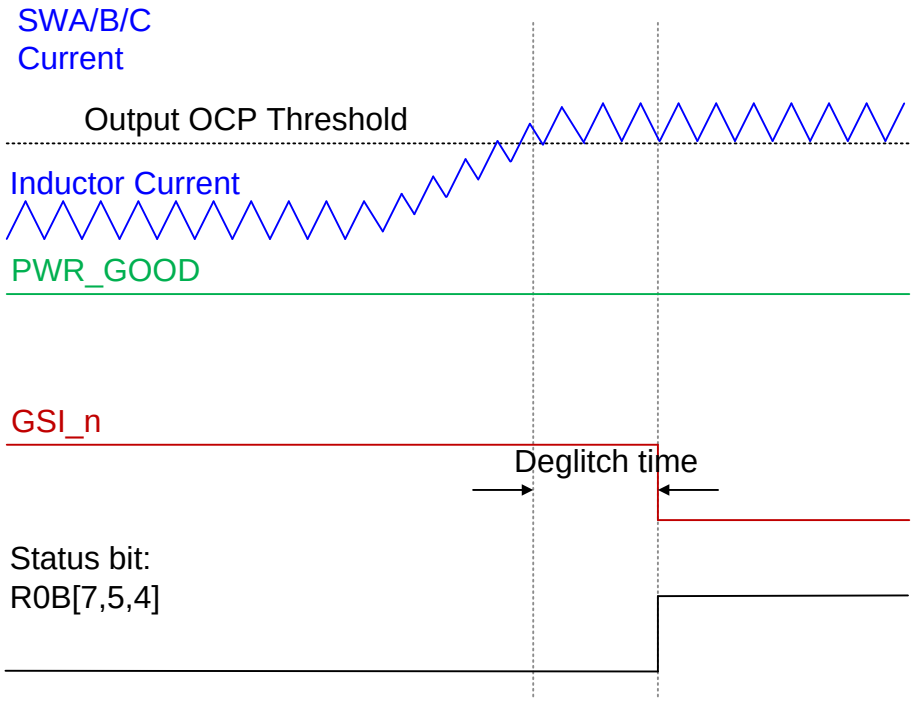


Figure 9. Output Current Limiter Protection

Output High Current Consumption Warning Event

The RTQ5132 supports high output current consumption warning mechanism for each of its regulator output. Through sensing the voltage drop across low-side MOSFET during conduction, the inductor current can be detected. If enabled, the RTQ5132 actively monitors the average output current of the regulator.

There are three possibilities where RTQ5132 recognizes the high output current consumption.

(1) SWA output regulator average current goes above the threshold set in “Register 0x1C” [7:2].

(2) SWB output regulator average current goes above the threshold set in “Register 0x1E” [7:2].

(3) SWC output regulator average current goes above the threshold set in “Register 0x1F” [7:2].

When either event occurs, then RTQ5132 sets the “Register 0x09” [3:0] appropriately, and drives GSI_n output signal as shown in Table 3 at the same time. The RTQ5132 continues to operate as normal.

The user can query the register space to determine the cause of the GSI_n signal assertion. Once user determines the cause, the user can clear the appropriate output current consumption warning status register as well as any other status registers individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. If the output current consumption warning condition is still present then RTQ5132 will continue to assert GSI_n output signal and the appropriate status “Register 0x09” [3:0] will remain at ‘1’. If the output current consumption warning condition persists, the user can set the appropriate mask register to remove GSI_n output signal as shown in Table 4 and Table 5.

PMIC LDO Output Failure

In the event where RTQ5132 LDO outputs (VLDO_1.8V or VLDO_1.0V) failure occurs and RTQ5132 cannot reliably support external communication, the RTQ5132 has no control of PWR_GOOD signal and it is floated. The RTQ5132 returns to “offline” state.

PMIC High Temperature Warning and Critical Temperature Protection

The RTQ5132 provides a high temperature warning mechanism as well as critical temperature shutdown. An internal temperature sensor is placed near the heating MOSFET to detect the die temperature and protects RTQ5132 from over-heat operation. There are two registers associated with RTQ5132’s die temperature: The high temperature warning threshold “Register 0x1B” [2:0] and shutdown temperature threshold “Register 0x2E” [2:0]. The value programmed in the shutdown temperature register must be equal or greater than value programmed in a warning threshold register.

If the die temperature goes above the threshold set in “Register 0x1B” [2:0] for a period longer than tHigh_Temp_Warning time (max. = 10μs), the RTQ5132 sets the “Register 0x09” [7] and drives GSI_n output signal as shown in Table 3 at the same time.

The user can query the register space to determine the cause of the GSI_n signal assertion. Once user determines the cause, the user can clear the temperature warning status register as well as any other status registers individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. If the high temperature warning condition is still present, then RTQ5132 will continue to assert GSI_n output signal and the appropriate status “Register 0x09” [7] will remain at ‘1’. If the high temperature warning condition persists, the user can set the appropriate mask register to remove GSI_n output signal as shown in Table 4 and Table 5.

If the die temperature goes above the threshold set in “Register 0x2E” [2:0] for a period longer than tShut_Down_Temp time (max.=10μs), the RTQ5132 internally generates VR Disable command and disables all of its switching output regulators, sets the code in “Register 0x05” [2:0], updates “Register 0x08” [6], and drives GSI_n and PWR_GOOD output signal as shown in Table 3 at the same time. The VLDO_1.8V and VLDO_1.0V output regulator keep active.

The user is expected to monitor the temperature status registers. When the temperature drops below the threshold, the user must re-start the RTQ5132 by going

through the power cycle of the VIN_BULK input supply.

Packet Error Code (PEC) & Parity Error Event

There are two types of error checking done by the RTQ5132. Parity error checking and packet error checking. By default, the parity error checking is always enabled and packet error checking is disabled. The user may enable the packet error checking at any time. The parity error is checked for each byte in a packet except for the device select code byte from the user. The user sends parity error information in “T” bit.

I^3C Basic defines S0, S1, S2, S3, S4, S5, S6 error detection for slave devices. Only S1 and S2 error detection is supported by the RTQ5132 for parity checking. All other errors are not supported and not applicable.

In I^3C Basic mode, on RTQ5132’s primary management interface, PEC function and parity function can be enabled. If enabled, when RTQ5132 detects either PEC error or parity error, the RTQ5132 sets the “Register 0x0A” [3:2] appropriately, drives GSI_n output signal as shown in Table 3, continues to operate as normal, and allows access to all registers.

The user can query the register space to determine the cause of the GSI_n signal assertion. Once user determines the cause, the user can clear the status register individually or by writing ‘1’ to global status clear “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. No further action is needed by the user at this point.

RTQ5132 Output Regulator Control Topology

The RTQ5132 applies A^2RCOT (Accurate Adaptive Ramp COT) to regulate the output voltage of VDD, VDDQ and VPP. The SWA and SWB can operate in either single phase mode or dual-phase mode. When operating as dual-phase mode, the interleaving PWM control is applied to balance the output current.

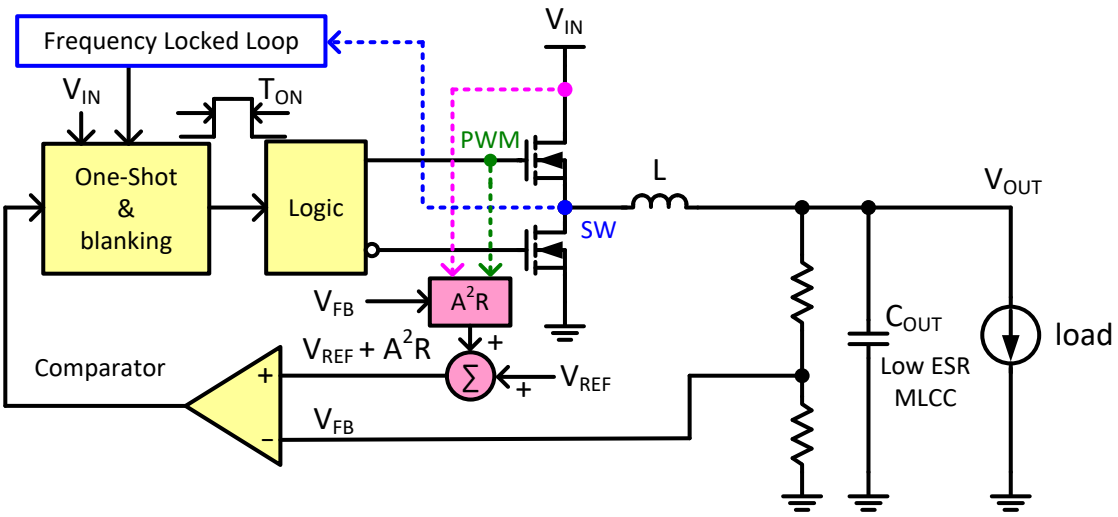


Figure 10. A^{2}RCOT Control Mechanism

Figure 10 illustrates a standard A^{2}RCOT control Buck converter. In order to achieve good stability with low-ESR ceramic capacitors, A^{2}RCOT generates an internal ramp by sensing V_{IN}, V_{FB} and PWM signal. The internal ramp is in phase with PWM signal and its magnitude is proportional to V_{IN}. Moreover, the average of V_{FB} can be well regulated at V_{REF} which makes good output load and line regulation. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

However, making the on-time proportional to V_{OUT} and inversely proportional to V_{IN} is not sufficient to achieve good constant-frequency behavior for following reasons. The voltage drops across MOSFET and inductor make equivalent conversion ratio to be smaller than ideal duty ratio. That is, the switching frequency is not fixed at different output load conditions. Frequency is increasing at higher loading and junction temperature as compared to smaller loading and junction temperature.

One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. The A^{2}RCOT uses the frequency locked loop, measuring the actual switching frequency and modifying the on-time with a feedback loop to make the average switching frequency in the desired range.

The RTQ5132 control algorithm is simple to understand as depicted in Figure 11. The feedback voltage is compared to the reference voltage, V_{REF}, with the accurate adaptive ramp (A^{2}R) added. When the feedback signal is less than the combined reference, the on-time one-shot is triggered as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

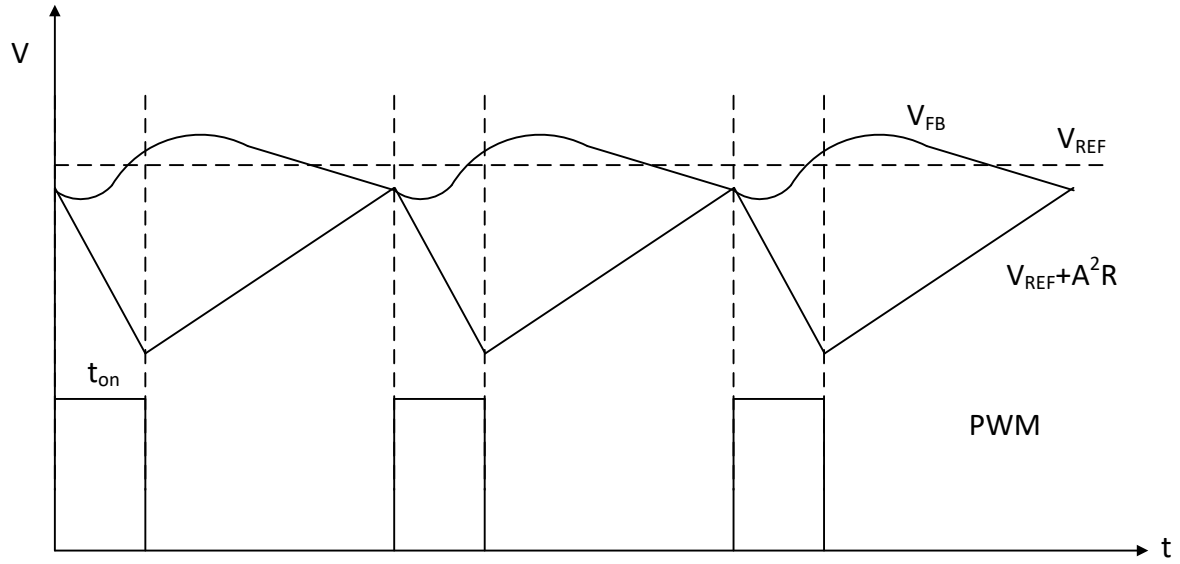


Figure 11. A^2RCOT PWM Control Diagram

Regulator Operating Mode Selection

The RTQ5132 offers two kinds of PWM operation in the light load. One is diode emulation mode (DEM), and another is forced continuous conduction mode (FCCM). The user can switch between DEM and FCCM by the “Register 0x29” [7:6], “Register 0x29” [3:2], “Register 0x2A” [7:6] and “Register 0x2A” [3:2] in diagnostic mode or in the configuration state of FSM before issuing the VR_EN command. The details of the two operation modes are described below.

(1) DEM (Diode Emulation Mode)

In diode emulation mode, the RTQ5132 automatically reduces switching frequency at light load conditions to maintain high efficiency. The reduction of frequency is achieved smoothly. As the output current decreases from heavy load conditions, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative current to flow when the inductor free-wheeling current becomes negative. As the load current is further decreased, it takes longer and longer time to discharge the output capacitor to the level that requires the next “ON” cycle. Contrarily, when the output current increases from light load to heavy load, the switching frequency increases to the pre-set value as the inductor current reaches the continuous conduction. The transition load point between DEM and CCM operation is shown in Figure 12 and can be calculated as follows:

$$I_{LOAD\_BCM} = \frac{V_{IN} - V_{OUT}}{2L} \times t_{ON}$$

, where t_{ON} is the on-time of high-side MOSFET.

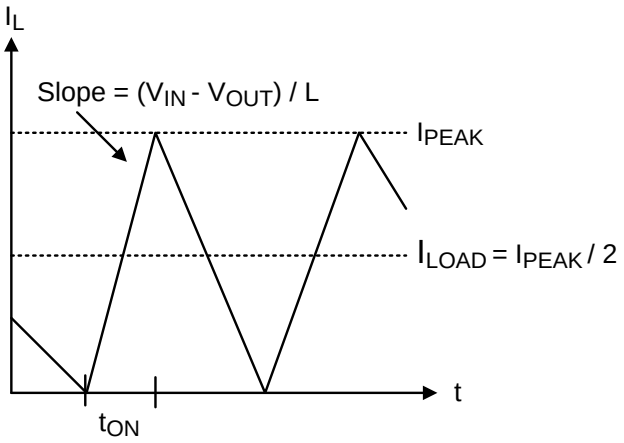


Figure 12. Boundary Condition of DEM/CCM

The switching frequency in DEM can be calculated as follows:

$$f_{SW}(I_{LOAD}) = \frac{2LI_{LOAD}}{V_{IN}t_{ON}^2\left(\frac{V_{IN}}{V_{OUT}}-1\right)}$$

, where I_{LOAD} is smaller than I_{LOAD_BCM}.

As can be shown in the equation, switching frequency is a function of output load current, I_{LOAD}, and it is proportional to I_{LOAD}, which means it becomes higher at heavy load and reduces to almost zero at a very light load. Besides, inductor selection can also change the switching frequency in DEM. Choosing large inductance makes more switching loss as compared to small inductance. However, the core loss of inductor increases with larger inductor current ripple for a given inductor. That is, proper selection of inductor based on efficiency target is important.

Moreover, in order to achieve smooth transition from DEM to CCM or backward, during discontinuous switching, the on-time is immediately increased to add “hysteresis” to discourage the IC from switching back to continuous switching unless the load increases substantially. The RTQ5132 returns to continuous conduction as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced back to the length needed for presetting switching frequency and encouraging the circuit to remain in continuous conduction, preventing repetitive mode transitions between continuous switching and discontinuous switching.

(2) FCCM (Forced Continuous Conduction Mode)

Unlike diode emulation mode (DEM) that enables zero current detection (ZDC) to reject negative inductor current during low-side MOSFET turns on. The inductor current can be negative until next on-time is generated in FCCM. The switching frequency is fixed from no load to full load. Therefore, benefits like better transient response from light load to heavy load and smaller EMI/EMC come along with FCCM. Nevertheless, poor efficiency in light load is a tradeoff.

Analog-to-Digital Converter (ADC)

The RTQ5132 supports analog to digital converter (ADC) to monitor input supply voltages VIN as well as output voltage regulator voltage (SWA, SWB, SWC, VOUT_1.8V and VOUT_1.0V). The “Register 0x30” [7:3] allows to enable the ADC and select the desire input supply voltage or output supply voltage. The “Register 0x31” [7:0] provides the actual voltage measurement. The accuracy of the voltage measurement is as follows:

Table 6. RTQ5132 ADC Accuracy Table

Input Rail	ADC Range	ADC Accuracy
SWA, SWB Output Voltage	1050mV to 1160mV	± 1 LSB
	Outside of 1050mV to 1160mV	± 3 LSB
SWC Output Voltage	1750mV to 1850mV	± 1 LSB
	Outside of 1750 mV to 1850mV	± 3 LSB
VOUT_1.8V, VOUT_1.0V Output Voltage, VIN Input Voltage	--	± 3 LSB

The RTQ5132 also monitors output voltage regulator current or power (SWA, SWB and SWC) and updates “Register 0x0C” [7:0] for SWA, “Register 0x0E” [5:0] for SWB and “Register 0x0F” [5:0] for SWC. The “Register 0x1B” [6] allows user to select whether RTQ5132 should report current measurements or power measurements. The current or power measurement reported in this registers are an average measurement over time period defined in “Register 0x30” [1:0]. If “Register 0x1B” [6] = ‘1’, the “Register 0x1A” [1] allows user to select whether RTQ5132 should report individual rail power or total power in “Register 0x0C” [7:0]. The register update frequency of this register is configured in “Register 0x30” [1:0]. The accuracy of the current (0.5A to 4A) or corresponding power measurement is ± 3 LSB or ± 6 LSB respectively. The accuracy of the current measurement (< 0.5 A) is ± 4 LSB or corresponding power measurement is ± 7 LSB respectively.

If “Register 0x1A” [1] = ‘1’, the accuracy of total power reported in “Register 0x0C” = ± 12 LSB

Besides, the RTQ5132 die temperature is also monitored and converted to ADC value, the temperature is reported in “Register 0x33” [7:5]. The ADC for temperature automatically works as die temperature is higher than 85°C.

Table 7. General Purpose of ADC Units

Default Monitoring (5-channel) ± User Selection (1-channel)			
Channel Sensor	**Type**	**Monitor Register**	**Current/Power Measurement Selector**
SWA Output Current or Power	Default monitor	R0C[7:0]	R1B[6]=0 Set for current R1B[6]=1 Set for power R1A[1]=0 Report power for single switcher output R1A[1]=1 Report the sum of power for all switcher outputs (SWA,SWB,SWC)
SWB Output Current or Power		R0E[5:0]	
SWC Output Current or Power		R0F[5:0]	
PMIC die Temperature		R33[7:5]	
SWA Output voltage	User selection R30[6:3]	R31[7:0]	
SWB Output voltage			
SWC Output voltage			
VIN Input voltage			
VLDO_1.8V Output voltage			
VLDO_1.0V Output voltage			

PMIC Address ID (PID)

The RTQ5132 has PID input pin which allows assigning up to three different unique ID for I^2C and I^3C Basic protocol.

At first power on, when VIN_BULK input is applied, the RTQ5132 automatically senses its ID as shown in Table 8.

Table 8. PMIC ID

PID Pin Connection on DIMM Board	PMIC ID	Comment
Short to GND	PID = 1001	PMIC can be configured
Floating	PID = 1000	
Short to 1.8V	PID = 1100	Connected to RTQ5132’s VLDO_1.8V

Error Injection

The RTQ5132 offers error injection capability for the purpose of debug, test and validation at various stages as well as to isolate and map out faulty PMIC in memory subsystem for normal application environment. There are two conditions for error injection test.

(1) Error Injection Function Usage prior to VR Enable:

Prior to VR Enable command, the Error injection function can be invoked by setting error injection enable bit “Register 0x35” [7] = ‘1’ during the configuration state. If any of either VIN_BULK UV/OV or SWx OV/UV or Critical Temp Shutdown error is injected prior to VR Enable command, the RTQ5132 will not execute power-on sequence and will not enable output regulators when receiving VR Enable command. The RTQ5132 will not update error log registers (“Register 0x04” to “Register 0x06”). The RTQ5132 enters in secure mode if “Register 0x2F” [2] = ‘0’.

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(2) Error Injection Function Usage after VR Enable:

After RTQ5132 output regulators are enabled with VR Enable command and RTQ5132 is in programmable mode, the error injection function can be invoked by setting error injection enable bit “Register 0x35” [7] = ‘1’. If any of either VIN_BULK UV/OV or SWx OV/UV or Critical Temp Shutdown error is injected, the RTQ5132 executes power-off sequence to disable output regulators and updates the error log registers (“Register 0x04” to “Register 0x06”) as well as status registers accordingly.

On the other hand, after RTQ5132 output regulators are enabled with VR Enable command and RTQ5132 is in secure mode, the error injection enabling “Register 0x35” [7] = ‘1’ is disallowed. The RTQ5132 ignores any attempts to inject any error and will not execute power-off sequence to disable output regulators and will not update any error log or status registers.

To exit error injection mode of operation, the RTQ5132 requires power cycle of VIN_BULK input supply.

Absolute Maximum Ratings (Note1)

- Supply Input Voltage, VINA, VINB, VINC ---------- –0.3V to 6V
- Supply Input Voltage, VIN ---------- –0.3V to 6V
- AGND to PGND ---------- –0.3V to 0.3V
- Switching PIN, SWA, SWB, SWC
  - DC ---------- –0.3V to 6V
  - < 25ns ---------- –3V to 9V
- Boot Voltage
  - BOOT to SWA (BOOT-SWA) ---------- –0.3V to +6V
  - BOOT to SWB (BOOT-SWB) ---------- –0.3V to +6V
  - BOOT to SWC (BOOT-SWC) ---------- –0.3V to +6V
- Other I/O ---------- –0.3V to +6V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-28L 3x4 (FC) ---------- 2.43W
- Package Thermal Resistance (Note 2)

  WQFN-28L 3x4 (FC), θ_{JA} ---------- 41°C/W

  WQFN-28L 3x4 (FC), θ_{JC} ---------- 15.8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- –40°C to 155°C
- Storage Temperature Range ---------- –55°C to 150°C
- ESD Susceptibility (Note 3)

  HBM ---------- 2kV

  CDM ---------- 500V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{INA}, V_{INB}, V_{INC}, V_{IND} ---------- 4.25V to 5.5V
- Supply Input Voltage, V_{IN} ---------- 4.25V to 5.5V
- Junction Temperature Range ---------- –10°C to 125°C
- Ambient Temperature Range ---------- 0°C to 85°C

Electrical Characteristics

(V_{IN_SWA} = V_{IN_SWB} = V_{IN_SWC} = 5V, V_{IN} = 5V, T_A = −10°C to 105°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply Electrical Characteristics						
Bulk Input Supply Voltage Ramp Up Rate	VIN_Bulk_Ramp_Up	The ramp up rate between 300 mV and 4.0V	0.1	--	3	V/ms
Bulk Input Supply Voltage Ramp Down Rate	VIN_Bulk_Ramp_Down	The ramp down rate between 4.0 V and 300mV.	0.5	--	1	V/ms
VIN Supply Current	I_{Q_VIN}	T_A = 25°C; VIN = VIN_Bulk = 5V, VR_EN = 0, All circuitry including output regulators and LDOs are off.	--	--	25	μA
		T_A = 25°C; I_{OUT} = 0mA, all LDO, SWA to SWC on, no switching	--	1.9	--	mA
VIN Power Good and OVP Threshold						
VIN Power Good High Threshold			--	4	--	V
VIN Power Good Low Threshold			--	3.8	--	V
VIN Overvoltage Threshold		Setting by reg_0x1B"[7] = "0"	--	6	--	V
I^2C, I^3C and Interface DC Electrical Specification						
SDA, SCL I^2C Operate Frequency	f_{SCL}		0.01	--	1	MHz
SDA, SCL I^3C Operate Frequency	f_{SCL}		0.01	--	12.5	MHz
SDA, SCL Input High Voltage	V_{IH}		0.7	--	3.6	V
SDA, SCL Input Low Voltage	V_{IL}		−0.3	--	0.3	V
PWR_GOOD, VR_EN Input High Voltage	V_{IH}		1.26	--	3.6	V
PWR_GOOD, VR_EN Input Low Voltage	V_{IL}		−0.3	--	0.3	V
PID Input High Voltage	V_{IH}		1.2	--	--	V
PID Input Low Voltage	V_{IL}		--	--	0.2	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SDA Output High Voltage	V_{OH}	I_O = -3mA	0.75	--	--	V
SDA, GSI_n, PWR_PGOOD Output Low Voltage	V_{OL}	I_O = 3mA	--	--	0.3	V
SDA Output High Current	I_{OH}		–3	--	--	mA
SDA, GSI_n, PWR_PGOOD Output Low Current	I_{OL}		--	--	3	mA
SDA Output Pull-Up Driver Impedance	R_{ON}		--	40	--	Ω
SDA Output Pull-Down Driver Impedance	R_{ON}		--	20	--	Ω
GSI_n, PWR_GOOD Output Pull-Down Driver Impedance	R_{ON}		--	50	--	Ω
SWA/B Rail – VDD (1.1V) - Dual Phase Regulator (0.8V to 1.435V, ITDC = 4A for each rail)						
Output Voltage Setting	V_{OUT}	SWA(single phase) or SWA+SWB(dual phase) setting by reg_0x21"[7:1] SWB(single phase) setting by reg_0x25"[7:1]	0.8	--	1.435	V
Output Voltage Accuracy	$V_{OUT\_SWA/B}$	I_{OUT} = 0A, operating at CCM	–0.75	--	0.75	% of V_{OUT}
Dynamic Voltage Scale Slew Rate			--	1	--	mV/ μs
SWA/B Soft-Start/Stop Time						
Soft-Start Time		t_{set} = 1ms to 14ms	–15	--	15	% of t_{set}
Soft-Stop Time		t_{set} = 0.5ms to 4ms	–20	--	20	% of t_{set}
SWA/B Internal MOSFET Turn On Resistance						
High-Side MOSFET $R_{DS(ON)}$	$R_{DS(ON)\_SWA, SWB\_H}$	T_A = 25°C	--	16	--	mΩ
Low-Side MOSFET $R_{DS(ON)}$	$R_{DS(ON)\_SWA, SWB\_L}$	T_A = 25°C	--	10	--	mΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SWA/B Switching Frequency						
Switching Frequency	$f_{SW\_SWA/B}$	Setting by reg_0x29"[5:4]/0x2A"[7:6] = "00" (default)	0.6375	0.75	0.8625	MHz
		Setting by reg_0x29"[5:4]/0x2A"[7:6] = "01"	0.85	1	1.15	
		Setting by reg_0x29"[5:4]/0x2A"[7:6] = "10"	1.0625	1.25	1.4375	
		Setting by reg_0x29"[5:4]/0x2A"[7:6] = "11"	1.275	1.5	1.725	
SWA/B Power Good Indicator						
Power Good Threshold Low-Side Voltage		Setting by reg_0x21"[0]/0x25"[0] = "0" (default)	--	–5	--	% of V_{OUT}
		Setting by reg_0x21"[0]/0x25"[0] = "1"	--	–7.5	--	
PG_L Propagation Delay	$t_{PGLDLY\_SWA/B}$		--	5	--	µs
Power Good Threshold High-Side Voltage		Setting by reg_0x22"[7:6]/0x26"[7:6] = "00"	--	5	--	% of V_{OUT}
		Setting by reg_0x22"[7:6]/0x26"[7:6] = "01" (default)	--	7.5	--	
		Setting by reg_0x22"[7:6]/0x26"[7:6] = "10"	--	10	--	
		Setting by reg_0x22"[7:6]/0x26"[7:6] = "11"	--	2.5	--	
PG_H Propagation Delay	$t_{PGHDLY\_SWA/B}$		--	5	--	µs
SWA/B Protections						
OVP Threshold		Setting by reg_0x22"[5:4]/0x26"[5:4] = "00"	--	7.5	--	% of V_{OUT}
		Setting by reg_0x22"[5:4]/0x26"[5:4] = "01"	--	10	--	
		Setting by reg_0x22"[5:4]/0x26"[5:4] = "10" (default)	--	12.5	--	
		Setting by reg_0x22"[5:4]/0x26"[5:4] = "11"	--	20	--	
OVP Propagation Delay	$t_{OVPDLY\_SWA/B}$		--	5	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UVP Threshold		Setting by reg_0x22"[3:2]/0x26"[3:2] = "00" (default)	--	–10	--	% of V_{OUT}
		Setting by reg_0x22"[3:2]/0x26"[3:2] = "01"	--	–12.5	--	
		Setting by reg_0x22"[3:2]/0x26"[3:2] = "10"	--	–7.5	--	
		Setting by reg_0x22"[3:2]/0x26"[3:2] = "11"	--	–20	--	
UVP Propagation Delay	$t_{UVPDLY\_SWA/B}$		--	5	--	µs
SWA/B Current Limit						
Current Limit	$I_{LIM\_SWA/B}$	Valley current limited Setting by reg_0x20"[7:6]/[3:2] = "00"	--	3	--	A
		Setting by reg_0x20"[7:6]/[3:2] = "01"	--	3.5	--	
		Setting by reg_0x20"[7:6]/[3:2] = "10"	--	4	--	
		Setting by reg_0x20"[7:6]/[3:2] = "11" (default)	--	4.5	--	
SWC Rail – VPP(1.8V) – Single Phase Regulator (1.5V to 2.135V, ITDC = 1A)						
Output Voltage Setting	V_{OUTC}	Setting by reg_0x27"[7:1], 5mV/Step	1.5	1.8	2.135	V
Output Voltage Accuracy	V_{OUT_SWC}	I_{OUT} = 0A, operating at CCM	–0.75	--	0.75	% of V_{OUT}
Dynamic Voltage Scale Slew Rate			--	1	--	mV/µs
SWC Soft-Start/Stop Time						
Soft-Start Time		t_{set} = 1ms to 14ms	–15	--	15	% of t_{set}
Soft-Stop Time		t_{set} = 1ms to 8ms	–20	--	20	% of t_{set}
SWC Internal MOSFET Turn On Resistance						
High-Side MOSFET $R_{DS(ON)}$	RDS(ON)_SWC_H	T_A = 25°C	--	55	--	mΩ
Low-Side MOSFET $R_{DS(ON)}$	RDS(ON)_SWC_L	T_A = 25°C	--	45	--	mΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SWC Switching Frequency						
Switching Frequency	f_{SW_SWC}	Setting by reg_0x2A"[1:0] = "00" (default)	0.6375	0.75	0.8625	MHz
		Setting by reg_0x2A"[1:0] = "01"	0.85	1	1.15	
		Setting by reg_0x2A"[1:0] = "10"	1.0625	1.25	1.4375	
		Setting by reg_0x2A"[1:0] = "11"	1.275	1.5	1.725	
SWC Power Good Indicator						
Power Good Threshold Low-Side Voltage		Setting by reg_0x27"[0] = "0" (default)	--	–5	--	% of V_{OUTC}
		Setting by reg_0x27"[0] = "1"	--	–7.5	--	
PG_L Propagation Delay	t_{PGLDLY_SWC}		--	5	--	µs
Power Good Threshold High-Side Voltage		Setting by reg_0x28"[7:6] = "00"	--	5	--	% of V_{OUTC}
		Setting by reg_0x28"[7:6] = "01" (default)	--	7.5	--	
		Setting by reg_0x28"[7:6] = "10"	--	10	--	
		Setting by reg_0x28"[7:6] = "11"	--	2.5	--	
PG_H Propagation Delay	t_{PGHDLY_SWC}		--	5	--	µs
SWC Protections						
OVP Threshold		Setting by reg_0x28"[5:4] = "00"	--	7.5	--	% of V_{OUTC}
		Setting by reg_0x28"[5:4] = "01"	--	10	--	
		Setting by reg_0x28"[5:4] = "10" (default)	--	12.5	--	
		Setting by reg_0x28"[5:4] = "11"	--	20	--	
OVP Propagation Delay	t_{OVPDLY_SWC}		--	5	--	µs
UVP Threshold		Setting by reg_0x28"[3:2] = "00" (default)	--	–10	--	% of V_{OUTC}
		Setting by reg_0x28"[3:2] = "01"	--	–12.5	--	
		Setting by reg_0x28"[3:2] = "10"	--	–7.5	--	
		Setting by reg_0x28"[3:2] = "11"	--	–20	--	
UVP Propagation Delay	t_{UVPDLY_SWC}		--	5	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SWC Current Limit						
Current Limit	$I_{LIM\_SWC\_LOW\ Current}$	For Low Current, valley current limited Setting by reg_0x20"[1:0] = "00"	--	0.5	--	A
		Setting by reg_0x20"[1:0] = "01"	--	1.0	--	
		Setting by reg_0x20"[1:0] = "10"	--	1.5	--	
		Setting by reg_0x20"[1:0] = "11" (default)	--	2.0	--	
VLDO_1.8V (1.8V, I_{MAX} = 25mA)						
Output Voltage	$V_{LDO\_1.8V}$	Setting by reg_0x2B"[7:6] = "00"	1.66	1.7	1.74	V
		Setting by reg_0x2B"[7:6] = "01" (default)	1.76	1.8	1.84	
		Setting by reg_0x2B"[7:6] = "10"	1.85	1.9	1.95	
		Setting by reg_0x2B"[7:6] = "11"	1.95	2.0	2.05	
Soft-Start Time			--	0.25	--	ms
Power Good Threshold		Setting by reg_0x1A"[2] = "0"	--	1.6	--	V
PG Propagation Delay	$t_{PGLDLY\_VLDO\_1.8V}$		--	5	--	μs
Current Limit			50	--	--	mA
VLDO_1.0V (1.0V, I_{MAX} = 20mA)						
Output Voltage	$V_{LDO\_1.0V}$	Setting by reg_0x2B"[2:1] = "00"	0.88	0.9	0.92	V
		Setting by reg_0x2B"[2:1] = "01" (default)	0.98	1.0	1.02	
		Setting by reg_0x2B"[2:1] = "10"	1.08	1.1	1.12	
		Setting by reg_0x2B"[2:1] = "11"	1.18	1.2	1.22	
Soft-Start Time			--	0.12	--	ms
Power Good Threshold		Setting by reg_0x1A"[0] = "0" (default)	--	−10	--	% of V_{LDO}
		Setting by reg_0x1A"[0] = "1"	--	−15	--	
PG Propagation Delay	$t_{PGLDLY\_VLDO\_1.0V}$		--	5	--	μs
Current Limit			50	--	--	mA

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

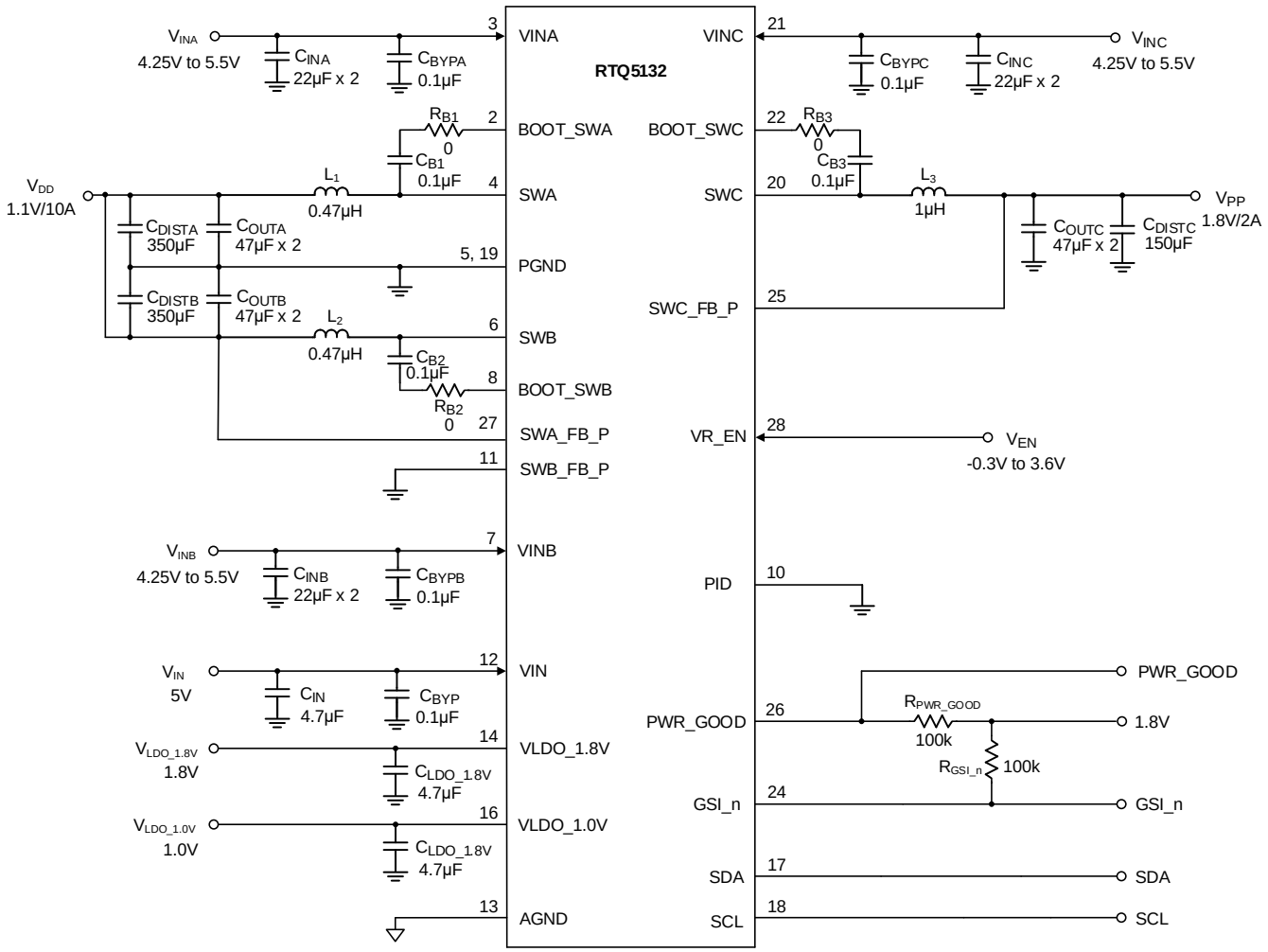


Figure 13. Typical Application Circuit when SWA and SWB are combined as Two Phase, Single Output Rail.

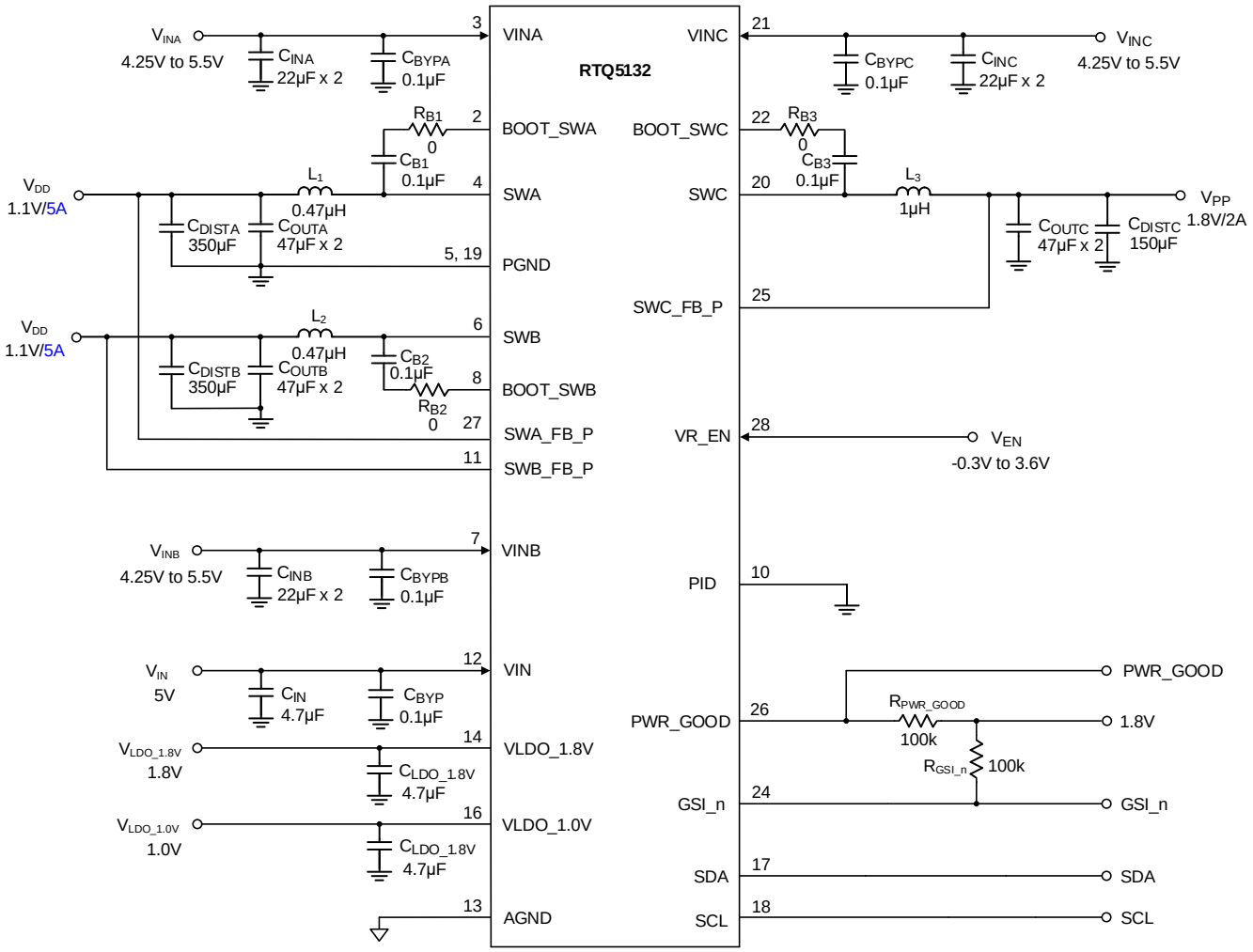
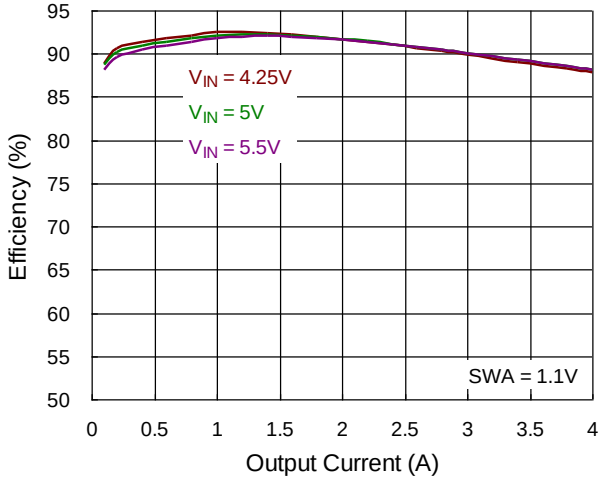
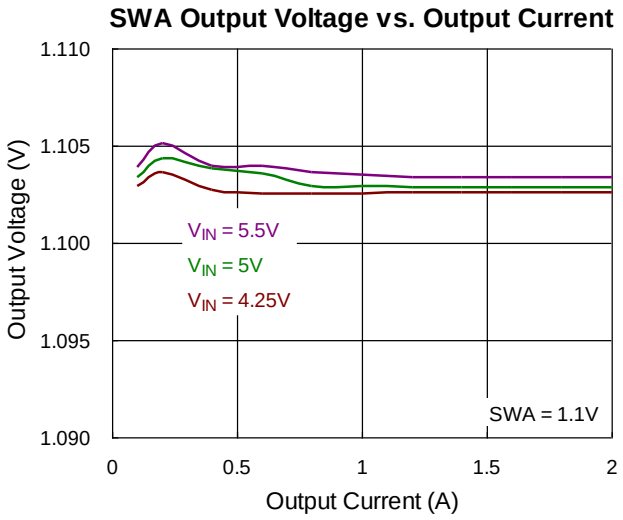
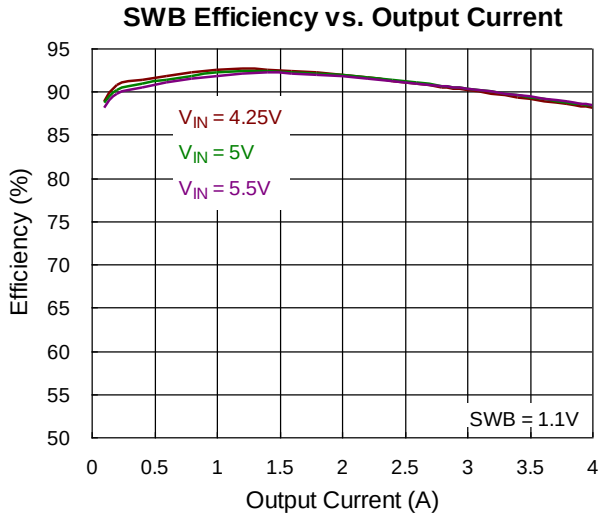


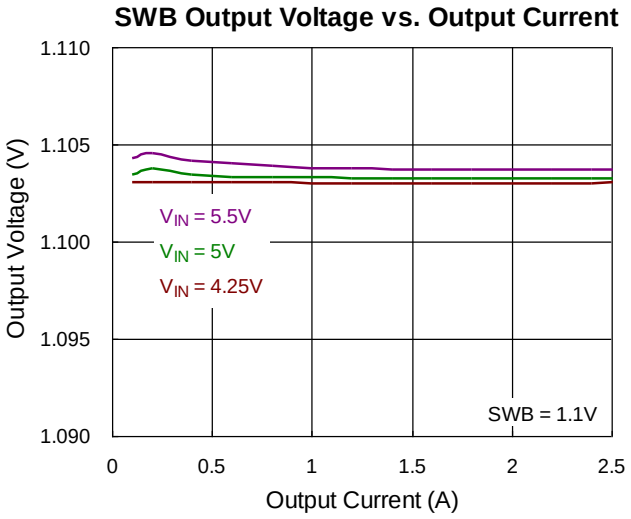
Figure 14. Typical Application Circuit when SWA and SWB are separated for 2-Outputs.

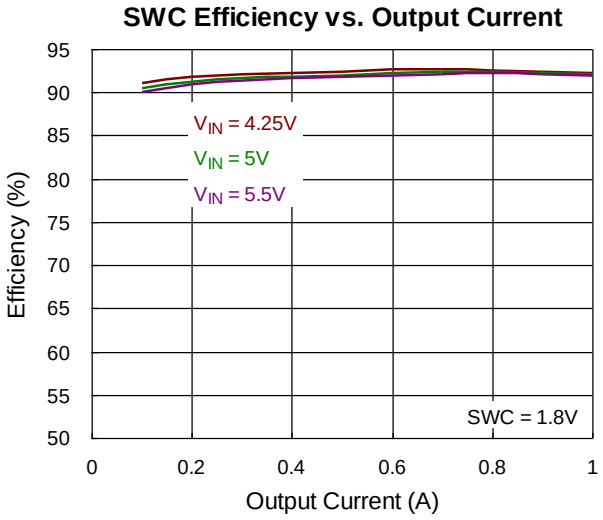
Typical Operating Characteristics

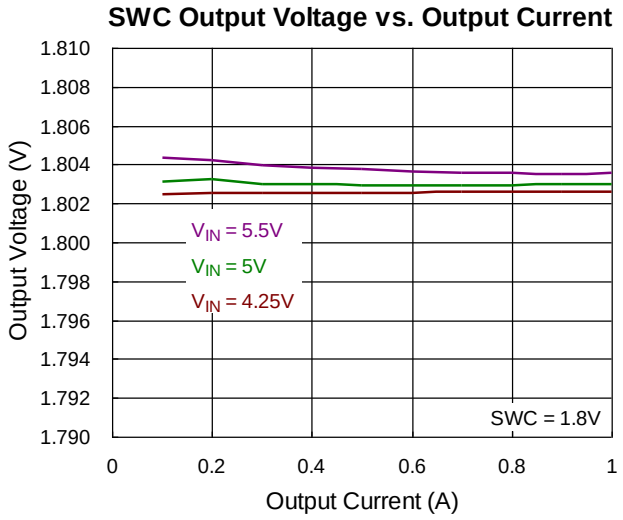




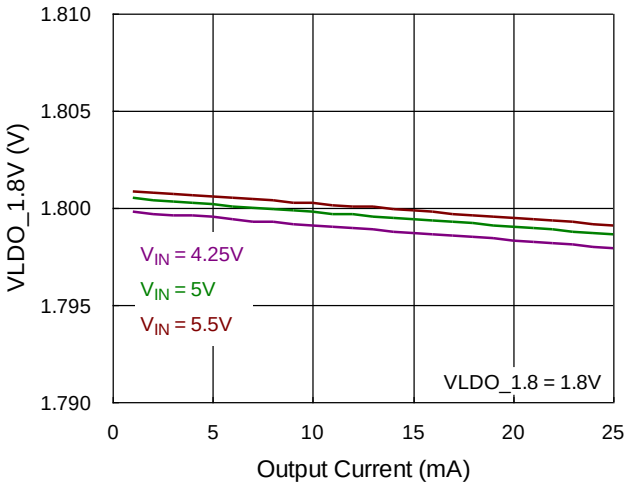




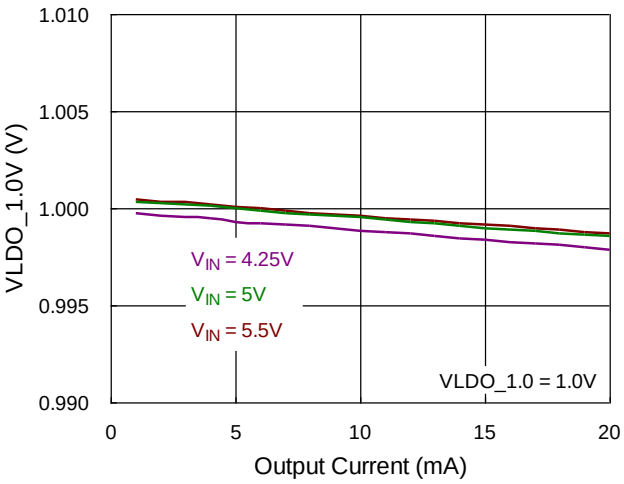




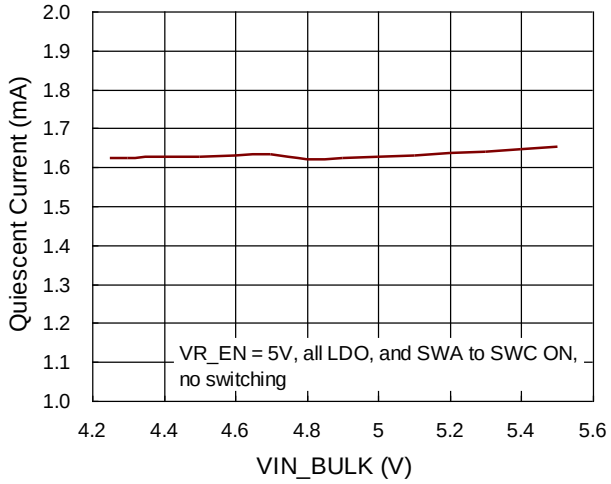
VLDO_1.8V vs. Output Current



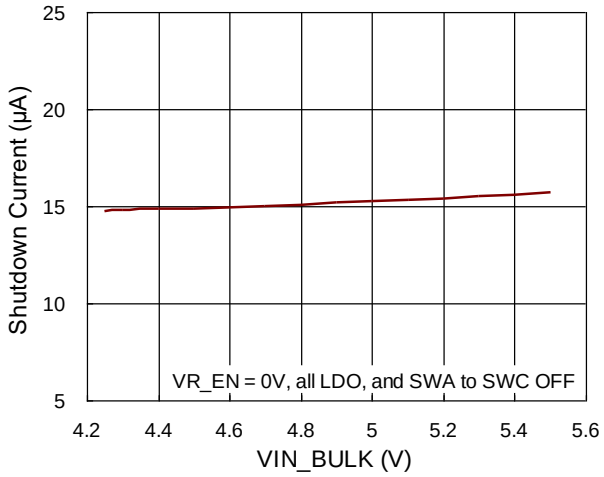
VLDO_1.0V vs. Output Current



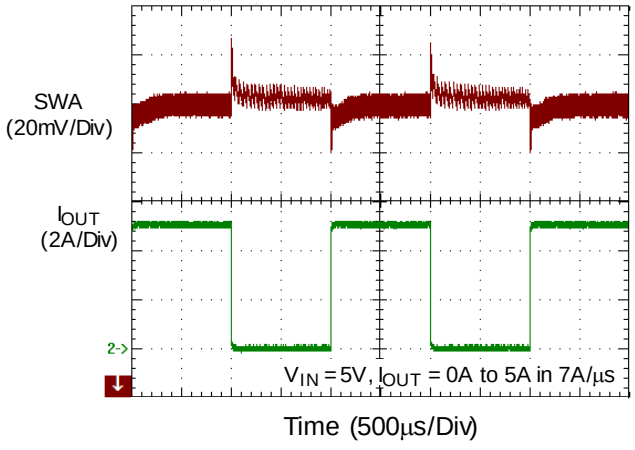
Quiescent Current vs. VIN_BULK



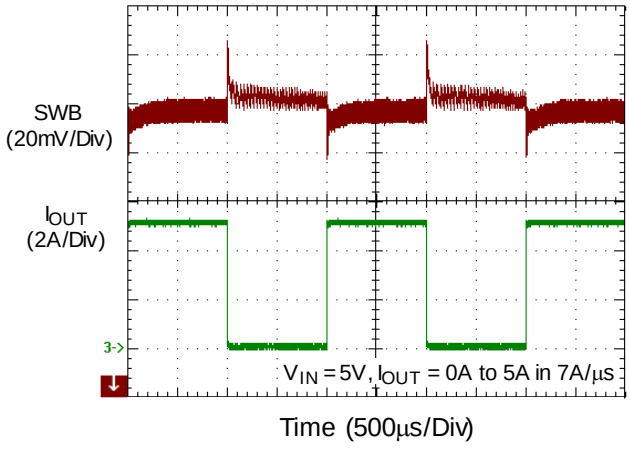
Shutdown Current vs. VIN_BULK



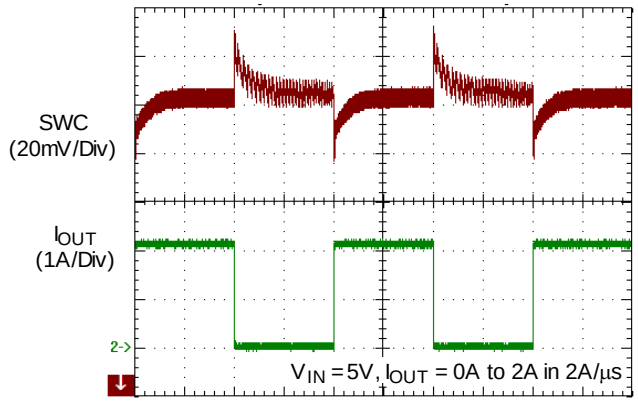
SWA Load Transient Response



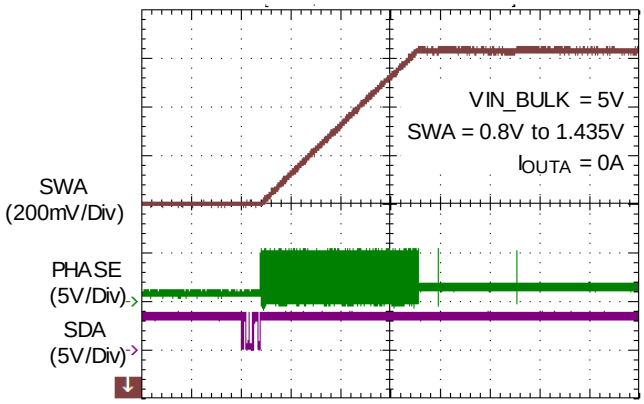
SWB Load Transient Response



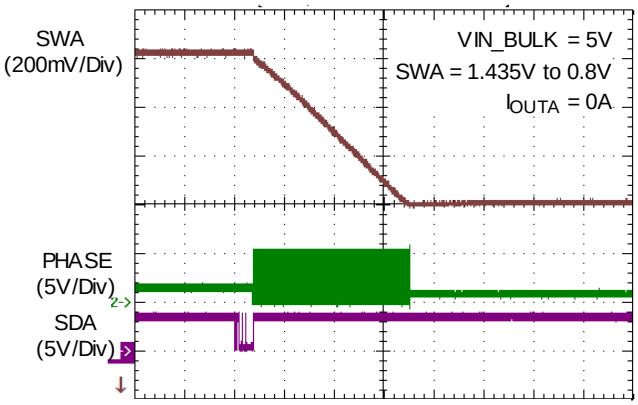
SWC Load Transient Response



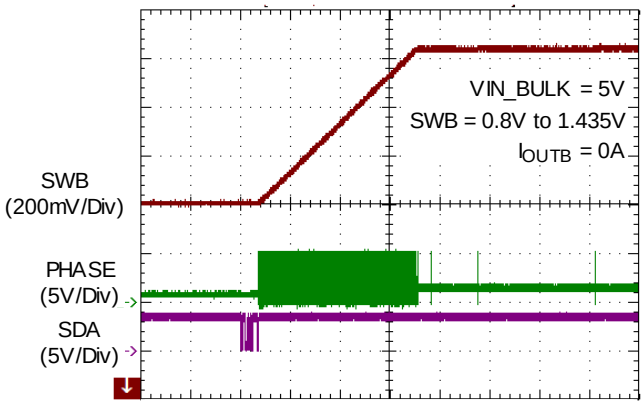
SWA VID Up



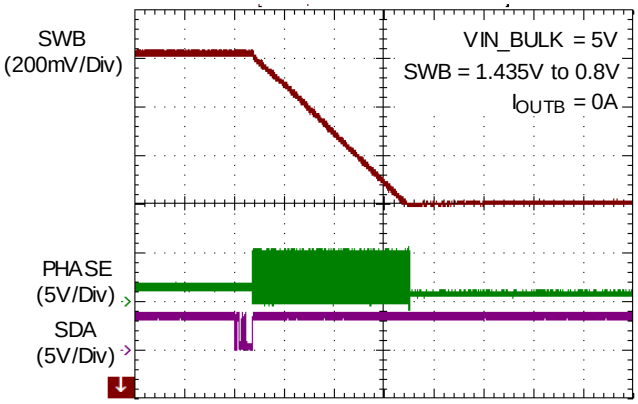
SWA VID Down



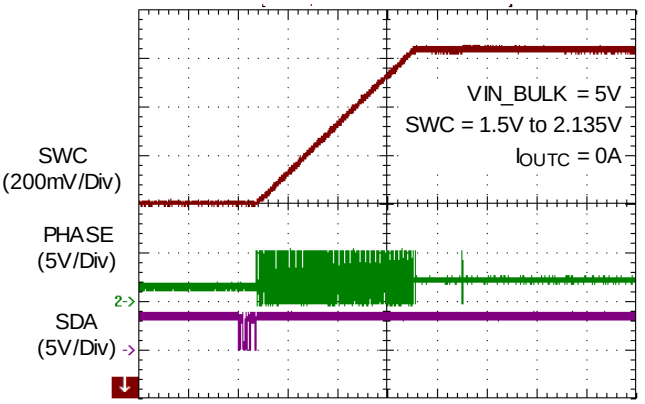
SWB VID Up



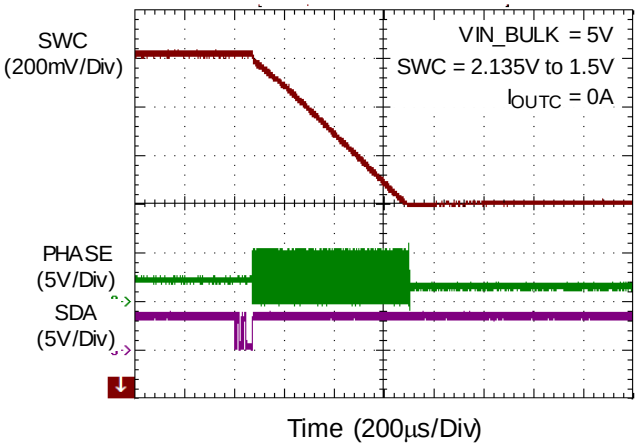
SWB VID Down



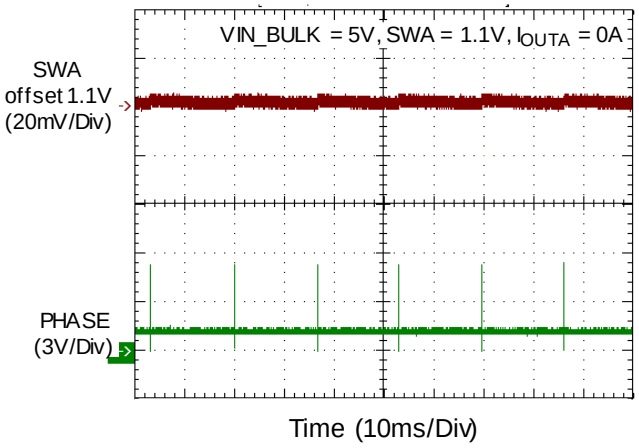
SWC VID Up



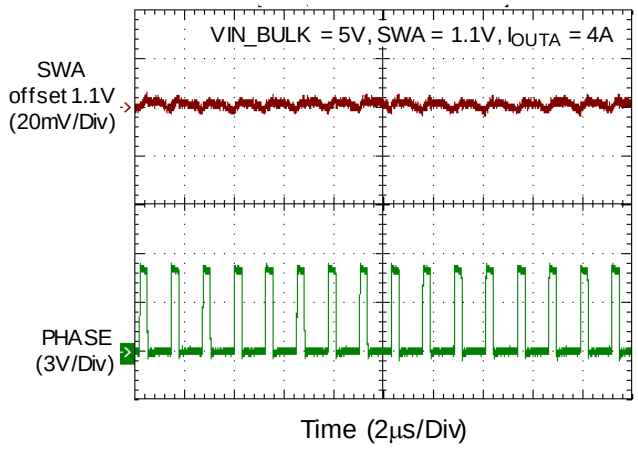
SWC VID Down



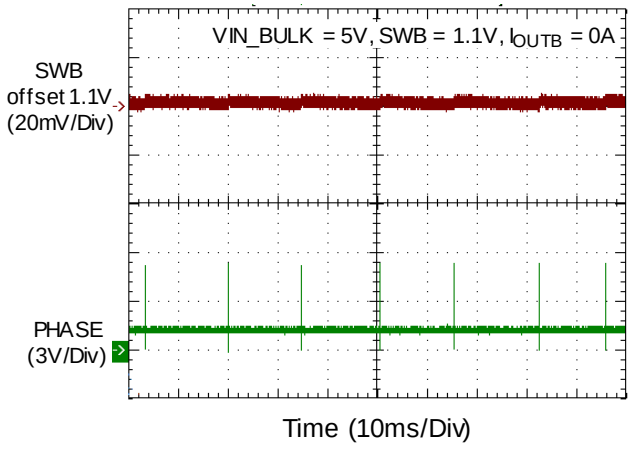
SWA Stability in DEM



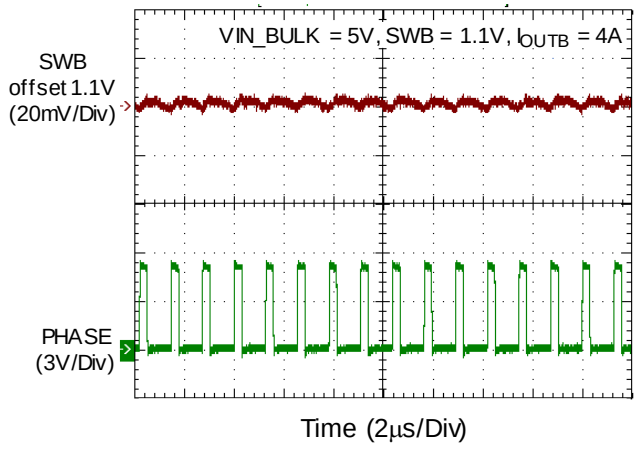
SWA Stability in CCM



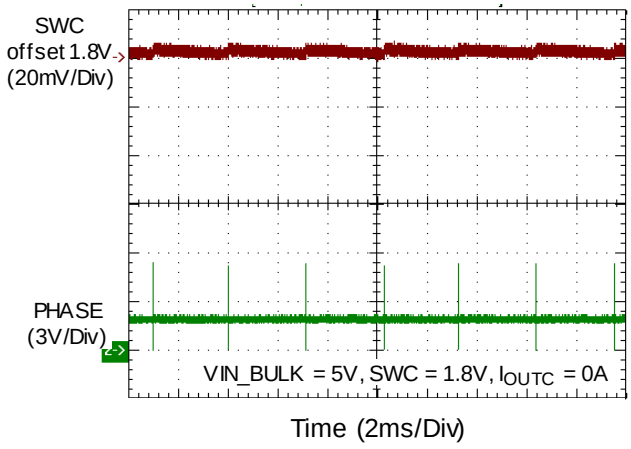
SWB Stability in DEM



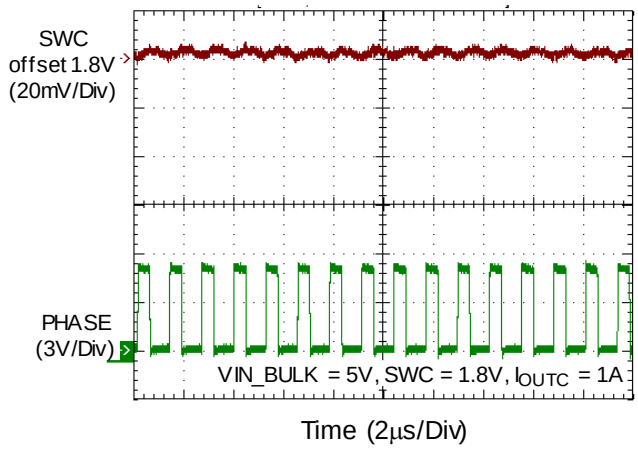
SWB Stability in CCM



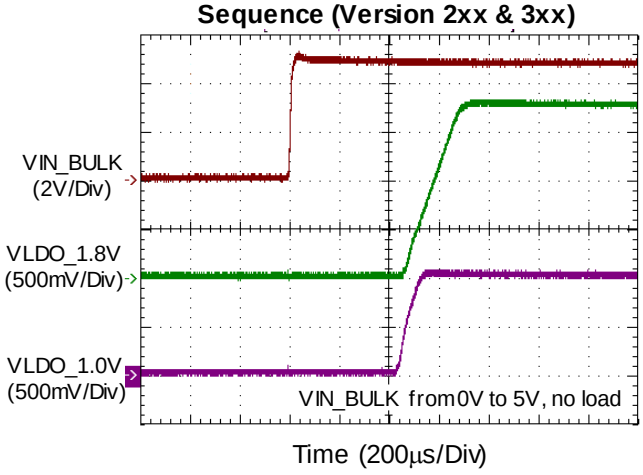
SWC Stability in DEM



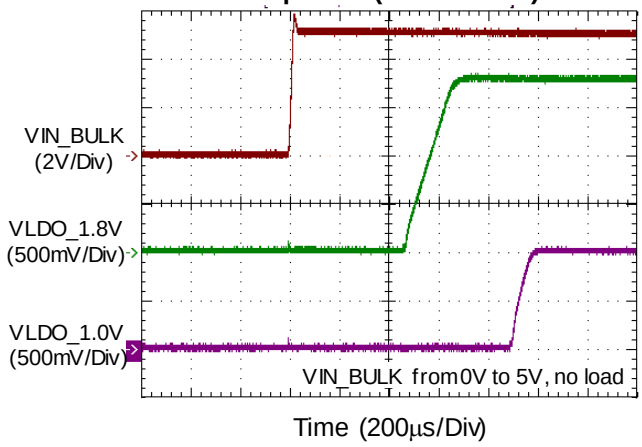
SWC Stability in CCM



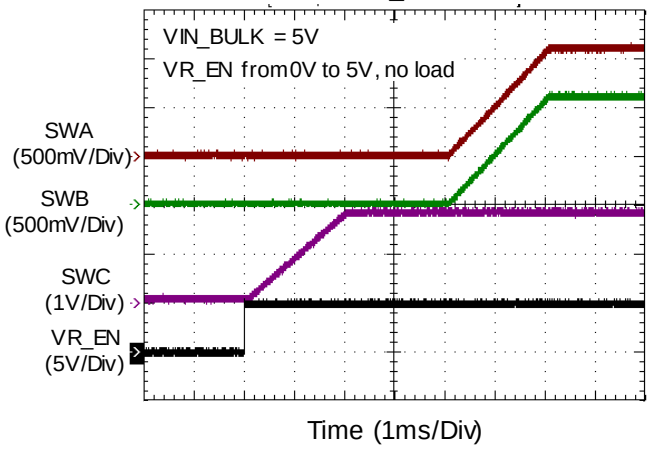
VLDO_1.8V and VLDO_1.0V Power-On Sequence (Version 2xx & 3xx)



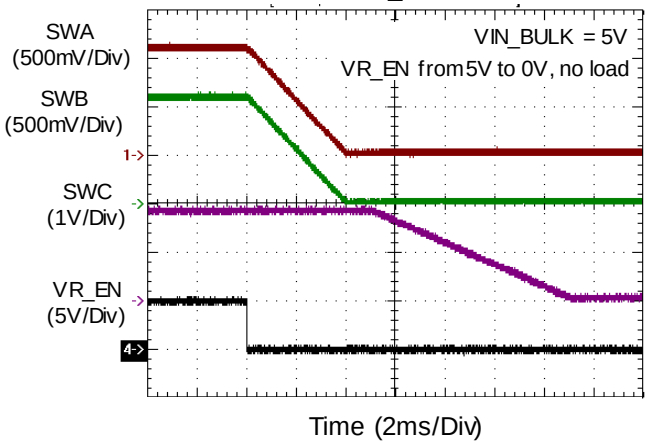
VLDO_1.8V and VLDO_1.0V Power-On Sequence (Version 5xx)



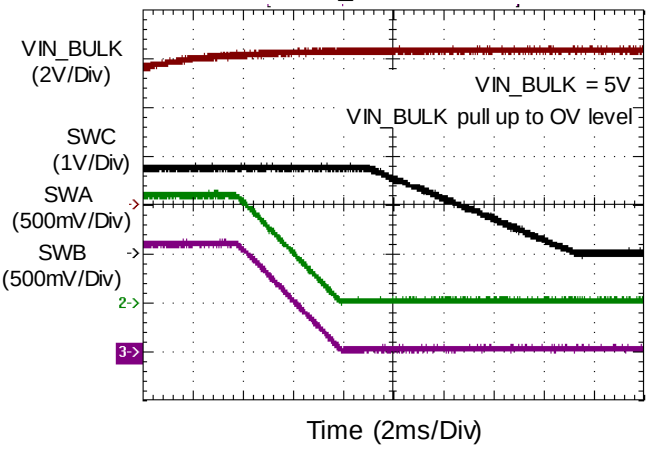
PMIC Power-On Sequence by VR_EN



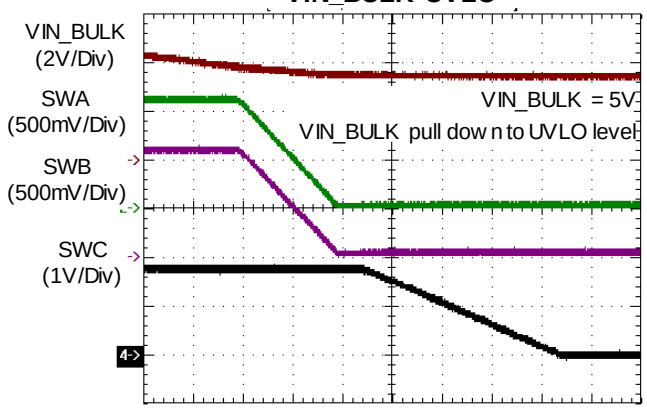
PMIC Power-Off Sequence by VR_EN



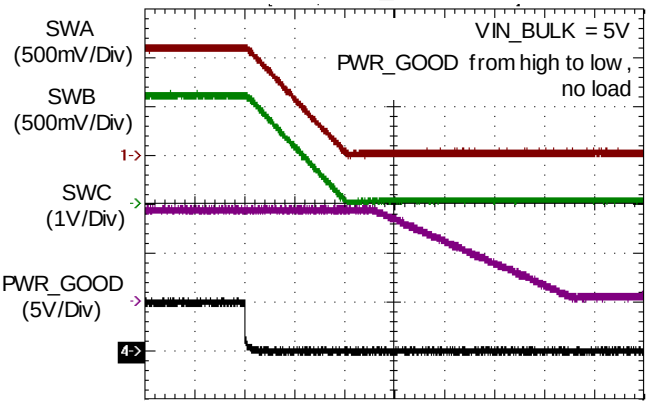
PMIC Power-Off Sequence by VIN_BULK OVP



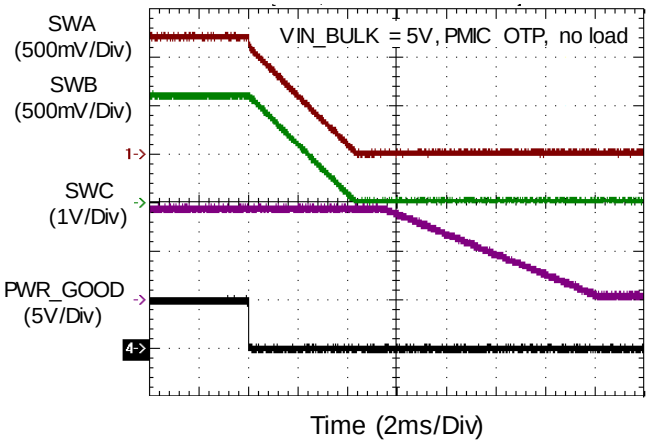
PMIC Power-Off Sequence by VIN_BULK UVLO



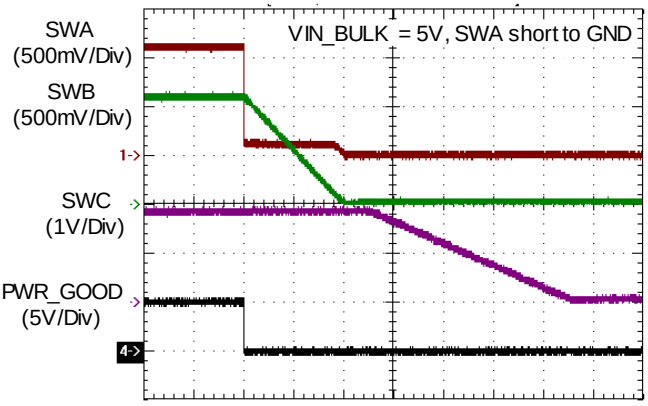
PMIC Power-Off Sequence by PWR_GOOD



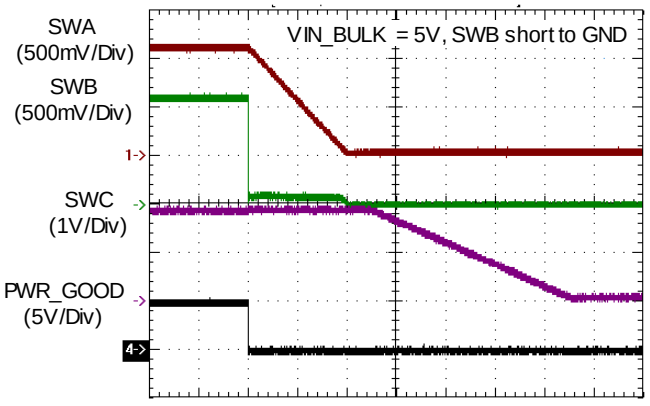
PMIC Power-Off Sequence by OTP



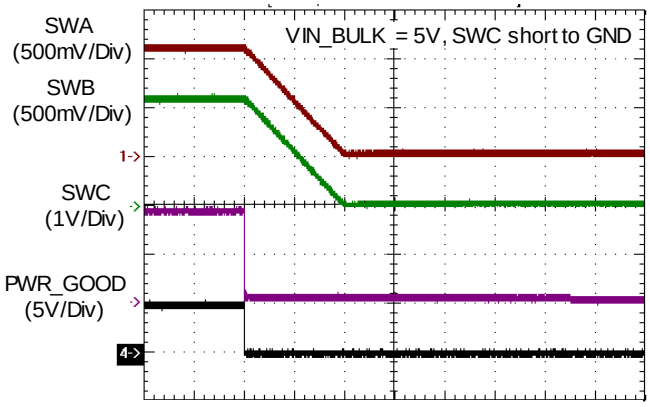
PMIC Power-Off Sequence by SWA Short to GND



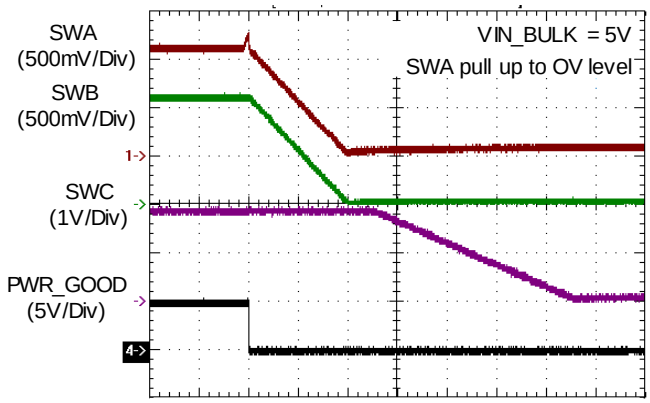
PMIC Power-Off Sequence by SWB Short to GND



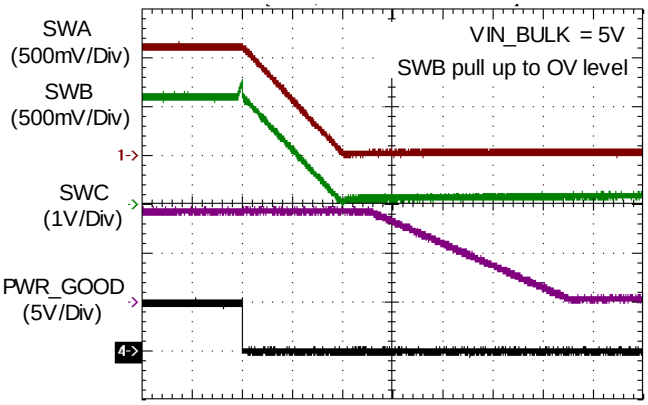
PMIC Power-Off Sequence by SWC Short to GND



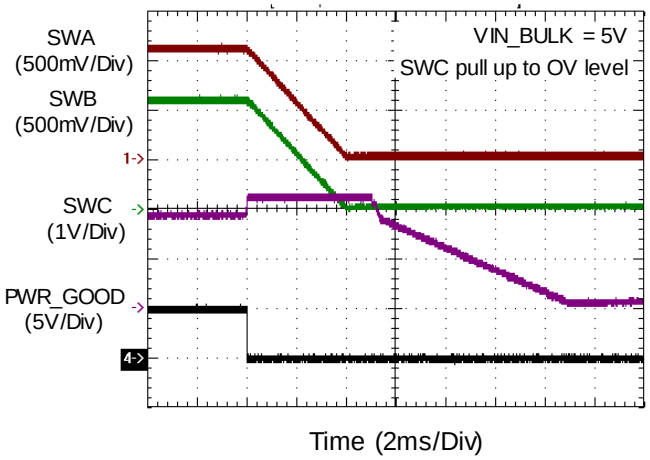
PMIC Power-Off Sequence by SWA OVP



PMIC Power-Off Sequence by SWB OVP



PMIC Power-Off Sequence by SWC OVP



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response; however, they increase the inductor ripple current and output voltage ripple, and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required. Also, transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) about 20-50% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \quad \text{and} \quad I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short-circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output undervoltage shutdown feature makes this unnecessary for most applications.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For low inductor core losses, some types of shielded ferrite core are usually better. Although they are possibly larger or more expensive, they will probably give fewer EMI and other noise problems.

Since DDR5 on DIMM has layout space limitation to power management IC on DIMM as well as the surrounding components like inductors and input/output capacitors, a standard inductor mechanical specification is defined in Table 9 and Table 10. Moreover, the electrical specification of inductor is also defined in Table 11. The electrical specifications include inductance, maximum DCR, maximum ACR and the minimum inductance requirement after de-rating at a specified operating current. The DIMM vendors can select an inductor based on the Table 11. Because the inductor size is fixed, the tradeoff between efficiency and transient response is the main concern on selection. Generally, the inductance for SWA, and SWB, which are 1.1V output rails, is recommended to choose between 0.47μH and 0.68uH. The transient performance with L = 0.47μH is better than that with L = 0.68μH. However, the efficiency performance with L = 0.68μH is better than that with L = 0.47μH. On the other hand, the output rail with V_{OUT} = 1.8V, which is SWC or VPP rail, is suggested to apply inductance between 1uH to 1.5μH.

Table 9. SWA an SWB Inductor Mechanical Specifications

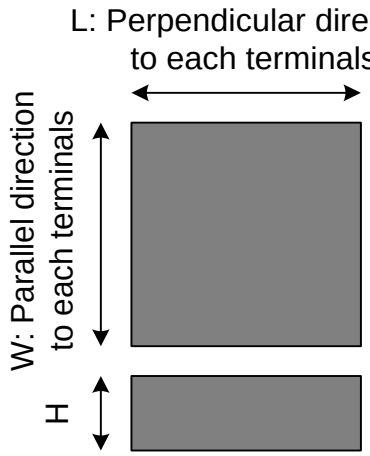
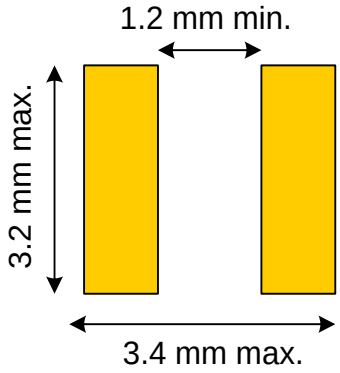
Package Size		Reference Drawings	Recommended Land Pattern
L [mm]	3.4max		
W [mm]	3.2max		
H [mm]	1.2max		

Table 10. SWC Inductor Mechanical Specifications

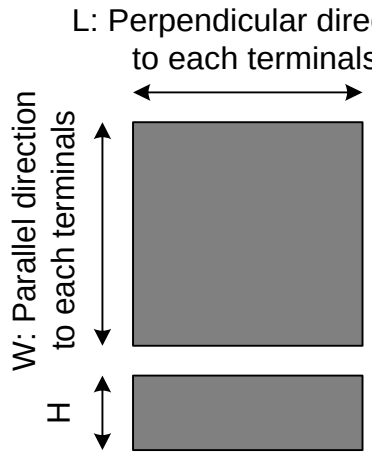
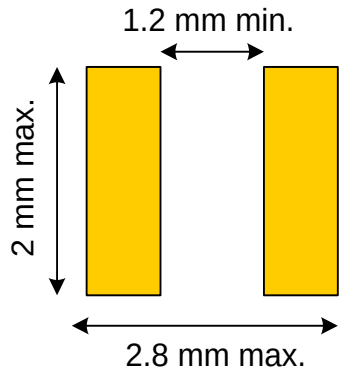
Package Size		Reference Drawings	Recommended Land Pattern
L [mm]	2.7max		
W [mm]	2.2max		
H [mm]	1.2max		

Table 11. SWA and SWB Inductor Electrical Specifications

Package Height	L @ 0.5-1MHz/0bias ± 20% [µH]	Max DCR [mΩ]	Max ACR @ 1MHz [mΩ]	Min. L @ 6A [µH]
1.2 Max [mm]	0.47	14.5	93	0.30
	0.68	18.5	113	0.38

Table 12. SWC Inductor Electrical Specifications

Package Height	L @ 0.5-1MHz/0bias ± 20% [µH]	Max DCR [mΩ]	Max ACR @ 1MHz [mΩ]	Min. L @ 2A [µH]
1.2 Max [mm]	1.0	48	182	0.56
	1.5	75	300	0.82

Output Cap. Selection

The Buck output regulators of RTQ5132 are optimized for ceramic output capacitors, and the best performance will be obtained by using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR, ESL and stored charge. These three ripple components are called ESR ripple, ESL ripple, and capacitive ripple. Since ceramic capacitors have extremely low ESR, ESL and relatively little capacitance, all these components should be considered if ripple is critical. The decomposition of output ripple is shown in Figure 15. The formulas to describe each component are listed below.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(ESL)} = \frac{d}{dt} I_L \times ESL$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

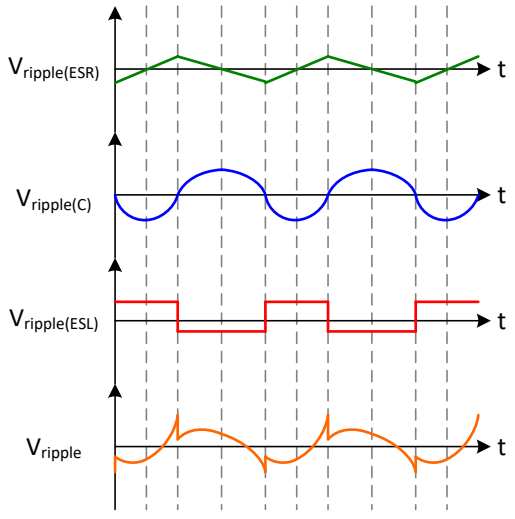


Figure 15. Output Ripple Decomposition

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The A^{2}RCOT transient response is very quick and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's switching frequency. But some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the A^{2}RCOT control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. The behavior diagram of output voltage drop is depicted as Figure 16. Calculate the approximate on-time (neglecting parasitic) and maximum duty cycle for a given input and output voltage as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ ,and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF(MIN)}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but it can be neglected both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as:

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

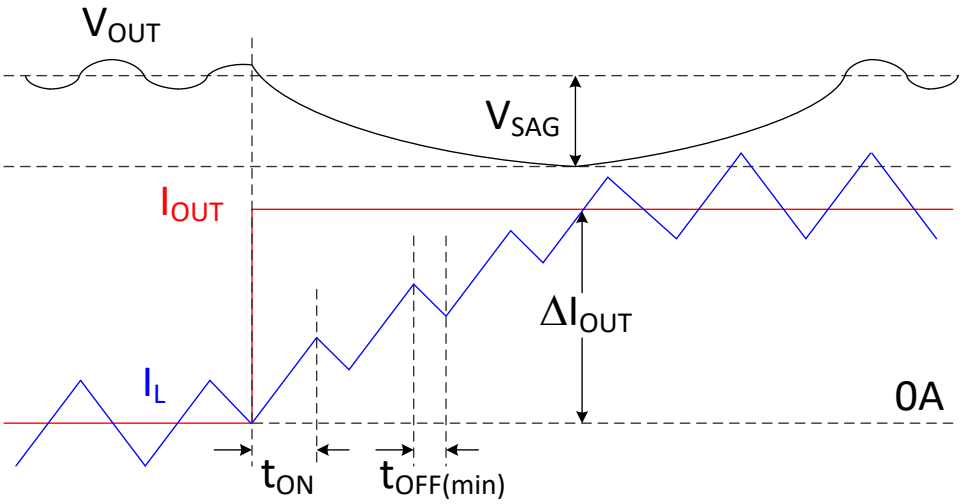


Figure 16. Output Voltage Drop (V_{SAG}) Estimation as Output Load Current Step Up

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage:

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

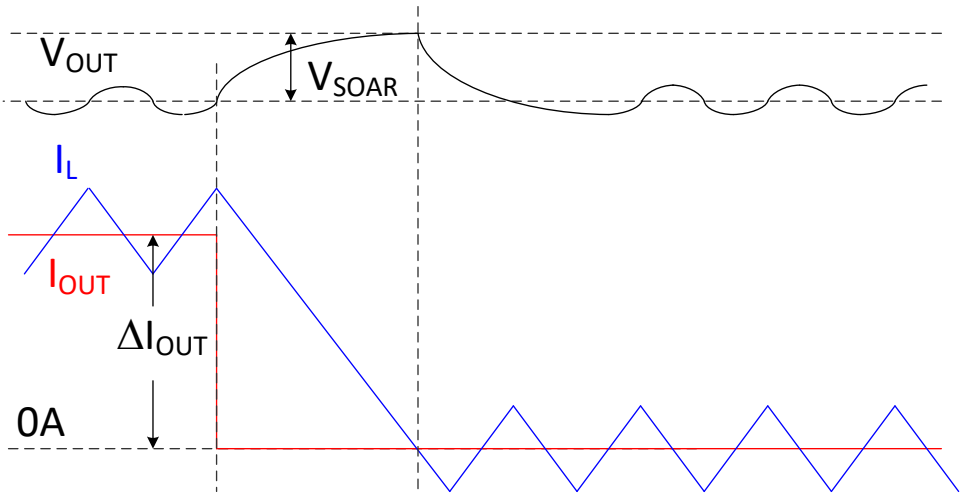


Figure 17. Output Voltage Soar (V_{SOAR}) Estimation as Output Load Current Step Down

Most applications never experience instantaneous full load steps and the RTQ5132's high switching frequency and fast transient response can easily control voltage regulation at all times. Therefore, sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitor (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

In any application with large quick transients, it should calculate soar and sag to make sure that overvoltage protection and undervoltage protection will not be triggered.

In addition, the recommended dielectric type of the capacitor is X7R which has the best performance

among temperature and DC and AC bias voltage variations. The variation of the capacitance value with temperature, DC bias voltage and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

A standard output capacitors' electrical specification is defined in Table 13. The electrical specifications include capacitance, rated voltage and the size code in inch. The DIMM vendors should select the capacitors based on the Table 13.

Table 13. Output Capacitor Electrical Specifications

Component	Value	Physical Size
C_{OUTA}	47µF (x2)	6.3V; 0603
C_{OUTB}	47µF (x2)	6.3V; 0603
C_{OUTC}	47µF (x2)	6.3V; 0603
C_{DISTA}*	350µF	6.3V
C_{DISTB}*	350µF	6.3V
C_{DISTC}*	150µF	6.3V
$C_{LDO\_1.8V}$	4.7µF	6.3V; 0402
$C_{LDO\_1.0V}$	4.7µF	6.3V; 0402

*Note that capacitors C_{DISTA}, C_{DISTB}, and C_{DISTC} represent the lump sum of distributed capacitance across the entire DIMM.

Input Cap. Selection

A buck converter generates a pulsating ripple current with high di/dt at the input. Without input capacitors, ripple current is supplied by the upper power source. Printed circuit board (PCB) resistance and inductance cause high-voltage ripple that disrupts electronic devices. The circulating ripple current results in increased conducted and radiated EMI. Input capacitors provide a short bypass path for ripple current and stabilize bus voltage during a transient event.

The capacitor voltage rating should meet reliability and safety requirements. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design. Among the different types of capacitors, the multilayer ceramic capacitor (MLCC) is particularly good regarding allowable ripple current due to low ESR and ESL. Following equation is used to estimate the required effective capacitance that will meet the ripple requirement.

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1-D)}{\Delta V_{IN\_PP} \times f_{SW}}$$

where D is calculated as below:

$$D = \frac{V_O}{V_{IN} \times \eta}$$

Besides the ripple-voltage requirement, the ceramic capacitors should meet the thermal stress requirement as well. The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation:

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left[(1-\frac{V_{OUT}}{V_{IN}}) \times {I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12} \right]}$$

Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Besides, since the ESL of ceramic capacitors plays a significant role on voltage spike at input and phase node, it is desirable to add a small capacitor with low ESL near VIN pin.

While the MLCC is excellent regarding allowable ripple current, it is well-known regarding effective capacitance that is necessary to meet transient response requirements. There can be two VIN spikes during the transient: the first spike is related to the ESR; and the second spike is caused by the difference between the buck-converter input current (i_{IN_B}) and the bus-converter output current (i_{PS}) as depicted in Figure 18. Both spikes should be lower than the VIN undershoot or overshoot requirement (VIN_tran). First, since the MLCCs have very small ESR, the component of ESR drop can almost be ignored. The second spike is related to the response of the bus converter. The converter output-current rise time during a transient event, T_{R_PS}, can be approximated by the following equation:

$$T_{R\_PS} \cong \frac{0.35}{f_{BW\_PS}}$$

, where f_{BW_PS} is the control loop bandwidth of Buck converter.

The equivalent capacitance of the input capacitors should be greater than that calculated with following equation:

$$C_{IN} \geq \frac{\frac{1}{2} \times I_{Step} \times D_{max} \times T_{R\_PS}}{V_{IN\_Tran}}$$

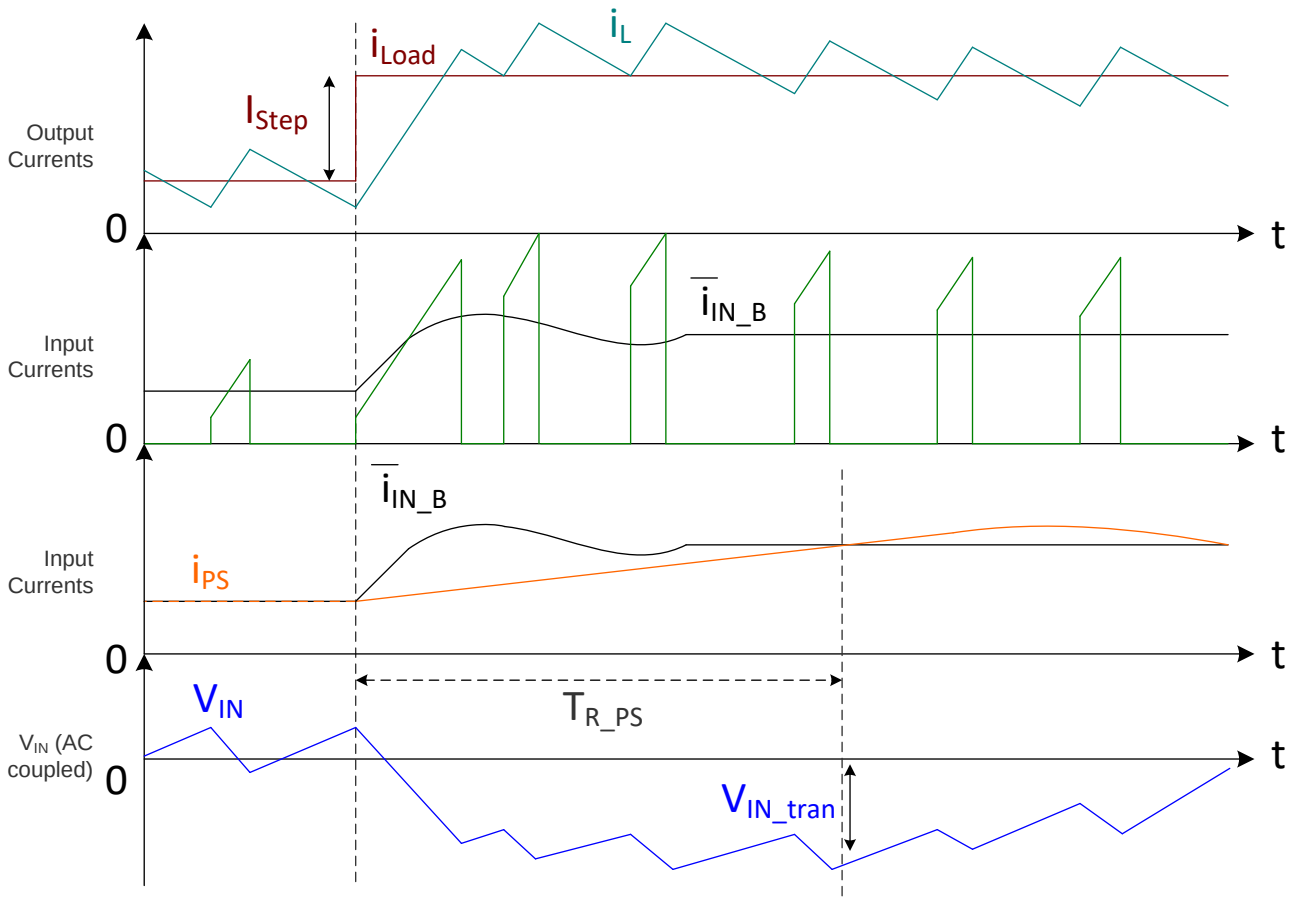


Figure 18. VIN Transient Current Diagram

Either VIN ripple (ΔV_{IN_PP}) or Vin transient ripple (V_{IN_Tran}) should meet the design requirements. For RTQ5132, the input voltage should be always higher than VIN_UVLO threshold to confirm the PMIC's functionality. Moreover, it should be noticed that many de-rating factors, including VIN dc voltage, ac voltage and operating temperature, make equivalent capacitance smaller than the capacitance without bias.

A standard input capacitors' electrical specification is defined in Table 14. The electrical specifications include capacitance, rated voltage and the size code in inch. The DIMM vendors should select the input capacitors based on the Table 14.

Table 14. Input Capacitor Electrical Specifications

Component	Value	Physical Size
C_{IN}	4.7µF	10V; 0402
C_{INA}	22µF (x2)	10V; 0402
C_{INB}	22µF (x2)	10V; 0402
C_{INC}	22µF (x2)	10V; 0402
C_{BYP}	0.1µF	10V; 0201
C_{BYPA}	0.1µF	10V; 0201
C_{BYPB}	0.1µF	10V; 0201
C_{BYPC}	0.1µF	10V; 0201

Bootstrap Circuit

The bootstrap circuit is useful in a high-voltage gate

driver and operates as follows. When the SW node goes below the IC supply voltage V_{CC} (V_{DD}) or is pulled down to ground (the low-side MOSFET is turned on and the high-side MOSFET is turned off), the bootstrap capacitor, C_{BOOT}, charges through the bootstrap resistor, R_{BOOT}, and bootstrap diode, D_{BOOT}, from the VCC power supply, as shown in Figure 19. On the other hand, the voltage across V_{BOOT} and SW can supply gate charge to high-side MOSFET when low-side MOSFET is turned off and SW node goes to a higher voltage, VOUT. In the meantime, the bootstrap diode reverses bias and blocks the rail voltage from the IC supply voltage, V_{CC}.

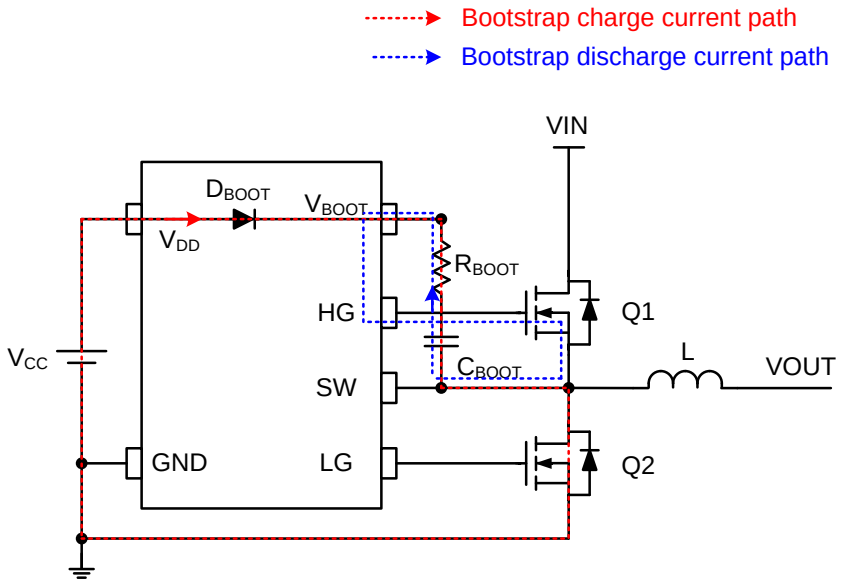


Figure 19. Bootstrap Power Supply Circuit

There are some design considerations for a bootstrap circuit. First, the selection of bootstrap capacitor (C_{BOOT}) is based on the maximum voltage drop across C_{BOOT} to guarantee the high-side MOSFET has enough charge to turn on periodically. The maximum allowable voltage drop (ΔV_{BOOT}) depends on the minimum gate drive voltage (for the high-side MOSFET) to maintain. If V_{GSMIN} is the minimum gate-source voltage, the capacitor drop must be:

$$\Delta V_{BOOT} = V_{CC} - V_F - V_{GSMIN}$$

where V_{CC} is the supply voltage of gate driver, and VF is the forward voltage drop of bootstrap diode.

Therefore, the value of bootstrap capacitor is calculated as:

$$C_{BOOT} = \frac{Q_{Total}}{\Delta V_{BOOT}}$$

where QTotal is the total amount of the charge required for driving the high-side MOSFET and some leakage charge in the chip.

Second, when the external bootstrap resistor is used, the resistance, RBOOT, introduces an additional voltage drop:

$$V_{RBOOT} = \frac{Q_{Total}}{t_{Charge}} \times R_{BOOT}$$

where t_{Charge} is the bootstrap charging time (the low-side MOSFET turn-on time).

The power dissipation on R_{BOOT} should be considered when choosing the package size of resistor. When estimating the maximum allowable voltage drop, the value of voltage drop of bootstrap resistor should be taken into account.

For example, assume V_{CC} = 5V, V_F = 0.7V, R_{BOOT} = 1Ω, V_{GSMIN} = 2.5V and QTotal = 5nC. The ΔV_{BOOT} can be calculated as 1.8V. The estimated C_{BOOT} is 2.8nF. Generally, the ΔV_{BOOT} is not suggested to be too large and also need to consider the additional voltage drop on R_{BOOT}. Moreover, the de-rating factors, including VIN dc voltage, ac voltage and operating temperature, makeor example, assume V_{CC} = 5V, V_F = 0.7V, R_{BOOT} = 1Ω, V_{GSMIN} = 2.5V and QTotal = 5nC. The ΔV_{BOOT} can be calculated as 1.8V. The estimated C_{BOOT} is 2.8nF. Generally, the ΔV_{BOOT} is not suggested to be too large and also need to consider the additional voltage drop on R_{BOOT}. Moreover, the de-rating factors, including VIN dc voltage, ac voltage and operating temperature, make quivalent capacitance be smaller. The common selection value of C_{BOOT} is 100nF~220nF, that makes the ΔV_{BOOT} to be 50mV and 25mV separately. If choosing the bias capacitor with 0201 package and 6.3V voltage rating, the de-rating factor is about 0.5. Therefore, the ΔV_{BOOT} increases to 100mV and 50mV. In addition, the voltage drop on R_{BOOT} = 1Ω is 25mV as t_{Charge} is 200nsec. Adding the R_{BOOT} can reduce the EMI noise as well as voltage spike on phase node. However, the additional power loss will reduce the system efficiency.

VLDO_1.8V and VLDO_1.0V Decoupling Capacitor

The RTQ5132 integrates three LDO regulators (VLDO_1.8V, VLDO_1.0V).

The VLDO_1.8V and VLDO_1.0V LDOs are supplied by VIN. They provide power to system devices such as SPD, TS and RCD on the DIMM. Both VLDO_1.8V and VLDO_1.0V need a decoupling capacitor placed near output pin and the equivalent minimum capacitance should be at least 2.2μF. In many applications, a 4.7μF/6.3V/X5R/0402 capacitor is recommended. When choosing the package size and voltage rating of a capacitor, the de-rating coefficient versus voltage and temperature is important for taking account of equivalent capacitance under actual operating condition.

Thermal Consideration

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended

Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-28L 3x4 (FC) package, the thermal resistance, θ_{JA}, is 41°C/W on high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C − 25°C)/(41°C/W) = 2.43W for a WQFN-28L 3x4 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 20 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

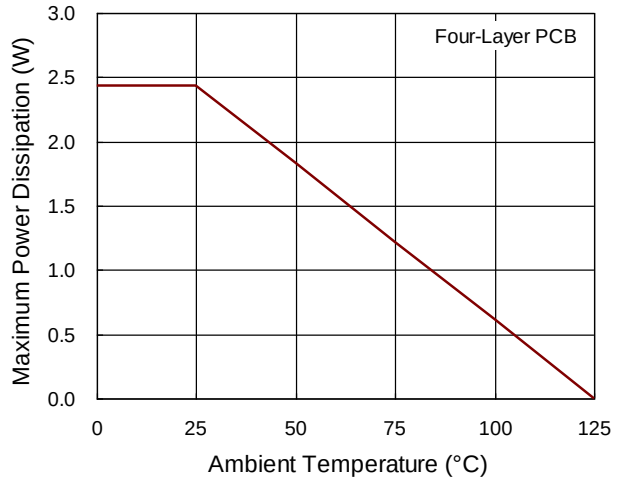


Figure 20. Derating Curve of Maximum Power Dissipation

Layout Consideration

Layout is very important in high frequency switching converter design. If designed improperly, the PCB can radiate excessive noise and contribute to the converter instability. Certain points must be considered before starting a layout for RTQ5132. Figure 21, show the recommended layout guide for reference. In Figure 21, the top layer layout of RTQ5132's EVB is demonstrated. It should be noticed that the components' size is considered and drawn in real relating size. Four inductors and one PMIC are on the same layer to avoid the necessary of phase node vias which can induce large phase ringing and EMI noise. Two bulk capacitors are placed at the same side the VIN pin for each rail. Place the small decoupling capacitor can help to filter out the high frequency voltage spike, reduce the phase ringing on phase pin. Bulk capacitors can provide prompt energy during output load transient. Most important thing is to keep away the noisy signal, like switching node, output caps' vias. Below are the key items of RTQ5132's EVB layout.

- Make traces of the high current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VINA, VINB and VINC).
- The SW node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the SW node to prevent noise couple.
- The PGND pin should be connected to a strong ground plane for heat sinking and noise protection. For better power dissipation, adding thermal vias near PGND pin to connect between different layers is recommended.
- The ground of VIN is recommended to connect to AGND then connect to PGND layer through via.
- Place the decoupling capacitors as close as possible to the device pins (VIN and AGND).
- Differential routing the feedback traces for each rail and keep away from noisy signal on the EVB.
- The NC pins at the four corners are recommended to connect to PGND for better heat dissipation.
- For the dual-phase application, must put the output capacitors (C_{OUTA} and C_{OUTB}) as close as possible, and put the sense feedback node of SWA_FB_P at the center of VDD and VDDQ is needed.

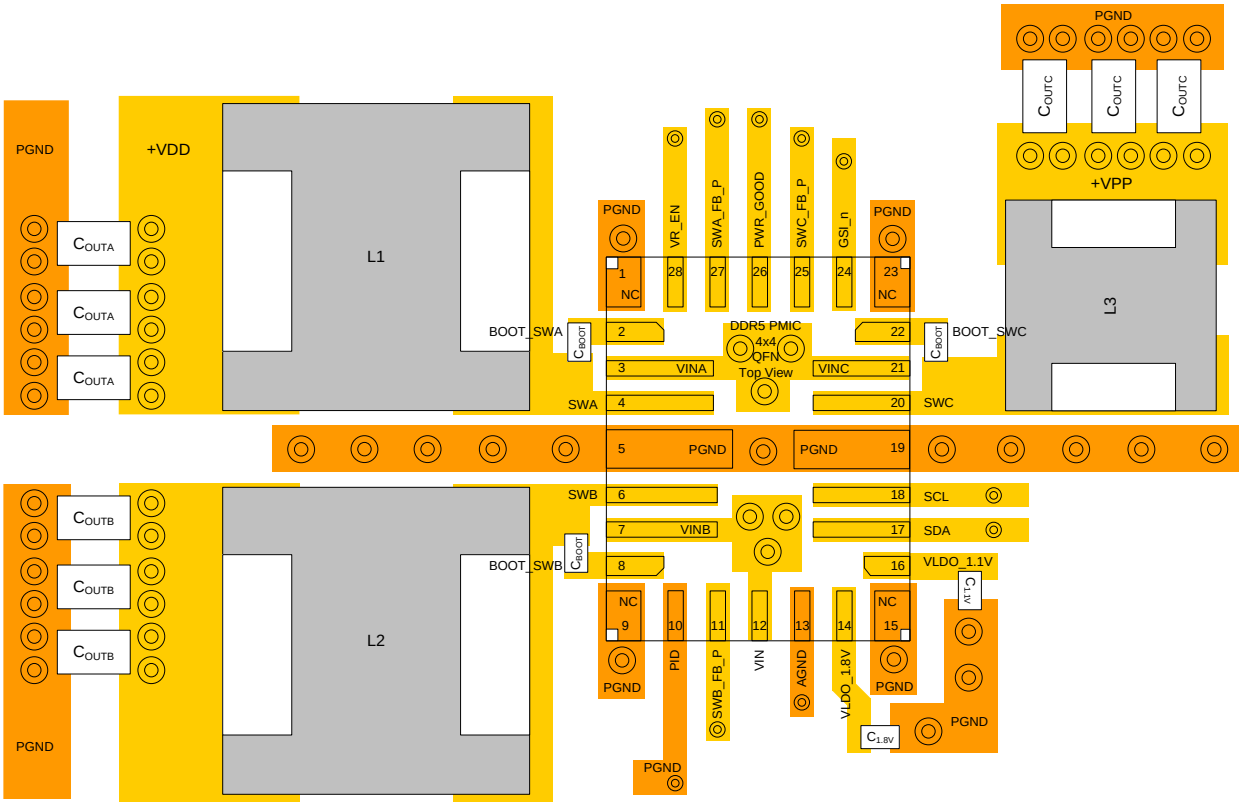


Figure 21. RTQ5132 Layout Guide (Top Layer)

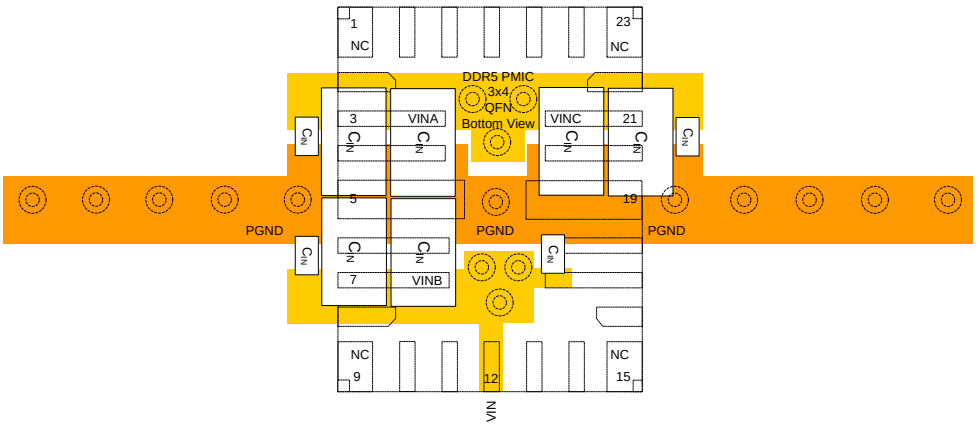


Figure 22. RTQ5132 Layout Guide (Bottom Layer)

Register Description

Register Attribute Definition

Attribute	Abbreviation	Description
Read Only	RO	This bit can be read by host. Write has no effect.
Read/Write	RW	This bit can be read or written by host.
Write Only	WO	This bit can only be written by host. Read from this bit return ‘0’.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by host. The bit will return ‘0’ when read. Write has no effect.
Write ‘1’ Only	1O	This bit can only be set (i.e. write ‘1’) but not reset (i.e. write ‘0’). Write ‘0’ has no effect.
Persistent	E	This bit is persistent during power cycle
Protected	P	This bit is protected by the password registers. This bit cannot be read to or written unless the password code has been written into the password registers.

Register Map Breakdown

Region	Register Range	Restriction
Host User (NVM and VM)	[R15 - R2F, R32]	Register Modification is NOT allowed in Secure Mode
DIMM Vendor (NVM)	[R40 - R6F]	
PMIC Vendor (NVM)	[R70 - RFF]	
Host Region	[R20 – R2D]	Registers are copied from DIMM Vendor Region Setting at power-on

Register Map (Host Region Map)

Register	Attribute	Description
R00	RV	R00 [7:0] - Reserved
R01	RV	R01 [7:0] - Reserved
R02	RV	R02 [7:0] - Reserved
R03	RV	R03 [7:0] - Reserved
R04	ROE	R04 [7] Global Error Count R04 [6] Global Error Log - Buck OV or UV R04 [5] Global Error Log - VIN_Bulk OV R04 [4] Global Error Log - Critical Temperature R04 [3:0] Reserved
R05	ROE	R05 [7] Reserved R05 [6] Power-On Reset - SWA Power Not Good R05 [5] Reserved R05 [4:3] Power-On Reset - SWB & SWC Power Not Good R05 [2:0] Power-On Reset - High Level Error Log Code

Register	Attribute	Description
R06	ROE	R06 [7] Power-On Reset - SWA Undervoltage Lockout R06 [6] Reserved R06 [5:4] Power-On Reset - SWB & SWC Undervoltage Lockout R06 [3] Power-On Reset - SWA Overvoltage R06 [2] Reserved R06 [1:0] Power-On Reset - SWB & SWC Overvoltage
R07	ROE	R07 [7:0] Reserved
R08	RO	R08 [7] Reserved R08 [6] Critical Temperature Shutdown Status R08 [5] SWA Output Power Good Status R08 [4] Reserved R08 [3:2] SWB, SWC Output Power Good Status R08 [1] Reserved R08 [0] VIN_Bulk Input Overvoltage Status
R09	RO	R09 [7] PMIC High Temperature Warning Status R09 [6] Reserved R09 [5] VOUT_1.8V Output Power Good Status R09 [4] Reserved R09 [3] SWA High Output Current Consumption Warning Status R09 [2] Reserved R09 [1:0] SWB, SWC High Output Current Consumption Warning Status
R0A	RO	R0A [7] SWA Output Overvoltage Status R0A [6] Reserved R0A [5:4] SWB, SWC Output Overvoltage Status R0A [3] PEC Error Status R0A [2] Parity Error Status R0A [1] IBI Status R0A [0] Reserved
R0B	RO	R0B [7] SWA Output Current Limiter Warning Status R0B [6] Reserved R0B [5:4] SWB, SWC Output Current Limiter Warning Status R0B [3] SWA Output Undervoltage Lockout Status R0B [2] Reserved R0B [1:0] SWB, SWC Output Current Limiter Warning Status
R0C	RO	R0C [7:0] SWA Output Current or Power or Total Output Power Measurement
R0D	RO	R0D [7:0] Reserved
R0E	RO	R0E [7:6] Reserved R0E [5:0] SWB Output Current or Power Measurement
R0F	RO	R0F [7:6] Reserved R0F [5:0] SWC Output Current or Power Measurement
R10	1O	R10 [7:6] Reserved R10 [5] Clear SWA Output Power Good Status R10 [4] Reserved R10 [3:2] Clear SWB, SWC Output Power Good Status R10 [1] Reserved R10 [0] Clear VIN_Bulk Input Overvoltage Status

Register	Attribute	Description
R11	1O	R11 [7] Clear PMIC High Temperature Warning Status R11 [6] Reserved R11 [5] Clear VOUT_1.8V Output Power Good Status R11 [4] Reserved R11 [3] Clear SWA High Output Current Consumption Warning Status R11 [2] Reserved R11 [1:0] Clear SWB, SWC High Output Current Consumption Warning Status
R12	1O	R12 [7] Clear SWA Output Overvoltage Status R12 [6] Reserved R12 [5:4] Clear SWB, SWC Output Overvoltage Status R12 [3] Clear PEC Error R12 [2] Clear Parity Error R12 [1:0] Reserved
R13	1O	R13 [7:4] Clear SWA Output Current Limiter Warning Status R13 [6] Reserved R13 [5:4] Clear SWB, SWC Output Current Limiter Warning Status R13 [3] Clear SWA Output Undervoltage Lockout Status R13 [2] Reserved R13 [1:0] Clear SWB, SWC Output Undervoltage Lockout Status
R14	RW	R14 [7:3] Reserved R14 [2] Clear VOUT_1.0V Output Power Good Status R14 [1] Reserved R14 [0] Clear Global Status
R15	RW	R15 [7:6] Reserved R15 [5] Mask SWA Output Power Good Status R15 [4] Reserved R15 [3:2] Mask SWB, SWC Output Power Good Status R15 [1] Reserved R15 [0] Mask VIN_Bulk Input Overvoltage Status
R16	RW	R16 [7] Mask PMIC High Temperature Warning Status R16 [6] Reserved R16 [5] Mask VOUT_1.8V Output Power Good Status R16 [4] Reserved R16 [3:0] Mask SWA High Output Current Consumption Warning Status R16 [2] Reserved R16 [1:0] Mask SWB, SWC High Output Current Consumption Warning Status
R17	RW	R17 [7] Mask SWA Output Overvoltage R17 [6] Reserved R17 [5:4] Mask SWB, SWC Output Overvoltage R17 [3] Mask PEC Error Status R17 [2] Mask Parity Error Status R17 [1:0] Reserved
R18	RW	R18 [7] Mask SWA Output Current Limiter Warning Status R18 [6] Reserved R18 [5:4] Mask SWB, SWC Output Current Limiter Warning Status R18 [3] Mask SWA Output Undervoltage Lockout Status R18 [2] Reserved R18 [3:0] Mask SWB, SWC Output Undervoltage Lockout Status
R19	RW	R19 [7:3] Reserved R19 [2] Mask VOUT_1.0 V Output Power Good Status R19 [1:0] Reserved

Register	Attribute	Description
R1A	RW	R1A [7:5] Reserved R1A [4] Quiescent Power State Entry Enable R1A [3] Reserved R1A [2] VOUT_1.8 V Power Good Threshold Voltage R1A [1] Output Power Select R1A [0] VOUT_1.0 V Power Good Threshold Voltage
R1B	RW	R1B [7] VIN_Bulk Input Overvoltage Threshold R1B [6] Current or Power Meter Select R1B [5] Reserved R1B [4] Global Mask PWR_GOOD Output Pin R1B [3] GSI_n Pin Enable R1B [2:0] PMIC High Temperature Warning Threshold
R1C	RW	R1C [7:2] SWA Output High Current Threshold R1C [1:0] Reserved
R1D	RW	R1D [7:0] Reserved
R1E	RW	R1E [7:2] SWB Output High Current Threshold R1E [1:0] Reserved
R1F	RW	R1E [7:2] SWC Output High Current Threshold R1E [1:0] Reserved
R20	RW	R20 [7:6] SWA Output Current Limiter Warning Threshold R20 [5:4] Reserved R20 [3:2] SWB Output Current Limiter Warning Threshold R20 [1:0] SWC Output Current Limiter Warning Threshold
R21	RW	R21 [7:1] SWA Voltage Setting R21 [0] SWA Power Good Low-Side Threshold
R22	RW	R22 [7:6] SWA Power Good High-Side Threshold R22 [5:4] SWA Overvoltage Threshold R22 [3:2] SWA Undervoltage Lockout Threshold R22 [1:0] SWA Soft-Stop Time
R23	RW	R23 [7:0] Reserved
R24	RW	R24 [7:0] Reserved
R25	RW	R25 [7:1] SWB Voltage Setting R25 [0] SWB Power Good Low-Side Threshold
R26	RW	R26 [7:6] SWB Power Good High-Side Threshold R26 [5:4] SWB Overvoltage Threshold R26 [3:2] SWB Undervoltage Lockout Threshold R26 [1:0] SWB Soft-Stop Time
R27	RW	R27 [7:1] SWC Voltage Setting R27 [0] SWC Power Good Low-Side Threshold
R28	RW	R28 [7:6] SWC Power Good High-Side Threshold R28 [5:4] SWC Overvoltage Threshold R28 [3:2] SWC Undervoltage Lockout Threshold R28 [1:0] SWC Soft-Stop Time
R29	RW	R29 [7:6] SWA Mode Select R29 [5:4] SWA Switching Frequency R29 [3:0] Reserved
R2A	RW	R2A [7:6] SWB Mode Select R2A [5:4] SWB Switching Frequency R2A [3:2] SWC Mode Select R2A [1:0] SWC Switching Frequency

Register	Attribute	Description
R2B	RW	R2B [7:6] VOUT_1.8 V LDO Setting R2B [5:3] Reserved R2B [2:1] VOUT_1.0 V LDO Setting R2B [0] Reserved
R2C	RW	R2C [7:5] SWA Soft-Start Time R2C [4:0] Reserved
R2D	RW	R2D [7:5] SWB Soft-Start Time R2D [4] Reserved R2D [3:1] SWC Soft-Start Time R2D [0] Reserved
R2E	RW	R2E [7:3] Reserved R2E [2:0] PMIC Shutdown temperature threshold
R2F	RW	R2F [7] Reserved R2F [6] SWA Enable R2F [5] Reserved R2F [4:3] SWB, SWC Enable R2F [2] Secure or Programmable Mode Select R2F [1:0] Mask Bits Register Control
R30	RW	R30 [7] ADC Enable R30 [6:3] ADC Select R30 [2] Reserved R30 [1:0] ADC Register Update Frequency
R31	RO	R31 [7:0] ADC Read Out
R32	RW, RO	R32 [7] VR Enable R32 [6] Management Interface Selection R32 [5] PWR_GOOD Signal IO Type R32 [4:3] PMIC Power Good Output Signal Control R32 [2:0] Reserved
R33	RO	R33 [7:5] Temperature Measurement R33 [4:3] Reserved R33 [2] VOUT_1.0V Output Power Good Status R33 [1:0] Reserved
R34	RW, RO	R34 [7] PEC Enable R34 [6] IBI Enable R34 [5] Parity Disable R34 [4] Reserved R34 [3:1] HID_CODE R34 [0] Reserved
R35	RW	R35 [7] Error Injection Enable R35 [6:4] Rail Selection R35 [3] Over and Undervoltage Select R35 [2:0] Misc. Error Injection Type
R36	RV	R36 [7:0] Reserved
R37	WO	R37 [7:0] Password Lower Byte 0
R38	WO	R38 [7:0] Password Upper Byte 1
R39	RW	R39 [7:0] Command Codes

Register	Attribute	Description
R3A	RW	R3A [7] Reserved R3A [6] Default Read Address Pointer Enable R3A [5:4] Default Read Address Pointer Selection R3A [3:2] Burst Length for Default Read Address Pointer Mode in PEC Enabled Mode R3A [1:0] Reserved
R3B	ROE	R3B [7:6] Reserved R3B [5:4] Major Revision ID R3B [3:1] Minor Revision ID R3B [0] Reserved
R3C	ROE	R3C [7:0] VENDOR_ID_BYTE0
R3D	ROE	R3D [7:0] VENDOR_ID_BYTE1
R3E	RV	R3E [7:0] Reserved
R3F	RV	R3E [7:0] Reserved

Register Map (DIMM Region Map)

Register	Attribute	Description
R40	RWPE	R40 [7:0] Power-On Sequence - Configuration 0
R41	RWPE	R41 [7:0] Power-On Sequence - Configuration 1
R42	RWPE	R42 [7:0] Power-On Sequence - Configuration 2
R43	RWPE	R43 [7:0] Reserved
R44	RV	R44 [7:0] Reserved
R45	RWPE	R45 [7:1] SWA Voltage Setting R45 [0] SWA Power Good Low-Side Threshold
R46	RWPE	R46 [7:6] SWA Power Good High-Side Threshold R46 [5:4] SWA Overvoltage Threshold R46 [3:2] SWA Undervoltage Lockout Threshold R46 [1:0] SWA Soft-Stop Time
R47	RWPE	R47 [7:0] Reserved
R48	RWPE	R48 [7:0] Reserved
R49	RWPE	R49 [7:1] SWB Voltage Setting R49 [0] SWB Power Good Low-Side Threshold
R4A	RWPE	R4A [7:6] SWB Power Good High-Side Threshold R4A [5:4] SWB Overvoltage Threshold R4A [3:2] SWB Undervoltage Lockout Threshold R4A [1:0] SWB Soft-Stop Time
R4B	RWPE	R4B [7:1] SWC Voltage Setting R4B [0] SWC Power Good Low-Side Threshold
R4C	RWPE	R4C [7:6] SWC Power Good High-Side Threshold R4C [5:4] SWC Overvoltage Threshold R4C [3:2] SWC Undervoltage Lockout Threshold R4C [1:0] SWC Soft-Stop Time
R4D	RWPE	R4D [7:6] SWA Mode Select R4D [5:4] SWA Switching Frequency R4D [3:0] Reserved

R4E	RWPE	R4E [7:6] SWB Mode Select R4E [5:4] SWB Switching Frequency R4E [3:2] SWC Mode Select R4E [1:0] SWC Switching Frequency
R4F	RWPE	R4F [7:1] Reserved R4F [0] SWA and SWB Single or Dual Phase Regulator Mode Select
R50	RWPE	R50 [7:6] SWA Output Current Limiter Warning Threshold R50 [5:4] Reserved R50 [3:2] SWB Output Current Limiter Warning Threshold R50 [1:0] SWC Output Current Limiter Warning Threshold
R51	RWPE	R51 [7:6] VOUT_1.8V LDO Output Voltage Setting R51 [5:3] Reserved R51 [2:1] VOUT_1.0V LDO Voltage Setting R51 [0] Reserved
R52-R57	RV	R52 [7:0] - R57 [7:0] Reserved
R58	RWPE	R58 [7:0] Power-off sequence - Configuration 0
R59	RWPE	R59 [7:0] Power-off sequence - Configuration 1
R5A	RWPE	R5A [7:0] Power-off sequence - Configuration 2
R5B	RWPE	R5B [7:0] Reserved
R5C	RV	R5C [7:0] Reserved
R5D	RWPE	R5D [7:5] SWA Soft-Start Time R5D [4:0] Reserved
R5E	RWPE	R5E [7:5] SWB Soft-Start Time R5E [4] Reserved R5E [3:1] SWC Soft-Start Time R5E [0] Reserved
R5F-R6F	RV	R5F [7:0] to R6F [7:0] Reserved

B-5 Host Region Registers

R00			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R00 [7:0]: Reserved

R01			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R01 [7:0]: Reserved

R02			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R02 [7:0]: Reserved

R03			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R03 [7:0]: Reserved

R04			
Bits	**Attribute**	**Default**	**Description**
7	ROE	0	R04 [7]: GLOBAL_ERROR_COUNT Global Error Count Since Last Erase Operation 0 = No Error or Only 1 Error Since Last Erase Operation 1 = > 1 Error Count since last Erase Operation
6	ROE	0	R04 [6]: GLOBAL_ERROR_LOG_BUCK_OV_OR_UV Global Error Log History for Buck Regulator Output Overvoltage or Undervoltage 0 = No Error Occurred 1 = Error Occurred
5	ROE	0	R04 [5]: GLOBAL_ERROR_LOG_VIN_BULK_OVER_VOTLAGE Global Error Log History for VIN_BULK Overvoltage 0 = No Error Occurred 1 = Error Occurred
4	ROE	0	R04 [4]: GLOBAL_ERROR_LOG_CRITICAL_TEMPERATURE Global Error Log History for Critical Temperature 0 = No Error Occurred 1 = Error Occurred
3:0	RV	0	R04 [3:0]: Reserved

R05			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R05 [7]: Reserved
6	ROE	0	R05 [6]: SWA_POWER_GOOD PMIC Power-On - SWA Power Not Good 0 = Normal Power-On 1 = SWA Power Not Good
5	ROE	0	R05 [5]: Reserved
4	ROE	0	R05 [4]: SWB_POWER_GOOD PMIC Power-On - SWB Power Not Good 0 = Normal Power-On 1 = SWB Power Not Good
3	ROE	0	R05 [3]: SWC_POWER_GOOD PMIC Power-On - SWC Power Not Good 0 = Normal Power-On 1 = SWC Power Not Good
2:0	ROE	0	R05 [2:0]: PMIC_ERROR_LOG PMIC Power-On - High Level Status Bit to Indicate Last Known Power Cycle or System Reset 000 = Normal Power-On 001 = Reserved 010 = Buck Regulator Output Over or Undervoltage 011 = Critical Temperature 100 = VIN_Bulk Input Overvoltage 101 = Reserved 110 = Reserved 111 = Reserved

R06			
Bits	**Attribute**	**Default**	**Description**
7	ROE	0	R06 [7]: SWA_UNDER_VOLTAGE_LOCKOUT PMIC Power-On - SWA Undervoltage Lockout 0 = Normal Power-On 1 = Power-On - SWA Undervoltage Lockout
6	ROE	0	R06 [6]: Reserved
5	ROE	0	R06 [5]: SWB_UNDER_VOLTAGE_LOCKOUT PMIC Power-On - SWB Undervoltage Lockout 0 = Normal Power-On 1 = SWB Undervoltage Lockout
4	ROE	0	R06 [4]: SWC_UNDER_VOLTAGE_LOCKOUT PMIC Power-On - SWC Undervoltage Lockout 0 = Normal Power-On 1 = SWC Undervoltage Lockout
3	ROE	0	R06 [3]: SWA_OVER_VOLTAGE PMIC Power-On - SWA Overvoltage 0 = Normal Power-On 1 = SWA Overvoltage
2	ROE	0	R06 [2]: Reserved
1	ROE	0	R06 [1]: SWB_OVER_VOLTAGE PMIC Power-On - SWB Overvoltage 0 = Normal Power-On 1 = SWB Overvoltage
0	ROE	0	R06 [0]: SWC_OVER_VOLTAGE PMIC Power-On - SWC Overvoltage 0 = Normal Power-On 1 = SWC Overvoltage

R07			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R07 [7:0]: Reserved

R08 - Power Good Status			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R08 [7]: Reserved
6	RO	0	R08 [6]: CRITICAL_TEMP_SHUTDOWN_STATUS Critical Temperature Shutdown Status 0 = No Critical Temperature Shutdown 1 = Critical Temperature Shutdown
5	RO	0	R08 [5]: SWA_OUTPUT_POWER_GOOD_STATUS Switch Node A Output Power Good Status 0 = Power Good 1 = Power Not Good
4	RO	0	R08 [4]: Reserved
3	RO	0	R08 [3]: SWB_OUTPUT_POWER_GOOD_STATUS Switch Node B Output Power Good Status 0 = Power Good 1 = Power Not Good
2	RO	0	R08 [2]: SWC_OUTPUT_POWER_GOOD_STATUS Switch Node C Output Power Good Status 0 = Power Good 1 = Power Not Good
1	RO	0	R08 [1]: Reserved
0	RO	0	R08 [0]: VIN_BULK_INPUT_OVER_VOLTAGE_STATUS VIN_BULK Input Supply Overvoltage Status 0 = No Overvoltage 1 = Overvoltage

R09			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R09 [7]: PMIC_HIGH_TEMP_WARNING_STATUS PMIC High Temperature Warning Status 0 = Temperature Below the Warning Threshold 1 = Temperature Exceeded the Warning Threshold
6	RO	0	R09 [6]: Reserved
5	RO	0	R09 [5]: VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS VOUT_1.8V LDO Output Power Good Status2 0 = Power Good 1 = Power Not Good
4	RO	0	R09 [4]: Reserved
3	RO	0	R09[3]: SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node A High Output Current Consumption Warning Status 0 = No High Current Consumption Warning 1 = High Current Consumption Warning
2	RO	0	R09 [2]: Reserved
1	RO	0	R09 [1]: SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node B High Output Current Consumption Warning Status 0 = No High Current Consumption Warning 1 = High Current Consumption Warning
0	RO	0	R09 [0]: SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node C High Output Current Consumption Warning Status 0 = No High Current Consumption Warning 1 = High Current Consumption Warning

R0A			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R0A [7]: SWA_OUTPUT_OVER_VOLTAGE_STATUS Switch Node A Output Overvoltage Status 0 = No Overvoltage 1 = Overvoltage
6	RO	0	R0A [6]: Reserved
5	RO	0	R0A [5]: SWB_OUTPUT_OVER_VOLTAGE_STATUS Switch Node B Output Overvoltage Status 0 = No Overvoltage 1 = Overvoltage
4	RO	0	R0A [5]: SWC_OUTPUT_OVER_VOLTAGE_STATUS Switch Node C Output Overvoltage Status 0 = No Overvoltage 1 = Overvoltage
3	RO	0	R0A [3]: PEC_ERROR_STATUS Packet Error Code Status 0 = No PEC Error 1 = PEC Error
2	RO	0	R0A [2]: PARITY_ERROR_STATUS T Bit Parity Error Status 0 = No Parity Error 1 = Parity Error
1	RO	0	R0A [1]: IBI_STATUS In Band Interrupt Status 0 = No Pending IBI 1 = Pending IBI
0	RV	0	R0A [0]: Reserved

R0B			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R0B [7]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node A Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
6	RO	0	R0B [6]: Reserved
5	RO	0	R0B [5]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node B Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
4	RO	0	R0B [4]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node C Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
3	RO	0	R0B [3]: SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node A Output Undervoltage Lockout Status 0 = No Undervoltage Lockout 1 = Undervoltage Lockout
2	RO	0	R0B [2]: Reserved
1	RO	0	R0B [1]: SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node B Output Undervoltage Lockout Status 0 = No Undervoltage Lockout 1 = Undervoltage Lockout
0	RO	0	R0B [0]: SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node C Output Undervoltage Lockout Status 0 = No Undervoltage Lockout 1 = Undervoltage Lockout

R0C - SWA Current & Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	0	R0C [7:0]: SWA_OUTPUT_CURRENT_POWER_MEASUREMENT If Register R1A [1] = 0, Switch Node A Output Current or Output Power Measurement 0000 0000 = Un-defined 0000 0001 = 0.125A or 125mW 0000 0010 = 0.25A or 250mW 0000 0011 = 0.375A or 375mW 0000 0100 = 0.5A or 500mW 0000 0101 = 0.625A or 625mW 0000 0110 = 0.75A or 750mW 0000 0111 = 0.875A or 875mW 0000 1000 = 1.0A or 1000mW 0000 1001 = 1.125A or 1125mW .. 0011 0111 = 6.875A or 6875mW 0011 1000 = 7.0A or 7000mW 0011 1001 = 7.125A or 7125mW 0011 1010 = 7.25A or 7250mW 0011 1011 = 7.375A or 7375mW 0011 1100 = 7.5A or 7500mW 0011 1101 = 7.625A or 7625mW 0011 1110 = 7.75A or 7750mW 0011 1111 >= 7.875A or 7875mW All other encodings are reserved If Register R1A [1] = 1, Sum of power measurement for Switch Outputs SW[A..C] 0000 0000 = Un-defined 0000 0001 = 125mW 0000 0010 = 250mW 0000 0011 = 375mW 0000 0100 = 500mW ... 1111 1100 = 31500mW 1111 1101 = 31625mW 1111 1110 = 31750mW 1111 1111 >= 31875mW

R0D			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R0D [7:0]: Reserved

R0E - SWB Current & Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R0E [7:6]: Reserved
5:0	RO	0	R0E [5:0]: SWB_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node B Output Current or Output Power Measurement 000000 = Un-defined 000001 = 0.125A or 125mW 000010 = 0.25A or 250mW 000011 = 0.375A or 375mW 000100 = 0.5A or 500mW 000101 = 0.625A or 625mW 000110 = 0.75A or 750mW 000111 = 0.875A or 875mW 001000 = 1.0A or 1000mW 001001 = 1.125A or 1125mW 001010 = 1.25A or 1250mW ... 110111 = 6.875A or 6875mW 111000 = 7.0A or 7000mW 111001 = 7.125A or 7125mW 111010 = 7.25A or 7250mW 111011 = 7.375A or 7375mW 111100 = 7.5A or 7500mW 111101 = 7.625A or 7625mW 111110 = 7.75A or 7750mW 111111 >= 7.875A or 7875mW

R0F - SWC Current & Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R0F [7:6]: Reserved
5:0	RO	0	R0F [5:0]: SWC_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node C Output Current or Output Power Measurement 000000 = Un-defined 000001 = 0.125A or 125mW 000010 = 0.25A or 250mW 000011 = 0.375A or 375mW 000100 = 0.5A or 500mW 000101 = 0.625A or 625mW 000110 = 0.75A or 750mW 000111 = 0.875A or 875mW 001000 = 1.0A or 1000mW 001001 = 1.125A or 1125mW ... 110111 = 6.875A or 6875mW 111000 = 7.0A or 7000mW 111001 = 7.125A or 7125mW 111010 = 7.25A or 7250mW 111011 = 7.375A or 7375mW 111100 = 7.5A or 7500mW 111101 = 7.625A or 7625mW 111110 = 7.75A or 7750mW 111111 >= 7.875A or 7875mW

R10			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R10 [7:6]: Reserved
5	1O	0	R10 [5]: CLEAR_SWA_OUTPUT_POWER_GOOD_STATUS Clear SWA Output Power Good Status. 1 = Clear “Register R08” [5]
4	1O	0	R10 [4]: Reserved
3	1O	0	R10 [3]: CLEAR_SWB_OUTPUT_POWER_GOOD_STATUS Clear SWB Output Power Good Status. 1 = Clear “Register R08” [3]
2	1O	0	R10 [2]: CLEAR_SWC_OUTPUT_POWER_GOOD_STATUS Clear SWC Output Power Good Status. 1 = Clear “Register R08” [2]
1	1O	0	R10 [1]: Reserved
0	1O	0	R10 [0]: CLEAR_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Clear VIN_BULK Input Supply Overvoltage Status. 1 = Clear “Register R08” [0]

R11			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	R11 [7]: CLEAR_PMIC_HIGH_TEMP_WARNING_STATUS Clear PMIC High Temperature Warning Status. 1 = Clear “Register R09” [7]
6	1O	0	R11 [6]: Reserved
5	1O	0	R11 [5]: CLEAR_VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS Clear VOUT_1.8V Output Power Good Status 1 = Clear “Register R09” [5]
4	1O	0	R11 [4]: Reserved
3	1O	0	R11 [3]: CLEAR_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node A High Output Current Consumption Warning Status. 1 = Clear “Register R09” [3]
2	1O	0	R11 [2]: Reserved
1	1O	0	R11 [1]: CLEAR_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node B High Output Current Consumption Warning Status. 1 = Clear “Register R09” [1]
0	1O	0	R11 [0]: CLEAR_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node C High Output Current Consumption Warning Status. 1 = Clear “Register R09” [0]

R12			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	R12 [7]: CLEAR_SWA_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node A Output Overvoltage Status. 1 = Clear “Register R0A” [7]
6	1O	0	R12 [6]: Reserved
5	1O	0	R12 [5]: CLEAR_SWB_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node B Output Overvoltage Status. 1 = Clear “Register R0A” [5]
4	1O	0	R12 [4]: CLEAR_SWC_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node C Output Overvoltage Status. 1 = Clear “Register R0A” [4]
3	1O	0	R12 [3]: CLEAR_PER_ERROR_STATUS Clear PEC Error Status. 1 = Clear “Register 0x0A” [3]
2	1O	0	R12 [2]: CLEAR_PARITY_ERROR_STATUS Clear Parity Error Status. 1 = Clear “Register 0x0A” [2]
1:0	RV	0	R12 [1:0]: Reserved

R13			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	R13 [7]: CLEAR_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node A Output Current Limiter Warning Status. 1 = Clear “Register R0B” [7]
6	1O	0	R13 [6]: Reserved
5	1O	0	R13 [5]: CLEAR_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node B Output Current Limiter Warning Status. 1 = Clear “Register R0B” [5]
4	1O	0	R13 [4]: CLEAR_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node C Output Current Limiter Warning Status. 1 = Clear “Register R0B” [4]
3	1O	0	R13 [3]: CLEAR_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node A Output Undervoltage Lockout Status. 1 = Clear “Register R0B” [3]
2	1O	0	R13 [2]: Reserved
1	1O	0	R13 [1]: CLEAR_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node B Output Undervoltage Lockout Status. 1 = Clear “Register R0B” [1]
0	1O	0	R13 [0]: CLEAR_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node C Output Undervoltage Lockout Status. 1 = Clear “Register R0B” [0]

R14			
Bits	**Attribute**	**Default**	**Description**
7:3	RV	0	R14 [7:3]: Reserved
2	1O	0	R14 [2]: CLEAR_VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS Clear VOUT_1.0V Output Power Good Status. 1 = Clear “Register R33” [2]
1	RV	0	R14 [1]: Reserved
0	1O	0	R14 [0]: GLOBAL_CLEAR_STATUS Clear all status bits. 1 = Clear all status bits

R15			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R15 [6]: Reserved
5	RW	1	R15 [5]: MASK_SWA_OUTPUT_POWER_GOOD_STATUS Mask SWA Output Power Good Status Event1. 0 = Do Not Mask SWA Output Power Good Status Event 1 = Mask SWA Output Power Good Status Event
4	RW	0	R15 [4]: Reserved
3	RW	1	R15 [3]: MASK_SWB_OUTPUT_POWER_GOOD_STATUS Mask SWB Output Power Good Status Event1,2. 0 = Do Not Mask SWB Output Power Good Status Event 1 = Mask SWB Output Power Good Status Event
2	RW	1	R15 [2]: MASK_SWC_OUTPUT_POWER_GOOD_STATUS Mask SWC Output Power Good Status Event1. 0 = Do Not Mask SWC Output Power Good Status Event 1 = Mask SWC Output Power Good Status Event
1	RW	0	R15 [1]: Reserved
0	RW	0	R15 [0]: MASK_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Mask VIN_Bulk Input Supply Overvoltage Status Event. 0 = Do Not Mask VIN_Bulk Input Supply Overvoltage Status Event 1 = Mask VIN_Bulk Input Supply Overvoltage Status Event

R16			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R16 [7]: MASK_PMIC_HIGH_TEMP_WARNING_STATUS Mask PMIC High Temperature Warning Status Event. 0 = Do Not Mask PMIC High Temperature Warning Status Event 1 = Mask PMIC High Temperature Warning Status Event
6	RW	0	R16 [6]: Reserved
5	RW	1	R16 [5]: MASK_VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS Mask VOUT_1.8V Output Power Good Status Event. 0 = Do Not Mask 1.8V Output Power Good Status Event 1 = Mask 1.8V Output Power Good Status Event
4	RW	0	R16 [4]: Reserved
3	RW	0	R16 [3]: MASK_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask Switch Node A High Output Current Consumption Warning Status Event. 0 = Do Not Mask Switch Node A Output Current Consumption Warning Status Event 1 = Mask Switch Node A Output Current Consumption Warning Status Event
2	RW	0	R16 [2]: Reserved
1	RW	0	R16 [1]: MASK_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask Switch Node B High Output Current Consumption Warning Status Event 0 = Do Not Mask Switch Node B Output Current Consumption Warning Status Event 1 = Mask Switch Node B Output Current Consumption Warning Status Event
0	RW	0	R16 [0]: MASK_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask Switch Node C High Output Current Consumption Warning Status Event. 0 = Do Not Mask Switch Node C Output Current Consumption Warning Status Event 1 = Mask Switch Node C Output Current Consumption Warning Status Event

R17			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R17 [7]: MASK_SWA_OUTPUT_OVER_VOLTAGE_STATUS Mask Switch Node A Output Overvoltage Status Event. 0 = Do Not Mask Switch Node A Output Overvoltage Status Event 1 = Mask Switch Node A Output Overvoltage Status Event
6	RW	0	R17 [6]: Reserved
5	RW	0	R17 [5]: MASK_SWB_OUTPUT_OVER_VOLTAGE_STATUS Mask Switch Node B Output Overvoltage Status Event2. 0 = Do Not Mask Switch Node B Output Overvoltage Status Event 1 = Mask Switch Node B Output Overvoltage Status Event
4	RW	0	R17 [4]: MASK_SWC_OUTPUT_OVER_VOLTAGE_STATUS Mask Switch Node C Output Overvoltage Status Event. 0 = Do Not Mask Switch Node C Output Overvoltage Status Event 1 = Mask Switch Node C Output Overvoltage Status Event
3	RW	0	R17 [3]: MASK_PEC_ERROR_STATUS Mask PEC Error Event for GSI_n output Only 0 = Do Not Mask PEC Error Status Event 1 = Mask PEC Error Status
2	RW	0	R17 [2]: MASK_PARITY_ERROR_STATUS Mask Parity Error Event for GSI_n output Only 0 = Do Not Mask Parity Error Status Event 1 = Mask Parity Error Status
1:0	RV	0	R17 [1:0]: Reserved

R18			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R18 [7]: MASK_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node A Output Current Limiter Warning Status Event. 0 = Do Not Mask Switch Node A Output Current Limiter Warning Status Event 1 = Mask Switch Node A Output Current Limiter Warning Status Event
6	RW	0	R18 [6]: Reserved
5	RW	0	R18 [5]: MASK_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node B Output Current Limiter Warning Status Event. 0 = Do Not Mask Switch Node B Output Current Limiter Warning Status Event 1 = Mask Switch Node B Output Current Limiter Warning Status Event
4	RW	0	R18 [4]: MASK_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node C Output Current Limiter Warning Status Event. 0 = Do Not Mask Switch Node C Output Current Limiter Warning Status Event 1 = Mask Switch Node C Output Current Limiter Warning Status Event
3	RW	0	R18 [3]: MASK_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node A Output Undervoltage Lockout Status Event. 0 = Do Not Mask Switch Node A Output Undervoltage Lockout Status Event 1 = Mask Switch Node A Output Undervoltage Lockout Status Event
2	RW	0	R18 [2]: Reserved
1	RW	0	R18 [1]: MASK_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node B Output Undervoltage Lockout Status Event3. 0 = Do Not Mask Switch Node B Output Undervoltage Lockout Status Event 1 = Mask Switch Node B Output Undervoltage Lockout Status Event
0	RW	0	R18 [0]: MASK_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node C Output Undervoltage Lockout Status Event. 0 = Do Not Mask Switch Node C Output Undervoltage Lockout Status Event 1 = Mask Switch Node C Output Undervoltage Lockout Status Event

R19			
Bits	**Attribute**	**Default**	**Description**
7:3	RV	0	R19 [7:3]: Reserved
2	RW	1	R19 [2]: MASK_VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS Mask VOUT_1.0V Output Power Good Status Event. 0 = Do Not Mask 1.0V Output Power Good Status Event 1 = Mask 1.0V Output Power Good Status Event
1:0	RV	0	R19 [1:0]: Reserved

R1A			
Bits	**Attribute**	**Default**	**Description**
7:5	RW	000	R1A [7:5]: Reserved
4	RV	0	R1A [4]: QUIESCENT_STATE_EN PMIC Quiescent State Entry Enable 0 = Disable 1 = Enable
3	RW	0	R1A [3]: Reserved
2	RW	0	R1A [2]: VOUT_1.8V_POWER_GOOD_THRESHOLD_VOLTAGE VOUT 1.8V LDO Output Threshold Voltage for Power Good Status 0 = 1.6V 1 = Reserved
1	RW	0	R1A [1]: OUTPUT_POWER_SELECT Switch Regulator Output Power Select 0 = Report Power Measurement for Each Rail in R0C, R0E & R0F 1 = Report Total Power Measurement of Each Rail in R0C
0	RW	0	R1A [0]: VLDO_1.0V_POWER_GOOD_THRESHOLD_VOLTAGE VOUT 1.0V LDO Output Threshold Voltage for Power Good Status 0 = –10% from the setting in “Register R51” [2:1] 1 = –15% from the setting in “Register R51” [2:1]

R1B			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R1B [7]: VIN_BULK_OVER_VOLTAGE_THRESHOLD VIN_Bulk Input Overvoltage Threshold Setting For GSI_n Assertion 0 = 5.8 V to 6 V (Varies across vendors) 1 = Reserved
6	RW	0	R1B [6]: CURRENT_OR_POWER_METER_SELECT PMIC Output Regulator Measurement - Current or Power Meter 0 = Report Current Measurements in registers 1 = Report Power Measurements in registers
5	RW	0	R1B [5]: Reserved
4	RW	0	R1B [4]: GLOBAL_PWR_GOOD_PIN_STATUS_MASK Global Mask PWR_GOOD Output Pin 0 = Not Masked 1 = Masked
3	RW	0	R1B [3]: GSI_N_PIN_ENABLE Enable GSI_n Pin 0 = Disable GSI_n Pin 1 = Enable GSI_n Pin
2:0	RW	101	R1B [2:0]: PMIC_HIGH_TEMPERATURE_WARNING_THRESHOLD PMIC High Temperature Warning Threshold 000 = Reserved 001 = PMIC temperature >= 85°C 010 = PMIC temperature >= 95°C 011 = PMIC temperature >= 105°C 100 = PMIC temperature >= 115°C 101 = PMIC temperature >= 125°C 110 = PMIC temperature >= 135°C 111 = Reserved

R1C - SWA High Current Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:2	RW	011000	R1C [7:2]: SWA_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node A Output High Current Consumption Warning Threshold 000000 = Un-defined 000001 = > 0.125A 000010 = > 0.25A 000011 = > 0.375A 000100 = > 0.5A 000101 = > 0.625A 000110 = > 0.75A 000111 = > 0.875A 001000 = > 1.0A 001001 = > 1.125A ... ... 010111 = > 2.875A 011000 = > 3.0A 011001 = > 3.125A ... 110111 = > 6.875A 111000 = > 7.0A 111001 = > 7.125A 111010 = > 7.25A 111011 = > 7.375A 111100 = > 7.5A 111101 = > 7.625A 111110 = > 7.75A 111111 = > 7.875A
1:0	RV	0	R1C [1:0]: Reserved

R1D			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R1D [7:0]: Reserved

R1E - SWB High Current Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:2	RW	011000	R1E [7:2]: SWB_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node B Output High Current Consumption Warning Threshold 000000 = Un-defined 000001 = > 0.125A 000010 = > 0.25A 000011 = > 0.375A 000100 = > 0.5A 000101 = > 0.625A 000110 = > 0.75A 000111 = > 0.875A 001000 = > 1.0A 001001 = > 1.125A ... 010111 = > 2.875A 011000 = > 3.0A ... 110111 = > 6.875A 111000 = > 7.0A 111001 = > 7.125A 111010 = > 7.25A 111011 = > 7.375A 111100 = > 7.5A 111101 = > 7.625A 111110 = > 7.75A 111111 = > 7.875A
1:0	RV	0	R1E [1:0]: Reserved

R1F - SWC High Current Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:2	RW	011000	R1F [7:2]: SWC_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node C Output High Current Consumption Warning Threshold 000000 = Un-defined 000001 = > 0.125A 000010 = > 0.25A 000011 = > 0.375A 000100 = > 0.5A 000101 = > 0.625A 000110 = > 0.75A 000111 = > 0.875A 001000 = > 1.0A 001001 = > 1.125A ... 010111 = > 2.875A 011000 = > 3.0A 011001 = > 3.125A ... 110111 = > 6.875A 111000 = > 7.0A 111001 = > 7.125A 111010 = > 7.25A 111011 = > 7.375A 111100 = > 7.5A 111101 = > 7.625A 111110 = > 7.75A 111111 = > 7.875A
1:0	RV	0	R1F [1:0]: Reserved

R20			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	11	R20 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, Ivalley_limit: 00 = 3A 01 = 3.5A 10 = 4A 11 = 4.5A
5:4	RV	00	R20 [5:4]: Reserved
3:2	RW	11	R20 [3:2]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, Ivalley_limit: 00 = 3A 01 = 3.5A 10 = 4A 11 = 4.5A
1:0	RW	11	R20 [1:0]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, Ivalley_limit: 00 = 0.5A 01 = 1.0A 10 = 1.5A 11 = 2.0A

R21 - SWA Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	R21 [7:1]: SWA_VOLTAGE_SETTING Switch Node A Output Regulator Voltage Setting 000 0000 = 800mV 000 0001 = 805mV 000 0010 = 810mV ... 011 1100 = 1100mV ... 111 1101 = 1425mV 111 1110 = 1430mV 111 1111 = 1435mV
0	RW	0	R21 [0]: SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register R21,” [7:1] 1 = –7.5% from the setting in “Register R21,” [7:1]

R22 - SWA Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R22 [7:6]: SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High-Side Voltage “Upper bound level” For Power Good Status 00 = +5% from the setting in “Register R21,” [7:1] 01 = +7.5% from the setting in “Register R21,” [7:1] 10 = +10% from the setting in “Register R21,” [7:1] 11 = +3% from the setting in “Register R21,” [7:1]
5:4	RW	10	R22 [5:4]: SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Overvoltage Status 00 = +7.5% from the setting in “Register R21,” [7:1] 01 = +10% from the setting in “Register R21,” [7:1] 10 = +12.5% from the setting in “Register R21,” [7:1] 11 = +5% from the setting in “Register R21,” [7:1]
3:2	RW	00	R22 [3:2]: SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Undervoltage Lockout Status 00 = –10% from the setting in “Register R21,” [7:1] 01 = –12.5% from the setting in “Register R21,” [7:1] 10 = –5% from the setting in “Register R21,” [7:1 11 = –7.5% from the setting in “Register R21,” [7:1]
1:0	RW	11	R22 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

R23			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R23 [7:0]: Reserved

R24			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R24 [7:0]: Reserved

R25 - SWB Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	R25 [7:1]: SWB_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting 000 0000 = 800mV 000 0001 = 805mV 000 0010 = 810mV ... 011 1100 = 1100mV ... 111 1101 = 1425mV 111 1110 = 1430mV 111 1111 = 1435mV
0	RW	0	R25 [0]: SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register R25,” [7:1] 1 = –7.5% from the setting in “Register R25,” [7:1]

R26 - SWB Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R26 [7:6]: SWB_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R25,” [7:1] 01 = +7.5% from the setting in “Register R25,” [7:1] 10 = +10% from the setting in “Register R25,” [7:1] 11 = +3% from the setting in “Register R25,” [7:1]
5:4	RW	10	R26 [5:4]: SWB_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Overvoltage Status 00 = +7.5% from the setting in “Register R25,” [7:1] 01 = +10% from the setting in “Register R25,” [7:1] 10 = +12.5% from the setting in “Register R25,” [7:1] 11 = +5% from the setting in “Register R25,” [7:1]
3:2	RW	00	R26 [3:2]: SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Undervoltage Lockout Status 00 = –10% from the setting in “Register R25,” [7:1] 01 = –12.5% from the setting in “Register R25,” [7:1] 10 = –5% from the setting in “Register R25,” [7:1] 11 = –7.5% from the setting in “Register R25,” [7:1]
1:0	RW	11	R26 [1:0]: SWB_OUTPUT_SOFT_STOP_TIME SWB Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

R27 - SWC Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	R27 [7:1]: SWC_VOLTAGE_SETTING Switch Node C Output Regulator Voltage Setting 000 0000 = 1500mV 000 0001 = 1505mV 000 0010 = 1510mV ... 011 1100 = 1800mV ... 111 1101 = 2125mV 111 1110 = 2130mV 111 1111 = 2135mV
0	RW	0	R27 [0]: SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register R27,” [7:1] 1 = –7.5% from the setting in “Register R27,” [7:1]

R28 - SWC Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R28 [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R27” [7:1] 01 = +7.5% from the setting in “Register R27” [7:1] 10 = +10% from the setting in “Register R27” [7:1] 11 = +3% from the setting in “Register R27” [7:1]
5:4	RW	10	R26 [5:4]: SWC_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Overvoltage Status 00 = +7.5% from the setting in “Register R25” [7:1] 01 = +10% from the setting in “Register R25” [7:1] 10 = +12.5% from the setting in “Register R25” [7:1] 11 = +5% from the setting in “Register R27” [7:1]
3:2	RW	00	R26 [3:2]: SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Undervoltage Lockout Status 00 = –10% from the setting in “Register R25” [7:1] 01 = –12.5% from the setting in “Register R25” [7:1] 10 = –5% from the setting in “Register R27” [7:1] 11 = –7.5% from the setting in “Register R27” [7:1]
1:0	RW	11	R26 [1:0]: SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft-Stop Time After VR Disable 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

R29 - SW[A:B] FSW & Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	10	R29 [7:6]: SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RW	00	R29 [5:4]: SWA_SWITCHING_FREQ Switch Node A Output Regulator Switching Frequency (Note) 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz
3:0	RW	0000	R29 [3:0]: Reserved

(Note: Notification for that only 750kHz operating frequency available in dual phase operation, 0x29[5:4]/0x2A[5:4] FREQ setting will be blocked.)

R2A - SWC FSW & Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	10	R2A [7:6]: SWB_MODE_SELECT Switch Node B Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RW	00	R2A [5:4]: SWB_SWITCHING_FREQ Switch Node B Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz
3:2	RW	10	R2A [3:2]: SWC_MODE_SELECT Switch Node D Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
1:0	RW	00	R2A [1:0]: SWC_SWITCHING_FREQ Switch Node C Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz

R2B			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R2B [7:6]: VOUT_1.8V _VOLTAGE_SETTING VLDO_1.8V Voltage Setting: 00 = 1.7V 01 = 1.8V 10 = 1.9V 11 = 2.0V
5	RV	0	R2B [5]: Reserved
4	RV	0	R2B [4]: Reserved
3	RV	0	R2B [3]: Reserved
2:1	RW	01	R2B [2:1]: VOUT_1.0V _VOLTAGE_SETTING VLDO_1.0V Voltage Setting: 00 = 0.9V 01 = 1.0V 10 = 1.1V 11 = 1.2V
0	RV	0	R2B [0]: Reserved

R2C - SWA Soft-Start & STOP Time			
Bits	**Attribute**	**Default**	**Description**
7:5	RW	001	R2C [7:5]: SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
4:0	RV	0	R2C [4:0]: Reserved

R2D - SW[B:C] Soft-Start & STOP Time			
Bits	**Attribute**	**Default**	**Description**
7:5	RW	001	R2D [7:5]: SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
4	RV	0	R2D [4]: Reserved
3:1	RW	001	R2D [3:1]: SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
0	RV	0	R2D [0]: Reserved

R2E - Shutdown Temp. Threshold			
Bits	**Attribute**	**Default**	**Description**
7:3	RV	0	R2E [7:3]: Reserved
2:0	RW	100	R2E [2:0]: PMIC_SHUTDOWN_TEMPERATURE_THRESHOLD PMIC Shutdown Temperature Threshold 000 = PMIC Temperature >= 105°C 001 = PMIC Temperature >= 115°C 010 = PMIC Temperature >= 125°C 011 = PMIC Temperature >= 135°C 100 = PMIC Temperature >= 145°C 101 = Reserved 110 = Reserved 111 = Reserved

R2F - PMIC Configuration			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R2F [7]: Reserved
6	RW	0	R2F [6]: SWA_REGULATOR_CONTROL Disable SWA Regulator Output 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RW	0	R2F [5]: Reserved
4	RW	0	R2F [4]: SWB_REGULATOR_CONTROL Disable SWB Regulator Output 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RW	0	R2F [3]: SWC_REGULATOR_CONTROL Disable SWC Regulator Output 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2	RW	0	R2F [2]: SECURE_MODE PMIC Mode Operation 0 = Secure Mode Operation 1 = Programmable Mode Operation
1:0	RW	10	R2F [1:0]: MASK_BITS_REGISTER_CONTROL Mask Bits Register Control 00 = Mask GSI_n Signal Only (PWR_GOOD Signal will assert) 01 = Mask PWR_GOOD Only (GSI_n signal will assert) 10 = Mask GSI_n and PWR_GOOD Signals (neither PWR_GOOD assert or GSI_n signal will assert) 11 = Reserved

R30 - ADC Enable			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R30 [7]: ADC_ENABLE Enable ADC (Analog to Digital Conversion) 0 = Disable 1 = Enable
6:3	RW	0	R30 [6:3]: ADC_SELECT Input Selection for ADC Readout 0000 = SWA Output Voltage 0001 = Reserved 0010 = SWB Output Voltage 0011 = SWC Output Voltage 0100 = Reserved 0101 = VIN_BULK Input Voltage 0110 = Reserved 0111 = Reserved 1000 = VOUT_1.8V Output Voltage 1001 = VOUT_1.0V Output Voltage All other encodings are reserved.
2	RV	0	R30 [2]: Reserved
1:0	RW	0	R30 [1:0]: ADC_REGISTER_UPDATE_FREQUENCY ADC Current or Power Measurement Update Frequency 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

R31 - ADC Read			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	0	R31 [7:0]: ADC_READ ADC Output Voltage Reading (Applies to SW[A:C], VOUT_1.8V, VOUT_1.0V) 0000 0000 = Undefined 0000 0001 = 15mV 0000 0010 = 30mV .. 1111 1111 >= 3825mV ADC Output Voltage Reading (Applies to VIN_BULK Input Voltage) 0000 0000 = Undefined 0000 0001 = 70mV 0000 0010 = 140mV .. 1111 1111 >= 17850mV

R32 - PMIC_EN & Mgmt Interface Selection			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R32 [7]: VR_ENABLE PMIC Enable 0 = PMIC Disable 1 = PMIC Enable
6	RO	0	R32 [6]: MANAGEMENT_INTERFACE_SELECTION PMIC Management Bus Interface Protocol Selection 0 = I^2C Interface (Max speed 1MHZ) 1 = I^3C Basic Protocol
5	RW	0	R32 [5]: PWR_GOOD_IO_TYPE PMIC PWR_GOOD Output Signal Type 0 = Output only 1 = Input and Output
4:3	RW	00	R32 [4:3]: PMIC_PWR _OUTPUT_SIGNAL_CONTROL PMIC PWR_GOOD Output Signal Control 0x = PMIC controls PWR_GOOD on its own based on internal status 10 = PWR_GOOD Output Low 11 = PWR_GOOD Output Float
2:0	RV	0	R32 [2:0]: Reserved

R33 - Temp_Meas & LDO Status			
Bits	**Attribute**	**Default**	**Description**
7:5	RO	0	R33 [7:5]: TEMPERATURE_MEASUREMENT PMIC Temperature 000 = ≤ 80°C (± 5°C) 001 = 85°C (± 5°C) 010 = 95°C (± 5°C) 011 = 105°C (± 5°C) 100 = 115°C (± 5°C) 101 = 125°C (± 5°C) 110 = 135°C (± 5°C) 111 = > 140°C (± 5°C)
4:3	RO	0	R33 [4]: Reserved
2	RO	0	R33 [2]: VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS VOUT_1.0V LDO Output Power Good Status 0 = Power Good 1 = Power Not Good
1:0	RV	0	R33 [1:0]: Reserved

R34 – PEC/IBI/PARITY/HID_CODE			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R34 [7]: PEC_ENABLE Packet Error Code Enable (Applicable Only if R32 [6] = ‘1’) 0 = Disable 1 = Enable
6	RO	0	R34 [6]: IBI_ENABLE In Band Interrupt Enable (Applicable Only if R32 [6] = ‘1’) 0 = Disable 1 = Enable
5	RW	0	R34 [5]: PARITY_DISABLE T Bit Parity Code Disable (Applicable Only if R32 [6] = ‘1’.) 0 = Enable 1 = Disable4
4	RV	0	R34 [4]: Reserved
3:1	RW	111	R34 [3:1]: HID_CODE PMIC’s 3-bit HID Code 000 001 010 011 100 101 110 111
0	RV	0	R34 [0]: Reserved

R35 - Error Injection			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R35 [7]: ERROR_INJECTION_ENABLE Error Injection Enable 0 = Disable 1 = Enable
6:4	RW	0	R35 [6:4]: ERROR_INJECTION_RAIL_SELECTION Error Injection - Input Rail and Output Rail Selection 000 = Undefined 001 = SWA Output Only 010 = Reserved 011 = SWB Output Only 100 = SWC Output Only 101 = VIN_Bulk Input Only 110 = Reserved 111 = Do Not Use
3	RW	0	R35 [3]: OVER_VOLTAGE_UNDER_VOLTAGE_SELECT Overvoltage or Undervoltage Selection for Bits R35[6:4] 0 = Overvoltage 1 = Undervoltage
2:0	RW	0	R35 [2:0]: MISC_ERROR_INJECTION_TYPE Miscellaneous Error Injection Type 000 = Undefined 001 = Reserved 010 = Critical Temperature Shutdown 011 = High Temperature Warning Threshold 100= VOUT_1.8V LDO Power Good 101 = High Current Consumption Warning 110 = Reserved 111 = Current Limiter Warning

R36 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R36 [7:0]: Reserved

R37 - DIMM Vendor Region Password Lower Byte			
Bits	**Attribute**	**Default**	**Description**
7:0	WO	0	R37 [7:0]: DIMM_VENDOR_MEMORY_REGION_PASSWORD_LOWER_BYTE DIMM Vendor Memory Region (R40 - R6F) Password - Lower Byte [7:0] = Code

R38 - DIMM Vendor Region Password Upper Byte			
Bits	**Attribute**	**Default**	**Description**
7:0	WO	0	R38 [7:0]: DIMM_VENDOR_MEMORY_REGION_PASSWORD_UPPER_BYTE DIMM Vendor Memory Region (R40 - R6F) Password - Upper Byte [7:0] = Code

R39 - DIMM Vendor Password Control			
Bits	**Attribute**	**Default**	**Description**
7:0	RW	0	Host Region Codes: 0x74: Clear Registers R04 to R07, Erase MTP memory for R04 Register. DIMM Vendor Region (R40 to R6F) Write Codes: 0x00: Lock DIMM Vendor Region. 0x40: Unlock DIMM Vendor Region. Password needs to be present in R37 & R38 registers. 0x80: Burn DIMM Vendor Region Password. New password needs to be present in R37 & R38. 0x81: Burn DIMM Vendor Region - R40 to R4F 0x82: Burn DIMM Vendor Region - R50 to R5F 0x85: Burn DIMM Vendor Region - R60 to R6F DIMM Vendor Region (R40 to R6F) Read Codes: 0x5A: Burning is complete in DIMM Vendor region.

R3A – Default Address Pointer			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R3A [7]: Reserved
6	RW	0	R3A [6]: DEFAULT_READ_ADDRESS_POINTER_ENABLE Enable Default Address Read Pointer when PMIC sees STOP operation 0 = Disable Default Address Pointer (address pointer is set by Host) 1 = Enable Default Address Pointer; Address selected by register bits [5:4]
5:4	RW	0	R3A [5:4]: DEFAULT_READ_STARTING_ADDRESS Default Read Address Pointer Selection when PMIC sees STOP operation 00 = R08 01 = R0C 10 = Reserved 11 = Reserved
3:2	RW	0	R3A [3:2]: BURST_LENGTH_FOR_READ_DEFAULT_ADDR_POINTER Burst Length (# of Bytes) to be transferred for Read Default Address Pointer Mode 00 = 2 Bytes 01 = 4 Bytes 10 = Reserved 11 = 16 Bytes
1:0	RV	0	R3A [1:0]: Reserved

R3B - Revision ID, PMIC Current Capability Selection			
Bits	**Attribute**	**Default**	**Description**
7:6	ROE	0	R3B [7:6]: Reserved
5:4	ROE	--	R3B [5:4]: REVISION_ID_MAJOR_STEPPING Major Revision Stepping 00 = Revision 1 01 = Revision 2 10 = Revision 3 11 = Revision 4
3:1	ROE	--	R3B [3:1]: REVISION_ID_MINOR_STEPPING Minor Revision Stepping 000 = Revision 0 001 = Revision 1 010 = Revision 2 011 = Revision 3 All other encodings are reserved.
0	ROE	--	R3B [0]: Reserved

R3C - Vendor ID Byte0			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	10001010	R3C [7:0]: VENDOR_ID_BYTE0 Vendor Identification Register Byte 0.

R3D - Vendor ID Byte1			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	10001100	R3D [7:0]: VENDOR_ID_BYTE1 Vendor Identification Register Byte 1.

R3E - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R3E [7:0]: Reserved

R3F - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R3F [7:0]: Reserved

DIMM Vendor Region Registers

R40 – Power-On Sequence Configuration 0			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R40 [7]: POWER_ON_SEQUENCE_CONFIG0 PMIC Power-On Sequence Config0 0 = Do Not Execute Config0 1 = Execute Config0
6	RWPE	0	R40 [6]: POWER_ON_SEQUENCE_CONFIG0_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RWPE	0	R40 [5]: Reserved
4	RWPE	0	R40 [4]: POWER_ON_SEQUENCE_CONFIG0_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RWPE	1	R40 [3]: POWER_ON_SEQUENCE_CONFIG0_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2:0	RWPE	001	R40 [2:0]: POWER_ON_SEQUENCE_CONFIG0_IDLE Idle time after Power-On Sequence Config0 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

R41 – Power-On Sequence Configuration 1			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R41 [7]: POWER_ON_SEQUENCE_CONFIG1 PMIC Power-On Sequence Config 1 0 = Do Not Execute Config 1 = Execute Command 1
6	RWPE	1	R41 [6]: POWER_ON_SEQUENCE_CONFIG1_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RWPE	0	R41 [5]: Reserved
4	RWPE	1	R41 [4]: POWER_ON_SEQUENCE_CONFIG1_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RWPE	1	R41 [3]: POWER_ON_SEQUENCE_CONFIG1_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2:0	RWPE	001	R41 [2:0]: POWER_ON_SEQUENCE_CONFIG1_IDLE Idle time after Power-On Sequence Config1 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

R42 – Power-On Sequence Configuration 2			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	R42 [7]: POWER_ON_SEQUENCE_CONFIG2 PMIC Power-On Sequence Config2 0 = Do Not Execute Config2 1 = Execute Config2
6	RWPE	0	R42 [6]: POWER_ON_SEQUENCE_CONFIG2_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RWPE	0	R42 [5]: Reserved
4	RWPE	0	R42 [4]: POWER_ON_SEQUENCE_CONFIG2_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RWPE	0	R42 [3]: POWER_ON_SEQUENCE_CONFIG2_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2:0	RWPE	000	R42 [2:0]: POWER_ON_SEQUENCE_CONFIG2_IDLE Idle time after Power-On Sequence Config2 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

R43- Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	-	R43 [7:0]: Reserved

R44 – Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	-	R44 [7:0]: Reserved

R45 – SWA Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	R45 [7:1]: SWA_VOLTAGE_SETTING Switch Node A Output Regulator Voltage Setting 000 0000 = 800mV 000 0001 = 805mV 000 0010 = 810mV … 011 1100 = 1100mV … 111 1101 = 1425mV 111 1110 = 1430mV 111 1111 = 1435mV
0	RWPE	0	R45 [0]: SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register R45” [7:1] 1 = –7.5% from the setting in “Register R45” [7:1]

R46 – SWA Threshold, Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R46 [7:6]: SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R45” [7:1] 01 = +7.5% from the setting in “Register R45” [7:1] 10 = +10% from the setting in “Register R45” [7:1] 11 = +3% from the setting in “Register R45” [7:1]
5:4	RWPE	10	R46 [5:4]: SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Overvoltage Status 00 = +7.5% from the setting in “Register R45” [7:1] 01 = +10% from the setting in “Register R45” [7:1] 10 = +12.5% from the setting in “Register R45” [7:1] 11 = +5% from the setting in “Register R45” [7:1]
3:2	RWPE	00	R46 [3:2]: SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Undervoltage Lockout Status 00 = –10% from the setting in “Regist r R45” [7:1] 01 = –12.5% from the setting in “Register R45” [7:1] 10 = –5% from the setting in “Register R45” [7:1] 11 = –7.5% from the setting in “Register R45” [7:1]
1:0	RWPE	11	R46 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

R47- Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	-	R47 [7:0]: Reserved

R48- Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	-	R48[7:0]: Reserved

R49 – SWB Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	R49 [7:1]: SWB_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting 000 0000 = 800mV 000 0001 = 805mV 000 0010 = 810mV … 011 1100 = 1100mV … 111 1101 = 1425mV 111 1110 = 1430mV 111 1111 = 1435mV
0	RWPE	0	R49 [0]: SWCB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register R49” [7:1] 1 = –7.5% from the setting in “Register R49” [7:1]

R4A – SWB Threshold, Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R4A [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R49” [7:1] 01 = +7.5% from the setting in “Register R49” [7:1] 10 = +10% from the setting in “Register R49” [7:1] 11 = +3% from the setting in “Register R49” [7:1]
5:4	RWPE	10	R4A [5:4]: SWB_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Overvoltage Status 00 = +7.5% from the setting in “Register R49” [7:2] 01 = +10% from the setting in “Register R49” [7:1] 10 = +12.5% from the setting in “Register R49” [7:1] 11 = +5% from the setting in “Register R49” [7:1]
3:2	RWPE	00	R4A [3:2]: SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Undervoltage Lockout Status 00 = –10% from the setting in “Register R49” [7:1] 01 = –12.5% from the setting in “Register R49” [7:1] 10 = –5% from the setting in “Register R49” [7:1] 11 = –7.5% from the setting in “Register R49” [7:1]
1:0	RWPE	11	R4A [1:0]: SWB_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

R4B – SWC Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	R4B [7:1]: SWC_VOLTAGE_SETTING Switch Node C Output Regulator Voltage Setting2 000 0000 = 1500mV 000 0001 = 1505mV 000 0010 = 1510mV … 011 1100 = 1800mV … 111 1101 = 2125mV 111 1110 = 2130mV 111 1111 = 2135mV
0	RWPE	0	R4B [0]: SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register R4B” [7:1] 1 = –7.5% from the setting in “Register R4B” [7:1]

R4C – SWC Threshold, Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R4C [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R4B” [7:1] 01 = +7.5% from the setting in “Register R4B” [7:1] 10 = +10% from the setting in “Register R4B” [7:1] 11 = +3% from the setting in “Register R4B” [7:1]
5:4	RWPE	10	R4C [5:4]: SWC_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Overvoltage Status 00 =+7.5% from the setting in “Register R4B” [7:1] 01 = +10% from the setting in “Register R4B” [7:1] 10 = +12.5% from the setting in “Register R4B” [7:1] 11 = +5% from the setting in “Register R4B” [7:1]
3:2	RWPE	00	R4C [3:2]: SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Undervoltage Lockout Status 00 = –10% from the setting in “Register R4B” [7:1] 01 = –12.5% from the setting in “Register R4B” [7:1] 10 = –5% from the setting in “Register R4B” [7:1] 11 = –7.5% from the setting in “Register R4B” [7:1]
1:0	RWPE	11	R4C [1:0]: SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft-Stop Time After VR Disable 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

R4D – SWA FSW & Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	10	R4D [7:6]: SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
5:4	RWPE	00	R4D [5:4]: SWA_SWITCHING_FREQ Switch Node A Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz
3:0	RWPE	0000	R4D [3:2]: Reserved

R4E – SW[B:C] FSW & Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	10	R4E [7:6]: SWB_MODE_SELECT Switch Node B Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
5:4	RWPE	00	R4E [5:4]: SWB_SWITCHING_FREQ Switch Node B Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz
3:2	RWPE	10	R4E [3:2]: SWC_MODE_SELECT Switch Node C Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
1:0	RWPE	00	R4E [1:0]: SWC_SWITCHING_FREQ Switch Node C Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz

R4F			
Bits	**Attribute**	**Default**	**Description**
7:1	RV	0	R4F [7]: Reserved
0	RWPE	0	R4F [0]: SWA_SWB_PHASE_MODE_SELECT Switch Node A and Switch Node B Phase Regulator Mode Selection. 0 = Single Phase Regulator Mode 1 = Dual Phase Regulator Mode

R50 – SW[A:C] Current Limited Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	11	R50 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Switch Node A Output Current Limiter Warning Threshold Setting For COT Mode, Ivalley_limit: 00 = 3.0A 01 = 3.5A 10 = 4.0A 11 = 4.5A
5:4	RWPE	00	R50 [5:4]: Reserved
3:2	RWPE	11	R50 [3:2]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Switch Node B Output Current Limiter Warning Threshold Setting1 For COT Mode, Ivalley_limit: 00 = 3.0A 01 = 3.5A 10 = 4.0A 11 = 4.5A
1:0	RWPE	11	R50 [1:0]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Switch Node C Output Current Limiter Warning Threshold Setting For COT Mode, Ivalley_limit: 00 = 0.5A 01 = 1.0A 10 = 1.5A 11 = 2.0A

R51 – LDO Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R51 [7:6]: VOUT_1.8V_VOLTAGE_SETTING VOUT 1.8 V LDO Output Voltage Setting1 00 = 1.7V 01 = 1.8V 10 = 1.9V 11 = 2.0V
5:3	RV	0	R51 [5:3]: Reserved
2:1	RWPE	01	R51 [2:1]: VOUT_1.0V_VOLTAGE_SETTING VOUT 1.0 V LDO Voltage Setting 00 = 0.9V 01 = 1.0V 10 = 1.1V 11 = 1.2V
0	RV	0	R51 [0]: Reserved

R52-R57 – Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R52 [7:0] – R57 [7:0]: Reserved
R58 – Power-off sequence Configuration 0			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R58 [7]: POWER_OFF_SEQUENCE_CONFIG0 PMIC Power-off sequence Config0 0 = Do Not Execute Config0 1 = Execute Config0
6	RWPE	1	R58 [6]: POWER_OFF_SEQUENCE_CONFIG0_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RV	0	R58 [5]: Reserved
4	RWPE	1	R58 [4]: POWER_OFF_SEQUENCE_CONFIG0_SWB_DISABLE Enable Switch Node B Output Regulator. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	0	R58 [3]: POWER_OFF_SEQUENCE_CONFIG0_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
2:0	RWPE	001	R58 [2:0]: POWER_OFF_SEQUENCE_CONFIG0_IDLE Idle time after Power-off sequence Config0 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

R59 – Power-off sequence Configuration 1			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R59 [7]: POWER_OFF_SEQUENCE_CONFIG1 PMIC Power-off sequence Config1 0 = Do Not Execute Config1 1 = Execute Config1
6	RWPE	1	R59 [6]: POWER_OFF_SEQUENCE_CONFIG1_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RV	0	R59 [5]: Reserved
4	RWPE	1	R59 [4]: POWER_OFF_SEQUENCE_CONFIG1_SWB_DISABLE Disable Switch Node B Output Regulator4. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	1	R59 [3]: POWER_OFF_SEQUENCE_CONFIG1_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
2:0	RWPE	001	R59 [2:0]: POWER_OFF_SEQUENCE_CONFIG1_IDLE Idle time after Power-off sequence Config1 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

R5A – Power-off sequence Configuration 2			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	R5A [7]: POWER_OFF_SEQUENCE_CONFIG2 PMIC Power-off sequence Config2 0 = Do Not Execute Config2 1 = Execute Config2
6	RWPE	0	R5A [6]: POWER_OFF_SEQUENCE_CONFIG2_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RWPE	0	R5A [5]: Reserved
4	RWPE	0	R5A [4]: POWER_OFF_SEQUENCE_CONFIG2_SWB_DISABLE Disable Switch Node B Output Regulator4. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	0	R5A [3]: POWER_OFF_SEQUENCE_CONFIG2_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
2:0	RWPE	0	R5A [2:0]: POWER_OFF_SEQUENCE_CONFIG2_IDLE Idle time after Power-off sequence Config2 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

R5B – Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R5B [7:0]: Reserved

R5C – Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R5C [7:0]: Reserved

R5D – SW[A:B] Soft-Start Time			
Bits	**Attribute**	**Default**	**Description**
7:5	RWPE	001	R5D [7:5]: SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms … 111 = 14ms
4:0	RV	0	R5D [4:0]: Reserved

R5E – SW[B:C] Soft-Start Time			
Bits	**Attribute**	**Default**	**Description**
7:5	RWPE	001	R5E [7:5]: SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms … 111 = 14ms
4	RV	0	R5E [4]: Reserved
3:1	RWPE	001	R5E [3:1]: SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms … 111 = 14ms
0	RV	0	R5E [0]: Reserved

Recommended Component Selection for Typical Application Circuit

Suggested Component for SWA and SWB

Component	Value	Physical Size	Part No.
L1, L2	0.47μH	3.2 x 2.5 x 1.2	HTTD32251BR47MMR/GLVQMR4701A
L1, L2	0.68μH	3.2 x 2.5 x 1.2	HTTD32251BR68MMR/GLVQMR6801A
C_{BYPx}	0.1μF	10V; 0201	GRM033C81E104KE14
C_{INx}	22μF (x2)	10V; 0402	GRM188R61A226ME15
C_{OUTx}	47μF (x2)	6.3V; 0603	GRM188R60J476ME01

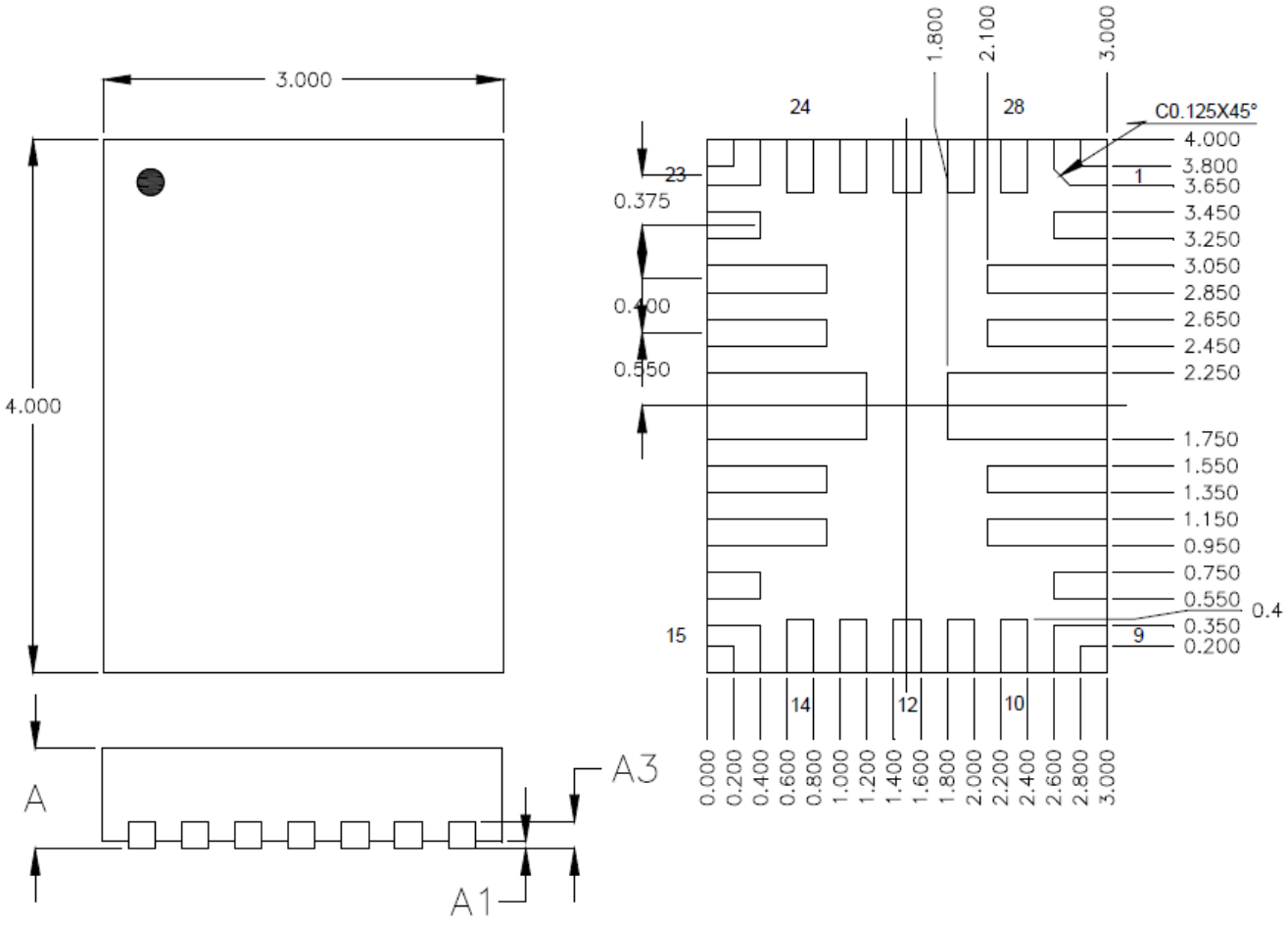
Suggested Component for SWC

Component	Value	Physical Size	Part No.
L3	1.0μH	2.5 x 2.0 x 1.2	HTTD25201B1R0MSR/GLULM1R001A/DFE252012P-1R0M
L3	1.5μH	2.5 x 2.0 x 1.2	HTTD25201B1R5MSR/GLULM1R501A/MEMK2520D1R5ML
C_{BYPC}	0.1μF	10V; 0201	GRM033C81E104KE14
C_{INC}	22μF (x2)	10V; 0402	GRM188R61A226ME15
C_{OUTC}	47μF (x2)	6.3V; 0603	GRM188R60J476ME01

Suggested Component for VLDO_1.8V and VLDO_1.0V

Component	Value	Physical Size	Part No.
C_{BYP}	0.1μF	10V; 0201	GRM033C81E104KE14
C_{IN}	4.7μF	10V; 0402	GRM155R61A475MEAA
$C_{LDO\_1.8V}$	4.7μF	6.3V; 0402	GRM155R60J475ME47
$C_{LDO\_1.0V}$	4.7μF	6.3V; 0402	GRM155R60J475ME47

Outline Dimension

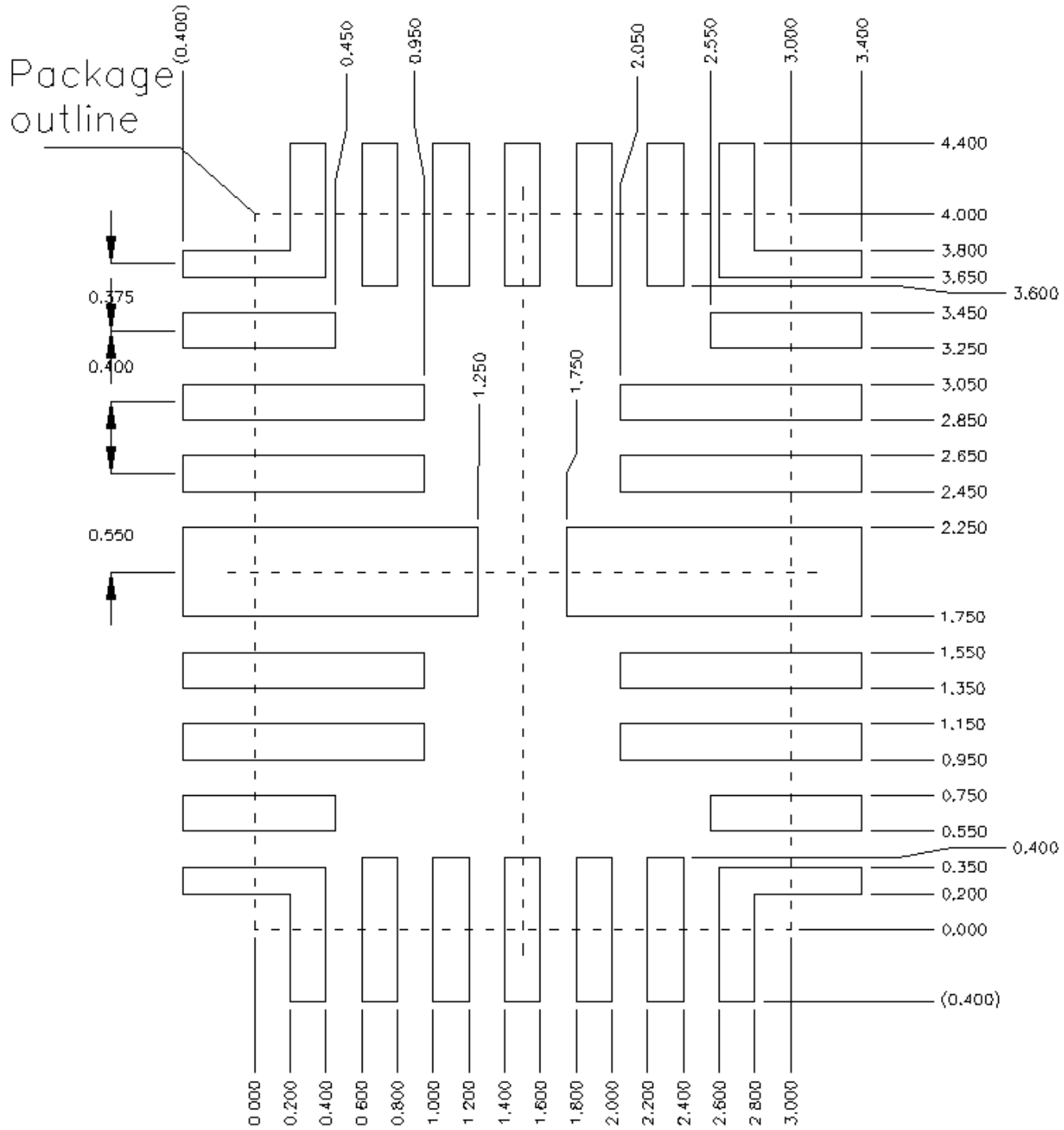


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050

W-Type 28L QFN 3x4 (FC) Package

Footprint Information



Package	Number of Pin	Tolerance
V/W/U/XQFN3x4-28(FC)	28	±0.05

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Datasheet Revision History

Version	Date	Description	Item
05	2022/12/19	Modify	Electrical Characteristics on P1 Application Information on P52
06	2023/9/14	Modify	Ordering Information on P1 General Description on P1 Simplified Application Circuit on P2 Electrical Characteristics P40 Note 2 on P42 Typical Application Circuit on P44 Application Information on P60, 61, 67