TFT LCD Integrated Power Module for Automotive

General Description

The RTQ6752-QT is an I2C interface programmable power management IC. The IC includes two synchronous boost converters for PAVDD, one synchronous NAVDD buck-boost, with 8-bit Calibrator and one RESET voltage detector. With available in a WET-WQFN-20L 5x5 package, this device is suitable for automotive TFT-LCD panel.

The IC can operate from 2.5V to 5.5V input voltages. High switching frequency operation prevent that the switching noise to interfere AM band. Current-limit functions are provided for all internal- switch converters, and output-fault shutdown protects all converters against output-fault conditions, and output the FAULT signal to communicate with automotive computer. Programmable soft-start functions for all output voltage to limit input inrush current during startup.

Ordering Information

RTQ6752 □□-QT

Package Type
QWT : WET-WQFN-20L 5x5 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RTQ6752GQWT-QT : Product Number
YMDNN : Date Code

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Features

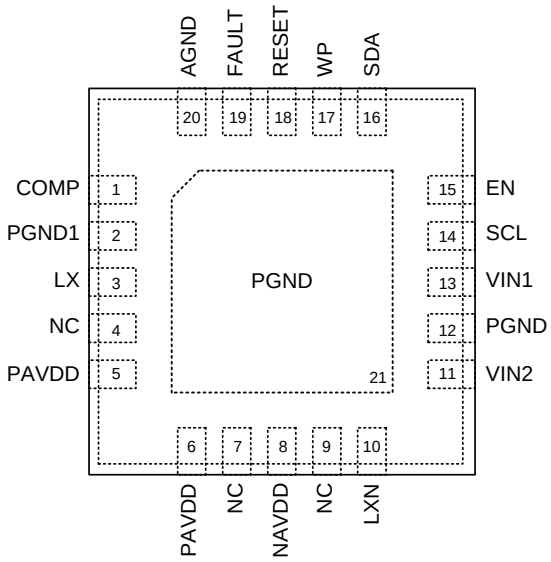
- **2.5V to 5.5V Input Supply Voltage**
- **I2C Interface**
- **Power-on and Power-off Sequence Free**
- **PAVDD Programmable Output Voltage 5V to 7.3V**
- **PAVDD Output Current Capability up to 200mA**
- **NAVDD Programmable Output Voltage –5V to –7.3V**
- **NAVDD Output Current Capability up to 200mA**
- **Outputs Power-off Discharge Function**
- **Programmable Voltage Detector**
- **AEC-Q100 Grade 2 Qualified**
- **Built in UVLO, UVP, OVP, SCP and OTP Protection**

Applications

- **Infotainment LCD panel**

Pin Configuration

(TOP VIEW)



WET-WQFN-20L 5x5

Typical Application Circuit

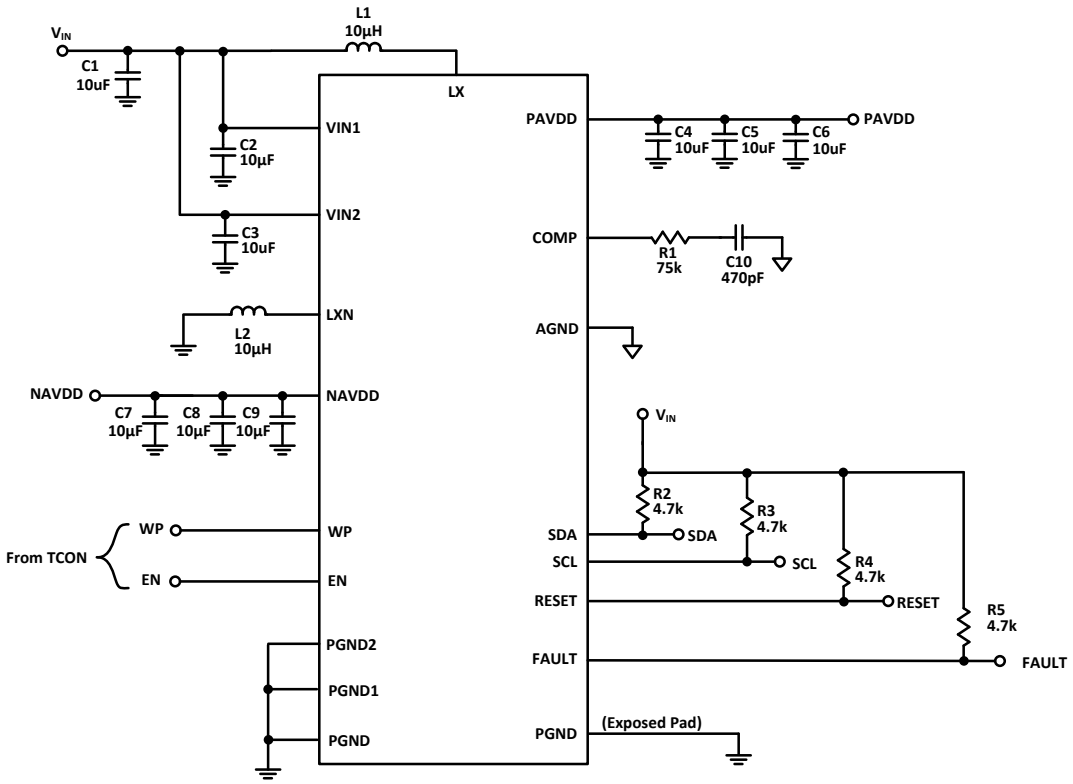


Figure 1. Typical Application Circuit

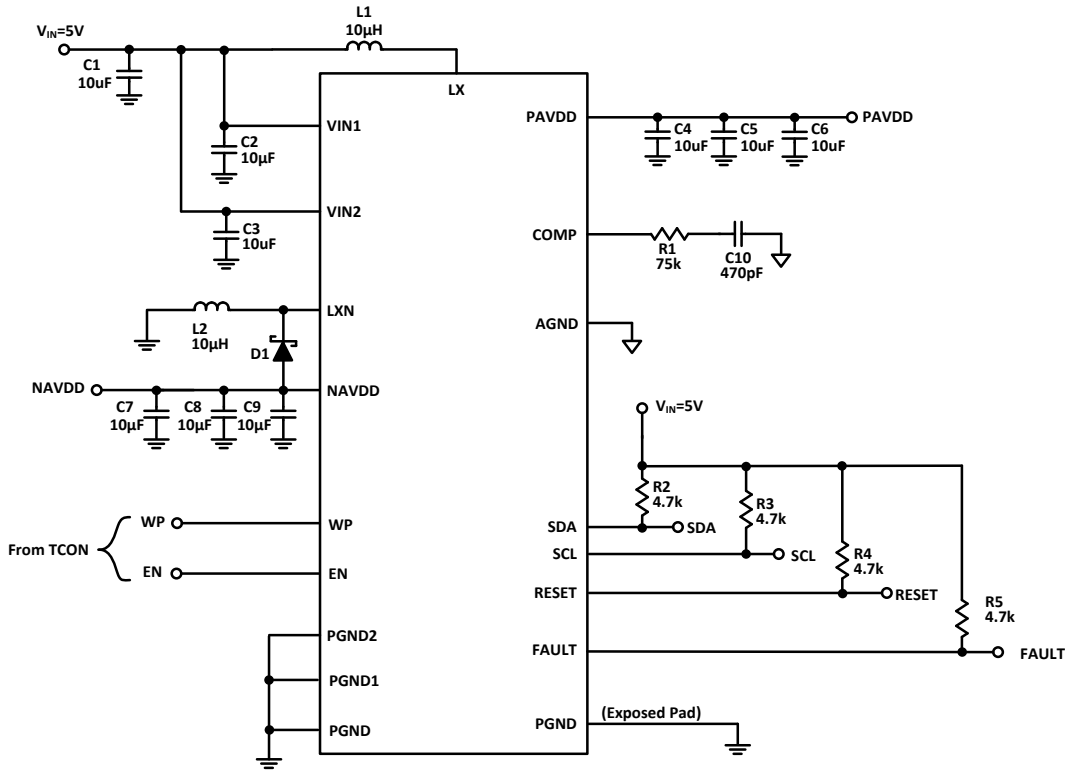


Figure 2. The Application Circuit of VIN > 4V Application

Timing Diagram

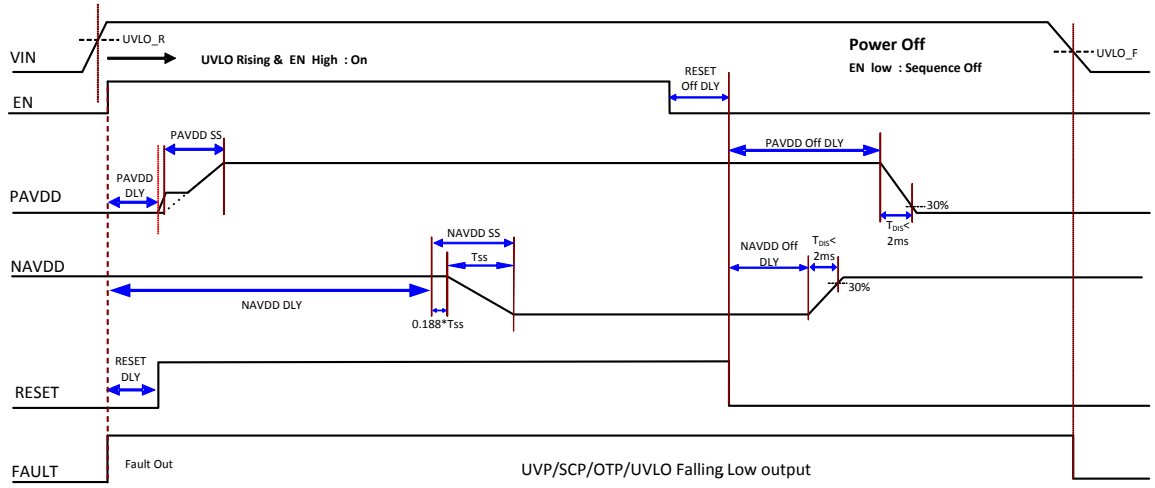


Figure 3. Power Sequence with Sequence Power-Off

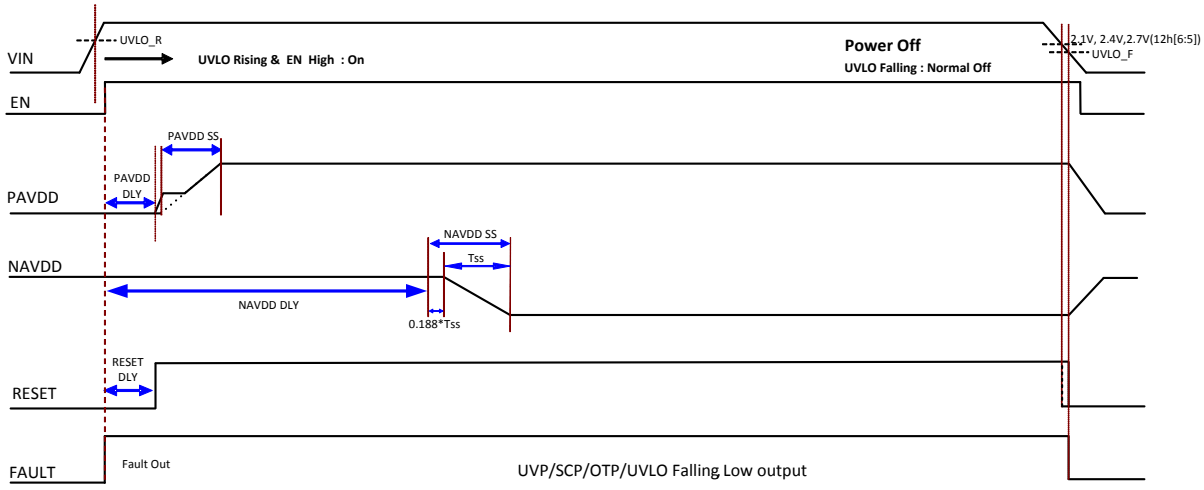


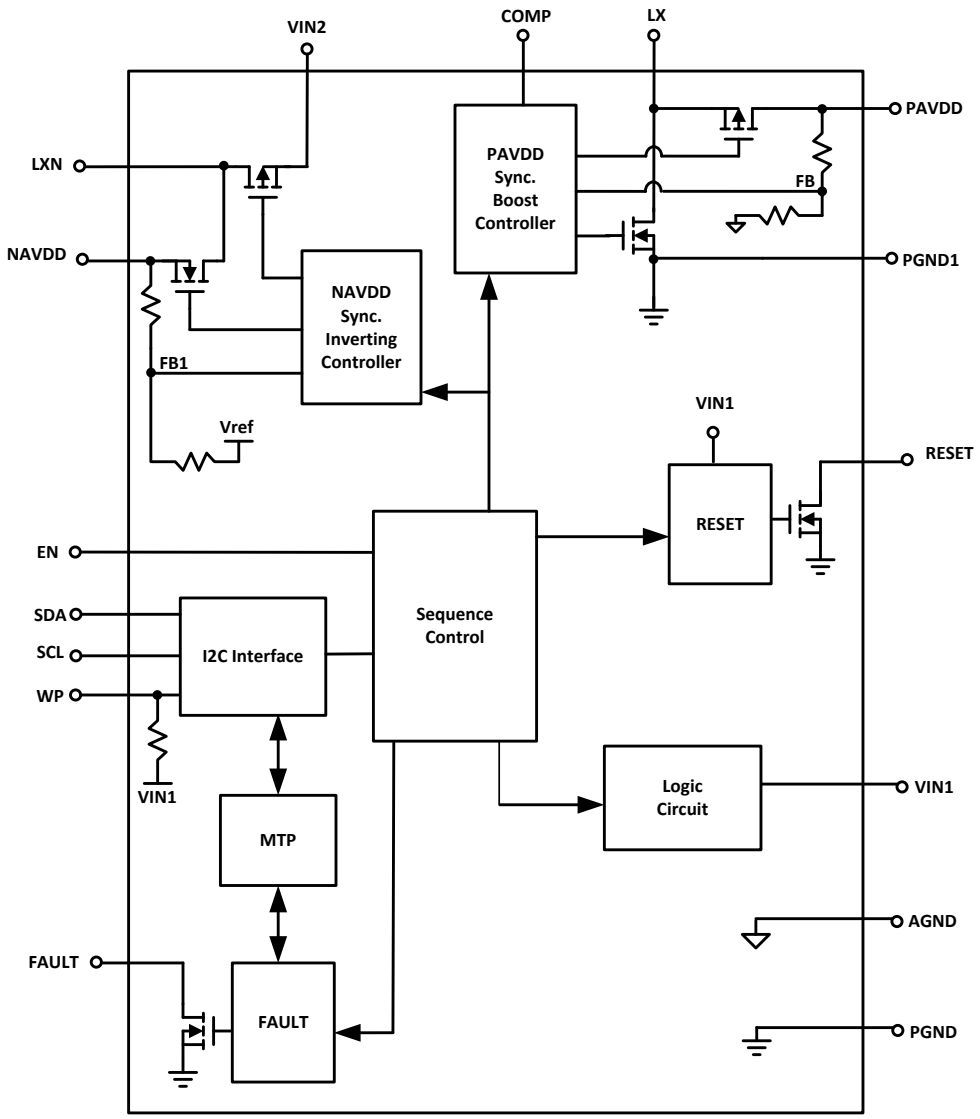
Figure 4. Power Sequence with Normal Power-Off

Note 1. Before IC power-up, the PAVDD and NAVDD outputs voltage will be detected. If the one of outputs voltage is not below the SCP level, IC will wait the output voltage fall below the SCP level, then power up with sequence.

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	COMP	PAVDD boost converter compensation input.
2	PGND1	Power ground of PAVDD boost converter.
3	LX	Switching node of PAVDD boost converter.
4	NC	No internal connection.
5	PAVDD	PAVDD output voltage sense feedback input.
6	PAVDD	PAVDD boost converter output.
7	NC	No internal connection.
8	NAVDD	NAVDD inverting converter output.
9	NC	No internal connection.
10	LXN	Switching node of NAVDD inverting converter.
11	VIN2	NAVDD supply voltage input.
12	PGND1	Power Ground of PAVDD boost converter.
13	VIN1	IC supply voltage input.
14	SCL	I2C clock input.
15	EN	Enable control input.
16	SDA	I2C clock input.
17	WP	MTP write protection. When WP = 1, MTP is protected, but register still can be written. WP = 0, register and MTP can be written.
18	RESET	Output of voltage detection function
19	FAULT	Fault signal output.
20	AGND	Analog ground.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- VIN1, VIN2 to AGND ---------- –0.3 to 6V
- PGND2, PGND1, AGND to PGND ---------- –0.3 to 0.3V
- COMP, RESET, FAULT, WP, SDA, SCL, EN to AGND ---------- –0.3 to 6V
- LX, PAVDD to PGND ---------- –0.3 to 10V
- VIN2 to LXN ---------- –0.3 to 13V
- NAVDD to PGND ---------- –12 to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  WET-WQFN-20L 5x5 ---------- 3.54W
- Package Thermal Resistance (Note 2)
  WET-WQFN-20L 5x5, θ_{JA} ---------- 28.2°C/W
  WET-WQFN-20L 5x5, θ_{JC} ---------- 7.1°C/W
- Lead Temperature (Soldering, 10 sec) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –60°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN1, VIN2 ---------- 2.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 150°C
- Ambient Temperature Range ---------- –40°C to 105°C

Electrical Characteristics

(VIN1 = 2.5V to 5.5V, T_A = –40°C to 105°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General						
VIN1 Range	V_{IN1}		2.5	--	5.5	V
VIN1 Under-Voltage-Lockout Threshold	V_{UVLO_R}	VIN1 rising, turn-on IC	2.16	2.33	2.5	V
	V_{UVLO_H}	$V_{UVLO\_H} = V_{UVLO\_R} - V_{UVLO\_F}$	0.01	0.15	0.3	V
EN/WP Input Threshold	V_{IH}		1.5	--	--	V
	V_{IL}		--	--	0.8	V
VIN1 Quiescent Current	I_{VIN1}	SW not switching	0	1.5	4.5	mA
		SW switching	0	1.75	5	mA
VIN1 Shutdown Current		EN = Low, VIN1 = 3.3V	0	200	400	μA
Switch Frequency Range	f_{OSC}		600	--	2200	kHz
Switch Frequency Accuracy			–15	--	15	%
UVP Voltage Percentage	UVP		58	70	78	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UVP Fault Delay Duration to IC Shutdown	t_{UVP}		30	50	70	ms
SCP Voltage percentage	SCP		23	30	37	%
SCP Delay	t_{SCP}		85	100	115	μs
Power Off Delay Time	t_{D_poff}	3ms/step, 16 steps	0	--	45	ms
Thermal Shutdown	T_{SD}	Temperature rising	--	150	--	°C
	ΔT_{SD}	Hysteresis	--	20	--	°C
PAVDD Sync. Boost Converter						
Output Voltage Range	V_{PAVDD}	0.05V/step, f_{SW} = 2.2MHz	5.0 VIN + 2.2	--	7.3	V
		0.05V/step, $f_{SW} \leq$ 1MHz	5.0 VIN + 0.9	--	7.3	V
Output Voltage Tolerance		T_A = 25°C, (V_O – V_S) / V_S x 100%	–1	--	1	%
		T_A= –40°C to 105°C, (V_O - V_S) / V_S x 100%	–2	--	2	%
Minimum On Time	TON_MIN		90	150	210	ns
Power On Delay Time	PAVDD ON DLY	5ms/step, 16 steps	0	--	75	ms
Power Off Delay Time	PAVDD OFF DLY	2ms/step, 8 steps	0	--	14	ms
Soft-start Time	PAVDD SS	5ms/step, 8 steps	5	--	40	ms
Delay/Soft-start Time Tolerance			–15	--	15	%
Max. Duty	D_{MAX_PAVDD}		83	90	97	%
OVP Voltage percentage	V_{OVP_PAVDD}	PAVDD rising	110	120	130	%
Current Limit	I_{LIM_PAVDD}		1.5	1.8	2.3	A
R_{ON} Low-Site	$R_{DSON\_LS\_PAVDD}$		0.05	0.2	0.4	Ω
R_{ON} High-Site	$R_{DSON\_HS\_PAVDD}$		0.05	0.3	0.4	Ω
Power On/Off Discharge R_{ON}	PAVDD_R_{DIS}		3	5	7	Ω
R_{ON} High-Site	$R_{DSON\_HS\_PAVDD}$		--	0.2	--	V
PAVDD SCP level	PAVDD_SCP_2	Before PAVDD soft-start finish	1.134	1.26	1.386	V
NAVDD Sync. Buck-Boost Converter						
Output Voltage Range	V_{NAVDD}	0.05V/step	–5	--	–7.3	V
Output Voltage Tolerance		T_A = 25°C, (V_O – V_S) / V_S x 100%	–1	--	1	%
		T_A= –40°C to 105°C, (V_O - V_S) / V_S x 100%	–2	--	2	%
Power On Delay Time	NAVDD ON DLY	5ms/step, 16 steps	0	--	75	ms
Power Off Delay Time	NAVDD OFF DLY	2ms/step, 8 steps	0	--	14	ms
Soft-Start Time	NAVDD SS	5ms/step, 8 steps	5	--	40	ms
Delay/Soft-start Time Tolerance			–15	--	15	%
Max. Duty	D_{MAX_NAVDD}		83	90	97	%
OVP Voltage percentage	V_{OVP_NAVDD}	NAVDD falling	110	120	130	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
R_{ON} High-Site	$R_{DSON\_HS\_NAVDD}$		0.05	0.14	0.4	Ω
R_{ON} Low-Site	$R_{DSON\_LS\_NAVDD}$		0.05	0.23	0.4	Ω
Power On/Off Discharge R_{ON}	NAVDD_R_{DIS}		8	10.5	13	Ω
Current Limit	I_{LIM_NAVDD}		1.5	1.9	2.6	A
RESET Function						
Delay Time	RESET ON DLY	5ms/step, 16 steps	0	--	75	ms
I2C Interface						
Logic-Input High Input	V_{IH}	SCL, SDA	1.05	--	--	V
Logic-Input Low Input	V_{IL}	SCL, SDA	--	--	0.4	V
SCL Clock Frequency	f_{SCL}		15	400	1000	kHz

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

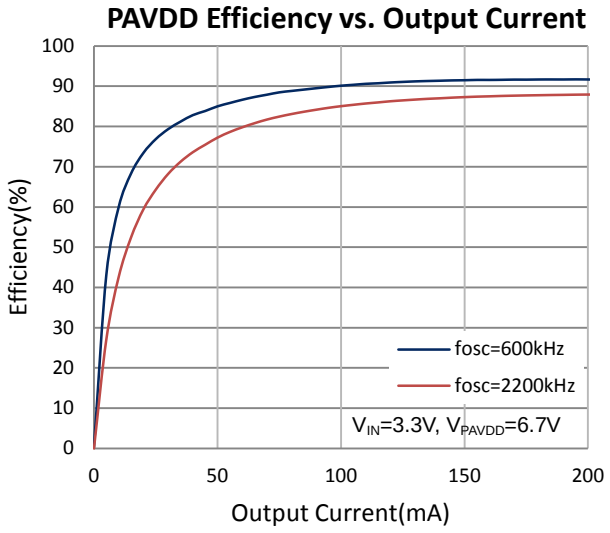
Note 4. Devices are ESD sensitive. Handling precautions are recommended.

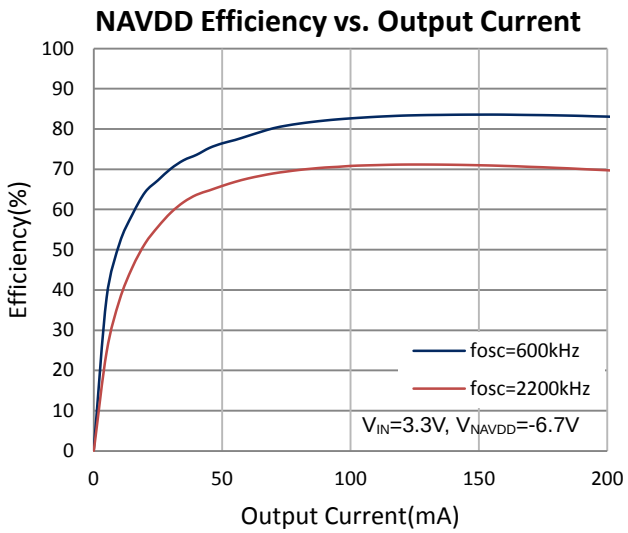
Note 5. The device is not guaranteed to function outside its operating conditions.

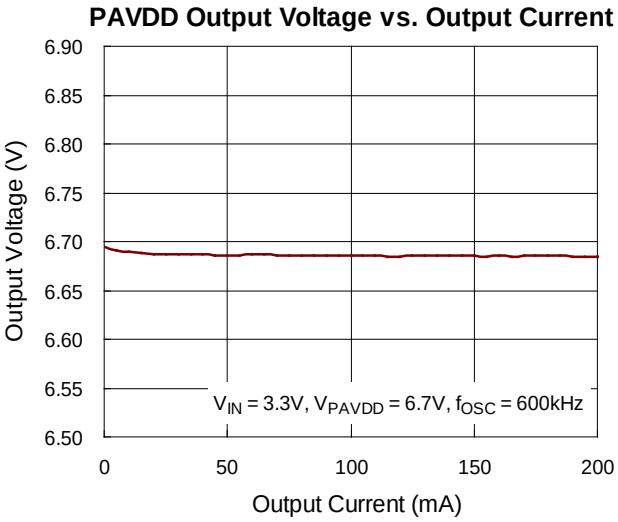
Note 6. Limits apply to the recommended operating temperature range of –40°C to 105°C, unless otherwise noted. Minimum and maximum limits are verified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN1 = 2.5V to 5.5V.

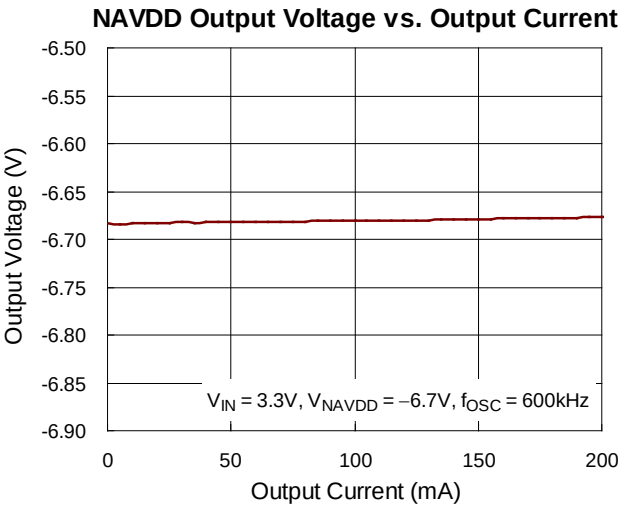
Note 7. In applications where high power dissipation or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX} = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application ($R\theta_{JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX} - (R\theta_{JA} \times P_{D-MAX})$.

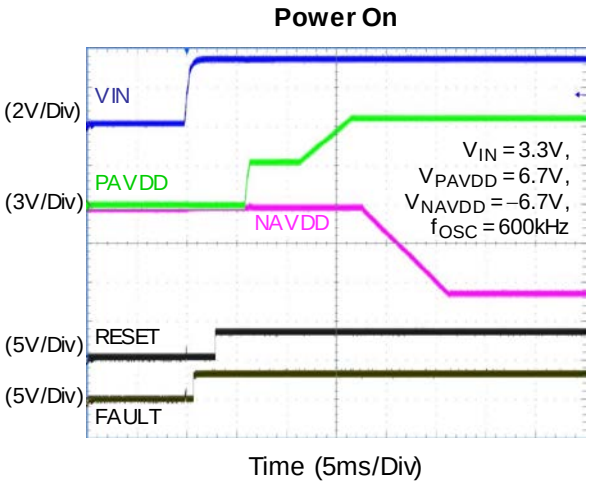
Typical Operating Characteristics

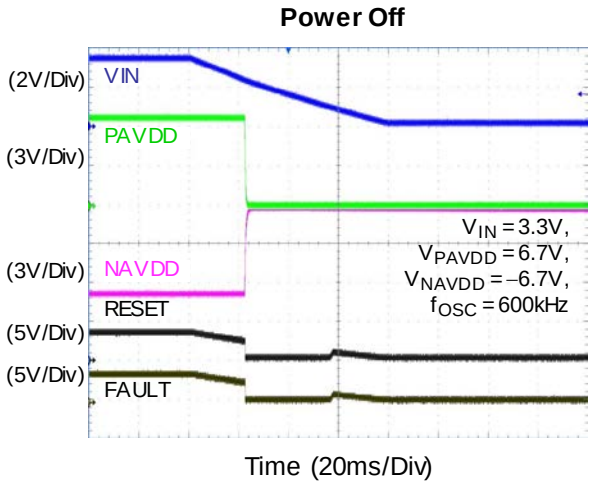












Applications Information

The RTQ6752-QT is an integrated solution for automotive TFT LCD panel, including PMIC and memory system. The RTQ6752 application mechanism is introduced in later sections. The RTQ6752-QT's slave address is 1101011.

PMIC - Power management system provides 2 sync-boost converters for PAVDD, one synchronous inverting converter for NAVDD. Power-on and Power-off sequences are control by EN input pin. Detail time sequence control is described in “Timing Diagram”. The I^2C interface can program each output channel as well as sequence control and voltage setting.

Switching Frequency Setting

The each channel switching frequency is set by the I^2C interface. It has a 2 bits register as 4 steps, the setting options are 600kHz, 800kHz, 1MHz and 2.2MHz. The switching frequency default value is 600kHz (0x00). Please refer to the register map for details.

Under Voltage Protection (UVP)

The RTQ6752-QT equip a fault conditions to shut down IC. Once the output voltage is below the 70% output voltage, the internal timer starts counting and the fault condition continued about 50ms, the IC will shut down. After the UVLO or EN started again, the fault protection would be released. The protection provided an option for user to enable or disable, the option can set by the register 14h[1].

Short Circuit Protection (SCP)

The RTQ6752 equip a fault conditions to shut down IC. In the power-on sequence, before the each channel power-up, the outputs voltage of each channel have to smaller than the SCP level of the channel. Or IC would wait the all of outputs voltage fall below the SCP level, then do the power-on sequence as the Figure 5 shown. The PAVDD_SCP_2 of PAVDD is 1.26V(typ) before PAVDD Soft-start, after soft-start finish the SCP will become 30% of voltage setting. the other channels are the 30% of voltage setting. The judgement point of the output voltage below SCP is from UVLO_R and plus 1ms.

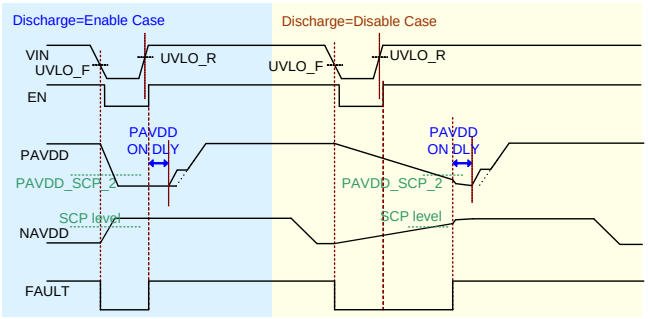


Figure 5. The Power-up Limitation of The Outputs Voltage must below the SCP level

In PAVDD pre-charge stage, the PAVDD SCP will be also checked after PAVDD power-on delay counting finish and plus 4ms. The SCP function also work during the soft-start period. If the PAVDD voltage is below the PAVDD_SCP_2 (1.26V_typ), IC will be protected at the delay counting finish and plus 4ms as the point “c” in the Figure 6 shown.

The pre-charging finish is going to judge the difference between PAVDD and VIN. When the difference is smaller than 0.2V(typ) that will be judged to pre-charge finished, and entry the soft-start stage. The SCP of the NAVDD channels is enabled after the soft-start of the channels is finished.

In another one case, If the PAVDD voltage is above PAVDD_SCP_2, but not satisfy the condition of pre-charging finish. Then IC will keep in pre-charge stage, until the condition is satisfied and then to entry soft-start stage as the Figure 7 shown.

Once the output voltage is below the 30% output voltage during operation stage, the high/low side MOSFET will stop switching immediately as the point “a” in the Figure 8 shown. The other channels will be stopped switching after 100μs and the FAULT pin go low as the point “b”.

After the UVLO or EN started again, the protection would be released. There is an option as 14h[0] for user to disable or enable this function. the first PAVDD_SCP_2 detection during new power on in Figure 5 cannot be disable by 14h[0].

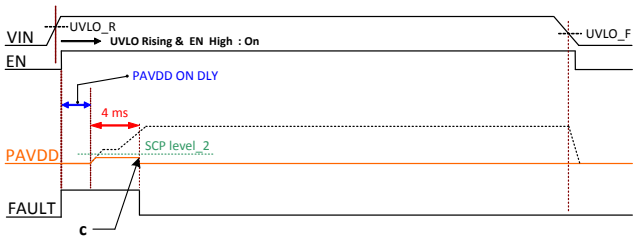


Figure 6. SCP Mechanism at PAVDD pre-charge when PAVDD with the Abnormal Heavy Load

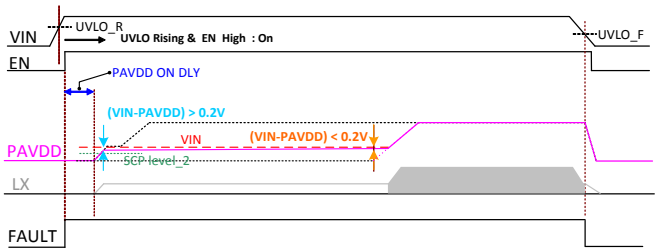


Figure 7. SCP Mechanism when PAVDD between SCP Level and Pre-charge Finish

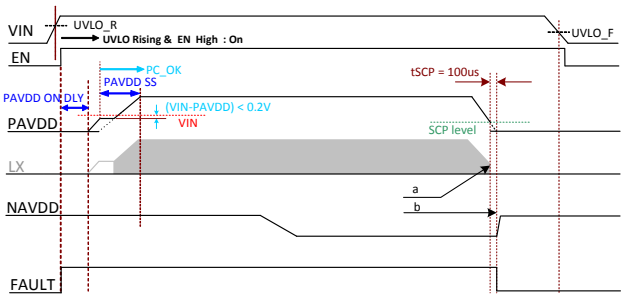


Figure 8. SCP Mechanism during Normal Operating

Over Temperature Protection (OTP)

The RTQ6752-QT equips an over temperature protection (OTP) to prevent the excessive power dissipation from overheating. The OTP will shutdown switching operation while junction temperature exceeds approximately 150°C. All of output channel starting work while junction temperature is cooled by approximately 20°C. Prevent the maximum junction temperature over around 150°C and maintain continuous operation. The protection provided an option for user to enable or disable, the option can set by the register 14h[2].

PAVDD Synchronous Boost Converter

The PAVDD synchronous Boost converter is high efficiency PWM architecture with programmable switching frequency. It performs fast transient responses to meet the requirement of source driver supplies for TFT-LCD display. The high operation frequency can prevent that switching frequency influence AM band range. The output voltage is controlled by a 6 bits register with 47 steps. The error amplifier varies the COMP voltage by sensing the PAVDD pin to regulate the output voltage.

PAVDD Slew Rate Setting

The PAVDD LX falling slew rate can be controlled by I^2C interface, to optimize the efficiency and EMI performance. The adjustable options are slowest, slow, normal and fast. The default value is normal option. Please refer to the register map for details.

PAVDD Output Voltage Setting

The PAVDD output voltage is set by I^2C interface. User can write the 00h[5:0] register to set PAVDD output voltage. It has 6 bits for output voltage adjustable, the setting range is from 5V to 7.3V, and each voltage step is about 50mV. The default voltage of PAVDD is 6V (0x14). Please refer the register map for detail on how to adjust the output voltage.

In addition, the PAVDD min on time typical is about 150ns, PAVDD output voltage setting shall not be smaller than VIN + 2.2V. To make sure the duty cycle can be normal operation. The duty cycle can be approximately as below formula.

- Boost Converter duty cycle :

$$D = \frac{(V_{OUT} - V_{IN} \times \eta)}{V_{OUT}}$$

PAVDD Soft-start time Setting

The PAVDD soft-start time could be adjusted by the register 08h[2:0]. There are 3 bits and 8 steps. The soft-start time setting range is from 5ms to 40ms, and each step is about 5ms. The soft-start time default value is 10ms (0x01). The soft- start mechanism is following the reference voltage to soft-start, the soft-start starting point is from the slope of the soft-start down to the point of crosses 0V. The soft-start finish point is PAVDD output voltage ready. Please refer to Figure 3 and register map for details.

PAVDD Power-on Delay Time Setting

The PAVDD power-on delay time is adjustable by I^2C interface. There are 16 steps within 4 bits register of 07h. The delay time setting range is from 0ms to 75ms, and each steps time is about 5ms. The delay time default value is 5ms (0x01). The delay time is from the MTP load data finish to PAVDD output voltage starting rising. Please refer the Figure 3, and register map for detail.

PAVDD Current Limit

The RTQ6752-QT can limit the peak current to achieve over-current protection. The IC senses the inductor current of on period that is flowing into LX pin. The minimum value of the current limit is 1.5A. The internal N-MOSFET will be turned off if the peak inductor current achieve current limitation level, so that the output current at current limit boundary is denoted as $I_{OUT(CL)}$ and can be calculated as shown in the following equation :

$$I_{OUT(CL)} = \eta \times \frac{V_{IN}}{V_{OUT}} \times \left(I_{CL} - \frac{1}{2} \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT}} \times \frac{T_S}{L} \right)$$

where η is the efficiency of the PAVDD sync-boost converter, I_{CL} is the value of the current limit and T_S is the switching period.

PAVDD Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisted of R1 and C21. Choose R1 to set high frequency integrator gain for fast transient response and C21 to set the integrator zero to maintain stability. The recommended values are 75kΩ and 470pF for most applications.

Sync-Boost Inductor Selection

The inductance depends on the maximum input current. The inductor ripple current range is 20% to 40% of maximum input current that is a general rule. If 40% is selected as an example, the inductor ripple current can be calculated as following equation :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$I_{RIPPLE} = 0.4 \times I_{IN(MAX)}$$

Where η is the efficiency of the synchronous boost converter, $I_{IN(MAX)}$ is the maximum input current and I_{RIPPLE} is the inductor ripple current. Beside, the input peak current can be calculated by maximum input current plus half of inductor ripple current shown as following equation :

$$I_{PEAK} = 1.2 \times I_{IN(MAX)}$$

Note that the saturated current of inductor must be greater than I_{PEAK}. The inductance can be eventually determined as following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

Where f_{OSC} is the PAVDD switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Sync-Boost Output Capacitor Selection

Output ripple voltage is an important index for estimating the performance. This portion consists of two parts, one is the product of $\left(I_{IN} + \frac{1}{2}\Delta I_L - I_{OUT}\right)$ and ESR of output capacitor, another part is formed by charging and discharging process of output capacitor. Refer to Figure 9, evaluate ΔV_{OUT1} by ideal energy equalization. According to the definition of Q, the Q value can be calculated as following equation :

$$Q = \frac{1}{2} \times \left[\left(I_{IN} + \frac{1}{2}\Delta I_L - I_{OUT} \right) + \left(I_{IN} - \frac{1}{2}\Delta I_L - I_{OUT} \right) \right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{OSC}} = C_{OUT} \times \Delta V_{OUT1}$$

Where T_S is the inverse of switching frequency and the ΔI_L is the inductor ripple current. Move C_{OUT} to left side to estimate the value of ΔV_{OUT1} as following equation :

$$\Delta V_{OUT1} = \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

Then take the ESR into consideration, the ESR voltage can be determined as the following equation :

$$\Delta V_{ESR} = \left(\frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D \times T_{OSC}}{2L} \right) \times R_{ESR}$$

Finally, the output ripple voltage ΔV_{OUT} is combined

from theΔV_{OUT1} and ΔV_{ESR} as following equation :

$\Delta V_{OUT} = \Delta V_{OUT1} + \Delta V_{ESR}$

In the general application, the PAVDD output capacitor is recommended that to use three 10μF/X7R/1206 capacitors and the effective capacitance value of output capacitance needs 13μF at least. In addition, the effective capacitance value of output capacitance needs 6uF at least.

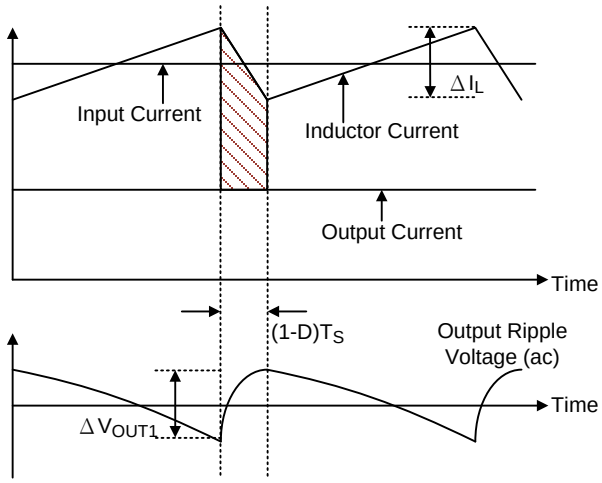


Figure 9. The Output Ripple Voltage without the Contribution of ESR

NAVDD Synchronous Buck-Boost Converter

The NAVDD synchronous Buck-Boost converter is high efficiency PWM architecture with programmable switching frequency. It performs fast transient responses to meet the requirement of source driver supplies for TFT-LCD display. The high operation frequency can prevent that switching frequency influence AM band range. The output voltage is controlled by a 6 bits register with 47 steps.

For VIN > 4V application, the an-synchronous topology should be applied as the Figure 2 shown. To get a better performance.

NAVDD Power-On Delay Time Setting

The NAVDD power-on delay time is adjustable by I^2C interface. There are 16 steps within 4 bits register of 0Dh[3:0]. The power-on delay time setting range is from 0ms to 75ms, and each steps time is about 5ms. The delay time default value is 5ms (0x01). The delay time is from the MTP load data finish to NAVDD output voltage starting falling. Please refer the Figure 3, and register map for detail.

NAVDD Soft-Start Time Setting

The NAVDD has an internal soft-start mechanism to reduce the input inrush current. The NAVDD soft-start time can be adjusted by the register 0Eh[2:0]. There are 3 bits and 8 steps for setting. The soft-start time setting range is from 5ms to 40ms, and each step is about 5ms. The soft-start time default value is 10ms (0x01). The soft-start time starts from the NAVDD delay time counting finish. The stop point of soft-start time is NAVDD output voltage ready. Please refer to Figure 3 and register map for details.

NAVDD Output Voltage Setting

The NAVDD output voltage is adjusted by I^2C interface. User can write data into the register 01h[5:0]. There are 6 bits for output voltage adjustable, the setting range is from -5V to -7.3V, and each voltage step is about -50mV. The default value is -6V (0x14). Please refer the register map for detail on how to adjust the output voltage.

NAVDD Inductor Selection

The first step in design procedure is to verify whether the maximum possible output current of the buck-boost converter support the specific application requirements. To simplify the calculation, the fastest approach is to estimate converter efficiency by taking the efficiency numbers from provided efficiency curves or to use a worst case assumption for the expected efficiency, ex 75%. The calculation must be performed for the minimum assumed input voltage where the peak switch current is the highest. The inductor and internal switch have to be able to handle this current.

- Converter duty cycle :

$$D = \frac{|V_{OUT}|}{V_{IN} \times \eta \times |V_{OUT}|}$$

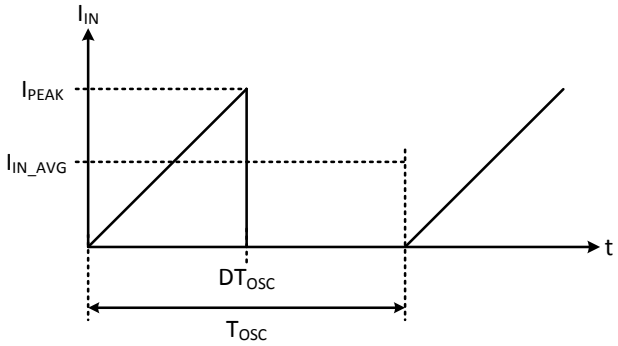
- Maximum output current :

$$I_{OUT} = \left(I_{PEAK} - \frac{V_{IN} \times D}{2 \times f_{OSC} \times L} \right) \times (1 - D)$$

- Inductor peak current :

$$I_{PEAK} = \frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D}{2 \times f_{OSC} \times L}$$

As for inductance, we are going to derive the transition point, there the converter toggle from CCM to DCM. We



need to define the point at which the inductor current ripple touches zero, and as the power switch SW is immediately reactivated, the current ramps up again. Figure 10 portrays the input current activity of the buck-boost converter.

Figure 10. The Buck-boost Input Signature in BCM

The inductance can eventually be determined according to the following equation :

$$L_{critical} = \frac{|V_{OUT}| \times \eta}{2 \times f_{OSC} \times I_{OUT}} + \left(\frac{V_{IN}}{V_{IN} + |V_{OUT}|} \right)^2$$

NAVDD Output Capacitor Selection

For the best output voltage filtering, low ESR ceramic capacitors are recommended. Three 10μF/X7R/1206 capacitors in parallel and the effective capacitance needs 13μF at least that are afford most applications. Additional capacitors can be added to improve output voltage ripple.

NAVDD Current Limitation

The RTQ6752-QT can limit the peak current to achieve over current protection. The IC senses the inductor current during an on period. The internal P-MOSFET will be turned off if the peak inductor current reaches 1.5A (min.)

RESET Voltage Detector

The voltage detector monitors the VIN voltage to generate a RESET signal from RESET pin while V_{IN} is lower than the detecting level and not latched. Both detecting level and power-on delay time could be set by I^2C interface. The detecting level could be adjusted by the register (0x12 [6:5]), it provided 4 options such as UVLO falling, 2.1V, 2.4V and 2.7V. The delay time could be set by register (0x10[3:0]), the setting range is from 0ms to 75ms, the each step is about 5ms. The delay time start from that the two conditions are achieved, one is VIN over UVLO threshold, and another one is the EN over VIH threshold, the stop point is that RESET signal goes to high.

In addition, the voltage detector also provided an option, user can chose which RESET goes low following power-off delay time. The options can be set by the register 12h[7].

Discharge Function

The PAVDD and NAVDD outputs voltage is integrated a discharge function. When EN go low or UVLO_F, the each output voltage would be discharged from 100% to 30% rapidly within 2ms at power-off as the Figure 3 shown. preventing phenomena such as residual image on the display at power-off. If user want to make the outputs voltage were discharged to GND level, user should add discharging resistances on the outputs. The discharge function also provided an option for user to enable or disable, the option can set by the register 12h[4:3] individually for each channel.

If the discharge function is enabled, except discharge is worked at power-off, it also be discharge at power-on. The power-on discharge start to work from UVLO and plus 1ms, until the delay time of the channel be counting finish. If the discharge function is disabled, except the power-off without discharge function, the power-on also does not have. However, the period still has discharge function from UVLO_R to MTP_LOAD_OK. The mechanism is shown in Figure 11. Beside the discharging function should be turned off at same time if the channels are unused.

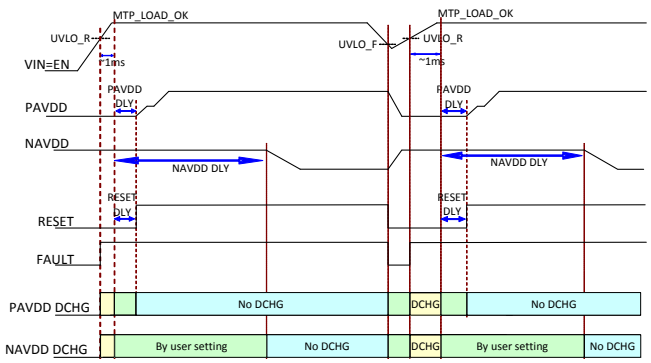


Figure 11. Discharge Function Enable Operation Mechanism

Slew Rate Control

The RTQ6752-QT provided options for switching node slew rate adjustment with I^{2}C interface. The slew rate can be adjusted by the register 13h[7:0]. The register 13h[7:6] is for PAVDD LX falling slew rate control and there are 4 options for setting such as fast, normal, slow and slowest. The register 13h[5:4] is for NAVDD LXN rising slew rate control, the options are same as PAVDD.

Power-Off Delay Time Setting

The PAVDD (18h[2:0]), NAVDD (19h[2:0]), power-off delay time are adjustable by I^{2}C interface. The each output channels 8 steps within 3 bits register. The delay time setting range is from 0ms to 14ms, and each steps time is about 2ms. The PAVDD and NAVDD power-off delay time default value is 14ms. The power-off delay time is from the RESET goes low to the delay counting finish. Please refer the Figure 3, and register map for detail.

Frequency Spread

The RTQ6752-QT is integrated a frequency spread of switching frequency function, it can reduce the noise level of the switching frequency point, it is good for EMI performance. There are 3 options for adjustment such as disabled, 3% and 6%. User can write data into the register 14h[4:3] to control the frequency spread.

FAULT Analysis Function

The RTQ6752-QT has provided a fault recording register that can help quickly user to know which output channel is UVP fault. If one of the output channels triggered UVP, the fault record will be saved into register 1Dh[3:0]. Then user can use I^{2}C interface to read the data of 1Dh register during the UVP is triggered. The 1Dh register will show which channel is fault.

In addition, there is an option (1Ch[3]) for clearing the record of the fault register. Users can choice that the fault record be cleared by EN going low, or VIN fall below the VIN1 UVLO_F that also can be cleared fault record.

Control Register (FFH)

The RTQ6752-QT provides a register for user choosing that write/read data into MTP or register. User can set the MSB of the register FFH goes to high, it means the data is written into MTP. But writing data into register don't need to set the register FFH. In addition, reading data from MTP need to set the LSB of register FFH to high. On the contrary, reading data from register need to set LSB to low. Please refer the "I^{2}C Write/Read Timing Sequence" for detail.

I^{2}C Communication

RTQ6752-QT reads default data from internal memory (MTP) at startup, and run. The customer can change the data in the internal memory via external I^{2}C communication, but I^{2}C communication is not possible until VIN over UVLO_R and EN = H are satisfied. In other words, I2C communication is not possible with VIN over UVLO_R and EN = L. When VIN over UVLO_R, EN = H, all of output power ready, and T1 are satisfied, settings such as output voltage and delay time can be changed via I^{2}C.

Auto Refresh Functions

The RTQ6752 has integrated registers code auto recovery function if the registers code is changed abnormally. The issue could be detected with Auto Refresh Function that has provided an option to enable and disable by setting 17h[0]. The refreshing time also can be adjusted with 17h[2:1]. In addition, the FAULT pin also can be choosing pull low or not, to adjusted by 17h[3]. Please refer the register map for detail.

The Auto Refresh Function behavior is going to check register code with 0.5s(default). If the code is wrong, the memory will re-load the code and FAULT pin go low. Until the next time the register code check is the same

as memory data. The FAULT pin go back to high as the Figure 12 shown.

However, if the second time check register code that is still wrong. The FAULT pin will go high a while then go low again. The high period is about 200μs.

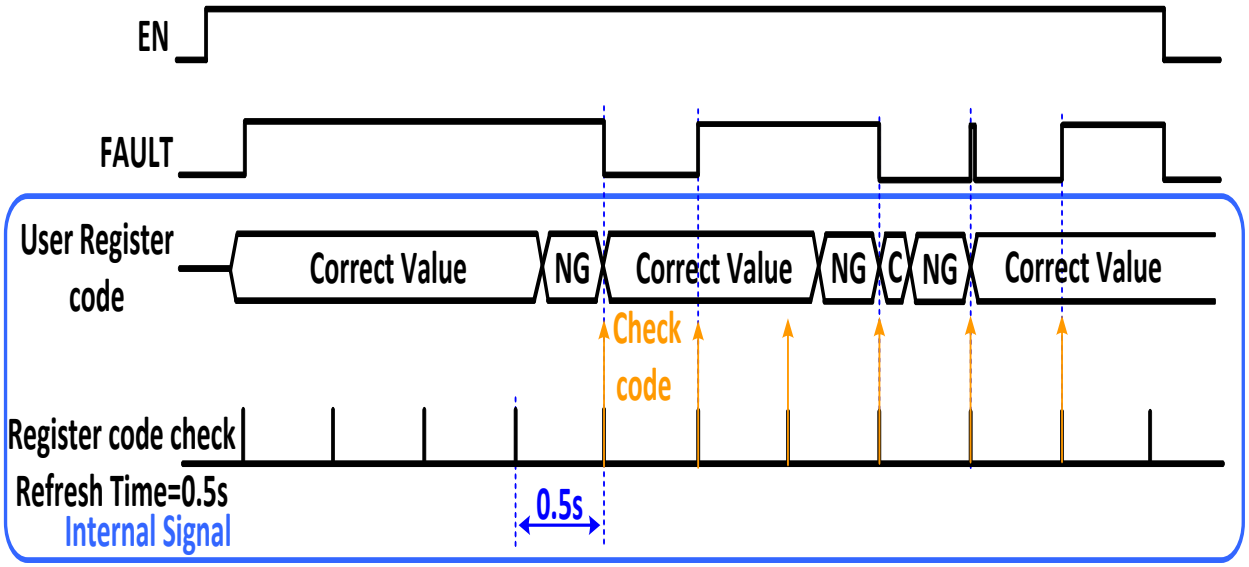


Figure 12. Auto Refresh Function Behavior

Table 1. FAULT Behavior Versus Protections

Block	Triggering Protection	FAULT Pin Behavior	Recovery
PAVDD	OVP	High(Normal state)	--
	UVP	Low	1. VIN re-power up. 2. EN toggle again.
	SCP	Low (Fault pin toggle one time)	1. VIN re-power up. 2. EN toggle again.
	OTP	Low	IC Temperature < OTP - Hys, Hys = 20°C(typ)
NAVDD	OVP	High(Normal state)	--
	UVP	Low	1. VIN re-power up. 2. EN toggle again.
	SCP	Low	1. VIN re-power up. 2. EN toggle again.
	OTP	Low	IC Temperature < OTP - Hys, Hys=20°C(typ)

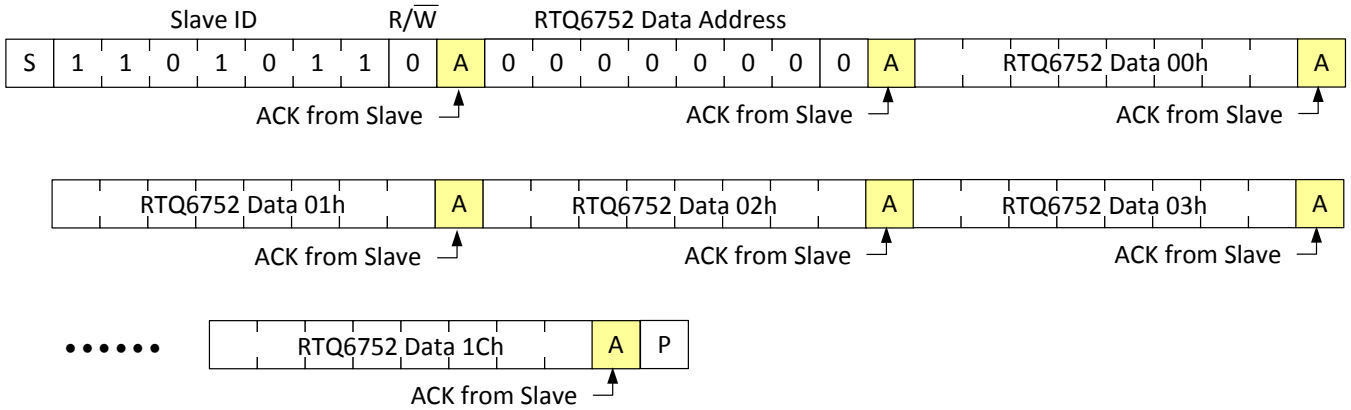
I²C Command

PMIC Slave Address

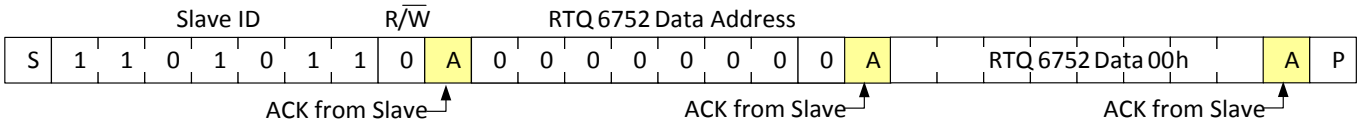
7	6	5	4	3	2	1	0 = R/W	
1	1	0	1	0	1	1	0	D6H
1	1	0	1	0	1	1	1	D7H

PMIC I2C Write Timing Sequence (To DAC Register)

Write Multiple Data (00h~1Ch)

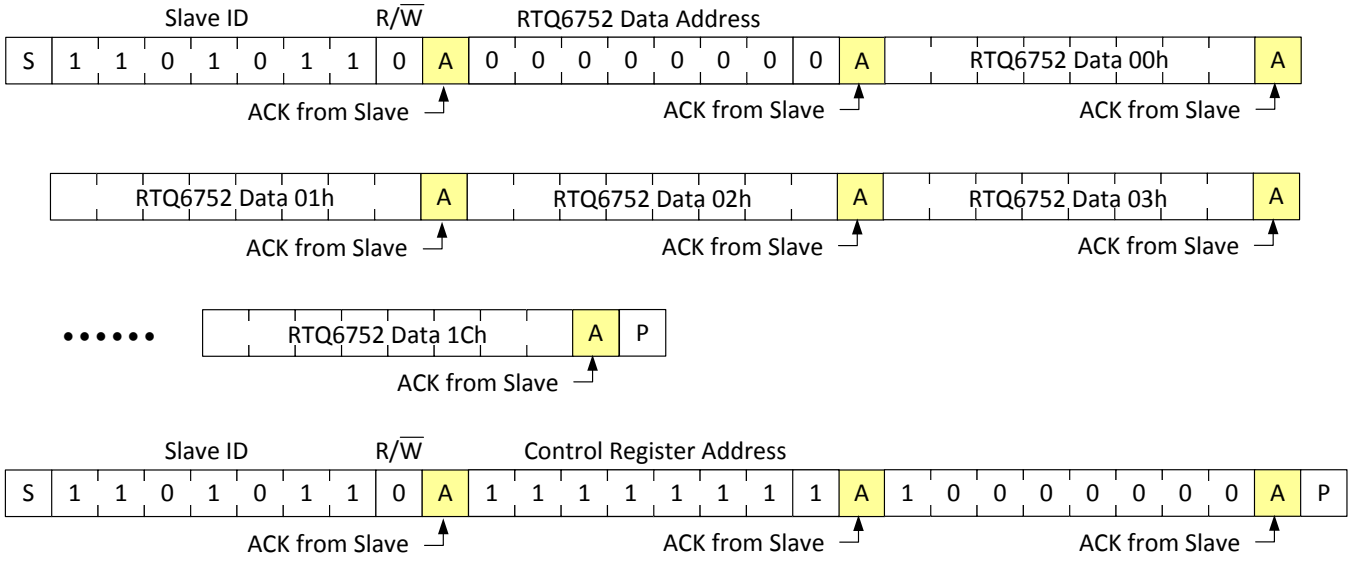


Write Single Data(00h)

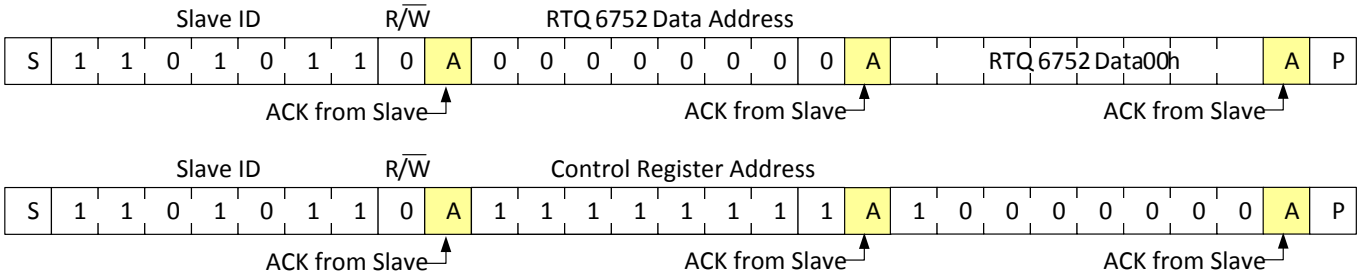


PMIC I2C Write Timing Sequence (To MTP)

Write Multiple Data (00h~1Ch)

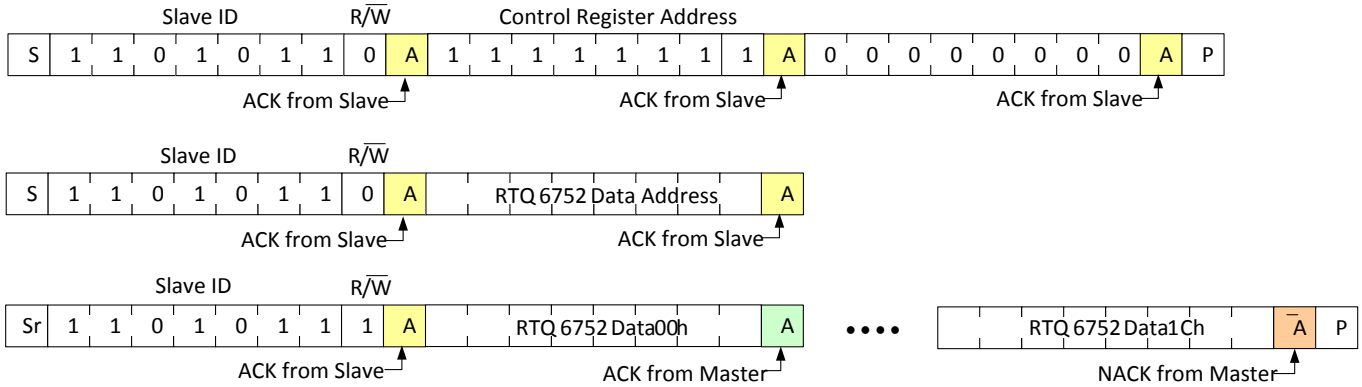


Write Single Data (00h)

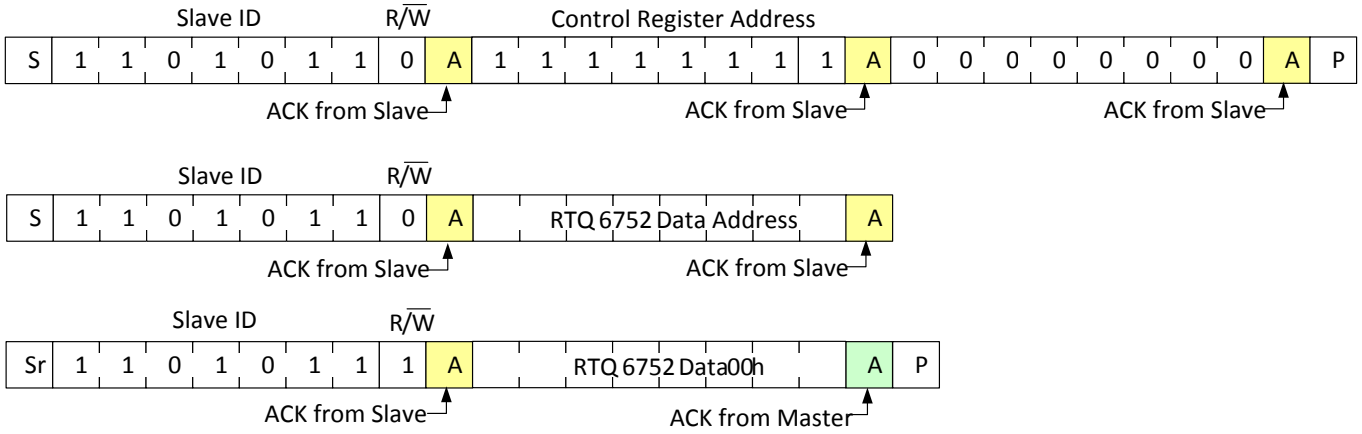


PMIC I2C Read Timing Sequence (From DAC Register)

Read Multiple Data(00h~ 1Ch)

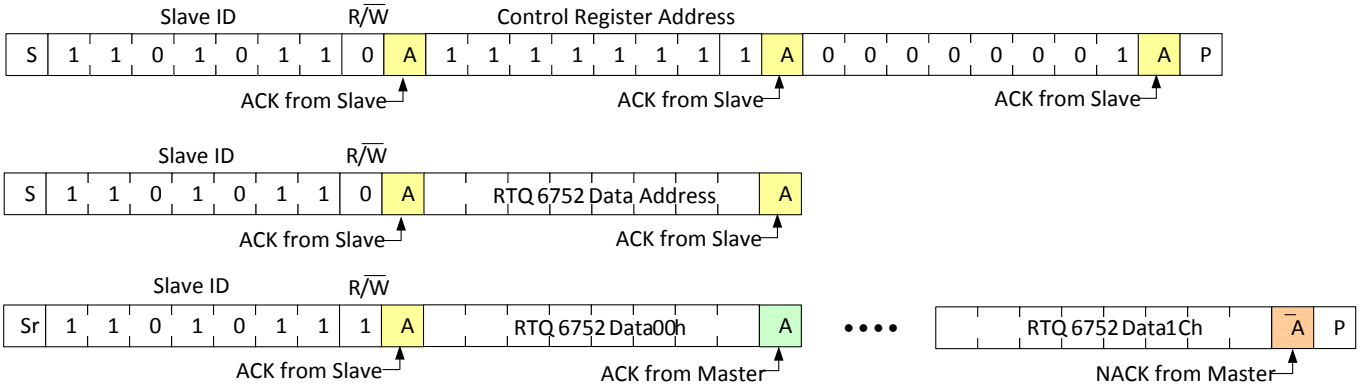


Read Single Data (00h)

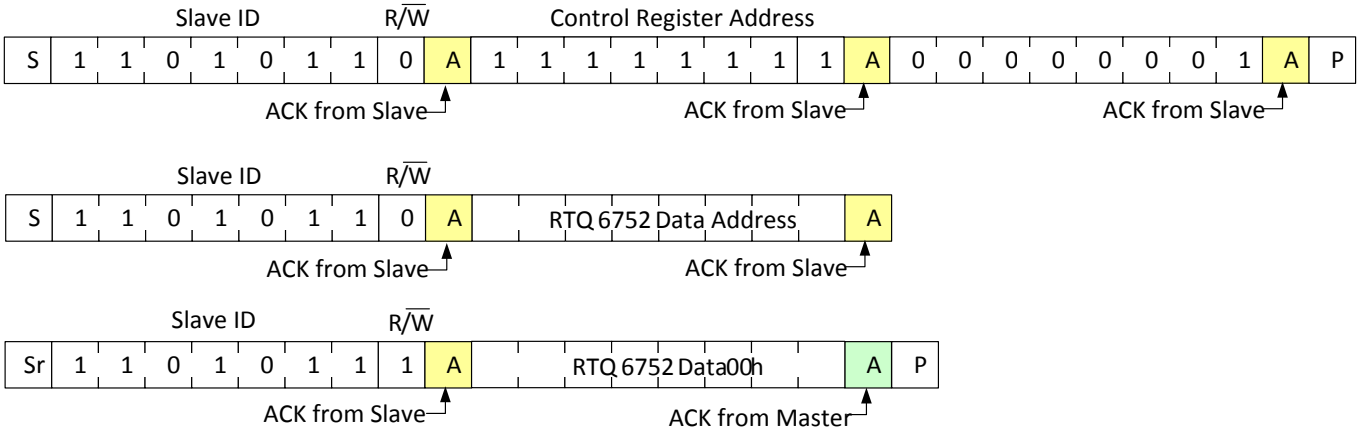


PMIC I2C Read Timing Sequence (From MTP)

Read Multiple Data(00h~1Ch)

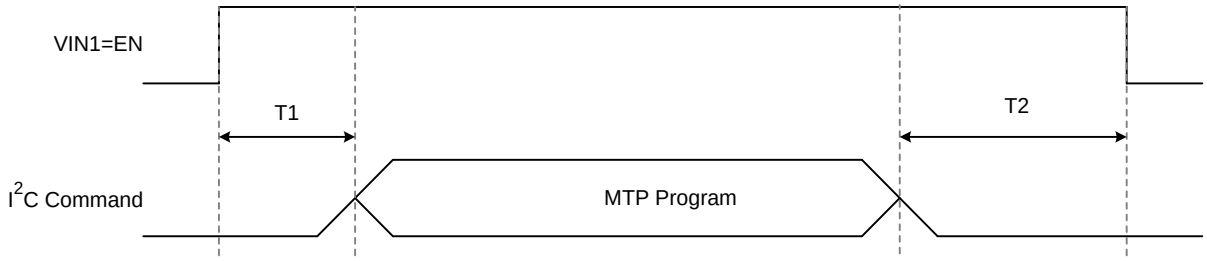


Read Single Data(00h)



MTP Program Sequence for Single Chip

MTP program timing sequence



Write Timing :

T1 = 50ms, T2 = 500ms

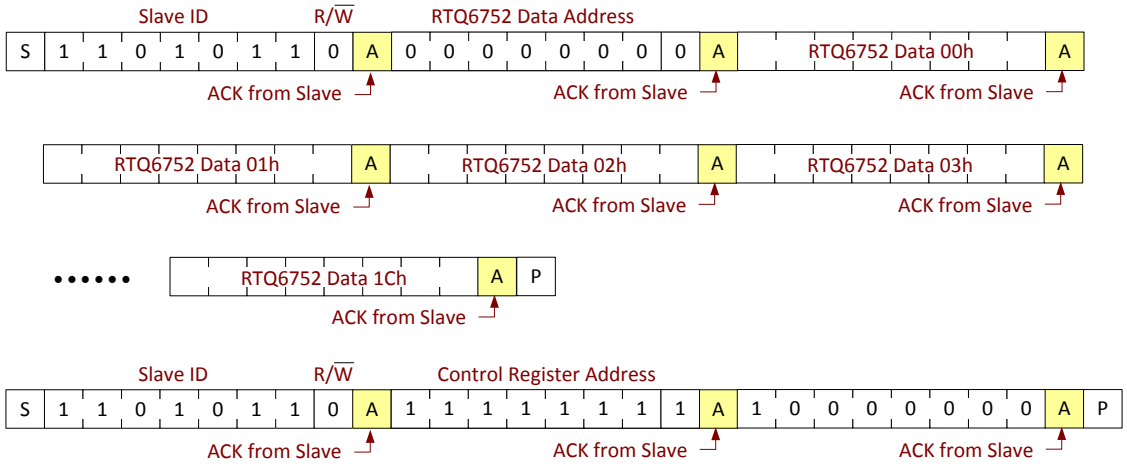
Read Timing:

T1=50ms, T2=10ms

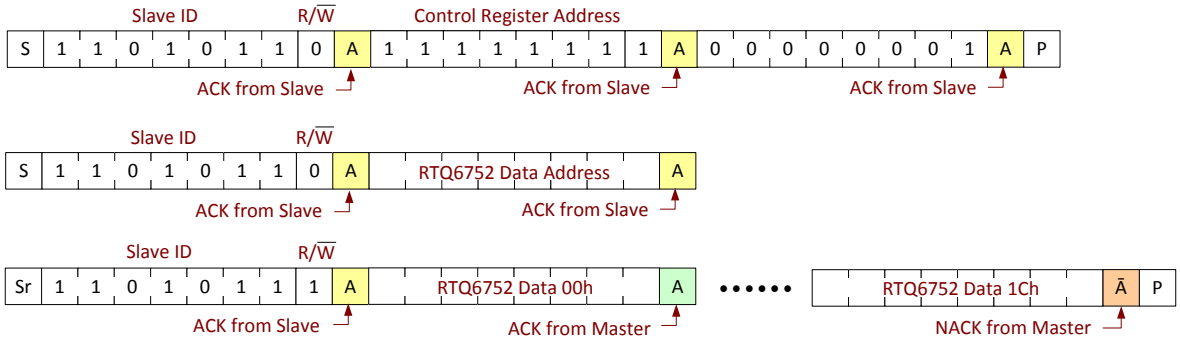
f_{SCL}=400kHz

I²C Protocol for MTP Program

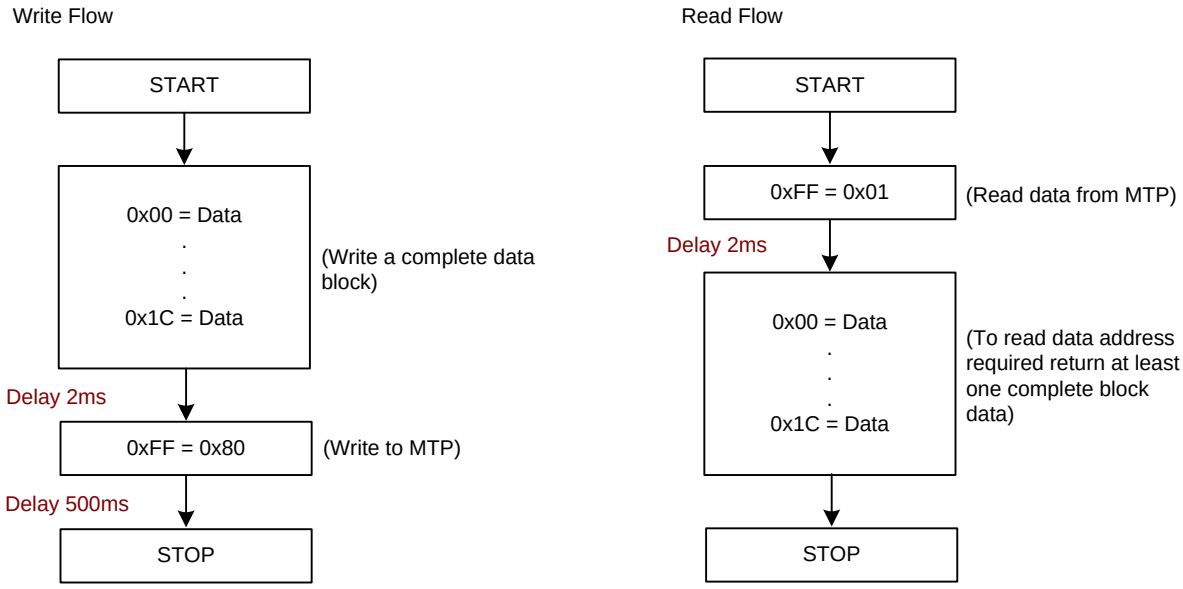
I²C Write Timing Sequence



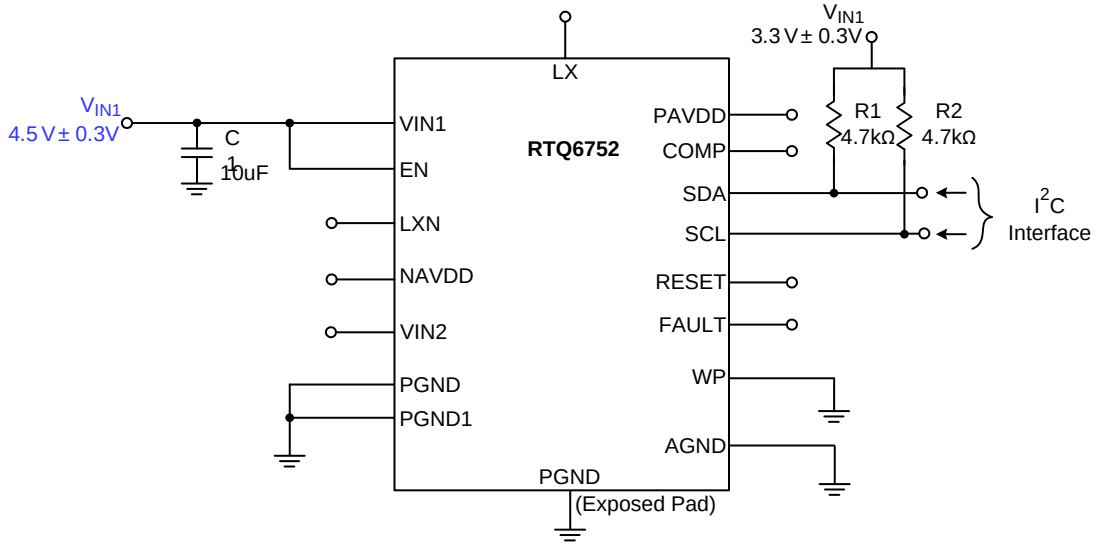
I²C Read Timing Sequence



I²C Read / Write Flow Chat

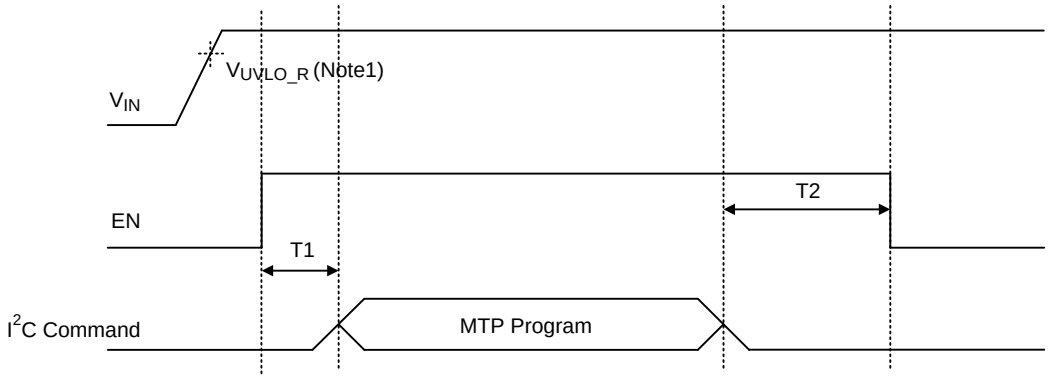


MTP Program Application Circuit for Single Chip



MTP Program Sequence on Board

MTP program timing sequence



I2C Writing Condition : (Note.2)

1. VIN over UVLO_R
2. EN = H
3. All of output power ready

Write Timing :

00h~1Ch：T1 = 50ms, T2 = 500ms

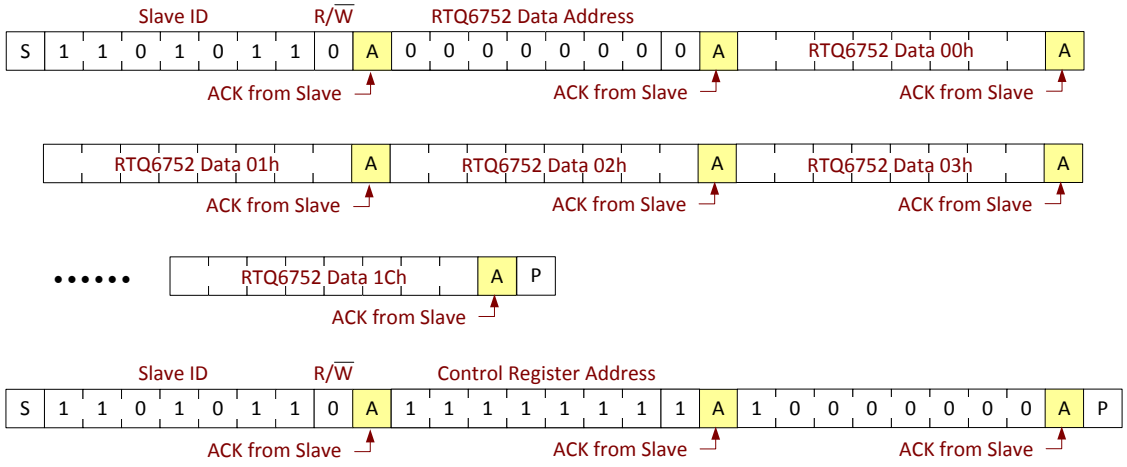
Read Timing :

T1 = 50ms, T2 = 10ms

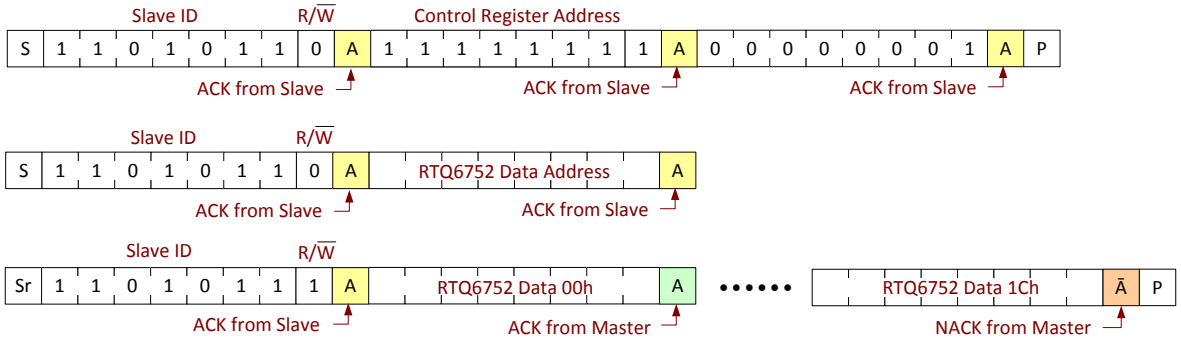
Note.1 : UVLO_R = UVLO_F + UVLO_H

I²C Protocol for MTP Program

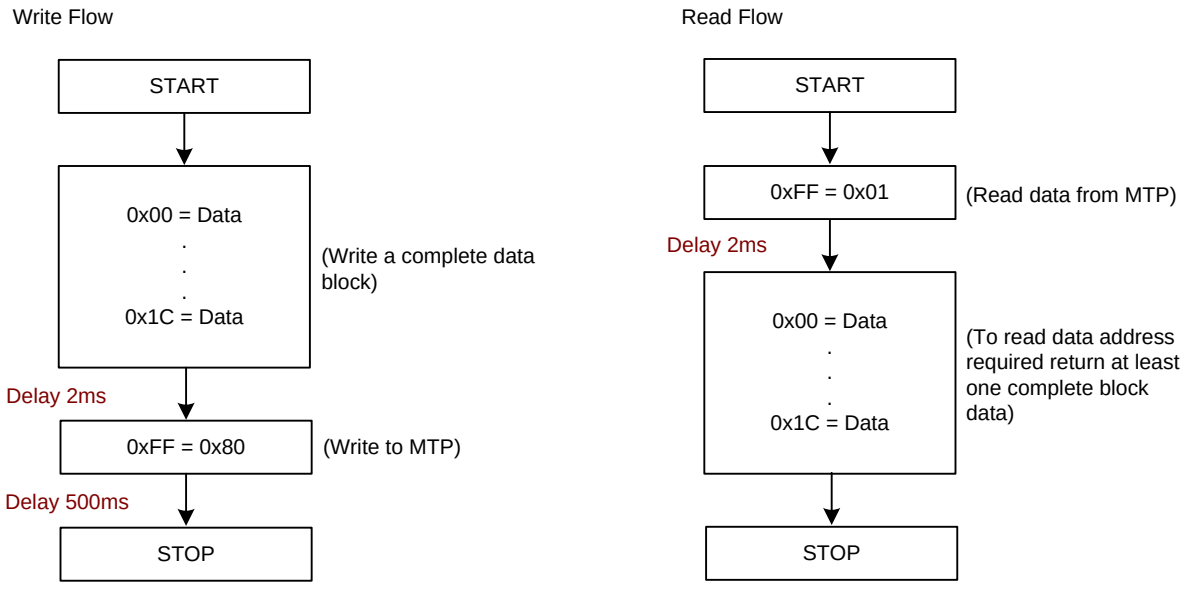
I²C Write Timing Sequence



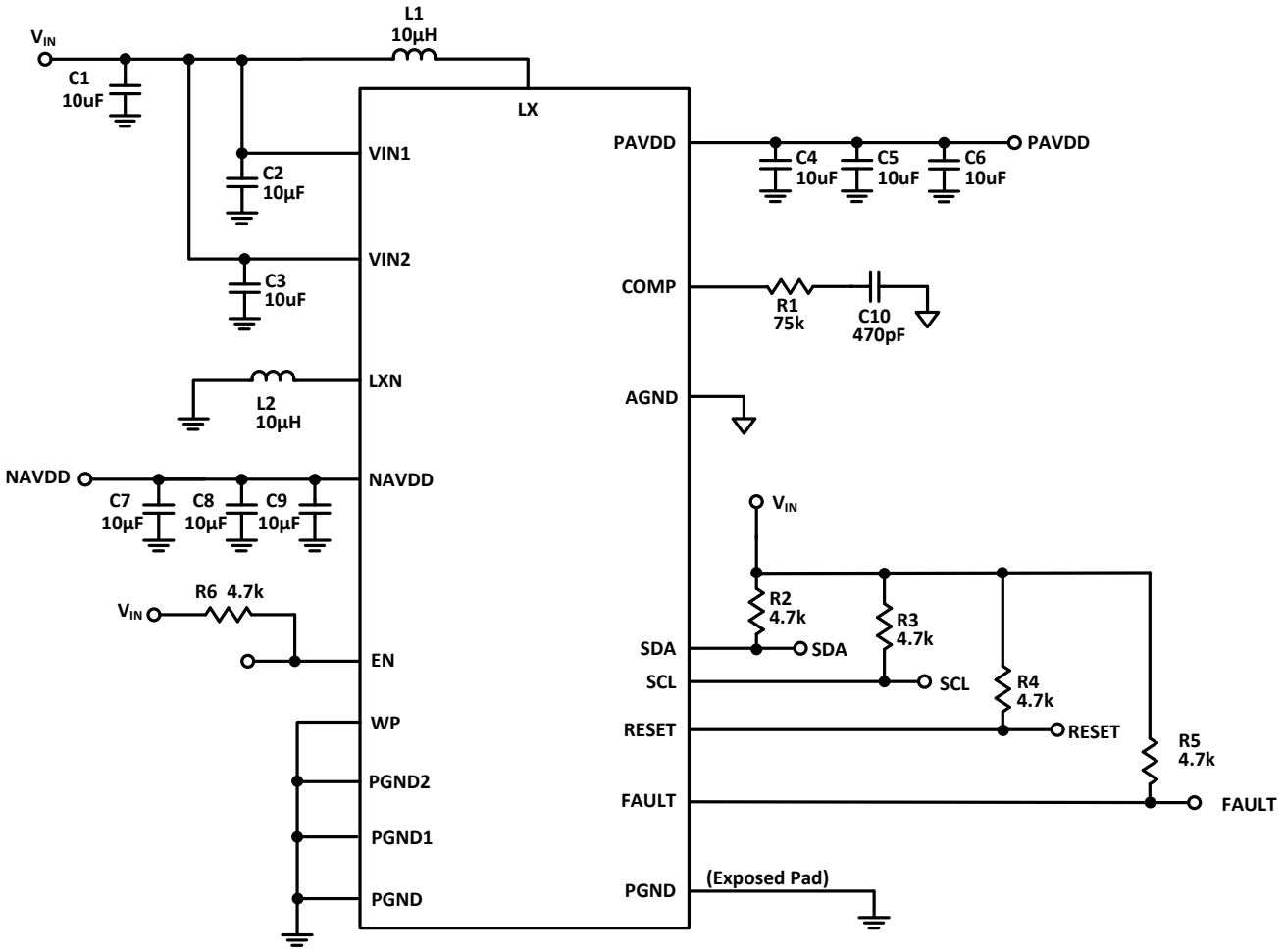
I²C Read Timing Sequence



I²C Read / Write Flow Chat



MTP Program Application Circuit on Board



Register Map

Items		Register Address	Resolution	Range	Default value	Default Code	Step	Bit
PMIC	PAVDD[5:0]	00h	0.05V	5.0~7.3V	6V	14h	47 Step	6 Bit
	NAVDD[5:0]	01h	0.05V	-5.0~-7.3V	-6V	14h	47 Step	6 Bit
	Reserved[5:0]	02h	--	--	--	6h	--	6 Bit
	Reserved [5:0]	03h	--	--	--	10h	--	6 Bit
	Reserved [7:0]	04h	--	--	--	64h	--	8 Bit
	Reserved [1:0]	05h	--	--	--	0h	--	2 Bit
	SW Freq.[1:0]	06h	--	600k/800k/1M/2.2M	600kHz	0h	4 Step	2 Bit
Power On Sequence	PAVDD ON Delay[3:0]	07h	5ms	0ms ~ 75ms	5ms	1h	16 Step	4 Bit
	PAVDD Soft Start[2:0]	08h	5ms	5ms ~ 40ms	10ms	1h	8 Step	3 Bit
	Reserved [3:0]	09h	--	--	--	5h	--	4 Bit
	Reserved [2:0]	0Ah	--	--	--	2h	--	3 Bit
	Reserved [3:0]	0Bh	--	--	--	5h	--	4 Bit
	Reserved [1:0]	0Ch	--	--	--	1h	--	2 Bit
	NAVDD ON Delay[3:0]	0Dh	5ms	0ms ~ 75ms	5ms	1h	16 Step	4 Bit
	NAVDD Soft Start[2:0]	0Eh	5ms	5ms ~ 40ms	10ms	1h	8 Step	3 Bit
	Reserved[3:0]	0Fh	--	--	--	5h	--	4 Bit
	RESET ON Delay[3:0]	10h	5ms	0ms ~ 75ms	5ms	1h	16 Step	4 Bit
	Power OFF Delay[3:0]	11h	3ms	0ms ~ 45ms	21ms	7h	16 Step	4 Bit
Option1	RESET Sync option[7]	12h	--	Power Off Delay/ Reserved	Power Off Delay	7h	2 Step	1 Bit
	Vin Detection[6:5]		--	UVLO Falling /2.1V/2.4V/2.7V	UVLO Falling		4 Step	2 Bit
	PAVDD D/C function[4]		--	On (0) / Off (1)	On		2 Step	1 Bit
	NAVDD D/C function[3]		--	On (0) / Off (1)	On		2 Step	1 Bit
	Reserved [2]		--	--	--		--	1 Bit
	Reserved [1]		--	--	--		--	1 Bit
	Reserved [0]		--	--	--		--	1 Bit
Option2	PAVDD Slew rate[7:6]	13h	--	Fast/normal/Slow/Slowest	Normal	55h	4 Step	2 Bit
	NAVDD Slew rate[5:4]		--	Fast/normal/Slow/Slowest	Normal		4 Step	2 Bit
	Reserved [3:2]		--	--	--		--	2 Bit
	Reserved [1:0]		--	--	--		--	2 Bit

Items		Register Address	Resolution	Range	Default value	Default Code	Step	Bit
Option3	Reserved [5]	14h	--	--	--	0h	--	1 Bit
	Freq. Spread Option(EMI)[4:3]		--	Off/ +3% / +6%	Off		3 Step	2 Bit
	OTP On / Off[2]		--	On (0) / Off (1)	On		2 Step	1 Bit
	UVP On / Off[1]		--	On (0) / Off (1)	On		2 Step	1 Bit
	SCP On / Off[0]		--	On (0) / Off (1)	On		2 Step	1 Bit
Channel ON/OFF Option	RESET EN[5]	16h	--	On (1) / Off (0)	On	29h	2 Step	1 Bit
	Reserved [4]		--	--	--		--	1 Bit
	NAVDD EN[3]		--	On (1) / Off (0)	On		2 Step	1 Bit
	Reserved [2]		--	--	--		--	1 Bit
	Reserved [1]		--	--	--		--	1 Bit
	PAVDD EN[0]		--	On (1) / Off (0)	On		2 Step	1 Bit
Auto Refresh Option	FAULT Behavior[3]	17h	--	Not Pull Low(0)/Pull Low(1)	Not Pull Low	2h	2 Step	1 Bit
	Refreshing Time[2:1]		--	0.25s/0.5s/1s/2s	0.5s		4 Step	2 Bit
	AR EN[0]		--	Off (0) / On (1)	Off		2 Step	1 Bit
Power Off Sequence	PAVDD OFF Delay[2:0]	18h	2ms	0ms ~ 14ms	14ms	7h	8 Step	3 Bit
	NAVDD OFF Delay[2:0]	19h	2ms	0ms ~ 14ms	14ms	7h	8 Step	3 Bit
	Reserved [2:0]	1Ah	--	--	--	0h	--	3 Bit
	Reserved [2:0]	1Bh	--	--	--	0h	--	3 Bit
	FAULT Analysis Clear Option[3]	1Ch	--	Not Clear by EN go low(0) / Clear by EN go low(1)	Not Clear	0h	2 Step	1 Bit
	Reserved [2:0]		--	--	--		--	3 Bit
Fault Analysis	PAVDD Fault[3]	1Dh	--	No Fault (0) / Fault Happen (1)	No Fault	--	2 Step	1 Bit
	Reserved [2]		--	--	--		--	1 Bit
	Reserved [1]		--	--	--		--	1 Bit
	NAVDD Fault[0]		--	No Fault (0) / Fault Happen (1)	No Fault		2 Step	1 Bit

Register Table

	PMIC						
	PAVDD	NAVDD	Reserved	Reserved	Reserved	Reserved	Switching Frequency
Data Address	00h	01h	02h	03h	04h	05h	06h
Bits	[5:0]	[5:0]	[5:0]	[5:0]	[7:0]	[1:0]	[1:0]
Min	5V	-7.3V	--	--	--	--	600kHz
Max	7.3V	-5V	--	--	--	--	2.2MHz
Default	14h	14h	06h	10h	61h	00h	00h
Resolution	50mV	50mV	--	--	--	--	-
0H	5.00V	-5.00V	--	--	--	--	600kHz
1H	5.05V	-5.05V	--	--	--	--	800kHz
2H	5.10V	-5.10V	--	--	--	--	1MHz
3H	5.15V	-5.15V	--	--	--	--	2.2MHz
4H	5.20V	-5.20V	--	--	--		
5H	5.25V	-5.25V	--	--	--		
6H	5.30V	-5.30V	--	--	--		
7H	5.35V	-5.35V	--	--	--		
8H	5.40V	-5.40V	--	--	--		
9H	5.45V	-5.45V	--	--	--		
AH	5.50V	-5.50V	--	--	--		
BH	5.55V	-5.55V	--	--	--		
CH	5.60V	-5.60V	--	--	--		
DH	5.65V	-5.65V	--	--	--		
EH	5.70V	-5.70V	--	--	--		
FH	5.75V	-5.75V	--	--	--		
10H	5.80V	-5.80V	--	--	--		
11H	5.85V	-5.85V	--	--	--		
12H	5.90V	-5.90V	--	--	--		
13H	5.95V	-5.95V	--	--	--		
14H	6.00V	-6.00V	--	--	--		
15H	6.05V	-6.05V	--	--	--		
16H	6.10V	-6.10V	--	--	--		
17H	6.15V	-6.15V	--	--	--		
18H	6.20V	-6.20V	--	--	--		
19H	6.25V	-6.25V	--	--	--		
1AH	6.30V	-6.30V	--	--	--		
1BH	6.35V	-6.35V	--	--	--		

	PMIC						
	PAVDD	NAVDD	Reserved	Reserved	Reserved	Reserved	Switching Frequency
1CH	6.40V	-6.40V	--	--	--	--	
1DH	6.45V	-6.45V	--	--	--	--	
1EH	6.50V	-6.50V	--	--	--	--	
1FH	6.55V	-6.55V	--	--	--	--	
20H	6.60V	-6.60V	--	--	--	--	
21H	6.65V	-6.65V	--	--	--	--	
22H	6.70V	-6.70V	--	--	--	--	
23H	6.75V	-6.75V	--	--	--	--	
24H	6.80V	-6.80V	--	--	--	--	
25H	6.85V	-6.85V	--	--	--	--	
26H	6.90V	-6.90V	--	--	--	--	
27H	6.95V	-6.95V	--	--	--	--	
28H	7.00V	-7.00V	--	--	--	--	
29H	7.05V	-7.05V	--	--	--	--	
2AH	7.10V	-7.10V	--	--	--	--	
2BH	7.15V	-7.15V	--	--	--	--	
2CH	7.20V	-7.20V	--	--	--	--	
2DH	7.25V	-7.25V	--	--	--	--	
2EH	7.30V	-7.30V	--	--	--	--	
2FH			--	--	--	--	
30H			--	--	--	--	
31H			--	--	--	--	
32H			--	--	--	--	
33H			--	--	--	--	
34H			--	--	--	--	
35H			--	--	--	--	
36H			--	--	--	--	
37H			--	--	--	--	
38H			--	--	--	--	
39H			--	--	--	--	
3AH			--	--	--	--	
3BH			--	--	--	--	
3CH			--	--	--	--	
3DH			--	--	--	--	

	Power On Sequence										
	PAVDD ON Delay Time	PAVDD Soft-start Time	Reserved	Reserved	Reserved	Reserved	NAVDD On Delay Time	*NAVDD Soft-start Time*	Reserved	RESET ON Delay Time	Power OFF Delay Time
Data Address	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h
Bits	[3:0]	[2:0]	[3:0]	[2:0]	[3:0]	[1:0]	[3:0]	[2:0]	[3:0]	[3:0]	[3:0]
Min	0ms	5ms	--	--	--	--	0ms	5ms	--	0ms	0ms
Max	75ms	40ms	--	--	--	--	75ms	40ms	--	75ms	45ms
Default	01h	01h	02h	01h	01h	01h	01h	01h	09h	01h	07h
Resolution	5ms	5ms	--	--	--	--	5ms	5ms	--	5ms	3ms
0H	0ms	5ms	--	--	--	--	0ms	5ms	--	0ms	0ms
1H	5ms	10ms	--	--	--	--	5ms	10ms	--	5ms	3ms
2H	10ms	15ms	--	--	--	--	10ms	15ms	--	10ms	6ms
3H	15ms	20ms	--	--	--	--	15ms	20ms	--	15ms	9ms
4H	20ms	25ms	--	--	--		20ms	25ms	--	20ms	12ms
5H	25ms	30ms	--	--	--		25ms	30ms	--	25ms	15ms
6H	30ms	35ms	--	--	--		30ms	35ms	--	30ms	18ms
7H	35ms	40ms	--	--	--		35ms	40ms	--	35ms	21ms
8H	40ms		--		--		40ms		--	40ms	24ms
9H	45ms		--		--		45ms		--	45ms	27ms
AH	50ms		--		--		50ms		--	50ms	30ms
BH	55ms		--		--		55ms		--	55ms	33ms
CH	60ms		--		--		60ms		--	60ms	36ms
DH	65ms		--		--		65ms		--	65ms	39ms
EH	70ms		--		--		70ms		--	70ms	42ms
FH	75ms		--		--		75ms		--	75ms	45ms

	Option 1						
	RESET Sync Option	VIN Detection	PAVDD Discharge Function	NAVDD Discharge Function	Reserved	Reserved	Reserved
Data Address	12h						
Bits	[7]	[6:5]	[4]	[3]	[2]	[1]	[0]
Min	-	-	-	-	-	-	-
Max	-	-	-	-	-	-	-
Default	00h	00h	00h	00h	01h	01h	00h
Resolution	-	-	-	-	-	-	-
0H	Power off Delay	UVLO Falling	On	On	--	--	--
1H	Reserved	2.1V	Off	Off	--	--	--
2H		2.4V					
3H		2.7V					

	Option 2				Option 3				
	PAVDD Slew Rate	NAVDD Slew Rate	Reserved	Reserved	Reserved	Freq. Spread Option(EMI)	OTP	UVP	SCP
Data Address	13h				14h				
Bits	[7:6]	[5:4]	[3:2]	[1:0]	[5]	[4:3]	[2]	[1]	[0]
Min	Slowest	Slowest	--	--	-	Off	-	-	-
Max	Fast	Fast	--	--	-	6%	-	-	-
Default	01h	01h	01h	01h	00h	00h	00h	00h	00h
Resolution	-	-	-	-	-	3%	-	-	-
0H	Fast	Fast	--	--	--	Off	On	On	On
1H	Normal	Normal	--	--	--	3%	Off	Off	Off
2H	Slow	Slow	--	--		6%			
3H	Slowest	Slowest	--	--					

	Channel ON/OFF Option						Auto Refresh Option		
	RESET EN	Reserved	NAVDD EN	Reserved	Reserved	PAVDD EN	FAULT Behavior	Refreshing Time	AR EN
Data Address	16h						17h		
Bits	[5]	[4]	[3]	[2]	[1]	[0]	[3]	[2:1]	[0]
Min	-	-	-	-	-	-	-	-	-
Max	-	-	-	-	-	-	-	-	-
Default	01h	01h	01h	00h	00h	01h	00h	01h	00h
Resolution	-	-	-	-	-	-	-	-	-
0H	Off	--	Off	--	--	Off	FAULT not pull low	0.25s	Off
1H	On	--	On	--	--	On	FAULT pull low	0.50s	On
2H								1.00s	
3H								2.00s	
4H									
5H									
6H									
7H									
8H									
9H									
AH									
BH									
CH									
DH									
EH									
FH									

	Power Off Sequence					
	PAVDD OFF Delay Time	NAVDD OFF Delay Time	Reserved	Reserved	FAULT Analysis Clear Option	Reserved
Data Address	18h	19h	1Ah	1Bh	1Ch	
Bits	[2:0]	[2:0]	[2:0]	[2:0]	[3]	[2:0]
Min	0ms	0ms	--	--	-	--
Max	14ms	14ms	--	--	-	--
Default	07h	07h	00h	00h	00h	00h
Resolution	2ms	2ms	--	--	-	--
0H	0ms	0ms	--	--	Not Clear	--
1H	2ms	2ms	--	--	Clear	--
2H	4ms	4ms	--	--		--
3H	6ms	6ms	--	--		--
4H	8ms	8ms	--	--		--
5H	10ms	10ms	--	--		--
6H	12ms	12ms	--	--		--
7H	14ms	14ms	--	--		--

	FAULT Analysis(DAC)			
	PAVDD FAULT	Reserved	Reserved	NAVDD FAULT
Data Address	1Dh			
Bits	[3]	[2]	[1]	[0]
Min	-	-	-	-
Max	-	-	-	-
Default	00h	00h	00h	00h
Resolution	-	-	-	-
0H	No Fault	--	--	No Fault
1H	Happen	--	--	Happen

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WET-WQFN-20L 5x5 package, the thermal resistance, θ_{JA}, is 28.2°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / 28.2°C/W) = 3.54W for a WET-WQFN-20L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 13 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

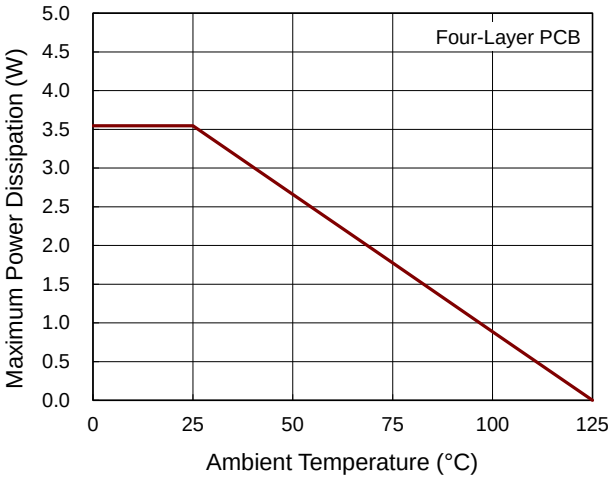


Figure 13. Derating Curve of Maximum Power Dissipation

Layout Consideration

For the best performance of the RTQ6752-QT. The following descriptions are the guidelines for better PCB layout :

- The power components such as inductor (L1, L2), input cap(C1, C2, C3) and output cap(C4, C5, C6, C7, C8, C9) must be placed as close as possible to reduce power loop. The PCB trace between power components must be as short and wide as possible.
- Minimize the size of the LX, LXN node and keep it wide and short. Keep the LX, LXN node away from those sensing pins (COMP, PAVDD feedback pin) and analog ground.
- The power ground (PGND1, PGND) consists of input and output capacitor grounds.
- The compensation circuit (R1, C10) should be kept away from the power loops and should be shielded with a ground trace to prevent any noise coupling. Place the compensation components as close as possible to COMP pin.
- The exposed pad of the chip should be connected to a large negative voltage plane for thermal consideration.

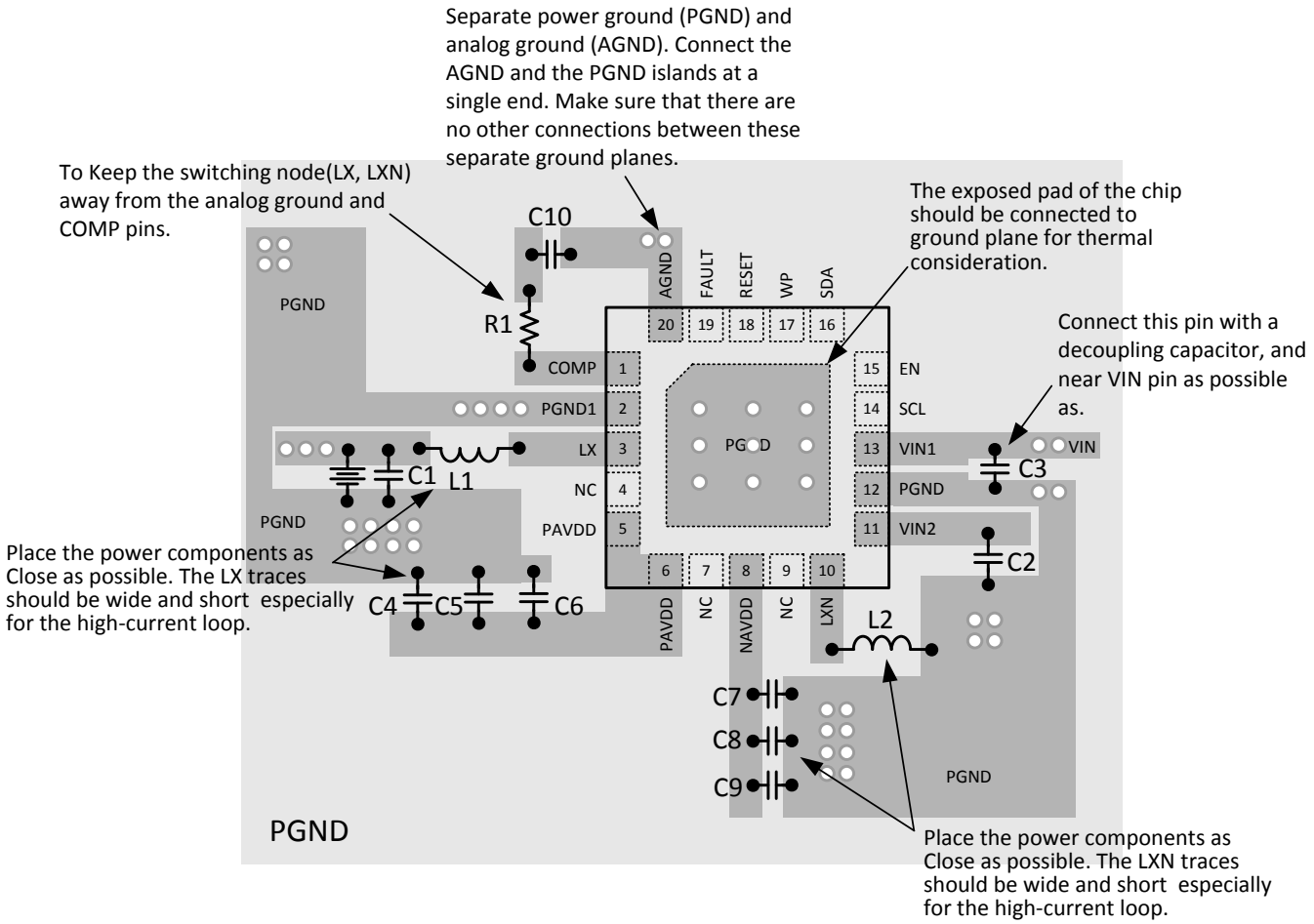
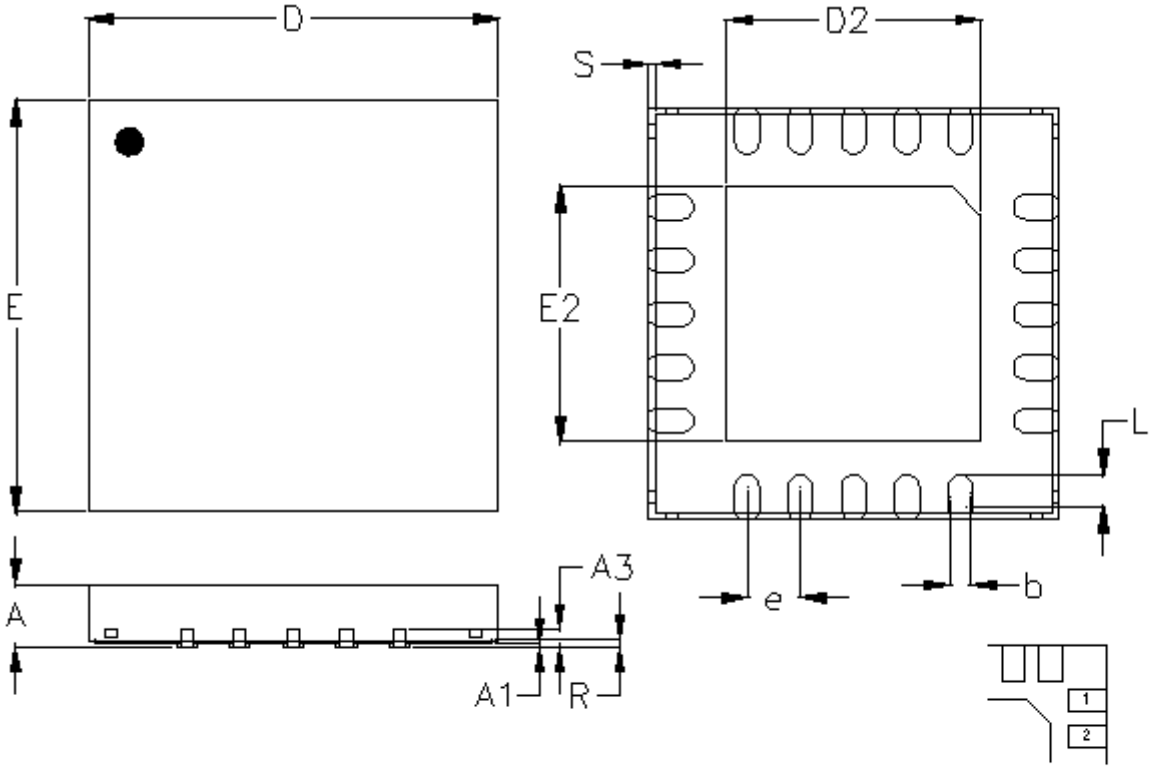


Figure 14. PCB Layout Guide

Outline Dimension



DETAIL A

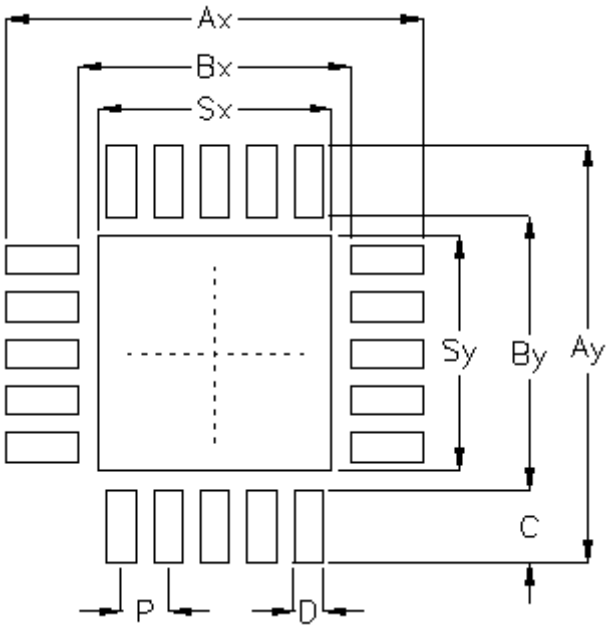
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.250	0.350	0.010	0.014
D	4.950	5.050	0.195	0.199
D2	3.050	3.150	0.120	0.124
E	4.950	5.050	0.195	0.199
E2	3.050	3.150	0.120	0.124
e	0.650		0.026	
L	0.500	0.600	0.020	0.024
R	0.050	0.150	0.002	0.006
S	0.001	0.090	0.000	0.004

WET W-Type 20L QFN 5x5 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
WET-V/W/U/XQFN5x5-20	20	0.65	5.80	5.80	3.80	3.80	1.00	0.40	3.25	3.25	±0.05

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