RICHTEK®

RTQ9124DL-QA

1x10W, Digital Input Automotive Class-D Audio Amplifier with Current Sense and Real-Time Load Diagnostics

1 General Description

The RTQ9124DL-QA is an ultra-low output noise, high-efficiency, mono channel class-D audio power amplifier, delivering 10W into 4Ω at 1% THD+N from a 14.4V supply. It can achieve over 80% power efficiency, with an output switching frequency of up to 2.1MHz, enabling a cost-optimized solution in a very small PCB size.

The RTQ9124DL-QA is fully configurable through the I²C bus interface and includes a comprehensive diagnostics array specifically designed for automotive applications. During audio playback, the status can be monitored through the output current sense, which reports measurements to a host processor via I²S or TDM with minimal delay.

The built-in anti-pop function reduces speaker pop noise under all scenarios. Additionally, the built-in protection circuits provide thermal fold-back, over-temperature, overcurrent, overvoltage, and undervoltage protection, and report error status.

The RTQ9124DL-QA is a 3-wire device that receives all clocks from external sources using standard I²S and TDM (Time-Division Multiplexing) formats. It supports a wide input sampling rate from 8kHz to 96kHz.

The RTQ9124DL-QA is intended for various automotive audio applications, including telematics and e-call systems.

The RTQ9124DL-QA is available in a WET-VQFN-32L 5x5 package. The recommended junction temperature range is –40°C to 150°C, and the ambient temperature range is –40°C to 125°C.

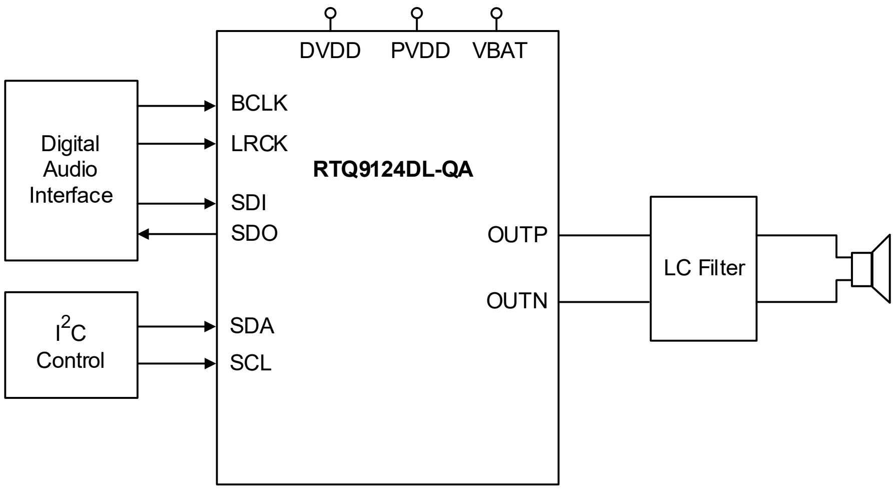
2 Features

- **AEC-Q100 Qualified**
- **I²S and TDM Input (up to 16CH TDM)**
- **1x10W, THD+N = 1%, 4Ω, 14.4V**
- **THD+N is 0.05%**
- **SNR up to 110dB**
- **Ultra-Low Noise = 18μV**
- **Switching Frequency up to 2.1MHz**
- **Sampling Frequency from 8kHz to 96kHz**
- **I²C Control with 4 Address Options**
- **Built-In Anti-Pop Function**
- **Built-In Thermal Fold-Back and Clip Detection**
- **Ultra-Low Quiescent Current Mode (ULQM)**
- **AC-DC Load Diagnostics**
- **Real Time Load Diagnostics**
- **Temperature and Voltage Sensing via I²C**
- **Protection Features**
  - **Output Short-Circuit**
  - **Overvoltage and Undervoltage**
  - **Overcurrent Warning**
  - **Overcurrent**
  - **Over-Temperature**
  - **DC Detection**
  - **40V Load Dump**
- **VQFN-32L Wettable Flanks**
- **Ambient Temperature Range: –40°C to 125°C**
- **Junction Temperature Range: –40°C to 150°C**

3 Applications

- e-Call Systems
- Telematics

4 Simplified Application Circuit



5 Ordering Information

RTQ9124DL□-QA□

Packing
A: Standard

Grade
QA: AEC-Q100 Qualified
Screened by High Temperature

Package Type(1)
N: WET-VQFN-32L 5x5 (V-Type)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

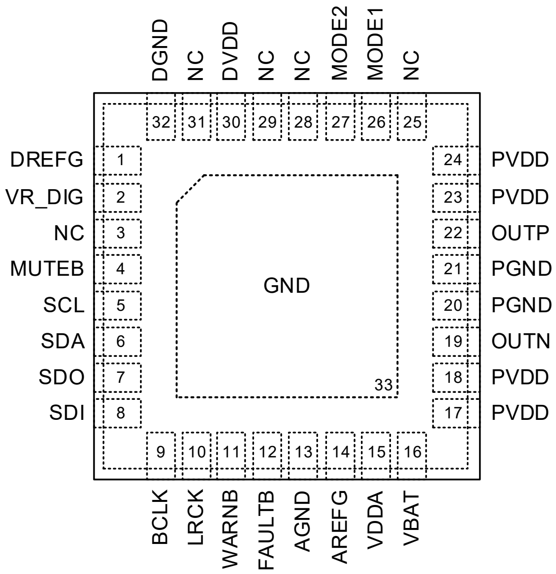
6 Marking Information

RTQ9124DLN: Product Code
QA: Automotive Product Grade
YMDAN: Date Code

Table of Contents

7 Pin Configuration

(TOP VIEW)



WET-VQFN-32L 5x5

8 Functional Pin Description

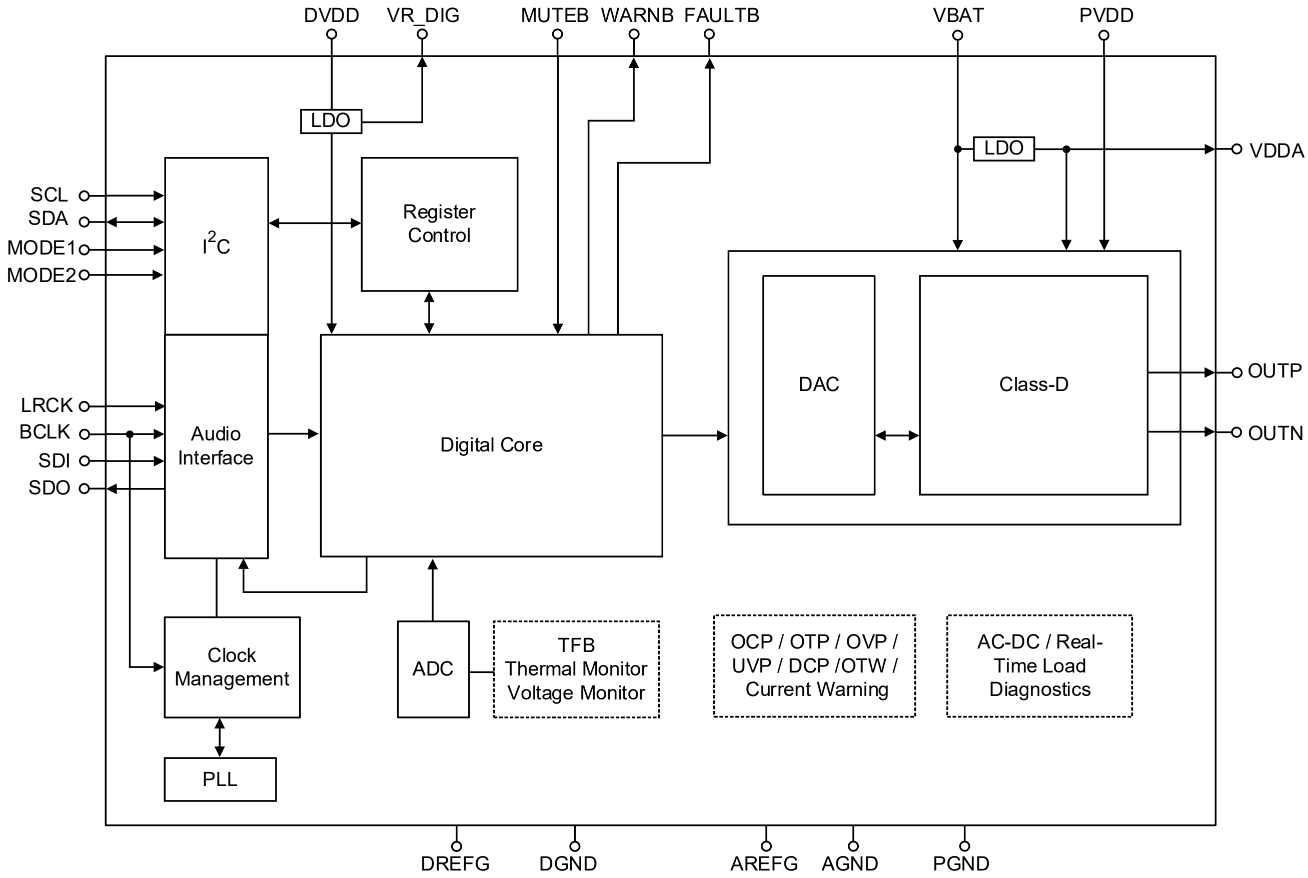
Pin No.	Pin Name	IO	Pin Function
1	DREFG	GND	Ground for digital circuit (Internally generated).
2	VR_DIG	PWR	Voltage regulator output is 1.8V; tie to DVDD when DVDD = 1.8V.
3, 25, 28, 29, 31	NC	NC	No internal connection.
4	MUTEB	DI	Mute control, 0 = mute; 1 = unmute.
5	SCL	DI	I^2C reference clock.
6	SDA	DI/DO	I^2C data.
7	SDO	DI	I^2S data out.
8	SDI	DI	I^2S data in.
9	BCLK	DI	I^2S bit clock.
10	LRCK	DI	I^2S frame clock.
11	WARNB	DO	Warning flag, 0 = warning happens, 1 = normal.
12	FAULTB	DO	Fault flag, 0 = fault happens; 1 = normal.
13	AGND	GND	Ground for analog circuit.
14	AREFG	GND	Ground for analog circuit (Internally generated).
15	VDDA	PWR	Voltage regulator output 5.1V.
16	VBAT	PWR	Battery voltage input.
17, 18, 23, 24	PVDD	PWR	Supply voltage for power stage.

Pin No.	Pin Name	IO	Pin Function
19	OUTN	NO	Negative PWM output.
20, 21	PGND	GND	Ground for power stage.
22	OUTP	PO	Positive PWM output.
26	MODE1	DI	I^2C address pins 1 / Enable function pin 1.
27	MODE2	DI	I^2C address pins 2 / Enable function pin 2.
30	DVDD	PWR	Supply voltage for digital circuit.
32	DGND	GND	Ground for digital circuit.
33 (Exposed Pad)	GND	P	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

8.1 IO Type Definition

- GND: Ground
- PWR: Power
- PO: Positive Output
- NO: Negative Output
- DI: Digital Input
- DO: Digital Output
- DI/DO: Digital Input/Output
- NC: No Connection

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, PVDD, VBAT, DVDD -- –0.3V to 28V
- Vpeak, transient supply voltage, PVDD, VBAT, DVDD ($t \leq$ 400ms Exposure) ------------------------ –1V to 40V
- Speaker Amplifier Output Voltage, OUTP, OUTN -- –0.3V to 28V
- SCL, SDA, FAULTB, WARNB, MODE1, MODE2, MUTEB, BCLK, LRCK, SDI, SDO----------------- –0.3V to 6V
- VDDA --- –0.3V to 6V
- VR_DIG -- –0.3V to 4V
- Power Dissipation, P_D @ T_A = 25°C

  WET-VQFN-32L 5x5--- 3.37W
- Package Thermal Resistance (Note 3)

  WET-VQFN-32L 5x5, θ_{JA}-- 29.67°C/W

  WET-VQFN-32L 5x5, θ_{JC}-- 0.85°C/W
- Lead Temperature (Soldering, 10sec.)-- 260°C
- Junction Temperature --150°C
- Storage Temperature Range --- –55°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model)-- ±2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, PVDD, VBAT, DVDD ---4.5V to 18 V
- MODE Input Voltage, MODE1, MODE2 ---1.8 or 3.3 V
- Ambient Temperature Range--–40°C to 125°C
- Junction Temperature Range--–40°C to 150°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(PVDD = VBAT = DVDD = 14.4V, R_L = 4Ω, f_{SW} = 2.1MHz, AES17 filter, BTL, T_A = 25°C, unless otherwise specified.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
MUTEB	VIH: High-Level-Input Voltage	V_{IH}		1.26	--	--	V
	VIL: Low-Level-Input Voltage	V_{IL}		--	--	0.54	
FAULTB, WARNB	VOL: Low-Level-Output Voltage	V_{OL}	I_O = 3mA	--	--	0.4	V
DVDD Quiescent Current		I_{Q_DVDD}	Output channel playing, switch 50% duty	--	2.2	--	mA
DVDD ULQM Current		I_{ULQM_DVDD}	ULQM	--	1.5	--	mA
DVDD Shutdown Current		I_{SD_DVDD}	MODE1 and MODE2 = 0V	--	1.7	--	μA
PVDD Quiescent Current (Normal Mode)		I_{Q_PVDD}	Output channel playing, switch 50% duty	--	41	--	mA
PVDD Quiescent Current (ULQM)		I_{ULQM_PVDD}	ULQM	--	0.1	--	mA
PVDD Shutdown Current		I_{SD_PVDD}	MODE1 and MODE2 = 0V	--	1.5	--	μA
VBAT Quiescent Current (Normal Mode)		I_{Q_VBAT}	Output channel playing, switch 50% duty	--	9.5	--	mA
VBAT Quiescent Current (ULQM)		I_{ULQM_VBAT}	ULQM	--	0.6	--	mA
VBAT Shutdown Current		I_{SD_VBAT}	MODE1 and MODE2 = 0V	--	7	--	μA
Drain-Source On-State Resistance		R_{DSON}	PVDD = 14.4V, I_O = 500mA, T_J = 25°C	--	200	--	mΩ
VDDA		V_{VDDA}		--	5.1	--	V
VR_DIG		V_{VR_DIG}		--	1.8	--	V
Speaker Gain variation		ΔGain	Gain variation	–0.5	--	0.5	dB
PWM Switching Frequency		f_{SW}	384kHz mode	--	384	--	kHz
			2100kHz mode	--	2100	--	
RMS Output Power Per Channel, BTL		P_O	4Ω, PVDD = 14.4V, T_A = 75°C	--	10	--	W
Total Harmonic Distortion + Noise		THD+N	P_O = 1W	--	0.05	--	%
Output Integrated Noise		Vn	20Hz to 20kHz, A-weighted	--	18	--	μV
Signal-to-Noise Ratio		SNR	PVDD = 14.4V, P_O = 10W	--	110	--	dB
Power Supply Rejection Ratio		PSRR	Frequency @ 1kHz	--	–75	--	dB
Dynamic Range		DR	Input level –60dBFS	--	110	--	dB
Output Attenuation			MUTEB = 0V	--	100	--	dB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Efficiency	η	10W output, 4Ω load, PVDD = 14.4V, including inductor loss	--	80	--	%
Click and POP		High-Z/MUTE to Play, Play to MUTE/High-Z	--	5	--	mV
Junction Over-Temperature Warning	T_{OTW}		--	150	--	°C
Junction Over-Temperature Protection	T_{OTP}		--	170	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
Overcurrent Warning	I_{OCW}		--	2.5	--	A
Overcurrent Protection	I_{OCP}	Any short to supply or ground	--	4.5	--	A
PVDD Overvoltage Protection	V_{OVP_PVDD}		--	19.5	--	V
PVDD Overvoltage Protection Hysteresis	$V_{OVP\_HYS\_PVDD}$		--	0.7	--	V
VBAT Overvoltage Protection	V_{OVP_VBAT}		--	19.5	--	V
VBAT Overvoltage Protection Hysteresis	$V_{OVP\_HYS\_VBAT}$		--	0.7	--	V
DVDD Overvoltage Protection	V_{OVP_DVDD}		--	19.5	--	V
DVDD Overvoltage Protection Hysteresis	$V_{OVP\_HYS\_DVDD}$		--	0.7	--	V
PVDD Undervoltage Protection	V_{UVP_PVDD}		--	4	--	V
PVDD Undervoltage Protection Hysteresis	$V_{UVP\_HYS\_PVDD}$		--	0.28	--	V
VBAT Undervoltage Protection	V_{UVP_VBAT}		--	4	--	V
VBAT Undervoltage Protection Hysteresis	$V_{UVP\_HYS\_VBAT}$		--	0.28	--	V
DVDD Undervoltage Protection	V_{UVP_DVDD}		--	1.4	--	V
DVDD Undervoltage Protection Hysteresis	$V_{UVP\_HYS\_DVDD}$		--	0.1	--	V
Resistance to Detect a Short from OUT Pins to PVDD	R_{S2P}		--	400	--	Ω
Resistance to Detect a Short from OUT Pins to Ground	R_{S2G}		--	200	--	Ω
Open Load	R_{OL}		--	50	--	Ω
DC Diagnostic Time	t_{DC_DIAG}		--	100	--	ms
AC Diagnostic Time	t_{AC_DIAG}		--	50	--	ms
ULQM Wake Up Time	t_{ULQM_WP}		--	--	10	ms

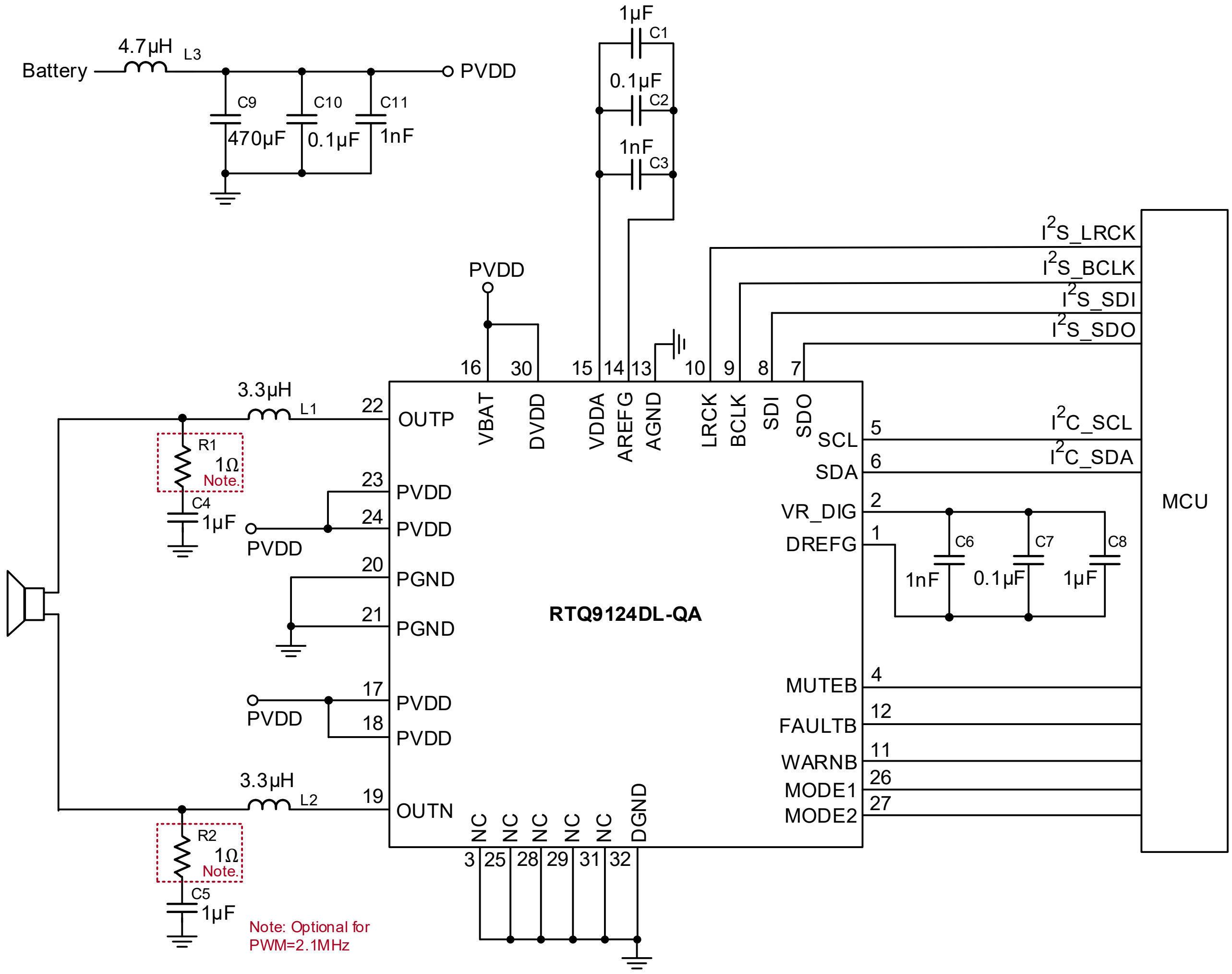
Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
I^{2}C Interface Electrical Characteristics							
High-Level Input Voltage (Belongs to the Internal 1.8V Domain)		V_{IH}		1.26	--	--	V
Low-Level Input Voltage (Belong to the Internal 1.8V Domain)		V_{IL}		--	--	0.54	V
Pull-Down Current		I_{FO2}	(Note 6)	--	2	--	μA
Clock Operating Frequency		f_{SCL}		--	--	1000	kHz
Bus Free Time Between Stop and Start Condition		t_{BUF}		0.5	--	--	μs
Hold Time After (Repeated) Start Condition		$t_{HD;STA}$		0.26	--	--	μs
Repeated Start Condition Setup Time		$t_{SU;STA}$		0.26	--	--	μs
Stop Condition Time		$t_{SU;STD}$		0.26	--	--	μs
Data Setup Time		$t_{SU;DAT}$		50	--	--	ns
Clock Low Period		t_{LOW}		0.5	--	--	μs
Clock High Period		t_{HIGH}		0.26	--	--	μs
Clock Data Fall Time		t_F		20	--	120	ns
Clock Data Rise Time		t_R		20	--	120	ns
Mode Function Electrical Characteristics							
High-Level Input Voltage		V_{IH}		1.4	--	--	V
Low-Level Input Voltage		V_{IL}		--	--	0.3	V
Slave Mode I^{2}S Interface Electrical Characteristics							
High-Level Input Voltage		V_{IH}		1.26	--	--	V
Low-Level Input Voltage		V_{IL}		--	--	0.54	V
SDO	VOH: High-Level Output Voltage	V_{OH}		--	--	3.3	V
	VOL: Low-Level Output Voltage	V_{OL}		--	--	0.4	
Frequency		f_{BCLKIN}		1.024	--	24.576	MHz
Setup Time, LRCK to BCLK Rising Edge		t_{SU1}		10	--	--	ns
Hold Time, LRCK from BCLK Rising Edge		t_{H1}		10	--	--	ns
Setup Time, SDIN to BCLK Rising Edge		t_{SU2}		10	--	--	ns
Hold Time, SDIN from BCLK Rising Edge		t_{H2}		10	--	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Rise/Fall Time for BCLK/LRCK	t_R/t_F		--	--	8	ns
I²S Duty Cycle for Rising	%		40	--	60	%

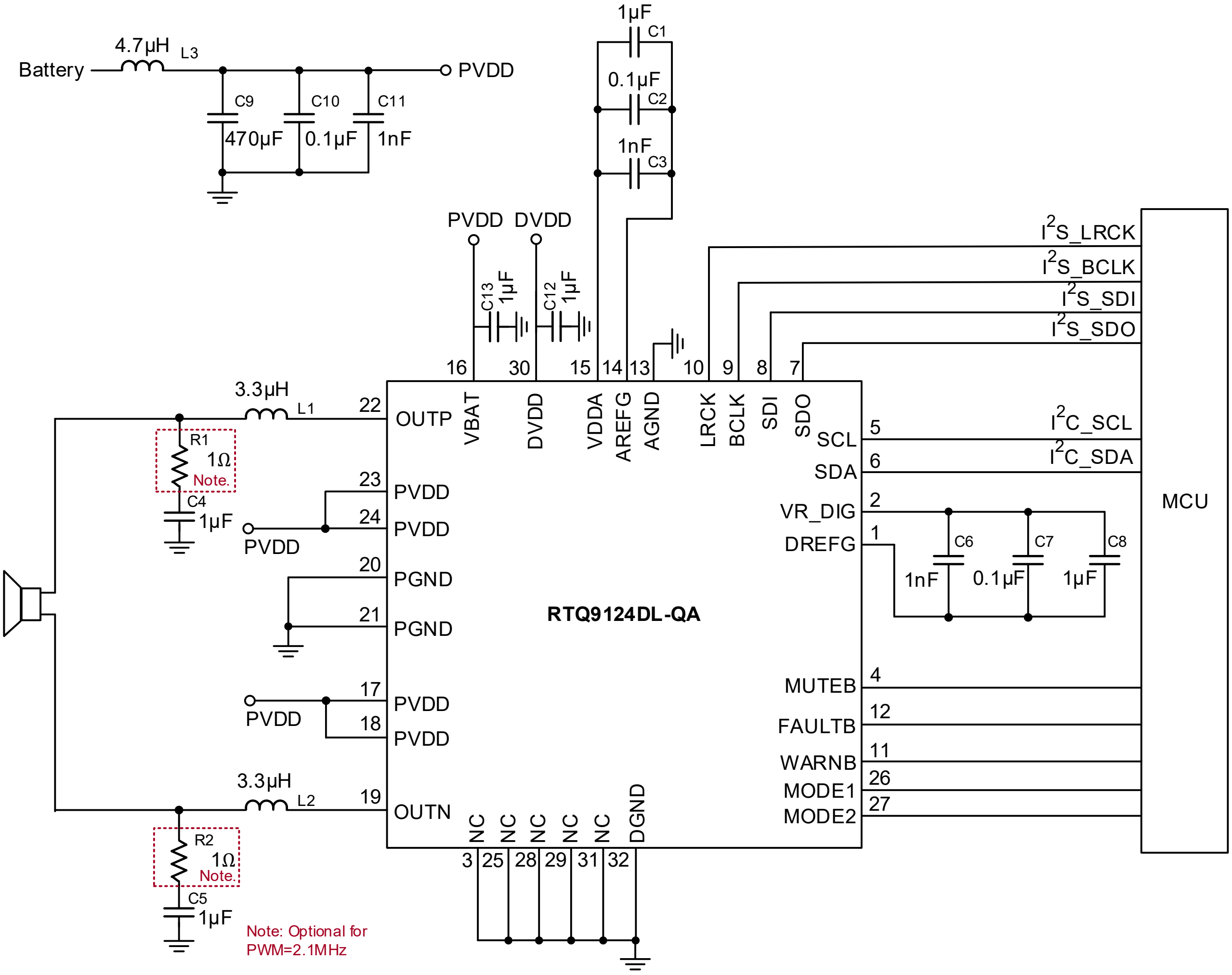
Note 6. The capability of the receiver to pull down the SDA line during the acknowledge clock pulse.

13 Typical Application Circuit

13.1 Single Power Source

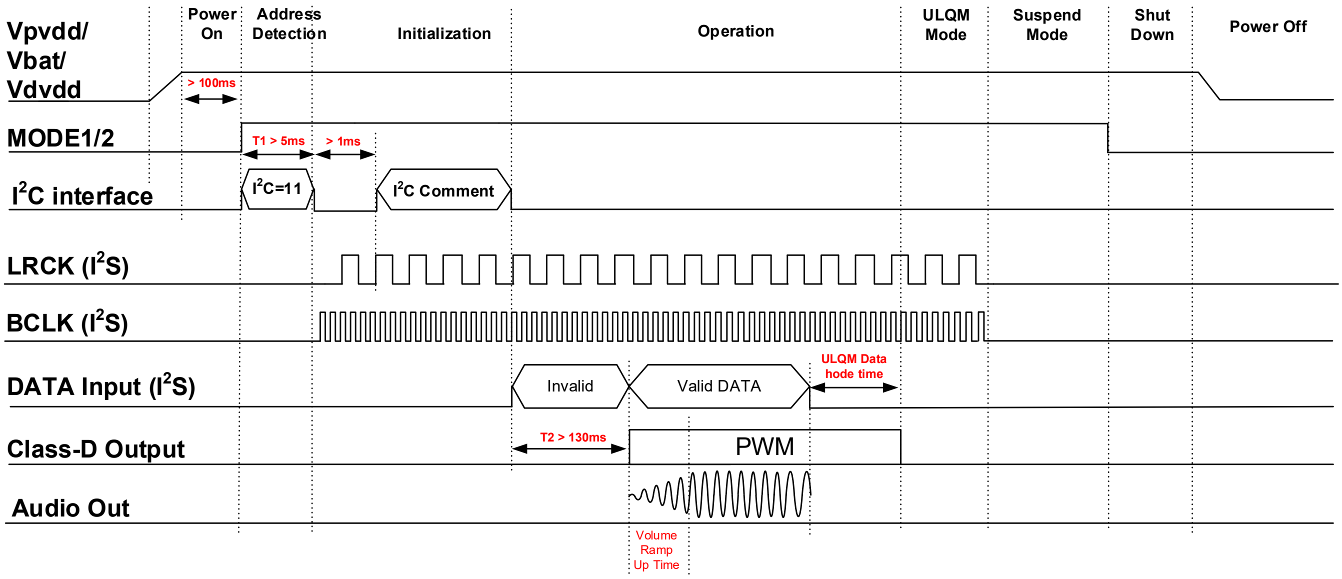


13.2 Dual Power Source

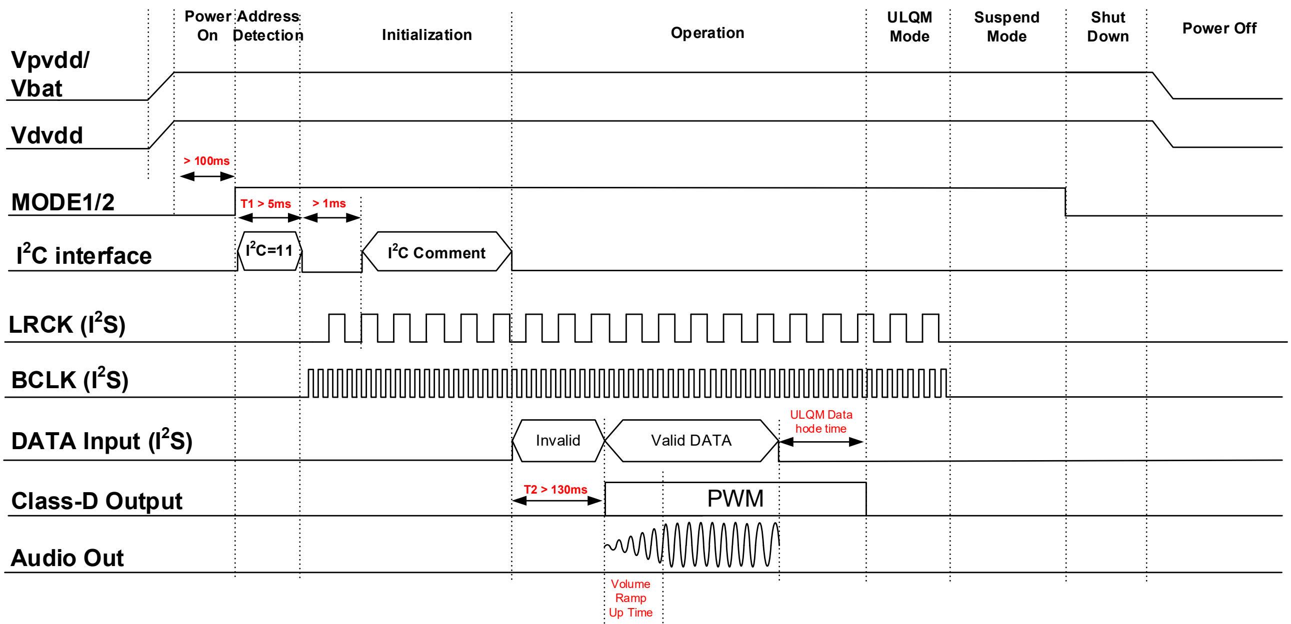


14 Timing Diagram

14.1 Power-On/Off Sequence (Single Power Source)



14.2 Power-On/Off Sequence (Dual Power Source)



14.3 Initial Sequence

14.3.1 Initial Sequence (PWM = 2.1MHz)

Sequence	reg_addr	reg_size	reg_value	Description
2	0x04	2	0x3D00	Amp Turn On

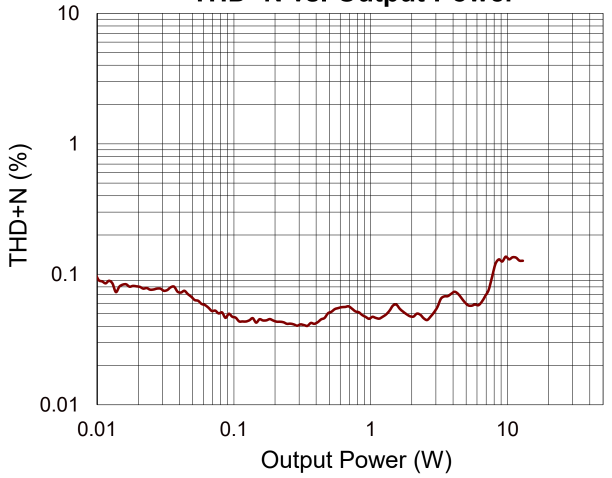
14.3.2 Initial Sequence (PWM = 2.1MHz with Real Time Protection)

Sequence	reg_addr	reg_size	reg_value	Description
1	0x01	2	0x0100	CS Data INV
2	0xFB	2	0x0065	Change RG Page
3	0x93	2	0x2000	CS Gain Setting
4	0xFB	2	0x0000	RG Page Back
5	0x49	2	0x03A0	RTLD Pilot tone
6	0x4B	2	0x5EAA	RTLD OPEN TH
7	0x4C	2	0x03FF	RTLD SHORT TH
8	0x58	2	0x03FC	RTLD SHORT EN
9	0x26	2	0x0000	RTLD Short Error Flag Unmask
10	0x04	2	0x3D00	Amp Turn On

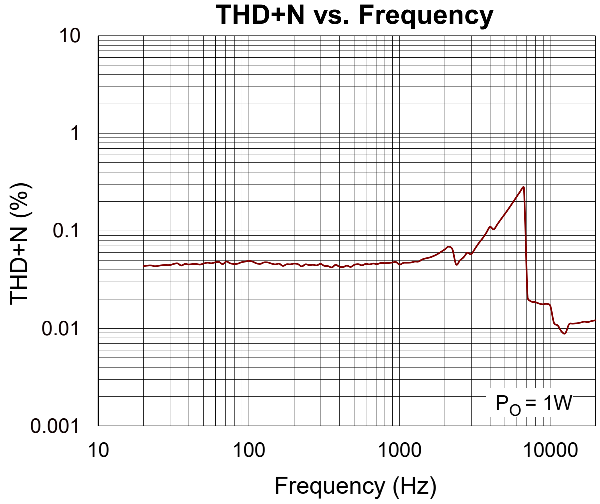
15 Typical Operating Characteristics

T_A = 25°C, VBAT = PVDD = DVDD =14.4V, R_L = 4Ω, fin = 1kHz, f_S = 48kHz, f_{SW} = 2.1MHz, BTL, AES17 filter, LC filter: 3.3μF –HCM1A0703V2-3R3-R, 1μF + 1Ω

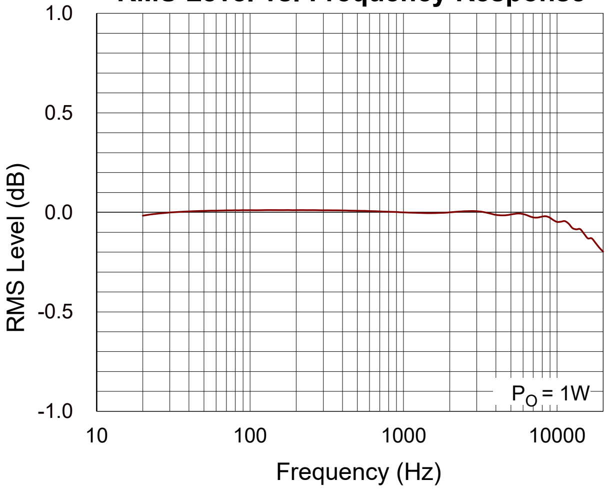
THD+N vs. Output Power



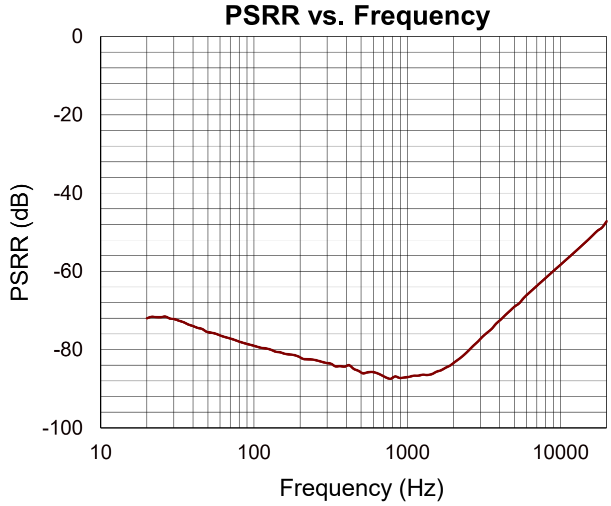
THD+N vs. Frequency



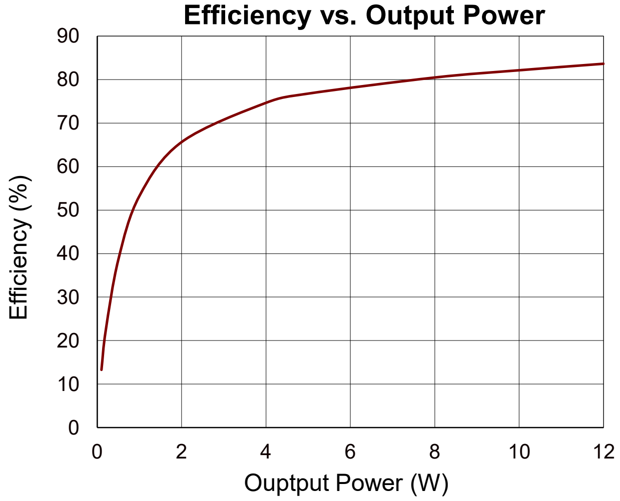
RMS Level vs. Frequency Response



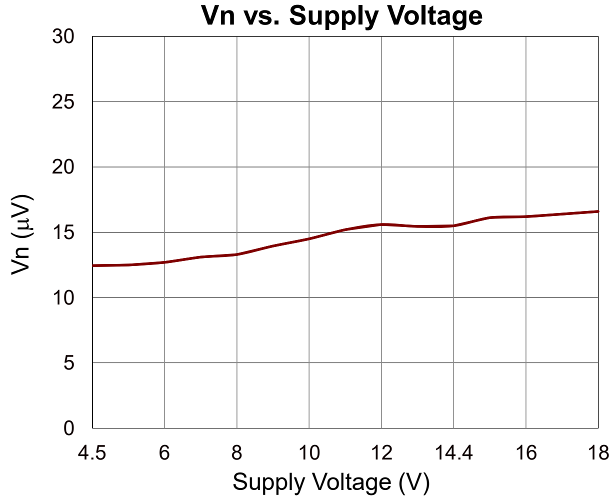
PSRR vs. Frequency

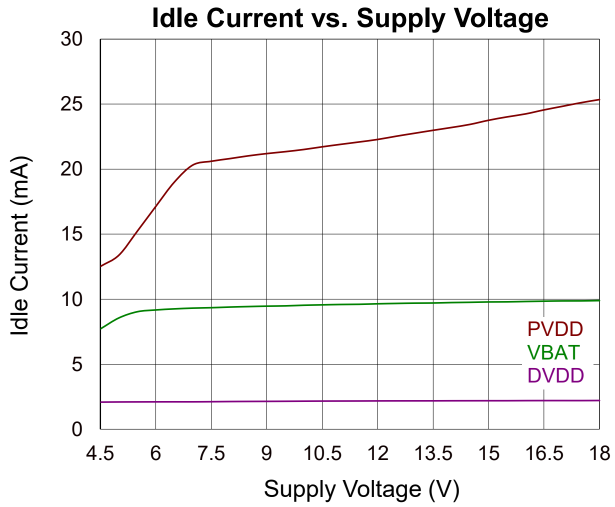


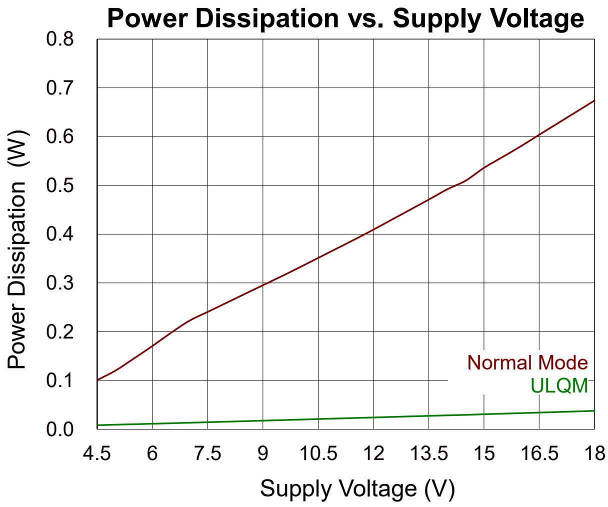
Efficiency vs. Output Power



Vn vs. Supply Voltage




Idle Current vs. Supply Voltage
Idle Current (mA)
Supply Voltage (V)
PVDD
VBAT
DVDD
0
5
10
15
20
25
30
4.5
6
7.5
9
10.5
12
13.5
15
16.5
18


Power Dissipation vs. Supply Voltage
Power Dissipation (W)
Supply Voltage (V)
Normal Mode
ULQM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
4.5
6
7.5
9
10.5
12
13.5
15
16.5
18

16 Application Information

(Note 7)

16.1 I^{2}C Serial Communication Bus

The RTQ9124DL-QA supports 4 sets of slave addresses, configurable through combinations of the MODE1 and MODE2 pins. These pins can be set using different resistors, each with a tolerance of 5%. Refer to the table below for specific address configurations.

The 3.3V input voltage application is for the MODE pins.

MODE1	MODE2	Slave Address	Write	Read
Pull high	Pull High with 560kΩ	0x11 (0010001x)	0x22	0x23
Pull high	Pull Low with 470kΩ	0x12 (0010010x)	0x24	0x25
Pull high	Pull low	0x13 (0010011x)	0x26	0x27
Pull High with 560kΩ	Pull high	0x14 (0010100x)	0x28	0x29
Pull low	Pull low	Shutdown	X	X

The 1.8V input voltage application is for the MODE pins.

MODE1	MODE2	Slave Address	Write	Read
Pull high	Pull High with 270kΩ	0x11 (0010001x)	0x22	0x23
Pull high	Pull Low with 470kΩ	0x12 (0010010x)	0x24	0x25
Pull high	Pull low	0x13 (0010011x)	0x26	0x27
Pull High with 270kΩ	Pull high	0x14 (0010100x)	0x28	0x29
Pull low	Pull low	Shutdown	X	X

The RTQ9124DL-QA is equipped with I^{2}C communication capabilities, utilizing the SCL and SDA input ports. In the I^{2}C protocol, devices transmitting data are designated as transmitters, while those reading the data are receivers. The master device initiates and controls the data transfer, supplying the serial clock to ensure synchronization. The RTQ9124DL-QA functions exclusively as a slave device in all communications and is capable of operating at speeds of up to 1000 kB/s. Its I^{2}C interface is designed to be slave-only.

16.2 I^{2}C Bus Protocol

Data transitions on the SDA line are only permitted when the SCL clock signal is low. Transitions on the SDA line while the SCL signal is high indicate a START or STOP condition. A START condition is signaled by a high-to-low transition on the SDA line while the SCL line remains high and stable. This condition must be established before any data transfer command is issued. Conversely, a STOP condition is signaled by a low-to-high transition on the SDA line while the SCL line remains high and stable, marking the end of communication between the RTQ9124DL-QA and the bus master. During data reception, the RTQ9124DL-QA samples the SDA line at the rising edge of the SCL signal. To ensure proper operation of the device, the SDA signal must remain stable during the rising edge of the SCL signal, and data changes on the SDA line should only occur when the SCL signal is low.

16.3 Audio Interface

The RTQ9124DL-QA supports four types of audio interfaces: I^{2}S, Left-Justified, Right-Justified, and TDM. Each interface is capable of handling audio data formats of 24-bits, 20-bits, and 16-bits. The corresponding timing diagrams are provided below.

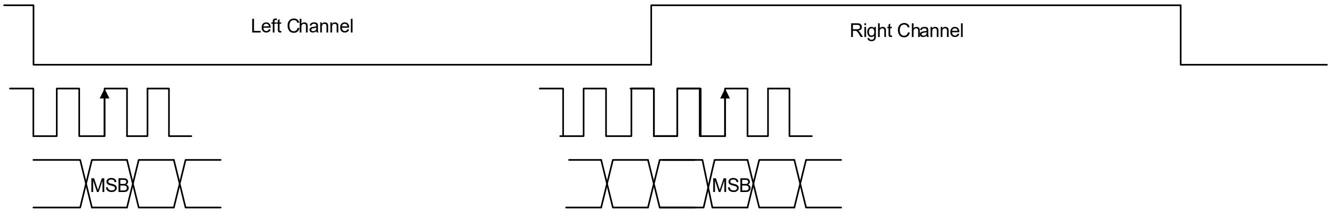


Figure 1. I^{2}S Format

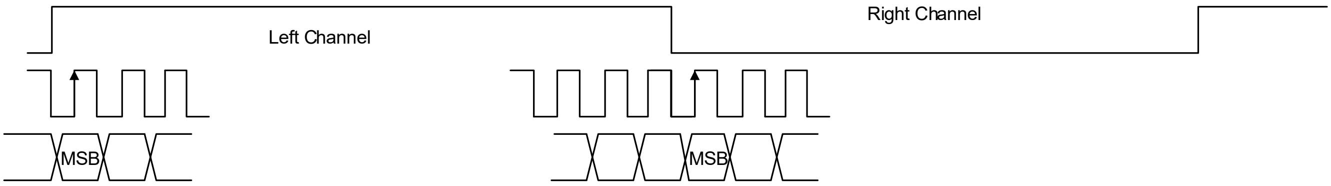


Figure 2. Left-Justified

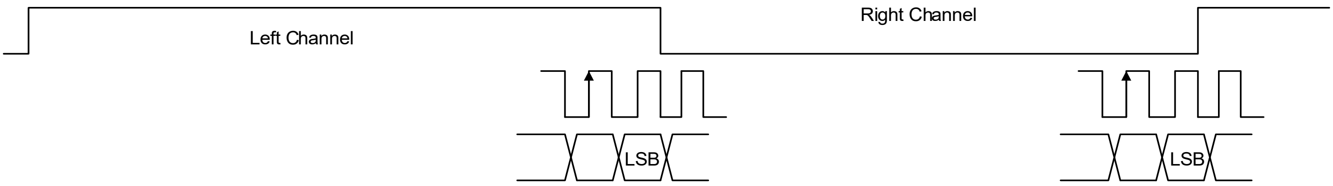


Figure 3. Right-Justified

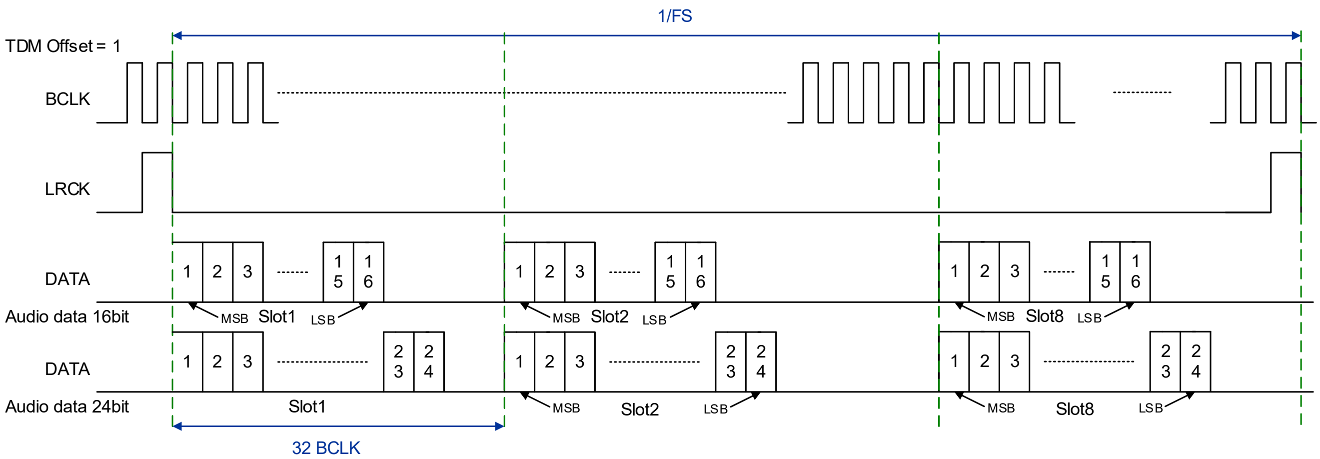


Figure 4. TDM (Offset = 1)

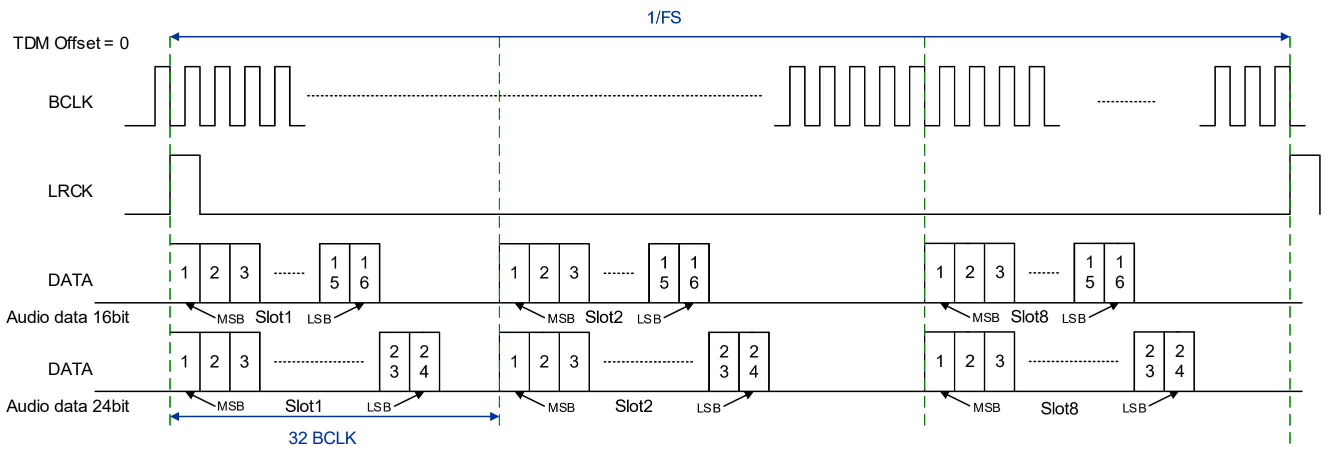


Figure 5. TDM (Offset = 0)

16.4 Time-Division Multiplexing (TDM) Mode

The TDM mode supports a maximum of 16 audio channels. The device can be configured via I^2C to select different channels within the TDM data stream. Refer to Register Map for details.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x02	2	2:0	RW	AUD_FMT	000: I^2S (default) 001: Left-Justify 010: Right-Justify 011: DSP mode 100: EIAJ Others: TDM mode	000
0x34	2	5:0	RW	TDM_RX_LOC_CH1	TDM start receiving location select for CH1 000000: Start from 0+offset (default) 000001: Start from 8+offset … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	000000

For example:

- TDM 8 Channels, Sampling Rate is 48KHz.

Channel Location	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8
0x34	Set to 0x00	Set to 0x04	Set to 0x08	Set to 0x0C	Set to 0x10	Set to 0x14	Set to 0x18	Set to 0x1C

- TDM 16 Channels, Sampling Rate is 48KHz.

Channel Location	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8
0x34	Set to 0x00	Set to 0x04	Set to 0x08	Set to 0x0C	Set to 0x10	Set to 0x14	Set to 0x18	Set to 0x1C
Channel Location	**Ch9**	**Ch10**	**Ch11**	**Ch12**	**Ch13**	**Ch14**	**Ch15**	**Ch16**
0x34	Set to 0x20	Set to 0x24	Set to 0x28	Set to 0x2C	Set to 0x30	Set to 0x34	Set to 0x38	Set to 0x3C

16.5 Digital Signal Processor

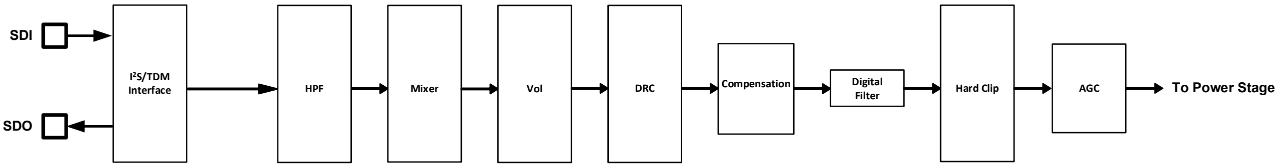


Figure 6. Digital Signal Processor

16.6 High-Pass Filter (HPF)

The RTQ9124DL-QA supports an input high-pass filter (HPF) for each channel, designed to act as a DC-cut filter with a cutoff frequency of 1.5Hz.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x08	2	6	RW	HPF_EN	High-Pass filter enable 0: Disable 1: Enable (default)	1

16.7 I²S Channel Selection

The RTQ9124DL-QA supports an input channel selection of I²S format.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x00	2	1:0	RW	CH_SI	I²S channel selection 01: L channel (default) 10: R channel others: (L+R)/2	01

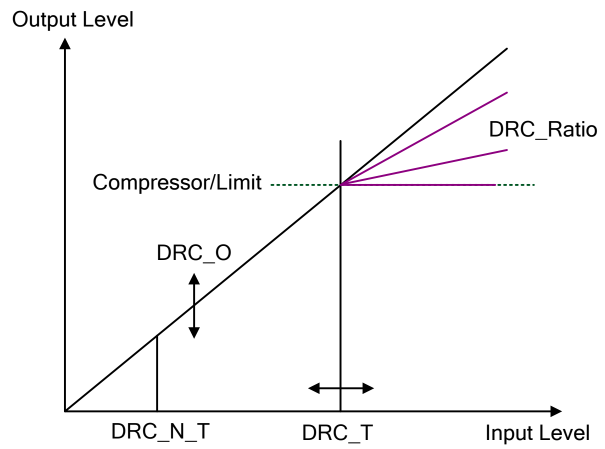
16.8 Volume

The RTQ9124DL-QA includes a volume control (VOL) feature. The volume can be adjusted in precise steps of 0.0625dB, with a range from 24dB to mute. A dedicated mute control is also provided for immediate muting of the output.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x38	2	10:0	RW	VOL	Master volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: Mute 0.0625dB per step	11'h180

16.9 Dynamic Range Control (DRC)

The RTQ9124DL-QA features Dynamic Range Control (DRC), which provides compression capabilities to adjust audio signals, making them sound softer or louder based on the input level.

DRC Description	Address	Description
DRC_TH: Threshold	0x3A	
DRC_O: Make up gain	0x3B	
DRC_Ratio: Compress ratio	0x3C	
DRC_NG_TH: Noise gate threshold	0x3D	
DRC_EN: DRC Enable	0x08	
DRC_N_EN: Noise gate enable	0x08	

16.9.1 DRC_TH

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x3A	2	10:0	RW	DRC_TH	DRC threshold 11'h000: 0dB (default) 11'h180: –24dB 11'h67E: –103.875dB 11'h67F ~ 11'h7FF: Not available 0.0625dB per step	11'h000

16.9.2 DRC_Offset

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x3B	2	10:0	RW	DRC_ OFFSET	DRC make up gain (Offset) 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: –103.9375dB 0.0625dB per step	11'h180

16.9.3 DRC_RATIO

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x3C	2	7:0	RW	DRC_ RATIO	DRC compress ratio 8'h00: No compression 8'h80 (default) ~8'hFF: Full compression 1/128 per step	8'h80

16.9.4 DRC_NG_TH

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x3D	2	10:0	RW	DRC_NG_TH	Noise gate threshold 11'h000: 0dB 11'h180: –24dB 11'h640: –100dB (default) 11'h67E: –103.875dB 11'h67F ~ 11'h7FF: Not available 0.0625dB per step	11'h640

16.9.5 DRC_EN/DRC_N_EN

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x08	2	4	RW	DRC_EN	DRC Enable 0: disable (default) 1: enable	0
		3	RW	DRC_N_EN	DRC Noise Gate Enable 0: disable (default) 1: enable	0

16.9.6 DRC Gain and Level Attack and Release Timing Settings

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x40	4	16:0	RW	DRC_AE	DRC_AE	17'h08000
0x41	4	16:0	RW	DRC_1_AE	DRC_1_AE	17'h00000
0x42	4	16:0	RW	DRC_AA	DRC_AA	17'h08000
0x43	4	16:0	RW	DRC_AD	DRC_AD	17'h08000

16.10 Compensation Filter

The compensation filter is used to adjust the internal gain from the DAC. This filter can also correct the frequency response affected by the LC filter. The recommended settings will vary based on different application circuits to achieve the desired response curve.

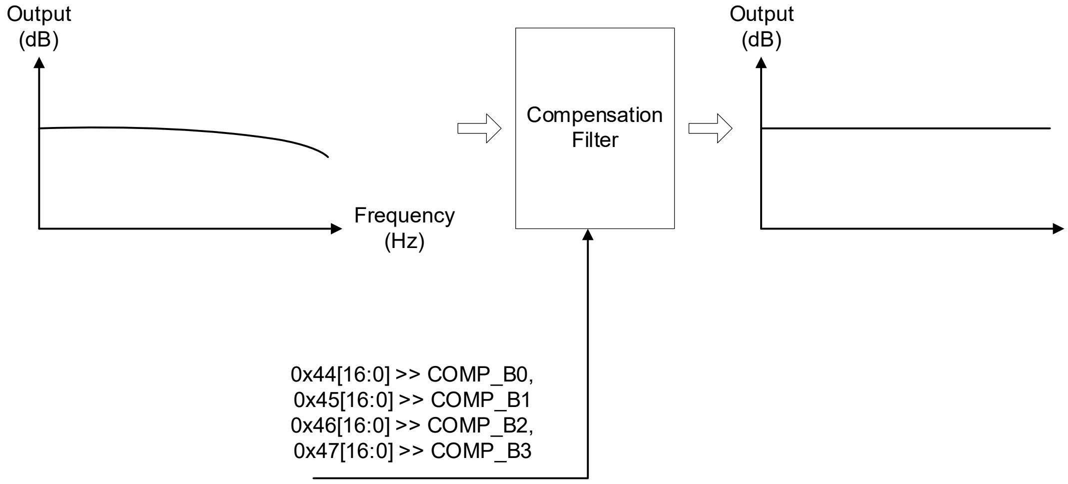


Figure 7. Compensation Filter

Table 1. Compensation Table for Fs=48k.

	−1.0	−0.9	−0.8	−0.7	−0.6	−0.5	−0.4	−0.3	−0.2	−0.1	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
B3 0x47	1FFE6	1FFE8	1FFEA	1FFED	1FFF0	1FFF2	1FFF5	1FFF8	1FFFA	1FFFE	0000	2	6	9	C	F	12	16	19	1D	21
B2 0x46	1FFBD	1FFC3	1FFCA	1FFD2	1FFD7	1FFDE	1FFE5	1FFEC	1FFF2	1FFF9	0000	7	E	14	1B	22	29	30	37	3B	43
B1 0x45	3D7	37A	31B	2B6	255	1F4	193	130	CC	62	0000	1FF9D	1FF2F	1FEC5	1FE5A	1FDED	1FD7F	1FD10	1FC9F	1FC2C	1FBB0
B0 0x44	790E	79B6	7A60	7B17	7BC9	7C77	7D27	7DDA	7E8F	7F50	8000	80B3	817A	823B	82FE	83C3	848B	8555	8622	86F6	87D9

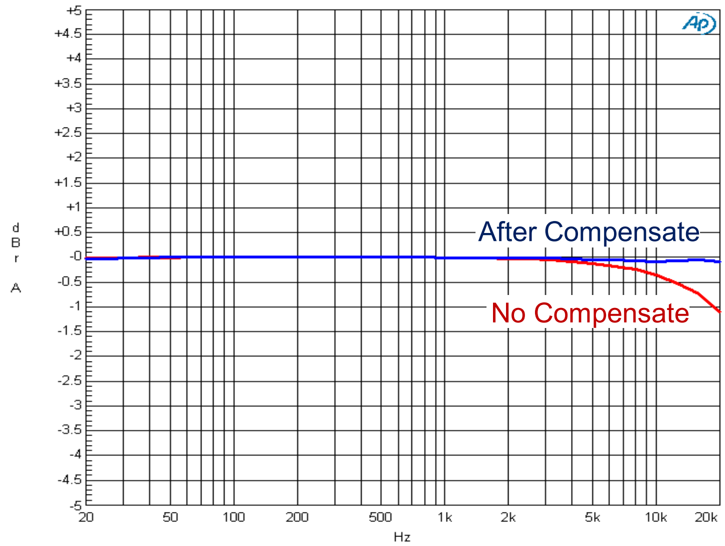


Figure 8. Compensation Filter Measured Result

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x44	4	16:0	RW	COMP_B0	Compensation filter coefficient B0.	17'h0_ 8000
0x45	4	16:0	RW	COMP_B1	Compensation filter coefficient B1.	17'h0_ 0000
0x46	4	16:0	RW	COMP_B2	Compensation filter coefficient B2.	17'h0_ 0000
0x47	4	16:0	RW	COMP_B3	Compensation filter coefficient B3.	17'h0_ 0000

16.11 Hard Clip Function

A hard clip can be employed to digitally maintain specified THD levels without resorting to voltage clipping. This feature enables users to consistently achieve the same THD (for example, 10% THD) across various power levels (15W, 10W, and 5W) while using the same PVDD level.

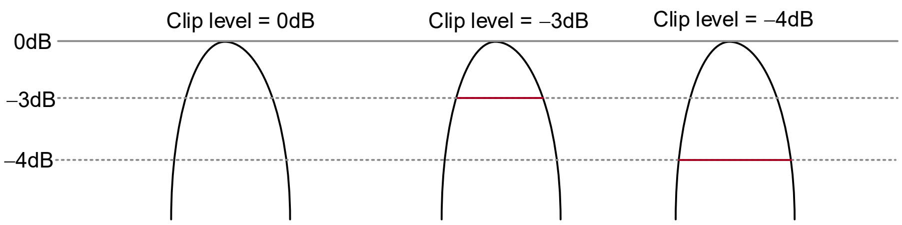


Figure 9. Hard Clip

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x39	2	10:0	RW	HC_TH	Hard clip threshold when HARD_CLIP_EN = 1 >0dB is not allowable for hard clip threshold setting 11'h18D: -0.825dB (default) 0.0625db per step	11'h18D

16.12 Auto-Gain Control (AGC)

The RTQ9124DL-QA supports AGC (Auto-Gain Control) for current limiting and clip detection functions. The AGC enable is independently controlled by the register at address 0x5A for both current limiting and clip detection.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x5A	2	0	RW	EN_CLIP_ AGC	Enable auto gain control for CLIP detection 0: Disable (default) 1: Enable	0

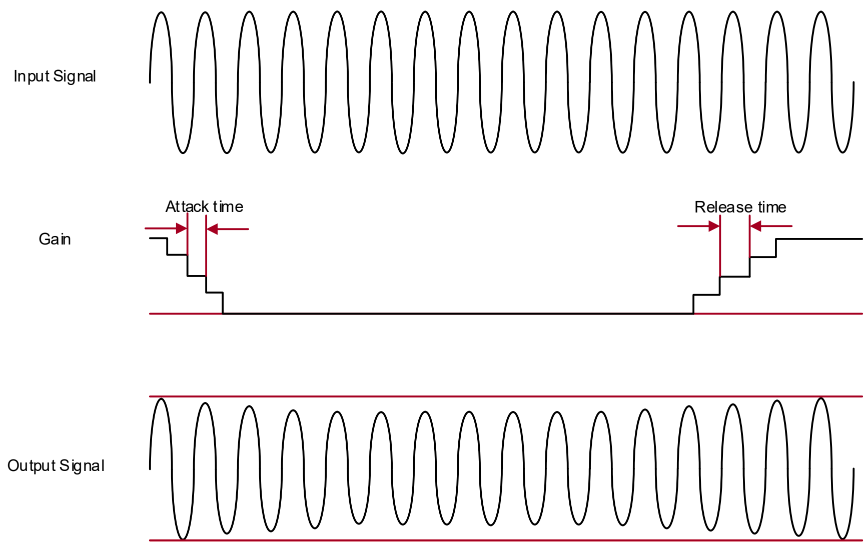


Figure 10. AGC Attack and Release

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x5B	2	3:2	RW	AGC_ ATTACK_ RATE	AGC attack time selection for clip AGC 00: 0.25dB/20μs 01: 0.25dB/40μs (default) 10: 0.25dB/80μs 11: 0.25dB/160μs	01
		1:0	RW	AGC_ RELEASE_ RATE	AGC release time selection for clip AGC 00: 0.25dB/200ms 01: 0.25dB/400ms (default) 10: 0.25dB/800ms 11: 0.25dB/1600ms	01

16.13 SDO Output Configure

The I^2S/TDM digital input signal path from the input pin to the power stage is illustrated in Figure 11. There are several nodes along the digital signal transmission path where the signal can be measured to verify proper functionality. The settings in register 0x01 Bit[7:0] can be output through the SDO pin.

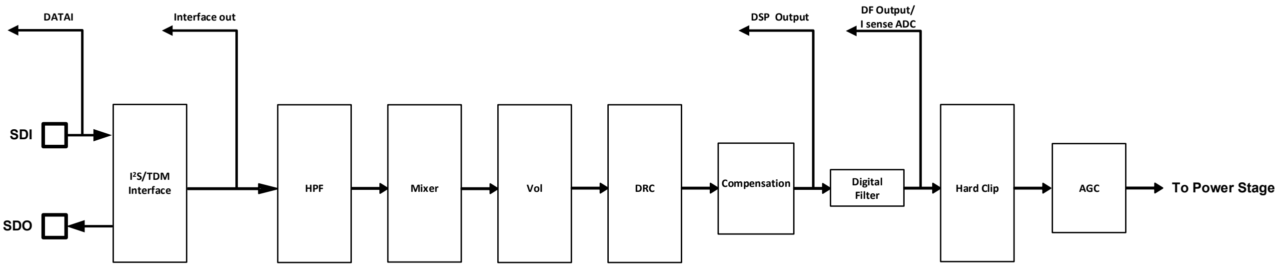


Figure 11. SDO Output Configure

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x01	2	7:4	RW	SDO_SEL_L	Left channel data 0000: No output (default) 0001: I^2S_DATAI 0010: Interface output 0011: DSP output 0100: DF output 0101: I sense ADC Others: Revered	0000
		3:0	RW	SDO_SEL_R	Right channel data 0000: No output (default) 0001: I^2S_DATAI 0010: Interface output 0011: DSP output 0100: DF output 0101: I sense ADC Others: Revered	0000

16.14 Hardware Control Pins

The device features four pins for control and status indication: FAULTB, MUTEB, WARNB and MODE1/2. The FAULTB pin reports faults and is active low under any of the following conditions:

- Any channel faults (overcurrent or DC detection)
- Over-temperature protection
- Overvoltage or undervoltage conditions on the PVDD, VBAT or DVDD pins
- Clock error

For all listed faults, the FAULTB pin remains asserted even after the fault condition is rectified. The register reports for all faults remain asserted until the CLEAR FAULT method is executed by writing to address 0x0F = FF. At that point, all fault register reports in ERR_INT_INDEX will be cleared to their default values, and the FAULTB pin will no longer remain asserted.

Register bits are available to mask fault categories from being reported to the FAULTB pin. These bits only mask the pin's status and do not affect the register reporting or the device's protection mechanisms. By default, all faults are reported to the pin. Refer to the Register Maps section for a description of the mask settings.

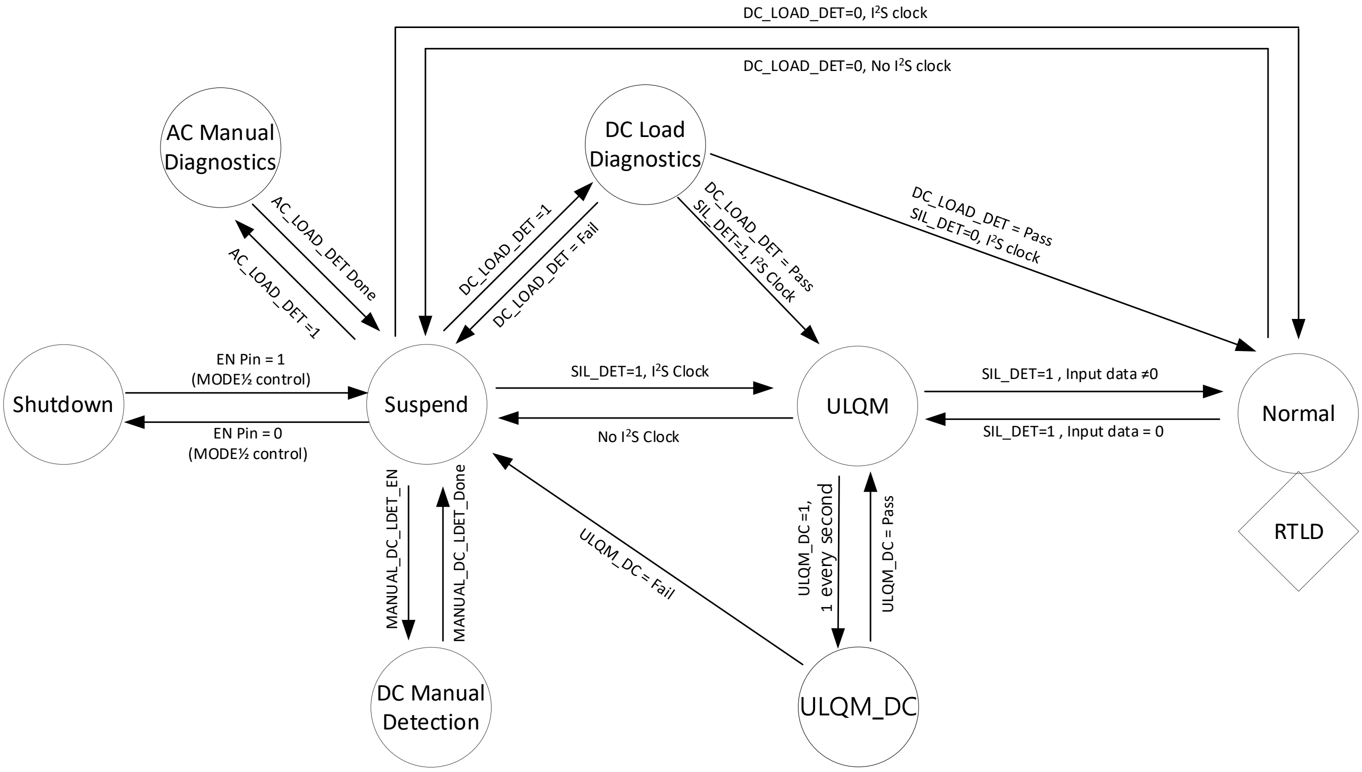
The active-low output WARNB pin reports audio clipping, over-temperature warnings, and overcurrent warnings. Clip is reported when any channel reaches maximum modulation for 20 consecutive PWM clocks (default value), resulting in a 10μs delay in reporting the onset of clipping. The Clip Detect Warning bit, which is sticky in latching mode, can be cleared by accessing the ERR_INT_INDEX in the register at address 0x0F and writing to address 0x0F=FF. An over-temperature warning (OTW) is triggered if the general temperature or any channel-specific temperature warnings are activated. Register bits are available to selectively mask the reporting of Clip, OTW, or IWARN to the pin. These bits solely affect the pin's setting and do not influence the register reporting. By default, Clip, IWARN, and OTW are reported at addresses 0x15 and 0x11.

The active-low input MUTEB pin controls the mute and unmute functions for output channel.

When the MODE1/2 pin is at a low level, the device enters shutdown mode, the I^2C function is disabled, and the current consumption is minimized. This pin allows for rapid shutdown of the device and resets the registers to their default values. When any MODE1/2 pin is at a high level, the device enters standby mode and the I^2C function is enabled. In this mode, the RTQ9124DL-QA can be commanded via I^2C to enter other modes.

16.15 Operating Modes and Faults

STATE_CTRL	Power MOSFETS	OSCILLATOR	I²C
Normal	Switching with input signal	Active	Active
MUTE	50% duty switching	Active	Active
ULQM	Hi-Z	Active	Active
Suspend	Hi-Z	Active	Active
Hi-Z	Hi-Z	Stopped	Active
Shutdown	Hi-Z	Stopped	Inactive



Fault Event	Reporting	Result	Monitor State	Protection Active	Behavior
CLK Error	I²C+FAULTB pin	Hi-Z	All	Output channel	Auto-recovery (default)
VDDA UV	I²C+FAULTB pin	Hi-Z	All	Output channel	Auto-recovery (default)
VBAT/PVDD/ DVDD UV	I²C+FAULTB pin	Hi-Z	All	Output channel	Auto-recovery (default)
VBAT/PVDD/ DVDD OV	I²C+FAULTB pin	Hi-Z	All	Output channel	Auto-recovery (default)
OTP	I²C+FAULTB pin	Hi-Z	All	Output channel	Auto-recovery (default)
S2P/S2G/OL	I²C+FAULTB pin	Hi-Z	Load detection	Output channel	Latch (default)

Fault Event	Reporting	Result	Monitor State	Protection Active	Behavior
Overcurrent	I^2C+FAULTB pin	Hi-Z	Normal, Mute	Output channel	Auto-recovery (default)
DC	I^2C+FAULTB pin	Hi-Z	Normal, Mute	Output channel	Latch (default)
POR	I^2C+WARNB pin	Shutdown	All	N/A	N/A
OTW	I^2C+WARNB pin	TFB (optional)	All	Output channel	N/A
Clip	I^2C+WARNB pin	AGC (optional)	Normal	Output channel	N/A

16.16 Ultra Low Quiescent Mode (ULQM)

The RTQ9124DL-QA implements automatic ULQM when there is no input signal and no LRCK/BCLK clock detected. Additionally, ULQM can be activated manually to further reduce power consumption for power-saving applications. In ULQM mode, the RTQ9124DL-QA powers the FETs in Hi-Z status with low standby current, and the transition time from ULQM to Normal mode is approximately 10ms.

- Support DATAI auto detection for ULQM mode. The hold time can be adjusted to 1, 20, 40, 80, 160, 320, 640 and 1280ms, and the time required to detect input data < ULQM threshold.
- Support I^2S clock detection for suspend mode, the time required to detect both LRCK/BCLK loss.

16.17 Pulse-Width-Modulator (PWM) Frequency

The output switching rate is synchronous to the serial audio clock input and is programmed through I^2C to match the input sample rate in the register (address 0x03[6:4]). The option to switch at a high frequency allows the use of smaller and lower-cost external filtering components.

Sample Rate	Reg 0x03h, BITS 6:4 Setting				
	000	001	010	011	100
8kHz	384kHz	480kHz	1.92MHz	2.1MHz	2.3MHz
16kHz	384kHz	480kHz	1.92MHz	2.1MHz	2.3MHz
24kHz	384kHz	480kHz	1.92MHz	2.1MHz	2.3MHz
32kHz	Not support	Not support	1.28MHz	1.41MHz	1.53MHz
44.1kHz	352kHz	441kHz	1.76MHz	1.94MHz	2.1MHz
48kHz	384kHz	480kHz	1.92MHz	2.1MHz	2.3MHz
88.2kHz	352kHz	441kHz	1.76MHz	1.94MHz	Not support
96kHz	384kHz	480kHz	1.92MHz	2.1MHz	Not support

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x03	2	6:4	RW	PWM_ FREQ	PWM frequency selection 000: 8*fs 001: 10*fs 010: 40*fs 011: 44*fs (default) 100: 48*fs Others: Reserved	011

16.18 AM-Radio Band Avoidance

By setting the switching frequency of the device above the AM frequency band, interference with AM radio frequencies can be avoided. The available switching frequency options include 38fs, 44fs, and 48fs. If the switching frequency cannot be set above the AM frequency band, the alternatives of 8fs and 10fs should be used. These settings should be adjusted to avoid active AM channels.

16.19 EMI Management Features

The RTQ9124DL-QA features a spread-spectrum function to address EMI issues.

16.19.1 Spread-Spectrum Function

There are two methods: varying the spread spectrum frequency and adding noise to the triangular modulation.

The spread-spectrum frequency variation amplitude is controlled via the register at address 0x07[1:0], and noise can be added to the triangular modulation through the register at address 0x07[6:2].

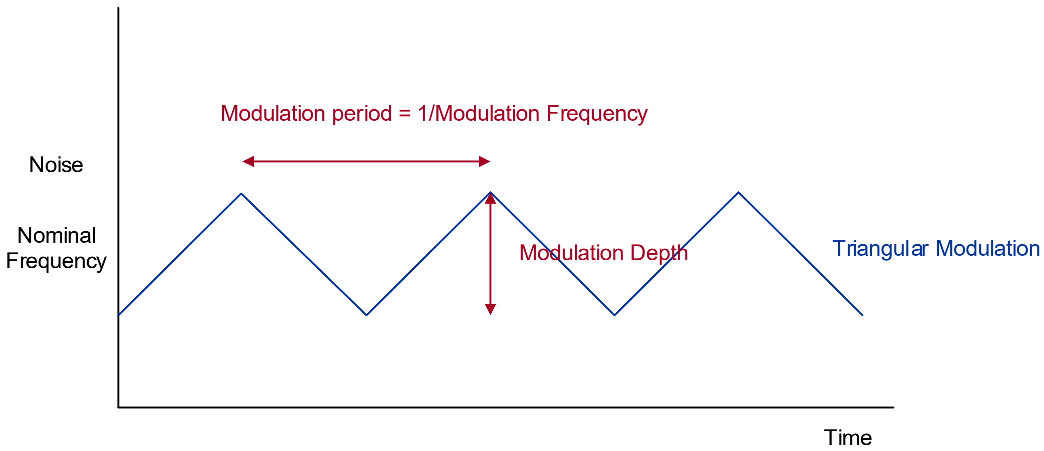


Figure 12. Spread-Spectrum Algorithm

16.20 Load Diagnostics

The device features both DC and AC load diagnostics to assess the status of the load. DC diagnostics are enabled by default via the register at address 0x04[13]. However, for a fast start-up that bypasses diagnostics, DC diagnostics can be disabled through I^{2}C. DC diagnostics activate when any channel transitions from the Hi-Z state to either the MUTE or Normal state. Additionally, DC diagnostics can be manually activated for any or all channels. They can commence under any operating condition; however, if a channel is in the Normal state, the diagnostic process takes longer. This delay occurs because the device must decrease the audio signal of that channel before it can switch to the Hi-Z state. DC diagnostics become available as soon as the device's power supply is within the recommended operating range. These diagnostics do not depend on the availability of audio input clocks. Results from the DC diagnostics are reported individually for each channel via the I^{2}C registers.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x04	2	13	RW	EN_DC_LOAD_DET	Execute DC load diagnostics before amp on sequence 0: Disable 1: Enable (default)	1

16.21 DC Load Detection

DC load detection assesses the status of the speaker side to prevent speaker damage. During this process, the device remains in a high-impedance state while playing a detection pattern. There are three types of DC load detection results: normal, S2G (short to ground), S2P (short to power) and OL (open load). The DC load detection method involves playing a pattern between the output channels OUTP and OUTN to diagnose the load (RL) status. DC load detection can be automatically initiated when the amplifier is powered on, as configured by bit 13 of register 0x04. It can also be manually triggered by setting bits [4] of register 0x51. The thresholds for S2G, S2P, and OL are controlled by registers at addresses 0x50.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x50	2	8	RW	S2P_TH	S2P threshold selection 0: 200 Ω 1: 400 Ω(default)	1
		7:6	RW	S2G_TH	S2G threshold selection 00: 200 Ω(default) 01: 400 Ω 10: 800 Ω 11: 1.2k Ω	00
		5:4	RW	OL_TH	OL threshold selection 00: 50 Ω(default) 01: 100 Ω 10: 200 Ω 11: 400 Ω	00

When the DC load detection result indicates an abnormal output channel, the device will pull the FAULTB voltage low. Registers 0x17 can be read to confirm the diagnostic result and identify the abnormal output channel.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x17	2	12	W1C	S2P	Output short to power 0: normal (default) 1: Warning (write 1 to clear)	0
		8	W1C	S2G	Output short to ground 0: normal (default) 1: Warning (write 1 to clear)	0
		4	W1C	OL	Output open load 0: normal (default) 1: Warning (write 1 to clear)	0

16.22 AC Load Detection

AC load detection can help distinguish speaker types such as woofers and tweeters. For AC load detection, the device must be in the Hi-Z state. The AC load gain is configured via the volume gain register 0x38[10:0], and a recommended setting for optimal detection is –40 dB. When detection finishes, users can obtain the magnitude and phase. The method of AC diagnosis involves playing a signal frequency pattern between the output channels OUTP and OUTN to diagnose the speaker status. The diagnostic result is obtained through an internal ADC, and the parameter values can be compensated and converted internally to obtain the magnitude and phase. AC load detection can be manually executed by setting bits [4] of register 0x53. The RTQ9124DL-QA GUI provides a load diagnostics function, which allows the load detection results to be displayed through the GUI without the need for manual calculation.

16.23 Real Time Load Diagnostics

Real-time diagnostics provide an on-site monitoring function to check the speaker wire connection status, regardless of whether the RTQ9124DL-QA is in ULQM or normal playback mode.

In ULQM, the RTQ9124DL-QA can enable real-time DC load detection function from register 0x04, bits [11:10]. When this function is enabled, the RTQ9124DL-QA automatically performs DC load detection at regular intervals. If the speaker wire is open, shorted to power, or shorted to ground, the RTQ9124DL-QA can notify the system to prevent risks, even when the amplifier is not active. Faults such as open or short-to-power/ground are handled as interrupts, eliminating the need for continuous polling through the I^2C bus.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x04	2	11:10	RW	ULQM_DCVT	ULQM Mode DCVT Mode 00: Disable 01: DC 10: VT 11: DC+VT (default)	11

In normal playback mode, the RTQ9124DL-QA features a built-in algorithm to obtain the speaker resistance in real-time from register 0x58, bits [8:7]. Unlike other products, the RTQ9124DL-QA does not require DSP resources to calculate the exact speaker DCR value. With the built-in DCR algorithm, the RTQ9124DL-QA can detect open load or short load by referencing the threshold settings in registers 0x4B and 0x4C. When the exact DCR value is available, the device can automatically reduce output gain to protect the speaker from overload. The measured DCR value is accessible via the I^2C bus for system monitoring.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x58	2	8	RW	LDET_OPEN_EN	Real Time Load Detection OPEN_EN 0: Disable 1: Enable (default)	1
0x58	2	7	RW	LDET_SHORT_EN	Real Time Load Detection SHORT_EN 0: Disable (default) 1: Enable	0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x4B	2	7:0	RW	DCR_OPEN_TH	Open_TH = X/2^12, Default = 4mA, LSB = 0.25mA	8'h10
0x4C	2	11:0	RW	DCR_SHORT_TH	S(2.10) Short_TH = X/2^10, Default = 0.02V	12'h018

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x93	2	13:12	RW	D_LD_GAIN_SEL	LD gain selection	00

16.24 Output Voltage

There are three types of gain in the RTQ9124DL-QA: digital volume gain, analog DAC gain, and speaker gain. The output voltage calculation formula is:

Output Voltage peak (Vp) = 10^ ((Input Level + Volume Gain) / 20) x 3.5 x SPK Gain (0.5 / 1 / 2 / 4 / 5 / 6.3 / 8).

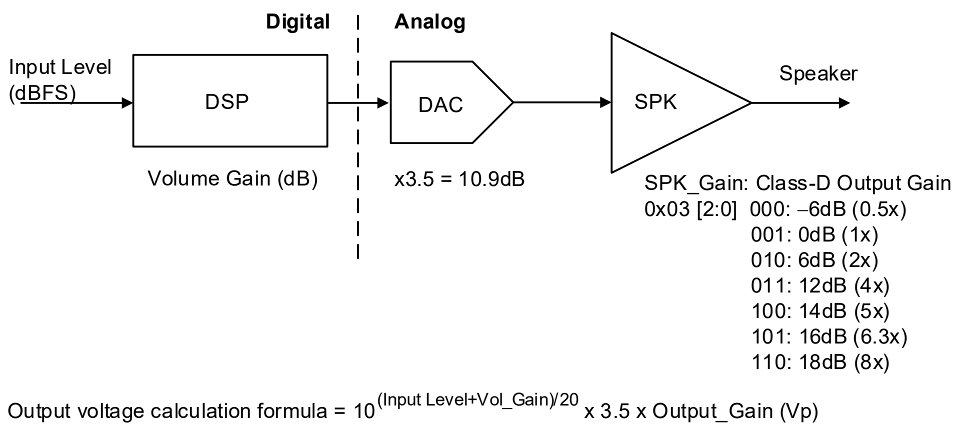


Figure 13. Output Voltage Calculation

16.25 Overcurrent Warning (IWARN)

When the overcurrent warning (IWARN) threshold is exceeded, a warning flag is triggered. IWARN is not reported as a fault condition to the fault registers or the FAULTB pin; instead, it is indicated as a warning on the WARNB pin and in the IWARN status register (address = 0x15[0]). Each channel is monitored and limited independently. Two programmable warning levels are available and can be configured using two bits in the register at address 0x60[0].

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x15	2	0	R1C	IWARN_Flag	Overcurrent warning flag 0: Normal (default) 1: Warning	0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x60	2	0	RW	IWARN_SEL	Overcurrent warning threshold selection 0: 2.5A 1: 3A (default)	1

16.26 Overcurrent Protection (OCP)

The RTQ9124DL-QA features an Overcurrent Protection (OCP) function to prevent damage to the device under overload or short-circuit conditions. This function is monitored by an internal sensing circuit. If the output current reaches the OC threshold, such as in case of an output short to GND, a peak current limit is triggered, which by default shuts down the channel in latch mode. Users can also select an auto-recovery mode for different applications.

16.27 DC Detection

During normal operation, the amplifier circuit continuously monitors the DC offset at the output. If the DC offset exceeds a specified threshold, the affected channel is placed in the Hi-Z state, a fault is reported to the I^2C register, and the FAULTB pin is activated. Optional register bits allow masking of this fault report to the FAULTB pin if desired. This DC monitoring is essential for protecting the loudspeaker from harmful DC at the output. The detection method involves analyzing the DC component at the final PWM stage, where the difference between the PWM output and a sinc filter is calculated to determine the DC level. If excessive DC is detected, the IC will automatically shut down to prevent damage.

16.28 Temperature and Voltage Sensing

16.28.1 Temperature Sensing.

The temperature sensing function continuously monitors the device temperature. The measured temperature is available in the register 0x0B (”Sense temp”). The output code is provided in decimal format and corresponds to the temperature in Kelvin, calculated as:

Code (DEC) = Temperature(K) = Temperature (°C) – 273

16.28.2 Voltage Sensing

The voltage sense function monitors the PVDD voltage within a range of 4.5V to 18V. The measured value is available in register 0x0A. The battery voltage can be calculated using the following equation:

Battery Voltage (V) = PVDD Code (DEC) / 160

16.29 Over-Temperature Warning (OTW) and Over-Temperature Protection (OTP)

The device offers four over-temperature warning levels (see the Register Map section for threshold values). When the junction temperature surpasses a warning level, the WARNB pin is activated unless the mask bit in the pin control register (address 0x21) is configured to disable this alert. The device operates normally until it reaches the OTSD threshold, at which point it places all channels in Hi-Z state and activates the FAULTB pin. By default, the device remains deactivated until the temperature normalizes. However, this behavior can be modified to automatic recovery by setting bits 2 in the miscellaneous control register (address 0x0D). Upon normalization of the junction temperature, the device automatically resumes operation and restores the channels to the configurations specified in the state control register. It is important to note that, even with automatic recovery enabled, the FAULTB pin stays active until the CLEAR FAULT bit (bit 1) in the register (address 0x11) is activated.

16.30 Undervoltage (UV) and Power-On-Reset (POR)

The RTQ9124DL-QA monitors the PVDD, VBAT and DVDD pins voltage threshold. When the voltage at the PVDD pin, VBAT pin or DVDD pin drops below the programmable undervoltage threshold of 4V, the Undervoltage Protection (UVP) circuit immediately shuts down the output. This device can also be configured to operate in latch mode instead.

When the DVDD voltage is set to 3.3V, the DVDD UVP is configured to 2.8V. If the DVDD operating voltage is 1.8V, then the VR_DIG pin must also be supplied with 1.8V, and the register must be configured to lower the DVDD UVP to 1.4V.

16.31 Overvoltage (OV) and Load Dump

The RTQ9124DL-QA monitors the voltage thresholds of the PVDD, VBAT and DVDD pins. When the voltage on the PVDD pin, VBAT pin or DVDD pin rises above the overvoltage threshold of 19.5V, the OVP circuit immediately shuts down the output. The device can then operate in auto-recovery mode or be configured to use latch mode.

16.32 Clip Detection

The clip detection is reported on the WARNB pin if a 100% duty-cycle PWM is sustained for a minimum number of PWM cycles as set by the Clip Window Register (address 0x5D). The default setting is 20 PWM cycles.

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x5D	2	3:0	RW	CLIP_DET_SEL	Clip detect threshold, release threshold (unit: PWM cycle) 0000: 1, 0 0001: 5, 3 0010: 10, 5 0011: 20, 5 (default) Others: Reserved	0011

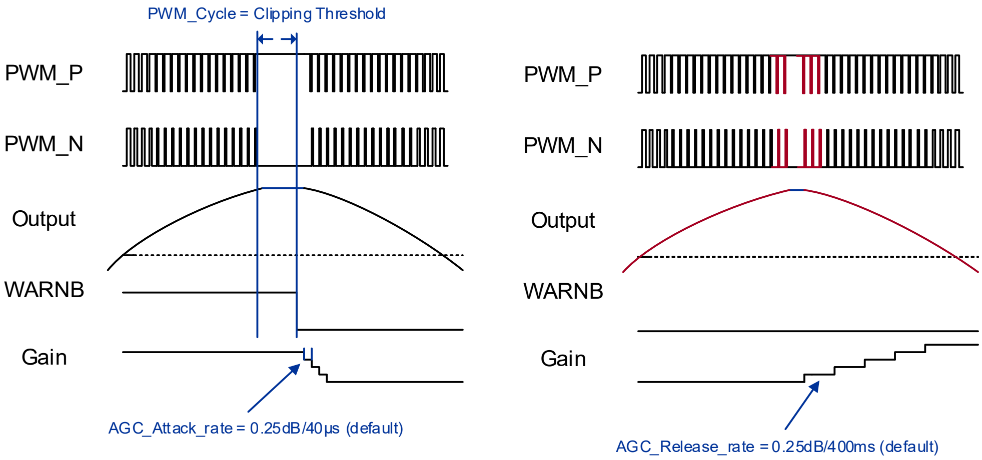


Figure 14. Clip Detection

16.33 Thermal Fold-Back (TFB)

The RTQ9124DL-QA features built-in Thermal Fold-Back protection (TFB), which is activated when the average junction temperature exceeds a specified threshold. TFB decreases the amplifier gain to reduce power dissipation, maintaining the junction temperature around the threshold level. The device will not completely switch off but will remain operational at lower output power levels. If the average junction temperature continues to rise, a second built-in temperature protection threshold will shut down the amplifier completely.

16.34 Recommended Operating Conditions

The RTQ9124DL-QA is designed for specific application conditions. It supports speakers with a typical impedance of 4Ω and a minimum impedance of 2Ω.

Minimum Speaker Load Impedance		
Min	Typ	Max
2Ω	4Ω	--

Based on the internal settings of the RTQ9124DL-QA and the LDMOS parameters, recommended application ranges are provided for the corresponding loaded speaker impedance and PVDD voltage.

Speaker Load	PVDD Range		
R_L (Ω)	Min	Typ	Max
2	4.5V	--	14.5V

16.35 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WET-VQFN-32L 5x5 package, the thermal resistance, θ_{JA}, is 29.67°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C − 25°C) / (29.67°C/W) = 3.37W for a WET-VQFN-32L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 15 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

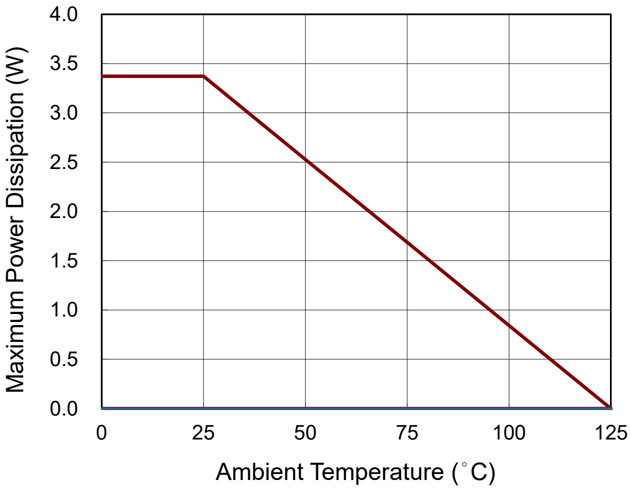


Figure 15. Derating Curve of Maximum Power Dissipation

16.36 Layout Consideration

For the best performance of the RTQ9124DL-QA, the following PCB layout guidelines must be strictly followed:

- The RTQ9124DL-QA features distinct digital signal pins and power pins. Ensure that digital signal traces and power traces are routed separately, and avoid crossing these traces. Implement a star grounding structure by gathering all ground points at a central location. The trace from VSYS or the battery to the PVDD pin should be sufficiently wide enough to support the required current.
- Pins 17, 18, 23, and 24 are PVDD power pins for the Class-D amplifier. Place the filter capacitors as close as possible to the PVDD pins, and use the shortest possible traces for connection. Capacitors with smaller capacitance values should be placed near the PVDD pins. To minimize parasitic inductance and resistance, use multiple vias to connect these capacitors directly to the main ground. The optimal approach is to use vias that are directly connected to the Main GND. Ensure that these vias are isolated to prevent unintended connections with other ground planes, as illustrated at position 1 in Figure 16.
- The ground associated with the VBAT pin is defined as AGND. The AGND pin trace should first connect to the ground terminal of the capacitor, then use a via to connect to the Main GND. The VBAT pin must use a star connection to reduce power noise, as indicated at position 2 in Figure 16.

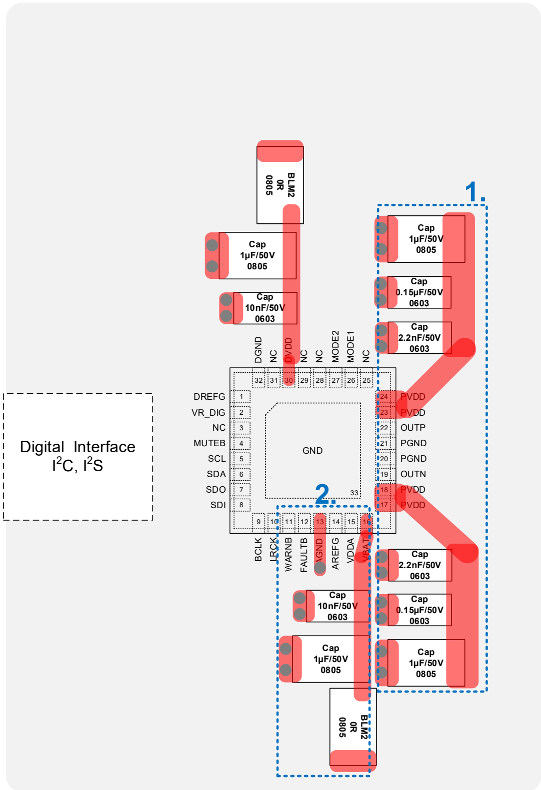


Figure 16. Layout Guide (Top Layer)

- The OUTP and OUTN traces should have equal widths and lengths to ensure balanced performance. When using an inductor or a ferrite bead filter, place it close to the chip as possible to optimize EMI performance. It is also recommended to position ground vias around the output traces to enhance grounding effectiveness.
- The ground associated with the VDDA pin is AREFG, and the ground associated with the VR_DIG pin is DREFG.

Place bypass capacitors as close as possible to these reference ground pins, using the shortest possible traces to connect the capacitors.

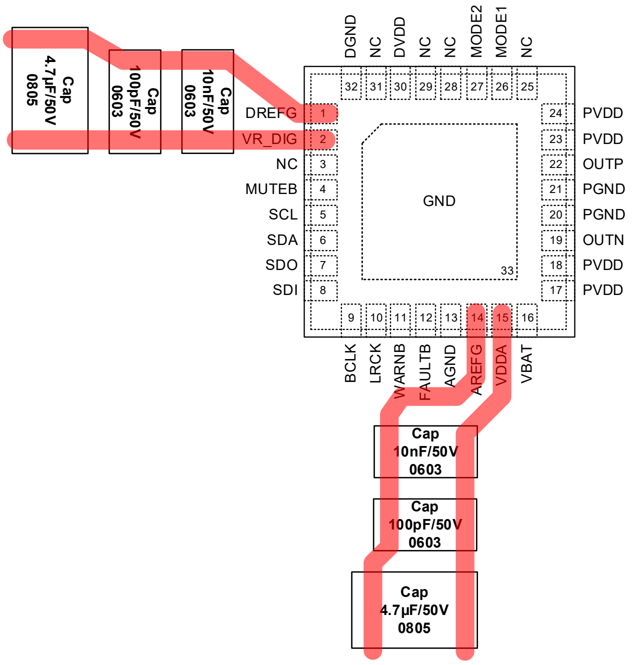


Figure 17. Bypass Capacitors

- Due to the numerous external traces, the ground of the RTQ9124DL-QA is connected to the MAIN GND using multiple vias. It is recommended to place a copper pour under the IC and add additional GND vias to improve the connection between the PGND pin on the top layer to the MAIN GND. This approach not only enhances grounding effectiveness but also increases the heat dissipation area.

Note 7. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Functional Register Description

17.1 I²C Command

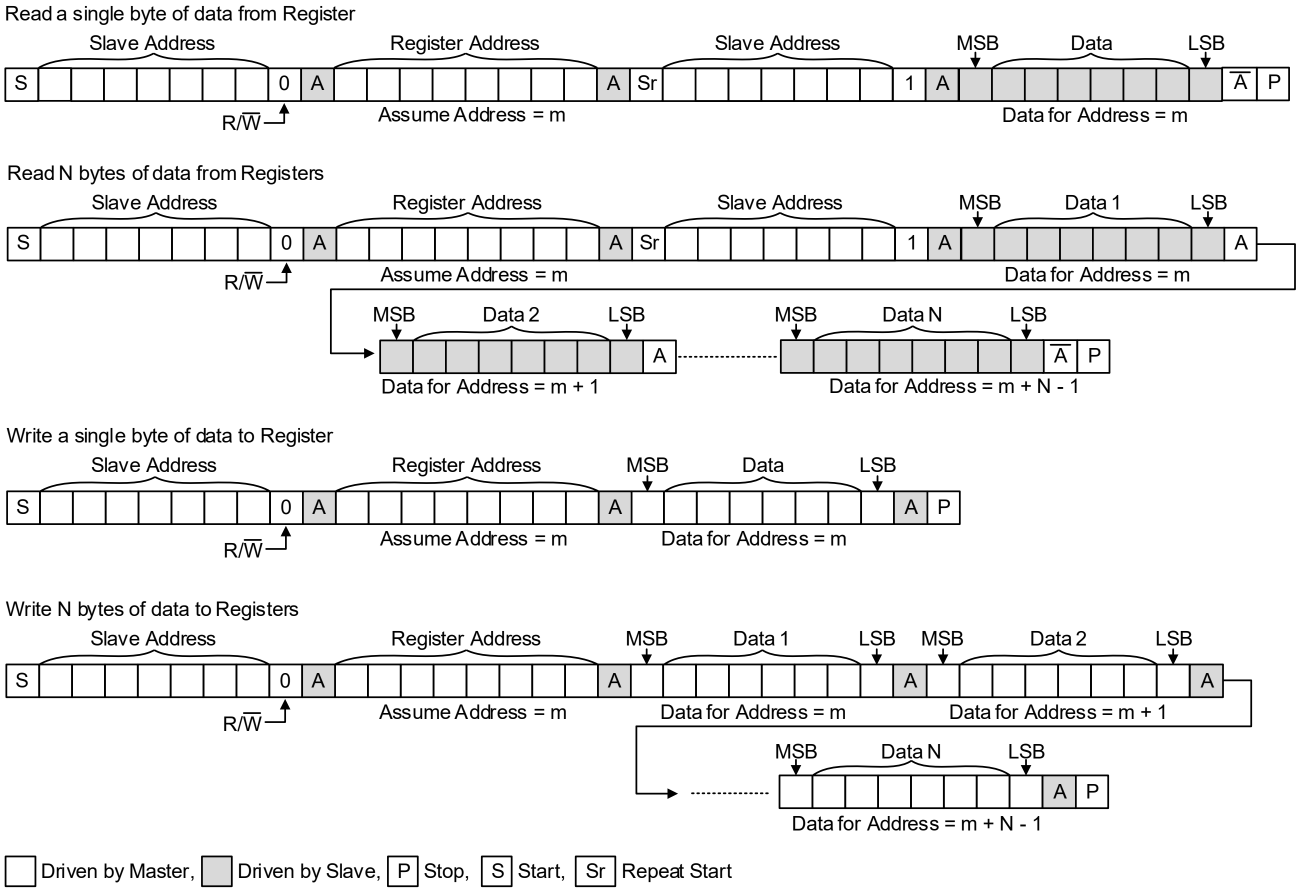


Figure 18. Read and Write Functions

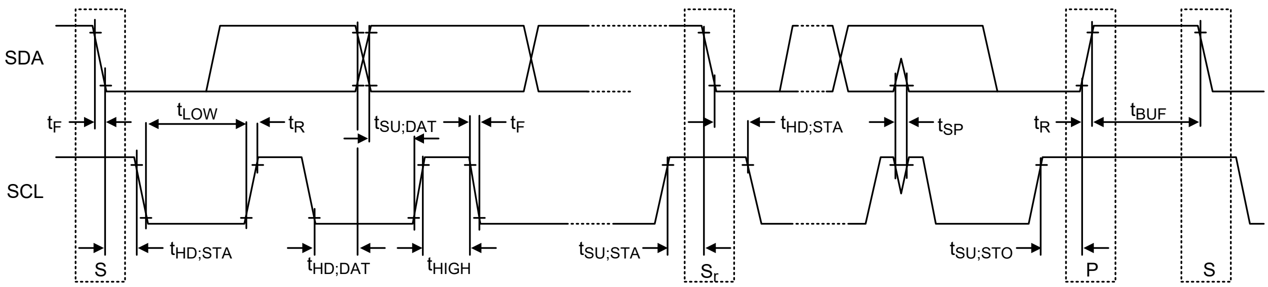


Figure 19. I²C Waveform Information

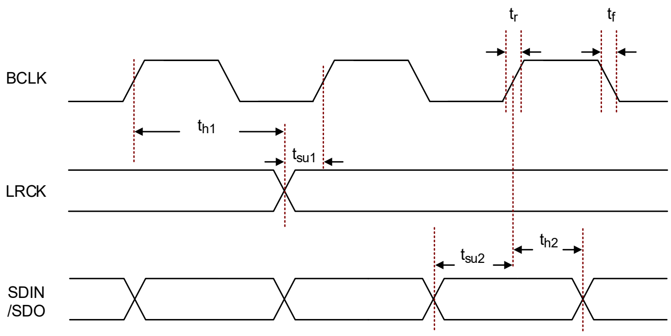


Figure 20. Timing Diagram of Slave Mode I²S Interface

Table 2. Register Map

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x00	2	8	RW	TDM_MONO_SEL	TDM mode: 0: Stereo 1: Mono (default)	1
0x00	2	1:0	RW	CH_SI	I²S channel selection 01: L channel (default) 10: R channel Others: (L+R)/2	01
0x01	2	9	RW	CS_DATA_INV	Current sense data output inversion 0: Normal 1: Inverted (Default)	1
0x01	2	8	RW	VDDIO_SDO_SEL	VDDIO-SDO selection 0: 1.8V, (default) 1: 3.3V	0
0x01	2	7:4	RW	SDO_SEL_L	Left channel data 0000: No output (default) 0001: I²S_DATAI 0010: Interface output 0011: DSP output 0100: DF output 0101: I sense ADC Others: Revered	0000
0x01	2	3:0	RW	SDO_SEL_R	Right channel data 0000: No output (default) 0001: I²S_DATAI 0010: Interface output 0011: DSP output 0100: DF output 0101: I sense ADC Others: Reserved	0000
0x02	2	7	RW	BCLK_EDGE_SEL	0: LRCK transition align with BCLK falling (default) 1: LRCK transition align with BCLK rising	0
0x02	2	6	RW	SDO_EDGE_SEL	I²S data out launch edge selection 0: BCLK_EDGE_SEL=0, launch with falling edge (default) 1: BCLK_EDGE_SEL=0, launch with rising edge	0
0x02	2	5:4	RW	AUD_BITS	00: 16 bits 01: 20 bits 10: 20 bits 11: 24 bits (default)	11
0x02	2	3	RW	TDM_DSP_OFFSET	TDM or DSPM offset selection 0: Without offset (DSPMB) 1: 1 bit clock offset (DSPMA) (default)	1
0x02	2	2:0	RW	AUD_FMT	000: I²S (default) 001: Left Justify 010: Right Justify 011: DSP mode 100: EIAJ Others: TDM mode	000

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x03	2	9	RW	EN_5V_APP	Enable when PVDD = 5V application 0: Disable (default) 1: Enable	0
0x03	2	8	RW	MODU_MODE	Reserved for new feature 0: BTL mode (default) 1: CMH mode	0
0x03	2	6:4	RW	PWM_FREQ	PWM frequency selection 000: 8*fs 001: 10*fs 010: 40*fs 011: 44*fs (default) 100: 48*fs Others: Reserved	011
0x03	2	2:0	RW	SPK_GAIN_SEL	Speaker gain selection 000: -6dB (0.5x) 001: 0dB (1x) 010: 6dB (2x) 011: 12dB (4x) 100: 14dB (5x) 101: 16dB (6.3x) (default) 110: 18dB (8x) 111: Reserved	101
0x04	2	15	WO	SF_RESET	Write 1 to trigger software reset	0
0x04	2	13	RW	EN_DC_LOAD_DET	Execute DC load diagnostics before amp on sequence 0: Disable 1: Enable (default)	1
0x04	2	12	RW	LDET_Operatoin_EN	Real Time Load Detection Mode_EN 0: Disable 1: Enable (default)	1
0x04	2	11:10	RW	ULQM_DCVT	ULQM Mode DCVT Mode 00: Disable 01: DC 10: VT 11: DC+VT (default)	11
0x04	2	8	RW	LDET_Operatoin	Real Time Load Detection Mode 0: CS 1: DCR (default)	1
0x04	2	1:0	RW	CH_STATE	Channel Mode 00: Normal 01: Hi-Z (default) 10: MUTE 11: ULQM	01
0x05	2	2:0	RW	OUT_PHASE	PWM output phase offset 000: 0 (default) 001: 45 010: 90 011: 135 100: 180 101: 225 110: 270 111: 315	000

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x06	2	7	RW	SIL_DET_EN	ULQM detection enable 0: Disable 1: Enable (default)	1
0x06	2	5:4	RW	SIL_TH_SEL	ULQM mode detection threshold (in different AUD_BITS setting) 00: Audio data <= +/- 7 01: Audio data <= +/- 3 10: Audio data <= +/- 1 11: All data zero (default)	11
0x06	2	2:0	RW	SIL_HOLD_TIME	ULQM mode hold time selection 000: 1ms 001: 20ms 010: 40ms (default) 011: 80ms 100: 160ms 101: 320ms 110: 640ms 111: 1.28s	010
0x07	2	7	RW	FSS_EN	Spread spectrum enable 0: Disable (default) 1: Enable	0
0x07	2	6	RW	PWM_MODE WHITE	Noise selection 0: Pink noise (default) 1: White noise	0
0x07	2	5	RW	PWM_SELCOEF	Pink noise coefficient This will affect the noise amplitude for spread spectrum signal, not recommended to modify it. 0: 1/2 (default) 1: 1/4	0
0x07	2	4	RW	PWM_NOISE_EN	Add noise to TRI_GEN 0: Disable (default) 1: Enable	0
0x07	2	3:2	RW	NOISE_AMP	Nosie amplitude for SSC 00: 6.3% (default) 01: 11.7% 10: 17.1% 11: 35.1%	00
0x07	2	1:0	RW	FSS_AMP	Spread spectrum frequency variation amplitude 00: 14.73% 01: 22.5% (default) 10: 22.5% 11: 30.35%	01
0x08	2	9	RW	VTMNT_EN	EN VT-monitor Gating CK_SAMPLE_SAR_ADC & CK_COMP_SAR_ADC 0: Disable 1: Enable (default)	1
0x08	2	8	RW	HPF_EN_ISNS	Digital high-pass filter for I-sense 0: Disable 1: Enable (default)	1
0x08	2	7	RW	ISENSE_EN	I-sense 0: Disable	1

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
					1: Enable (default)	
0x08	2	6	RW	HPF_EN	High-Pass filter enable 0: Disable 1: Enable (default)	1
0x08	2	5	RW	COMP_EN	Compensation filter enable 0: Disable (default) 1: Enable	0
0x08	2	4	RW	DRC_EN	DRC enable 0: Disable (default) 1: Enable	0
0x08	2	3	RW	DRC_N_EN	DRC noise gate enable 0: Disable (default) 1: Enable	0
0x08	2	2	RW	HARD_CLIP_EN	Hard clip enable 0: Disable (default) 1: Enable	0
0x08	2	1	RW	DRE_EN	DRE enable 0: Disable 1: Enable (default)	1
0x08	2	0	RW	MS_MUTE	Mute function 0: Un-mute (default) 1: Master soft mute	0
0x09	2	6	RW	FAULTB_WARNB_EN	FAULTB/ WARNB output status 0: Non-Active 1: Active when fault event and diagnostic(default)	1
0x09	2	5	RW	WARN_B_TYPE	WARNB status 0: Fault status (Recovery type) 1: Interrupt Reg (Latch type) (default)	1
0x09	2	4	RW	FAULT_B_TYPE	FAULTB status 0: Fault status (Recovery type) 1: Interrupt Reg (Latch type) (default)	1
0x09	2	3:0	RW	RCVRY_TIME	Power Stage auto recovery time 0000: 100ms 0001: 150ms 0010: 300ms (default) 0011: 450ms 0100: 600ms 0101: 750ms 0110: 900ms 0111: 1050ms 1000: 1200ms 1001: 1350ms Others: 1500ms	0010
0x0A	2	12:0	RO	PVDD_MNT_CODE	Voltage of PVDD(Volt) = PVDD_MNT_CODE/160	13'h0000
0x0B	2	8:0	RO	TEMP_MNT_CODE	Temperature(K) = Temperature(°C) - 273	9'h000
0x0C	2	3	RW	I2S_FAULT_TYPE	I^2S fault behavior type select. 0: Auto recovery (default) 1: Latch	0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x0C	2	2	RW	OVP_DVDD_TYPE	OVP DVDD fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0C	2	1	RW	UVP_DVDD_TYPE	UVP DVDD fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0C	2	0	RW	UVP_VBAT_TYPE	UVP VBAT fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0D	2	7	RW	OVP_VBAT_TYPE	OVP VBAT fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0D	2	6	RW	UVP_VDDA_TYPE	UVP VDDA fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0D	2	5	RW	UVP_PVDD_TYPE	UVP PVDD fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0D	2	4	RW	OVP_PVDD_TYPE	OVP PVDD fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0D	2	2	RW	OTP_TYPE	OTP fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0D	2	1	RW	OCP_TYPE	OCP fault behavior type select. 0: Auto recovery (default) 1: Latch	0
0x0E	2	15:1	RW	REG_RSV	Reserved Reg	15'h0000
0x0E	2	0	RW	LD_REF_SEL	Manual mode DC/AC load diagnostic clock source selection 0: Reference internal clock (default) 1: Reference BCLK	0
0x0F	2	7:0	RO	ERR_INT_INDEX	Report ERR_INT summary from ERR_INT0 (0x10) ~ ERR_INT7 (0x17)	8'h01
0x10	2	6	W1C	POR	Power-on reset 0: Normal 1: Warning (write 1 to clear) (default)	1
0x10	2	5	W1C	ADS_ERR_2	Address R detection error I^2C_ADDR2 0: R detect correct (default) 1: R detect error (write 1 to clear)	0
0x10	2	4	W1C	ADS_ERR_1	Address R detection error I^2C_ADDR1 0: R detect correct (default) 1: R detect error (write 1 to clear)	0
0x10	2	3	W1C	PWM_ERR	PWM frequency setting error under sampling rate 0: PWM is supported (default) 1: PWM is non-supported (write 1 to clear)	0
0x10	2	2	W1C	PLL_UNLOCK	0: No PLL unlock error (default) 1: PLL Unlock error (write 1 to clear)	0
0x10	2	1	W1C	BCLK_ERR	0: No BCLK error (default) 1: BCLK error (write 1 to clear flag)	0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x10	2	0	W1C	LRCK_ERR	0: No LRCK clock error (default) 1: LRCK clock error (write 1 to clear)	0
0x11	2	7	W1C	VDDA_UV	VDDA UVP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x11	2	5	W1C	DVDD_OV	DVDD OVP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x11	2	4	W1C	DVDD_UV	DVDD UVP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x11	2	3	W1C	VBAT_UV	VBAT UVP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x11	2	2	W1C	VBAT_OV	VBAT OVP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x11	2	1	W1C	OTP	OTP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x11	2	0	W1C	OTW	OT warning 0: Normal (default) 1: Warning (write 1 to clear)	0
0x12	2	6	W1C	PVDD_UV	PVDD UVP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x12	2	4	W1C	PVDD_OV	PVDD OVP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x12	2	0	W1C	DCP	Output DC detected flag 0: Normal (default) 1: fault (write 1 to clear)	0
0x13	2	0	W1C	OCP	Channel OCP 0: Normal (default) 1: Fault (write 1 to clear)	0
0x15	2	4	W1C	CLIP	Clip detection 0: Normal (default) 1: Warning (write 1 to clear)	0
0x15	2	0	W1C	IWARN	Overcurrent warning flag 0: Normal (default) 1: Warning (write 1 to clear)	0
0x16	2	4	W1C	LDET_OPEN	LDET open error flag 0: Normal (default) 1: Open is triggered (write 1 to clear)	0
0x16	2	0	W1C	LDET_SHORT	LDET short error flag 0: Normal (default) 1: Current error is triggered (write 1 to clear)	0
0x17	2	12	W1C	S2P	Output short to power 0: Normal (default) 1: Warning (write 1 to clear)	0
0x17	2	8	W1C	S2G	Output short to ground 0: Normal (default) 1: Warning (write 1 to clear)	0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x17	2	4	W1C	OL	Output open load 0: Normal (default) 1: Warning (write 1 to clear)	0
0x20	2	3	RW	MASK_PWM_ERR	Fault mask for PWM setting error 0: Not mask (default) 1: Mask	0
0x20	2	2	RW	MASK_PLL_FAULT	Fault mask for PLL unlock error 0: Not mask (default) 1: Mask	0
0x20	2	0	RW	MASK_I2S_FAULT	Fault mask for BCLK/LRCK error 0: Not mask (default) 1: Mask	0
0x21	2	7	RW	MASK_UV_VDDA	Fault mask for VDDA UV 0: Not mask (default) 1: Mask	0
0x21	2	5	RW	MASK_OV_DVDD	Fault mask for DVDD OV 0: Not mask (default) 1: Mask	0
0x21	2	4	RW	MASK_UV_DVDD	Fault mask for DVDD UV 0: Not mask (default) 1: Mask	0
0x21	2	3	RW	MASK_UV_VBAT	Fault mask for VBAT UV 0: Not mask (default) 1: Mask	0
0x21	2	2	RW	MASK_OV_VBAT	Fault mask for VBAT OV 0: Not mask 1: Mask (default)	1
0x21	2	1	RW	MASK_OTP	Fault mask for OTP 0: Not mask (default) 1: Mask	0
0x21	2	0	RW	MASK_OTW	Fault mask for OTW 0: Not mask (default) 1: Mask	0
0x22	2	6	RW	MASK_UV_PVDD	Fault mask for PVDD UV 0: Not mask (default) 1: Mask	0
0x22	2	4	RW	MASK_OV_PVDD	Fault mask for PVDD OV 0: Not mask (default) 1: Mask	0
0x22	2	0	RW	MASK_DCP	Fault mask for DCP 0: Not mask (default) 1: Mask	0
0x23	2	0	RW	MASK_OCP	Fault mask for OCP 0: Not mask (default) 1: Mask	0
0x25	2	4	RW	MASK_CLIP	Fault mask for chip detection 0: Not mask (default) 1: Mask	0
0x25	2	0	RW	MASK_IWARN	Fault mask for current limit 0: Not mask (default) 1: Mask	0
0x26	2	4	RW	MASK_LDET_OPEN	Fault mask for LDET OPEN 0: Not mask (default) 1: Mask	0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x26	2	0	RW	MASK_LDET_SHORT	Fault mask for LDET SHORT 0: Not mask 1: Mask (default)	1
0x27	2	12	RW	MASK_S2P	Fault mask for S2P 0: Not mask (default) 1: Mask	0
0x27	2	8	RW	MASK_S2G	Fault mask for S2G 0: Not mask (default) 1: Mask	0
0x27	2	4	RW	MASK_OL	Fault mask for OL 0: Not mask (default) 1: Mask	0
0x30	2	3	RW	I2C_TIMEOUT_TIME_SEL	I^2C timeout timing selection 0: 100ms (default) 1: 150ms	0
0x30	2	2	RW	I2C_TIMEOUT_TYPE_SEL	I^2C timeout check pin type 0: SCL & SDAO both keep low start timeout counting 1: SDAO keep low start timeout counting (default)	1
0x30	2	1	RW	I2C_TIME_OUT_SEL	I^2C timeout reset selection 0: Reset I^2C IP only (default) 1: Reset whole chip	0
0x30	2	0	RW	I2C_TIME_OUT_EN	I^2C timeout function: If SDA&SCL keep low 100ms, I^2C timeout reset occur. 0: Disable 1: Enable (default)	1
0x31	2	7	RO	PWM_STATUS	PWM status 0: Sampling rate vs. PWM frequency is supported (default) 1: Sampling rate vs. PWM frequency is non-supported	0
0x31	2	6:4	RW	SR_MODE	Sampling rate (manual setting or report) If auto sampling rate detection, SR_MODE reports detection result. 100: 32KHz 101: 44.1/48KHz (default) 110: 88.2/96KHz Others: Reserved	101
0x31	2	3:0	RW	BCLK_MODE	BCLK mode report 0000: BCLK=32fs 0001: BCLK=48fs 0010: BCLK=64fs (default) 0011: BCLK=96fs 0100: BCLK=128fs 0101: BCLK=192fs 0110: BCLK=256fs 0111: BCLK=384fs (not support 96K-SR) 1000: BCLK=512fs (not support 96K-SR) Others: Reserved	0010
0x32	2	5:0	RW	TDM_TX_LOC_CH1	TDM start transmitting location select for CH1 000000: Start from 0+offset (default) 000001: Start from 8+offset …	000000

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
					111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	
0x33	2	5:0	RW	TDM_TX_LOC_CH2	TDM start transmitting location select for CH2 000000: Start from 0+offset 000001: Start from 8+offset … 000100: Start from 32+offset (default) … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	000100
0x34	2	5:0	RW	TDM_RX_LOC_CH1	TDM start receiving location select for CH1 000000: Start from 0+offset (default) 000001: Start from 8+offset … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	000000
0x35	2	5:0	RW	TDM_RX_LOC_CH2	TDM start receiving location select for CH2 000000: Start from 0+offset 000001: Start from 8+offset … 000100: Start from 32+offset (default) … 111100: Start from 480+offest 111101: Start from 488+offset 111110: Not available 111111: Not available	000100
0x36	2	6	RW	DRC_IN_SEL	DRC Static Curve input selection 0: Audio input 1: DCR calibration result (default)	1
0x36	2	5	RW	DRC_PEAK	DRC mode selection 0: RMS Mode 1: Peak Mode (default)	1
0x36	2	4	RW	DRC_GAIN_HYS_EN	DRC gain hysteresis enable 0: Disable, 1: Enable (default) Gain release condition is gain difference >= 0.125 dB	1
0x36	2	2	RW	VTMNT_CLK_SEL	0: t=1/96k/32 1: t=1/48k/32 (default) 96k/48k is sampling rate (LRCK)	1
0x36	2	1:0	RW	VTMNT_AVG_SEL	00: avg*1 (default) 01: avg*2 10: avg*4 11: avg*8	00
0x37	2	7	RW	SKIP_RAMP	Skip volume ramp 0: Disable (default) 1: Enable	0

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x37	2	6	RW	FAST_RAMP_MUTE	Mute pin fast mute, mute time < 1ms 0: Normal ramp time (default) 1: Fast mute time	0
0x37	2	5	RW	MUTE_MODE	Mute pin behavior 0: Mute only (default) 1: Enter ULQM	0
0x37	2	1:0	RW	VOL_RAMP_MODE	Volume slew step control 00: 4.33ms from mute to 0dB (0.5dB/20.83us) 01: 8.66ms from mute to 0dB (0.25dB/20.83us) 10: 17.33ms from mute to 0dB (0.125dB/20.83us) 11: 34.65ms from mute to 0dB (0.0625dB/20.83us) (default)	11
0x38	2	10:0	RW	VOL	Volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: Mute 0.0625dB per step	11'h180
0x39	2	10:0	RW	HC_TH	Hard clip threshold when HARD_CLIP_EN=1 11'h18D: –0.8125dB (default) 0.0625db per step	11'h18D
0x3A	2	10:0	RW	DRC_TH	DRC threshold 11'h000: 0dB (default) 11'h180: –24dB 11'h67E: –103.875dB 11'h67F~11'h7FF: not available 0.0625dB per step	11'h000
0x3B	2	10:0	RW	DRC_OFFSET	DRC make up gain (Offset) 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: –103.9375dB 0.0625dB per step	11'h180
0x3C	2	7:0	RW	DRC_RATIO	DRC compress ratio 8'h00: No compression 8'h80 (default) ~8'hFF: Full compression 1/128 per step	8'h80
0x3D	2	10:0	RW	DRC_NG_TH	Noise gate threshold 11'h000: 0dB 11'h180: –24dB 11'h640: –100dB (default) 1'h67E: –103.875dB 11'h67F~11'h7FF: not available 0.0625dB per step	11'h640
0x40	4	16:0	RW	DRC_AE	DRC_AE	17'h08000
0x41	4	16:0	RW	DRC_1_AE	DRC_1_AE	17'h00000
0x42	4	16:0	RW	DRC_AA	DRC_AA	17'h08000
0x43	4	16:0	RW	DRC_AD	DRC_AD	17'h08000

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
0x44	4	16:0	RW	COMP_B0	Compensation filter coefficient B0	17'h08000
0x45	4	16:0	RW	COMP_B1	Compensation filter coefficient B1	17'h00000
0x46	4	16:0	RW	COMP_B2	Compensation filter coefficient B2	17'h00000
0x47	4	16:0	RW	COMP_B3	Compensation filter coefficient B3	17'h00000
0x48	2	7:0	RW	PILOT_FREQ	W0 = (2*pi*fpil/fs)*2^15, Default = 10Hz	8'h2A
0x49	2	10:0	RW	PILOT_GAIN	Gain = (24 - pilot_gain/16)dB 11'h0400: -40dB (default)	11'h400
0x4A	2	7:0	RW	DCR_EST_MU	4.4 format, Mu = x/2^4, Default = 0.75	8'h0C
0x4B	2	7:0	RW	DCR_OPEN_TH	Open_TH = X/2^12, Default = 4mA, LSB = 0.25mA	8'h10
0x4C	2	11:0	RW	DCR_SHORT_TH	S(2.10) Short_TH = X/2^10, Default = 0.02V	12'h018
0x4D	2	13:0	RW	DCR_INIT	Init_dcr = x/2^9, Default = 4ohm	14'h0800
0x4E	2	13:0	RW	Dmg_DCR	Dmg_dcr = x/2^9, Default = 31.99ohm	14'hFFFF
0x4F	2	13:0	RO	DCR_RPT	DCR calculation result = x/2^9, Default = 4ohm	14'h0800
0x50	2	8	RW	S2P_TH	S2P threshold selection 0: 200Ω 1: 400Ω (default)	1
0x50	2	7:6	RW	S2G_TH	S2G threshold selection 00: 200Ω (default) 01: 400Ω 10: 800Ω 11: 1.2kΩ	00
0x50	2	5:4	RW	OL_TH	OL threshold selection 00: 50 Ω (default) 01: 100 Ω 10: 200 Ω 11: 400 Ω	00
0x51	2	4	RW	EN_DC_DET	DC load detection enable 0: disable (default) 1: enable	0
0x51	2	0	RO	DC_DET_DONE	DC detection done flag after enabling DC load detection 0: DC load detection not execute or not finish (default) 1: DC load detection finish	0
0x52	2	4:0	RW	AC_PHI	Generated signal frequency: 00000: no signal 00001: set 1 = 1kHz 00010: set 2 = 2kHz …	10011

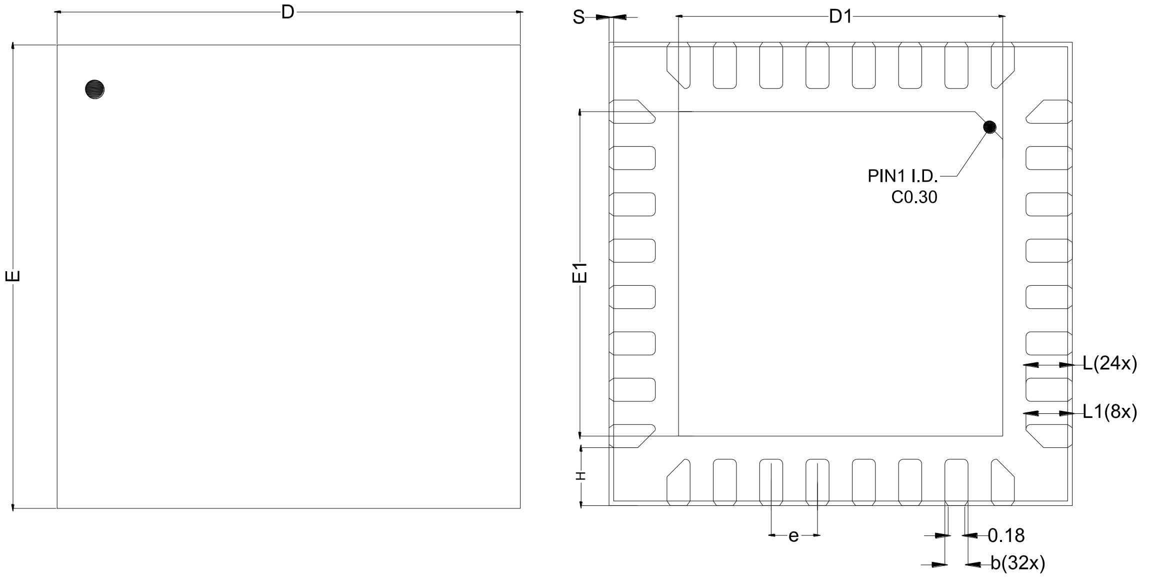
ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
					10011: set 19 = 19kHz (default) Others: Reserved	
0x53	2	4	RW	EN_AC_DET	AC load detection enable 0: Disable (default) 1: Enable	0
0x53	2	0	RO	AC_DET_DONE	AC detection done flag after enabling AC load detection 0: AC_PHASE_R and AC_PHASE_I keep the last result if ever enabling detection (default) 1: AC_PHASE_R and AC_PHASE_I is valid	0
0x54	2	15:0	RO	AC_MAG	Report magnitude	16'h0000
0x55	2	15:0	RO	AC_PHA	Report phase	16'h0000
0x56	2	15:0	RO	AC_SPK_R	Report the real part of speaker phase	16'h0000
0x57	2	15:0	RO	AC_SPK_I	Report the imaginary part of speaker phase	16'h0000
0x58	2	8	RW	LDET_OPEN_EN	Real time load detection OPEN_EN 0: Disable 1: Enable (default)	1
0x58	2	7	RW	LDET_SHORT_EN	Real time load detection SHORT_EN 0: Disable (default) 1: Enable	0
0x58	2	6	RW	EN_OTP	Channel OT protection enable 0: Disable 1: Enable (default)	1
0x58	2	5	RW	EN_OTW	Channel OT warning enable 0: Disable 1: Enable (default)	1
0x58	2	4	RW	EN_UVOVOT	Enable UV/OV/OT 0: Disable 1: Enable (default)	1
0x58	2	3	RW	EN_IWARN	Enable overcurrent warning function 0: Disable 1: Enable (default)	1
0x58	2	2	RW	EN_DC_PROT	DC protection enable 0: Disable 1: Enable (default)	1
0x58	2	1	RW	EN_CLIP_DET	Clip detection enable 0: Disable (default) 1: Enable	0
0x59	2	13:12	RW	OC_RCVRY_TIME	DCR OC auto recovery time 00: 50ms 01: 150ms 10: 300ms (default) 11: 450ms	10
0x59	2	11:10	RW	OPEN_DET_TIME	DCR open detection time 00: 25ms 01: 50ms (default)	01

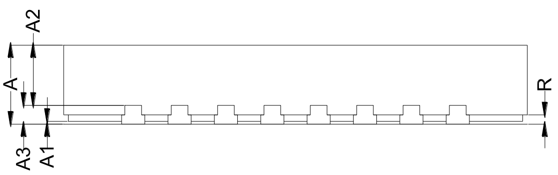
ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
					10: 125ms 11: 250ms	
0x59	2	9:8	RW	CURRENT_ERR_RCVRY_TIME	DCR current error auto recovery time 00: 50ms 01: 150ms (default) 10: 300ms 11: 450ms	01
0x5A	2	6	RW	DVDD_UV_CTRL_SEL	DVDD UV protection behavior 0: Mute discharge time then HZ_PROT (default) 1: Fast ramp mute to off sequence	0
0x5A	2	5	RW	PVDD_VBAT_UV_CTRL_SEL	PVDD VBAT UV protection behavior 0: Mute discharge time then HZ_PROT (default) 1: Fast ramp mute to off sequence	0
0x5A	2	4	RW	OV_CTRL_SEL	DVDD PVDD VBAT protection behavior 0: Mute discharge time then HZ_PROT (default) 1: HZ_PROT directly	0
0x5A	2	2	RW	EN_OTW_TFB	Enable thermal fold-back 0: Disable (default) 1: Enable	0
0x5A	2	0	RW	EN_CLIP_AGC	Enable auto gain control for CLIP detection 0: Disable (default) 1: Enable	0
0x5B	2	7:6	RW	TFB_ATTACK_RATE	Thermal foldback attack rate 00: 0.0625dB/25ms (default) 01: 0.0625dB/50ms 10: 0.0625dB/100ms 11: 0.0625dB/200ms	00
0x5B	2	5:4	RW	TFB_RELEASE_RATE	Thermal foldback release rate 00: 0.0625dB/50ms (default) 01: 0.0625dB/100ms 10: 0.0625dB/200ms 11: 0.0625dB/400ms	00
0x5B	2	3:2	RW	AGC_ATTACK_RATE	AGC attack time selection for clip AGC 00: 0.25dB/20us 01: 0.25dB/40us (default) 10: 0.25dB/80us 11: 0.25dB/160us	01
0x5B	2	1:0	RW	AGC_RELEASE_RATE	AGC release time selection for clip AGC 00: 0.25dB/200ms 01: 0.25dB/400ms (default) 10: 0.25dB/800ms 11: 0.25dB/1600ms	01
0x5C	2	15:14	RW	OV_DVDD_SEL	OV threshold selection of DVDD 00: 18.8V 01: 19.5V (default) 10: 20V 11: Reserved	01
0x5C	2	13:12	RW	OV_VBAT_SEL	OV threshold selection of VBAT 00: 18.8V 01: 19.5V (default)	01

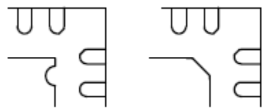
ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
					10: 20V 11: Reserved	
0x5C	2	11:10	RW	OV_PVDD_SEL	OV threshold selection of PVDD 00: 18.8V 01: 19.5V (default) 10: 20V 11: Reserved	01
0x5C	2	9:8	RW	UV_DVDD_SEL	UV threshold selection of DVDD 00: 1.4V (default) 01: 2.8V 10: 3.8V 11: Reserved	00
0x5C	2	5:4	RW	UV_VBAT_SEL	UV threshold selection of VBAT 00: 4V (default) 01: 6V 10: 7V 11: 9.1V	00
0x5C	2	1:0	RW	UV_PVDD_SEL	UV threshold selection of PVDD 00: 4V (default) 01: 6V 10: 7V 11: 9.1V	00
0x5D	2	5:4	RW	OTP_SEL	Channel OTP threshold selection 00: 160C 01: 170C (default) Others: Reserved	01
0x5D	2	3:0	RW	CLIP_DET_SEL	Clip detect threshold, release threshold (unit: PWM cycle) 0000: 1, 0 0001: 5, 3 0010: 10, 5 0011: 20, 5 (default) Others: Reserved	0011
0x60	2	0	RW	IWARN_SEL	Overcurrent warning threshold selection 0: 2.5A 1: 3A (default)	1
0x61	2	2	RW	DC_TIME_SEL	DC Detection time 0: 342ms (default) 1: 684ms	0
0x61	2	1:0	RW	DC_TH	DC threshold for DC detection 00: No available 01: 12.5% (default) 10: 18.75% 11: 25%	01
0x62	2	7:4	RW	DRE_RAMP_TIME	Exit DRE gain ramp time selection ramp time = (DRE_RAMP_TIME+1)/1536KHz 0000: 0.651us 0001: 1.302us 0010: 1.953us 0011: 2.604us 0100: 3.255us (default) 0101: 3.906us 0110: 4.557us	0100

ADDR	Byte Number	BITS	R/W	Reg Name	Description	Default
					0111: 5.208us 1000: 5.859us 1001: 6.510us 1010: 7.161us 1011: 7.812us 1100: 8.463us 1101: 9.114us 1110: 9.765us 1111: 10.416us	
0x62	2	3	RW	DRE_EXIT_RAMP_EN	Exit DRE ramp enable bit 0: Disable 1: Enable (default)	1
0x62	2	2	RW	DRE_ENTRY_RAMP_EN	Entry DRE ramp enable bit 0: Disable (default) 1: Enable	0
0x62	2	1:0	RW	DRE_HOLD_TIME	Hold time before enter DRE 00: 16ms 01: 32ms 10: 64ms (default) 11: 128ms	10
0x63	2	7:0	RW	DRE_TH	Threshold of digital input for changing D_DRE DRE threshold = 20 * log10 (TH_DRE / 2^11) + 2	8'h02
0x64	2	1:0	RW	DRE_MNT_SEL	DRE monitor data for compare threshold selection 00: Before Digital Filter (default) 01: After Digital Filter 1x: Max (before DF, after DF)	00
0x65	2	7:0	RW	DIG_DELAY_ENTRY	Digital path delay when dre_en rising (DIG_DELAY_RISING / PLL Freq.)	8'h00
0x66	2	7:0	RW	DIG_DELAY_EXIT	Digital path delay when dre_en falling (DIG_DELAY_FALLING / PLL Freq.)	8'h00
0x67	2	7:0	RW	ANA_DELAY_ENTRY	Analog path delay when dre_en rising (ANA_DELAY_RISING / PLL Freq.)	8'hF6
0x68	2	7:0	RW	ANA_DELAY_EXIT	Analog path delay when dre_en falling (ANA_DELAY_FALLING / PLL Freq.)	8'hF6

18 Outline Dimension







DETAILA

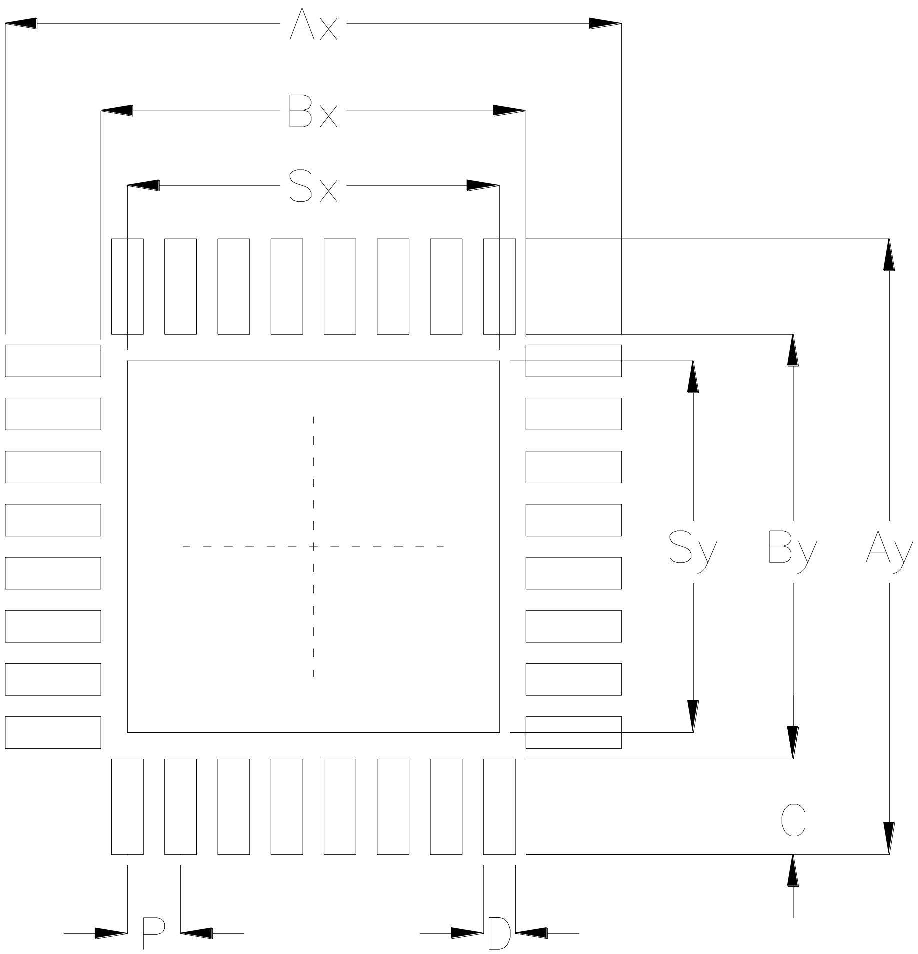
Pin #1 ID and Tie Bar Mark Options

Note: The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A2	0.600	0.700	0.024	0.028
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	4.950	5.050	0.195	0.199
D1	3.450	3.550	0.136	0.140
E	4.950	5.050	0.195	0.199
E1	3.450	3.550	0.136	0.140
e	0.500		0.020	
L	0.450	0.550	0.018	0.022
L1	0.400	0.550	0.016	0.022
R	0.050	0.150	0.002	0.006
S	0.001	0.090	0.000	0.004
H	0.625		0.025	

WET V-Type 32L QFN 5x5 Package

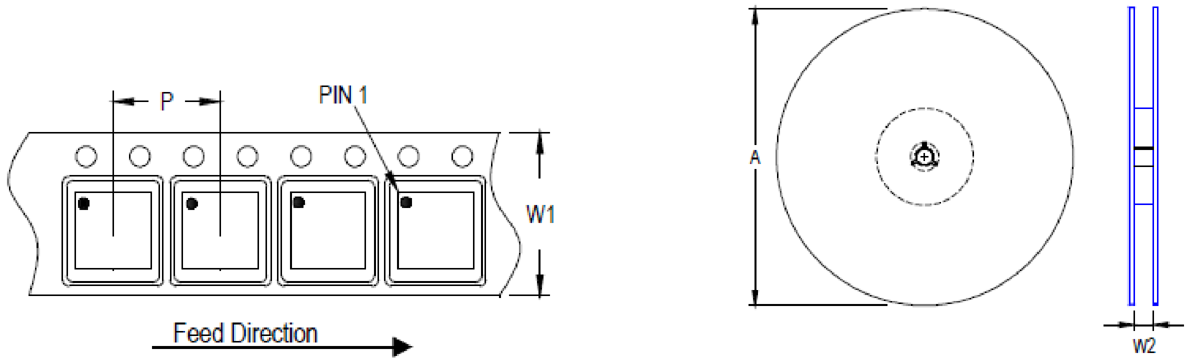
19 Footprint Information

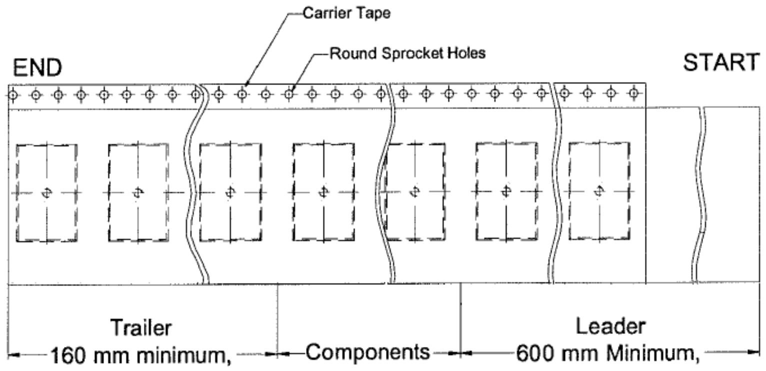


Package	Number of Pins	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
WET-VQFN5x5-32	32	0.50	5.80	5.80	4.00	4.00	0.90	0.30	3.50	3.50	±0.05

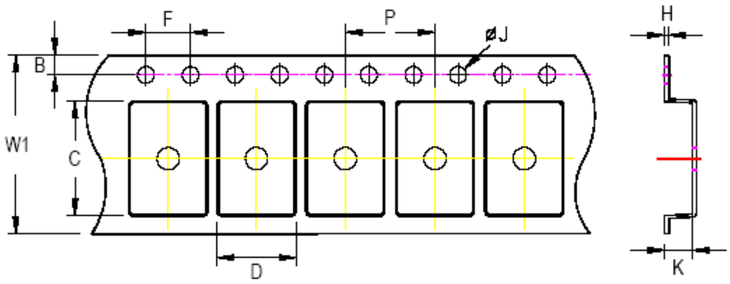
20 Packing Information

20.1 Tape and Reel Data





Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 5x5	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN/DFN 5x5	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description
00	2026/2/12	First Edition