

## 3A High Performance Step-Up DC-DC Converter

### General Description

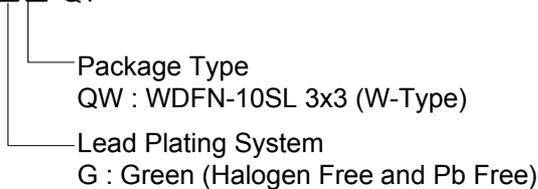
The RTQ9297-QT includes a high performance step-up DC-DC converter that provides a regulated supply voltage for active-matrix thin-film transistor (TFT) liquid-crystal displays (LCDs).

The Boost Converter incorporates current mode, fixed-frequency, pulse-width modulation (PWM) circuitry with a built-in N-Channel power MOSFET to achieve high efficiency and fast transient response.

The RTQ9297-QT is available in a WDFN -10SL 3x3 package.

### Ordering Information

RTQ9297□□-QT

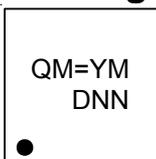


Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

### Marking Information



QM= : Product Code  
YMDNN : Date Code

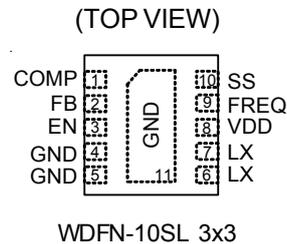
### Features

- High Efficiency Up to 90%
- Adjustable Output Voltage :  $V_{DD}$  to 24V
- Wide Input Supply Voltage : 2.6V to 5.5V
- Input Under Voltage Lockout
- Pin-Programmable Switching Frequency 640kHz/1.2MHz
- Programmable Soft-Start
- AEC-Q100 Grade 2 Qualified
- Small 10S-Lead WDFN Package
- RoHS Compliant and Halogen Free

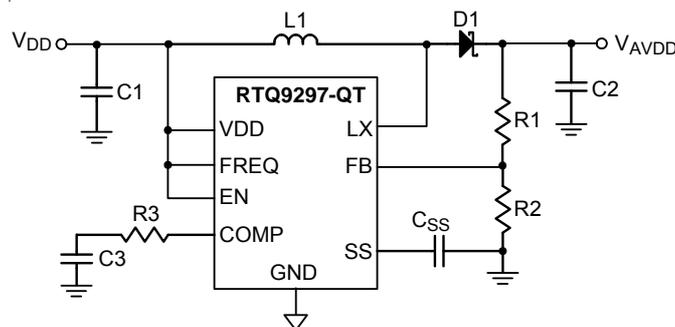
### Applications

- Notebook Computer Displays
- LCD Monitor Panels
- LCD TV Panels

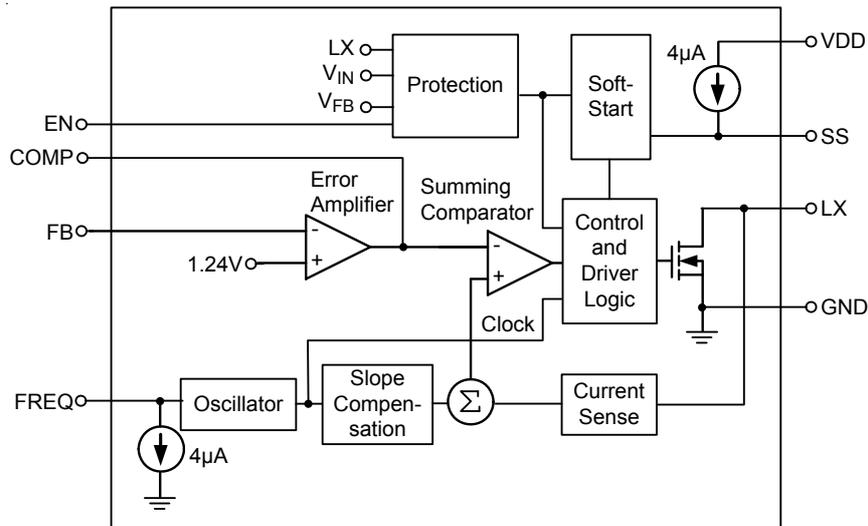
### Pin Configuration



### Simplified Application Circuit



## Functional Block Diagram



## Operation

The RTQ9297-QT includes a high performance step-up DC-DC converter that provides a regulated supply voltage for active-matrix thin-film transistor (TFT) liquid-crystal displays (LCDs).

The Boost Converter covering a wide  $V_{IN}$  range from 2.6V to 5.5V. It performs high efficiency and fast transient responses to generate source driver supplies for TFT LCD display. The converter uses a current mode, pulse width modulation (PWM) topology with a built in N-MOSFET to achieve high efficiency and fast transient response in TFT-LCD applications. The output voltage can be adjusted by setting the resistive voltage-divider sensing at the FB pin. The error amplifier varies the COMP voltage by sensing the FB pin to regulate the output voltage.

**Functional Pin Description**

Pin No.	Pin Name	Pin Function
1	COMP	Compensation Pin for Error Amplifier. Connect a series RC from COMP to ground.
2	FB	Feedback. The feedback regulation voltage is 1.24V nominal. Connect an external resistive voltage-divider between the step-up regulator's output (VAVDD) and GND, with the center tap connected to FB. Place the divider close to the IC and minimize the trace area to reduce noise coupling.
3	EN	Enable Control Input. Drive EN low to turn off the Boost Converter.
4, 5 11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6, 7	LX	Switch. LX is the drain of the internal MOSFET. Connect the inductor/rectifier diode junction to LX and minimize the trace area for lower EMI.
8	VDD	Supply Pin. Bypass VDD with a minimum 1 $\mu$ F ceramic capacitor directly to GND.
9	FREQ	Frequency-Select Input. When FREQ is low, the oscillator frequency will be set to 640kHz. When FREQ is high, the frequency will be set to 1.2MHz. This input has a 6 $\mu$ A pull-down current.
10	SS	Soft-Start Control. Connect a soft-start capacitor (C <sub>SS</sub> ) to this pin. A 4 $\mu$ A constant current charges the soft-start capacitor. When EN connected to GND, the soft-start capacitor is discharged. When EN connected to VDD high, the soft-start capacitor is charged to VDD. Leave floating for not using soft-start.

## Absolute Maximum Ratings (Note 1)

- LX to GND ----- -0.3V to 26V
- LX to GND AC pulse ----- -5V/100ns
- Other Pins to GND ----- -0.3V to 6V
- Power Dissipation,  $P_D$  @  $T_A = 25^\circ\text{C}$ 
  - WDFN-10SL 3x3 ----- 3.27W
- Package Thermal Resistance (Note 2)
  - WDFN-10SL 3x3,  $\theta_{JA}$  ----- 30.5°C/W
  - WDFN-10SL 3x3,  $\theta_{JC}$  ----- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model), LX Pin ----- 1.75kV
  - HBM (Human Body Model), Other Pins ----- 2kV
  - MM (Machine Model) ----- 200V

## Recommended Operating Conditions (Note 4)

- Supply Input Voltage,  $V_{DD}$  ----- 2.6V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 105°C

## Electrical Characteristics

( $V_{DD} = 3.3V$ ,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Supply Current</b>						
Input Voltage Range	$V_{DD}$	$V_{AVDD} < 18V$	2.6	--	5.5	V
		$18V < V_{AVDD} < 24V$	4	--	5.5	
Output Voltage Range	$V_{AVDD}$		$V_{DD}$	--	24	V
Under-Voltage Lockout Threshold	$V_{UVLO}$	$V_{DD}$ rising	2.17	2.4	2.55	V
		Hysteresis	--	50	240	mV
Quiescent Current	$I_Q$	$V_{FB} = 1.3V$ , LX not switching	--	0.5	0.8	mA
		$V_{FB} = 1V$ , LX switching	--	4	8	
Shutdown Current	$I_{SHDN}$	$EN = GND$ , $V_{IN} = 5V$	--	0.1	10	$\mu\text{A}$
<b>Oscillator</b>						
Oscillator Frequency	$f_{OSC}$	FREQ = GND	450	640	800	kHz
		FREQ = $V_{IN}$	900	1240	1500	
Maximum Duty Cycle			87	90	95	%
<b>Error Amplifier</b>						
Feedback Regulation Voltage	$V_{FB}$	$T_A = 25^\circ\text{C}$	1.22	1.24	1.26	V
		$T_A = \text{full range}$	-3	--	2	%
Feedback Input Bias Current	$I_{FB}$		--	125	250	nA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Line Regulation			--	0.05	0.2	%/V
Transconductance	gm	$\Delta I = \pm 2.5\mu A$ at COMP = 1V	20	100	170	$\mu A/V$
<b>N-MOSFET</b>						
Current Limit	ILIM	TA = 25°C	3	3.8	5	A
		TA = full range	2	3.8	7	
On-Resistance	RDS(ON)		--	125	250	mΩ
Leakage Current	ILEAK	VLX = 24V, TA = 25°C	--	30	45	$\mu A$
		VLX = 24V, TA = full range	--	--	200	
<b>Soft-Start</b>						
Charge Current	ISS		2.8	4	8	$\mu A$
<b>Control Inputs</b>						
EN, FREQ Input Low Voltage	VIL		--	--	0.2 x VDD	V
EN, FREQ Input High Voltage	VIH		0.8 x VDD	--	--	V
EN, FREQ Input Hysteresis			0.01	--	0.32	V
FREQ Pull-down Current			1	6	16	$\mu A$
EN Input Current	IEN	EN = 5V	--	0.001	1	$\mu A$

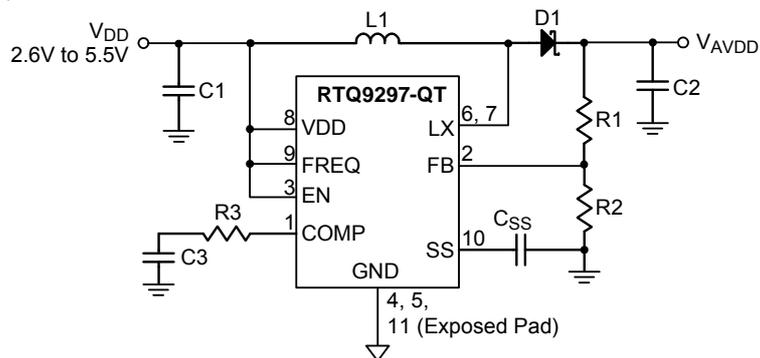
**Note 1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.**  $\theta_{JA}$  is measured at TA = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.  $\theta_{JC}$  is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

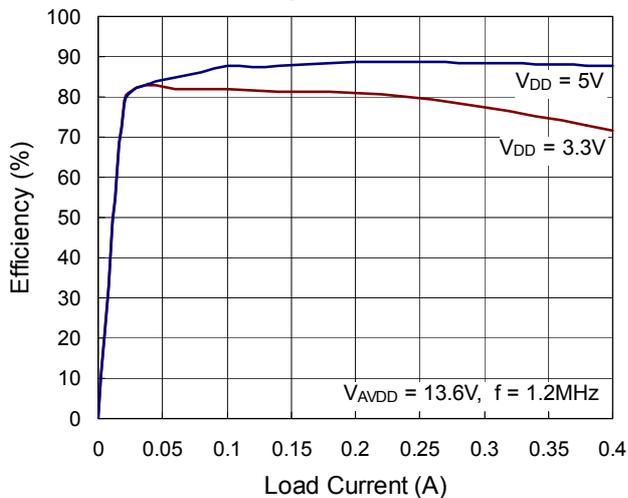
**Note 4.** The device is not guaranteed to function outside its operating conditions.

## Typical Application Circuit

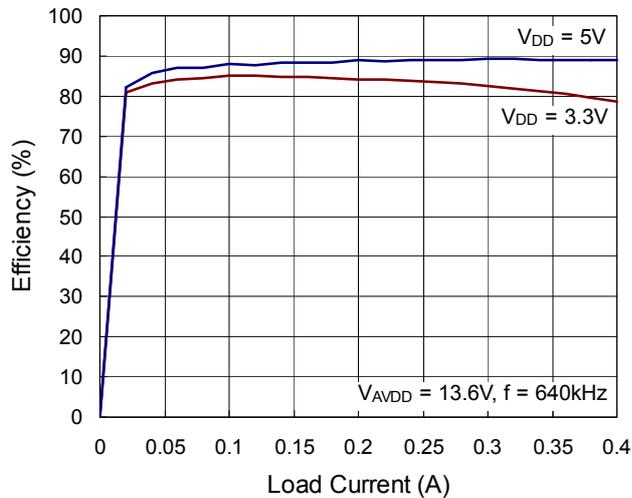


Typical Operating Characteristics

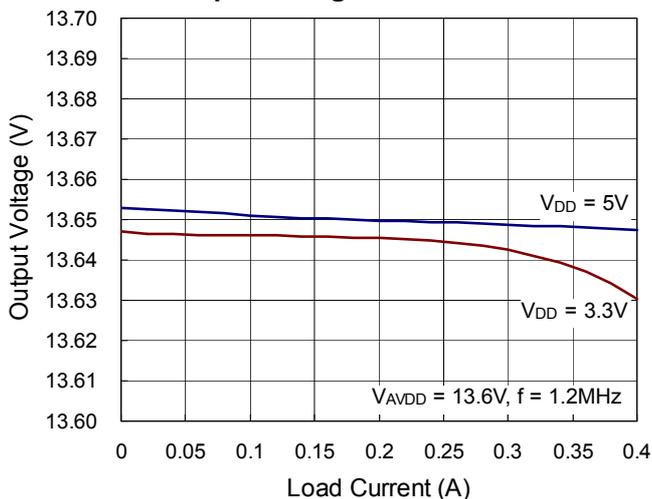
Efficiency vs. Load Current



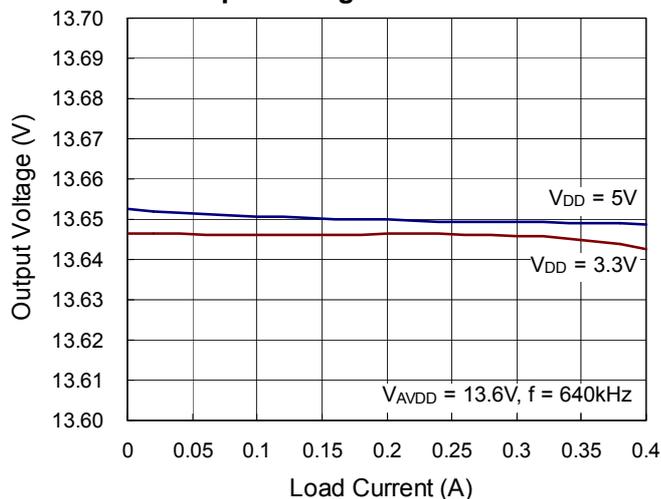
Efficiency vs. Load Current



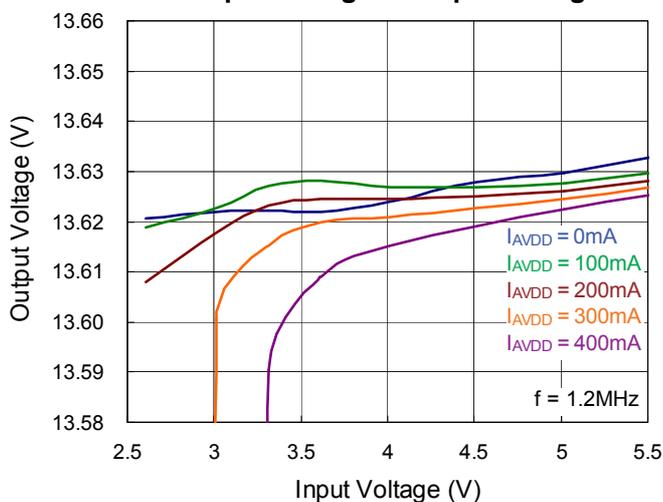
Output Voltage vs. Load Current



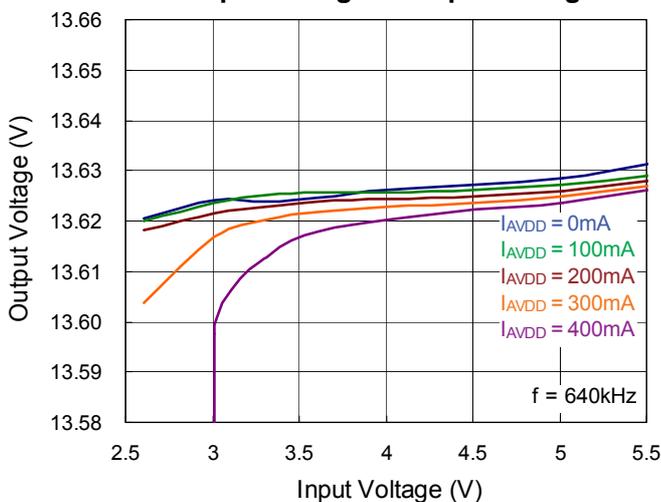
Output Voltage vs. Load Current

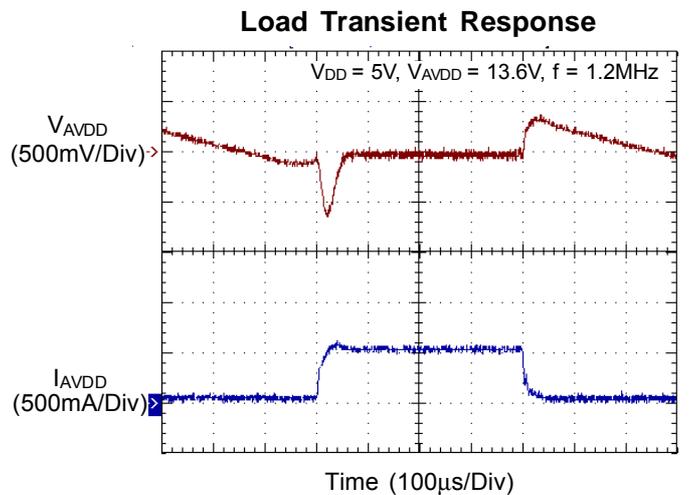
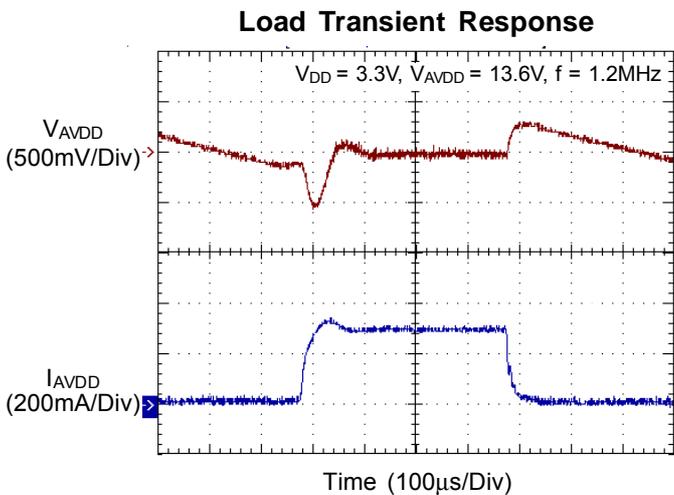
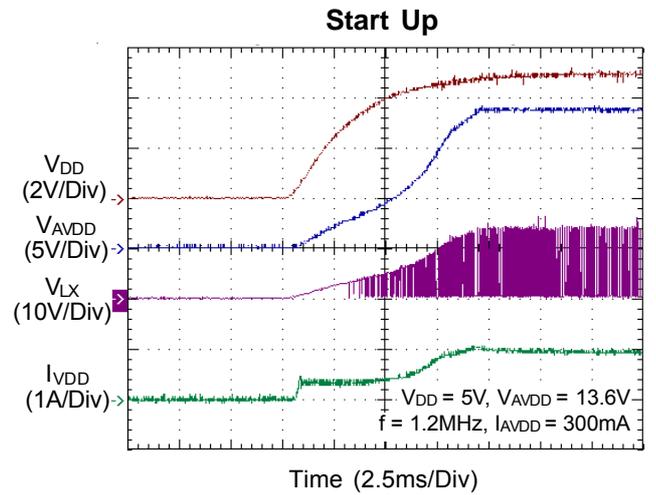
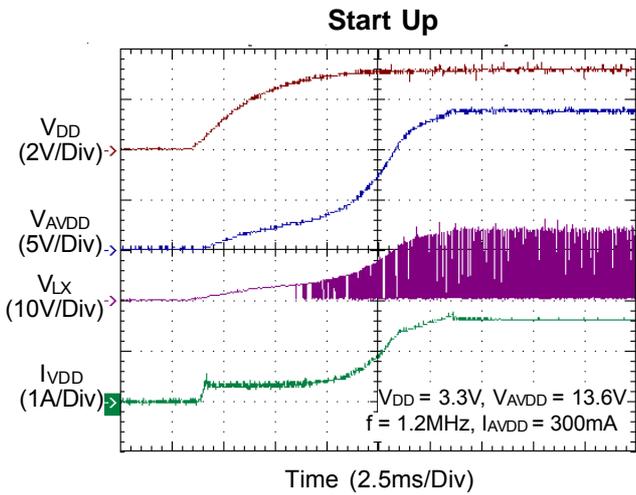
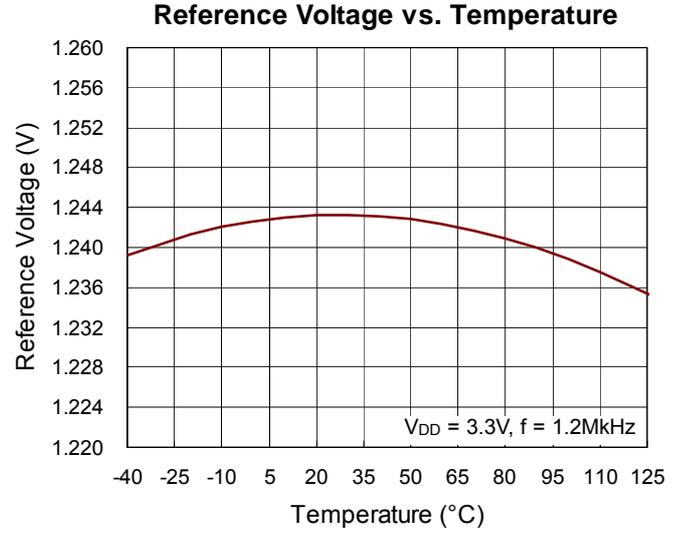
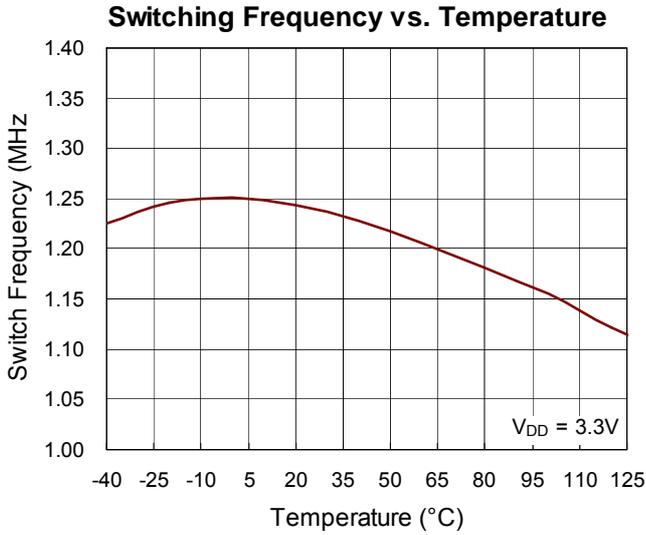


Output Voltage vs. Input Voltage



Output Voltage vs. Input Voltage





## Application Information

The RTQ9297-QT contains a high performance boost regulator to generate voltage for the panel source driver ICs. The following content contains the detailed description and the information of component selection.

### Boost Regulator

The boost regulator is a high efficiency current-mode PWM architecture with 640K / 1.2MHz operation frequency. It performs fast transient responses to generate source driver supplies for TFT LCD display. The high operation frequency allows smaller components used to minimize the thickness of the LCD panel. The output voltage setting can be achieved by setting the resistive voltage-divider sensing at FB pin. The error amplifier varies the COMP voltage by sensing the FB pin to regulate the output voltage. For better stability, the slope compensation signal summed with the current-sense signal will be compared with the COMP voltage to determine the current trip point and duty cycle.

### Soft-Start

The RTQ9297-QT provides soft-start function to minimize the inrush current. When power on, an internal constant current charges an external capacitor. The rising voltage rate on the COMP pin is limited during the charging period and the inductor peak current will also be limited at the same time. When power off, the external capacitor will be discharged for next soft start time.

The soft-start function is implemented by the external capacitor with a 4μA constant current charging to the soft-start capacitor. Therefore, the capacitor should be large enough for output voltage regulation. Typical value for soft-start capacitor range is 33nF. The available soft-start capacitor range is from 10nF to 100nF.

### Output Voltage Setting

The regulated output voltage is shown as following equation :

$$V_{AVDD} = 1.24V \times \left(1 + \frac{R_1}{R_2}\right)$$

The recommended value for R2 should be up to 10kΩ without some sacrificing. To place the resistor divider as close as possible to the chip can reduce noise sensitivity.

### Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisted of R<sub>COMP</sub> and C<sub>COMP</sub>. Choose R<sub>COMP</sub> to set high frequency integrator gain for fast transient response and C<sub>COMP</sub> to set the integrator zero to maintain loop stability. For typical application V<sub>DD</sub> = 3.3V , V<sub>AVDD</sub> = 13.6V , C4 = 4.7μF x 3 , L = 3.6μH, the recommended value for compensation is as below : R<sub>COMP</sub> = 56kΩ, C<sub>COMP</sub> = 330pF.

### Over Current Protection

The RTQ9297-QT boost converter has over-current protection to limit peak inductor current. It prevents large current from damaging the inductor and diode. During the ON-time, once the inductor current exceeds the current limit, the internal LX switch turns off immediately and shortens the duty cycle. Therefore, the output voltage drops if the over-current condition occurs. The current limit there should be also affected by the input voltage, duty cycle and inductor value.

### Over Temperature Protection

The RTQ9297-QT boost converter has thermal protection function to prevent the chip from overheating. When the junction temperature exceeds 155°C, it will shut down the device. Once the device cools down by approximately 30°C, it will start to operate normally. For continuous operation, do not operate over the maximum junction temperature rating 125°C.

### Inductor Selection

The inductance depends on the maximum input current. The inductor current ripple is 20% to 40% of maximum input current that is a general rule. Assume, choose 40% as the criterion then

$$I_{VDD(MAX)} = \frac{V_{AVDD} \times I_{AVDD(MAX)}}{\eta \times V_{DD}}$$

$$I_{RIPPLE} = 0.4 \times I_{VDD(MAX)}$$

Where η is the efficiency, I<sub>IN(MAX)</sub> is the maximum input current, I<sub>RIPPLE</sub> is the inductor current ripple. Beside, the input peak current is maximum input current plus half of inductor current ripple.

$$I_{PEAK} = 1.2 \times I_{VDD(MAX)}$$

Note that the saturated current of inductor must be greater than  $I_{PEAK}$ . The inductance can be eventually determined as follow equation :

$$L = \frac{\eta \times (V_{DD})^2 \times (V_{AVDD} - V_{DD})}{0.4 \times (V_{AVDD})^2 \times I_{AVDD(MAX)} \times f_{OSC}}$$

Where  $f_{OSC}$  is the switching frequency. To consider the system performance, a shielded inductor is preferred to avoid EMI issue.

### Diode Selection

Schottky diode is a good choice for an asynchronous Boost converter due to the small forward voltage. However, power dissipation, reverse voltage rating and pulsating peak current are the important parameters for Schottky diode selection. It is recommended to choose a suitable diode whose reverse voltage rating is greater than the maximum output voltage.

### Capacitor Selection

Output ripple voltage is an important index for estimating the performance. This portion consists of two parts, one is the product of input current and ESR of output capacitor, another part is formed by charging and discharging process of output capacitor. Refer to Figure 1, evaluate  $\Delta V_{OUT1}$  by ideal energy equalization. According to the definition of Q, the Q value can be calculated as following equation :

$$Q = \frac{1}{2} \times \left[ \left( I_{IN} + \frac{1}{2} \Delta I_L - I_{OUT} \right) + \left( I_{IN} - \frac{1}{2} \Delta I_L - I_{OUT} \right) \right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{SW}} = C_{OUT} \times \Delta V_{OUT1}$$

where  $f_{SW}$  is the switching frequency, and  $\Delta I_L$  is the inductor ripple current. Move  $C_{OUT}$  to the left side to estimate the value of  $\Delta V_{OUT1}$  as the following equation :

$$\Delta V_{OUT1} = \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{SW}}$$

Finally, by taking ESR into consideration, the overall output ripple voltage can be determined as the following equation :

$$\Delta V_{OUT} = I_{IN} \times ESR + \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{SW}}$$

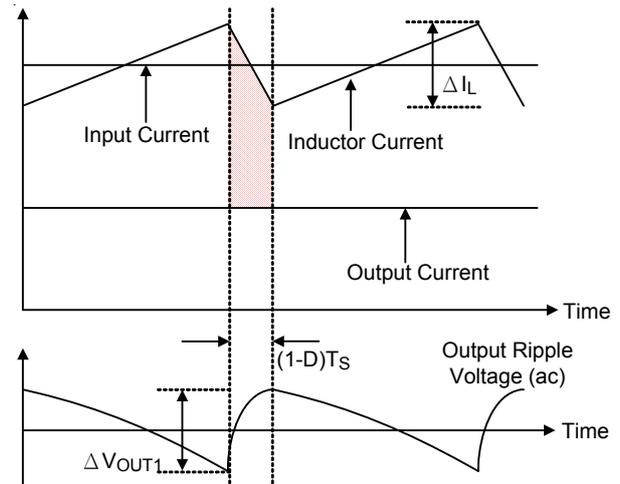


Figure 1. The Output Ripple Voltage without the Contribution of ESR

### Input Capacitor Selection

Low ESR ceramic capacitors are recommended for input capacitor applications. Low ESR will effectively reduce the input voltage ripple caused by switching operation. A 10 $\mu$ F is sufficient for most applications. Nevertheless, this value can be decreased for lower output current requirement. Another consideration is the voltage rating of the input capacitor must be greater than the maximum input voltage.

### Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature  $T_{J(MAX)}$ , listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where  $T_{J(MAX)}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating

Conditions is 125°C. The junction-to-ambient thermal resistance,  $\theta_{JA}$ , is highly package dependent. For a WDFN-10SL 3x3, the thermal resistance,  $\theta_{JA}$ , is 30.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated as below :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (30.5^\circ\text{C/W}) = 3.27\text{W for a WDFN-10SL 3x3 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed  $T_{J(MAX)}$  and the thermal resistance,  $\theta_{JA}$ . The derating curves in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

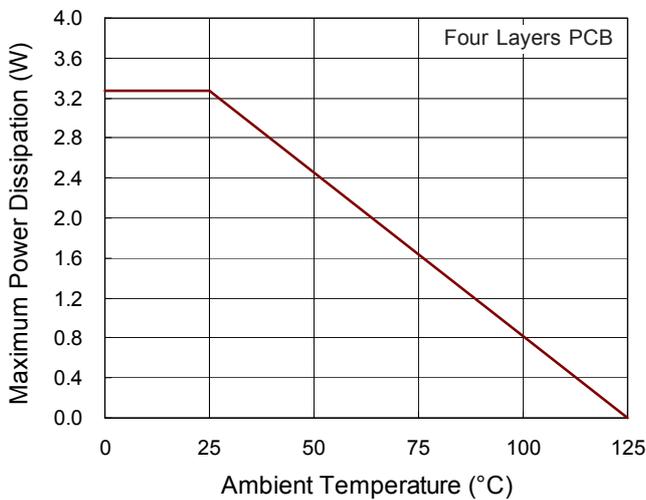


Figure 2. Derating Curve of Maximum Power Dissipation

**Layout Considerations**

For high frequency switching power supplies, the PCB layout is important to get good regulation, high efficiency and stability. The following descriptions are the guidelines for better PCB layout.

- ▶ For good regulation, place the power components as close as possible. The traces should be wide and short enough especially for the high-current output loop.
- ▶ The feedback voltage-divider resistors must be near the feedback pin. The divider center trace must be shorter and the trace must be kept away from any switching nodes.
- ▶ The compensation circuit should be kept away from the power loops and be shielded with a ground trace to prevent any noise coupling.
- ▶ Minimize the size of the LX node and keep it wide and shorter. Keep the LX node away from the FB.
- ▶ The exposed pad of the chip should be connected to a strong ground plane for maximum thermal consideration.

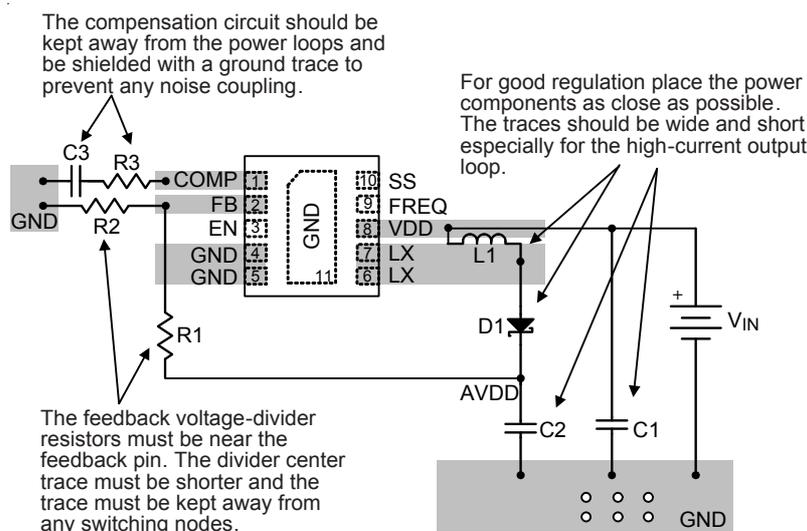
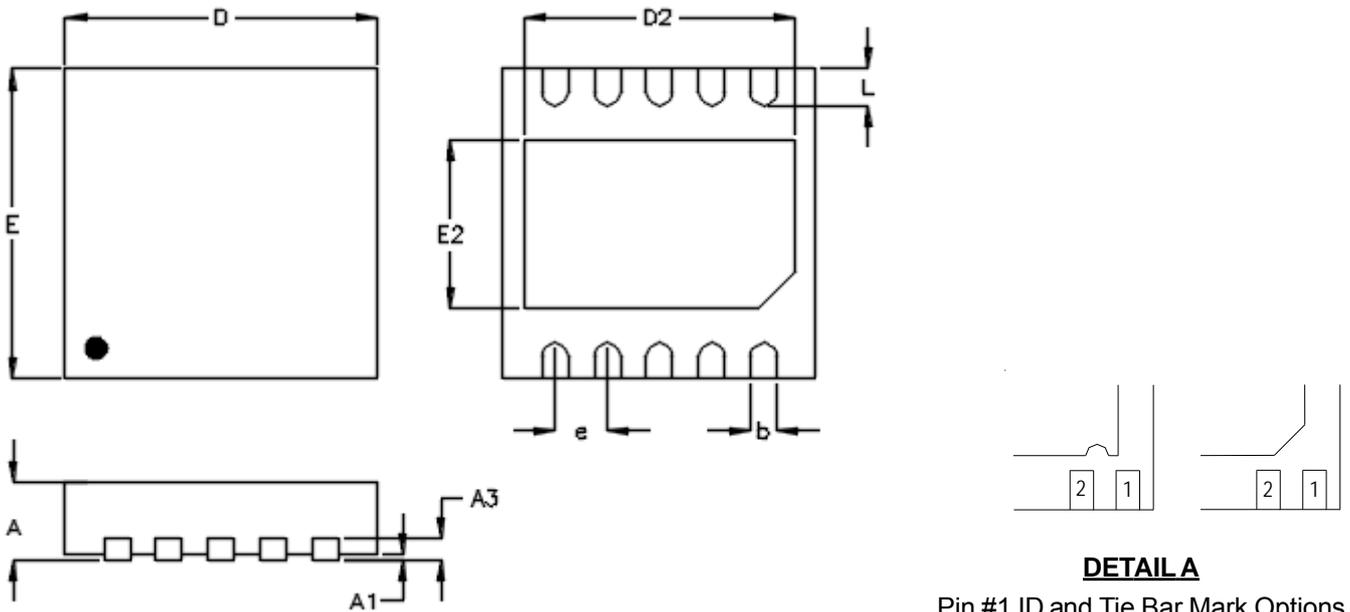


Figure 3. PCB Layout Guide

Outline Dimension



**DETAIL A**

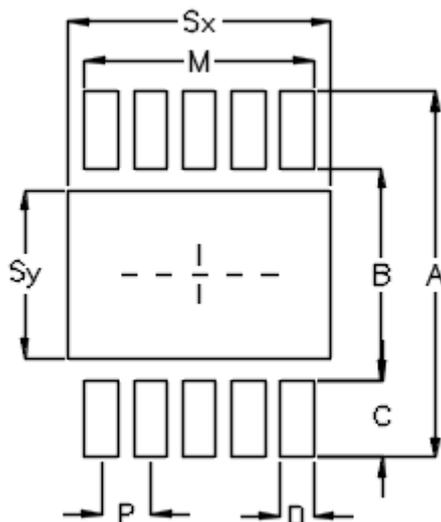
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.900	3.100	0.114	0.122
D2	2.550	2.650	0.100	0.104
E	2.900	3.100	0.114	0.122
E2	1.590	1.690	0.063	0.067
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 10SL DFN 3x3 Package

**Footprint Information**



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN3*3-10S	10	0.50	3.80	2.20	0.80	0.35	2.70	1.74	2.35	±0.05

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