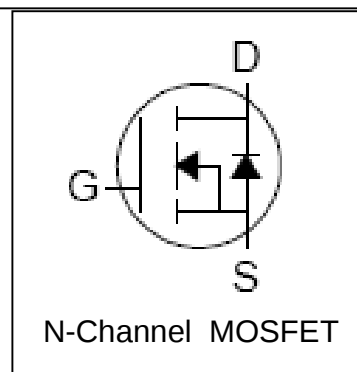
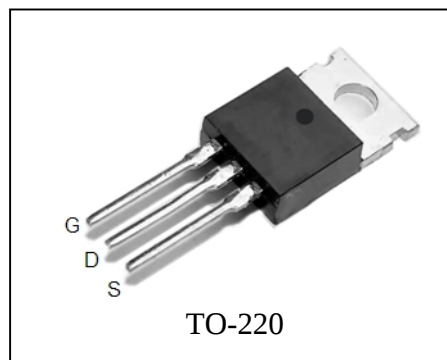


Features

- 100V/40A,
 $R_{DS(ON)} = 21m\Omega(Typ.) @ V_{GS}=10V$
- Super High Dense Cell Design
- 100% avalanche tested
- Lead Free and Green Devices Available
(RoHS Compliant)

Pin Description



Applications

- Switching application

Absolute Maximum Ratings

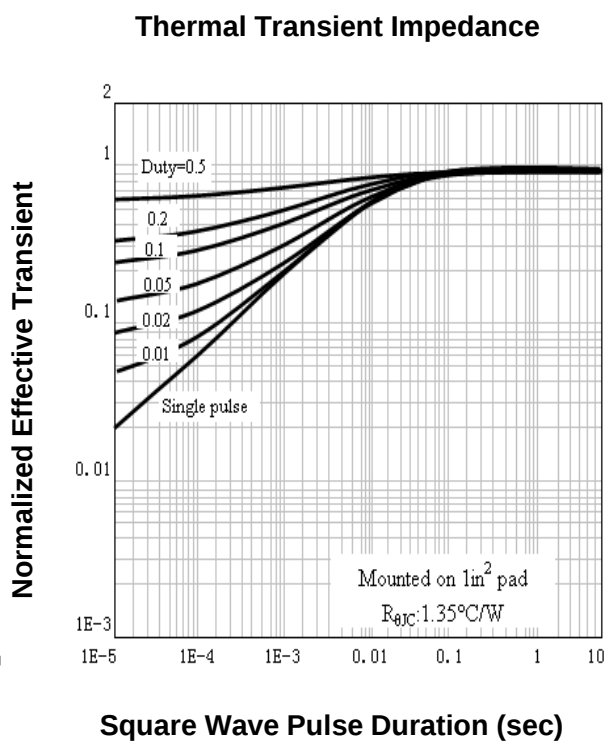
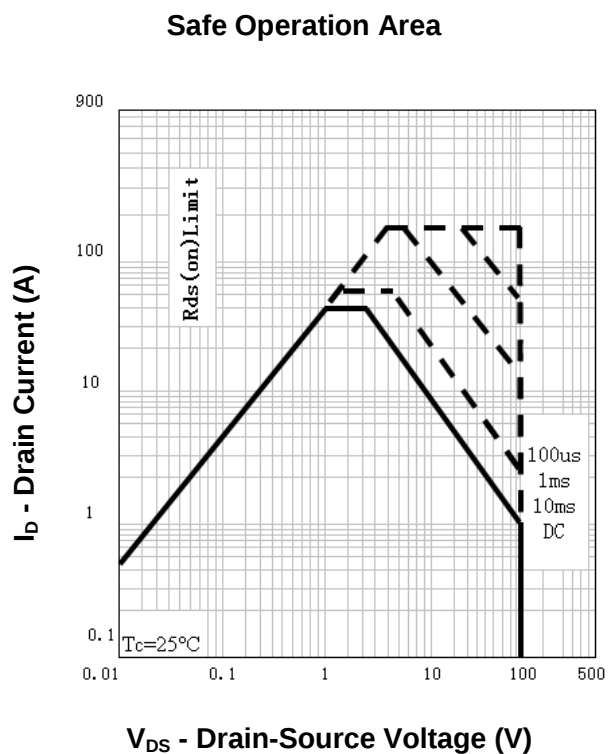
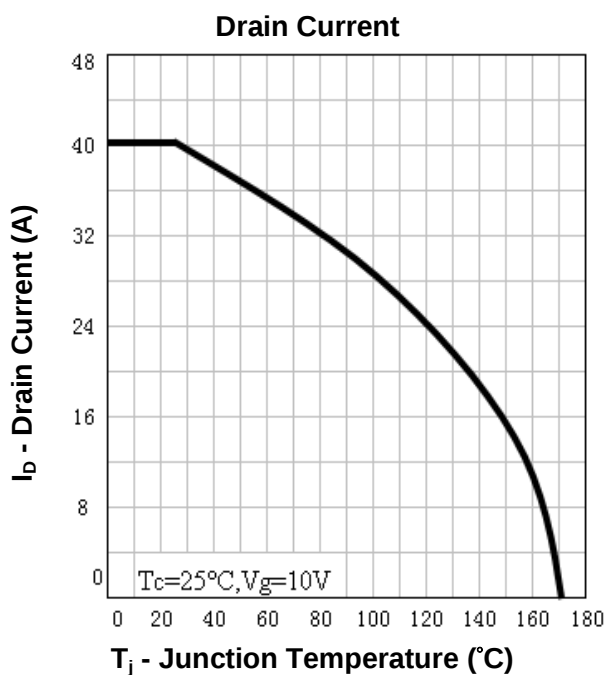
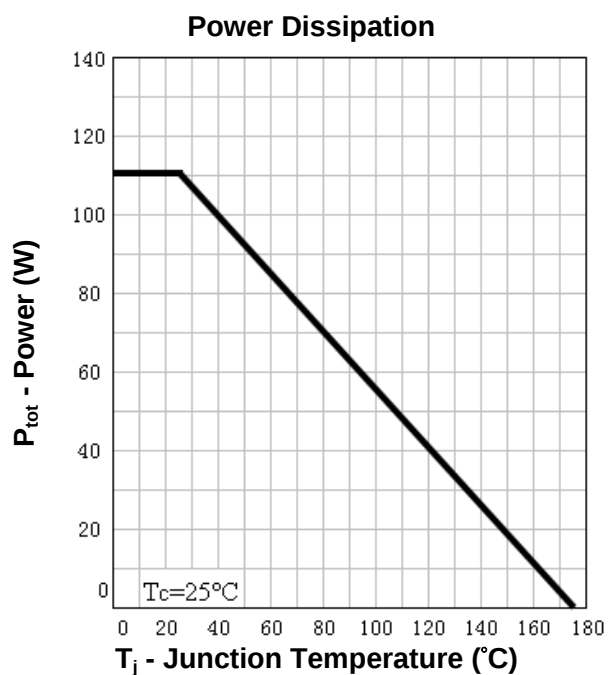
Symbol	Parameter		Rating	Unit
Common Ratings (T _A =25°C Unless Otherwise Noted)				
V _{DSS}	Drain-Source Voltage		100	V
V _{GSS}	Gate-Source Voltage		±25	
T _J	Maximum Junction Temperature		175	°C
T _{STG}	Storage Temperature Range		-55 to 175	°C
I _S	Diode Continuous Forward Current	T _C =25°C	40	A
Mounted on Large Heat Sink				
I _{DP}	300μs Pulse Drain Current Tested	T _C =25°C	160 ^①	A
I _D	Continuous Drain Current(V _{GS} =10V)	T _C =25°C	40 ^②	A
		T _C =100°C	27	
P _D	Maximum Power Dissipation	T _C =25°C	111	W
		T _C =100°C	56	
R _{θJC}	Thermal Resistance-Junction to Case		1.35	°C/W
Drain-Source Avalanche Ratings				
E _{AS} ^③	Avalanche Energy, Single Pulsed		220	mJ

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Condition	RU1H35R			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 100V, V _{GS} =0V			1	μA
		T _J =85°C			10	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250μA	2	3	4	V
I _{GSS}	Gate Leakage Current	V _{GS} =±25V, V _{DS} =0V			±100	nA
R _{DS(ON)} ^④	Drain-Source On-state Resistance	V _{GS} = 10V, I _{DS} =16A		21	25	mΩ
Diode Characteristics						
V _{SD} ^④	Diode Forward Voltage	I _{SD} =16A, V _{GS} =0V		0.8	1.2	V
t _{rr}	Reverse Recovery Time	I _{SD} =16A, dI _{SD} /dt=100A/μs		100		ns
Q _{rr}	Reverse Recovery Charge			430		nC
Dynamic Characteristics ^⑤						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz		2.8		Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} = 25V, Frequency=1.0MHz		2100		pF
C _{oss}	Output Capacitance			250		
C _{rss}	Reverse Transfer Capacitance			115		
t _{d(ON)}	Turn-on Delay Time	V _{DD} =50V, R _L =30Ω, I _{DS} =16A, V _{GEN} = 10V, R _G =4.7Ω		22		ns
t _r	Turn-on Rise Time			76		
t _{d(OFF)}	Turn-off Delay Time			60		
t _f	Turn-off Fall Time			23		
Gate Charge Characteristics ^⑤						
Q _g	Total Gate Charge	V _{DS} =80V, V _{GS} = 10V, I _{DS} =16A		44		nC
Q _{gs}	Gate-Source Charge			10		
Q _{gd}	Gate-Drain Charge			21		

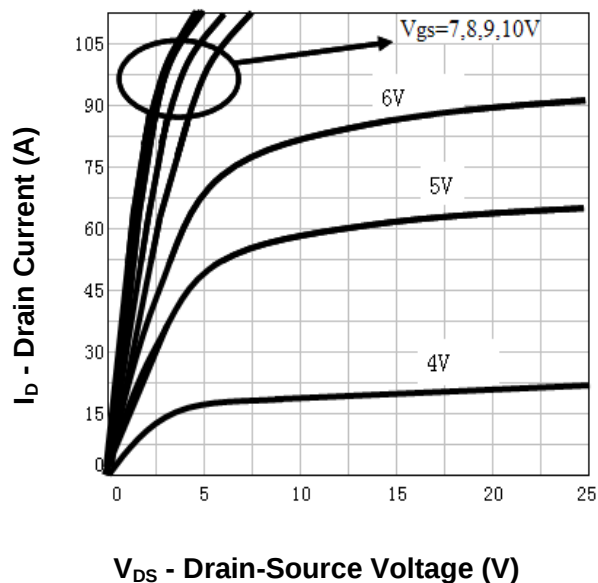
- Notes: ① Pulse width limited by safe operating area.
 ② Calculated continuous current based on maximum allowable junction temperature.
 ③ Limited by $T_{Jmax}, I_{AS}=21A, V_{DD}=48V, R_G=50\Omega$, Starting $T_J=25^{\circ}\text{C}$.
 ④ Pulse test; Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
 ⑤ Guaranteed by design, not subject to production testing.

Typical Characteristics

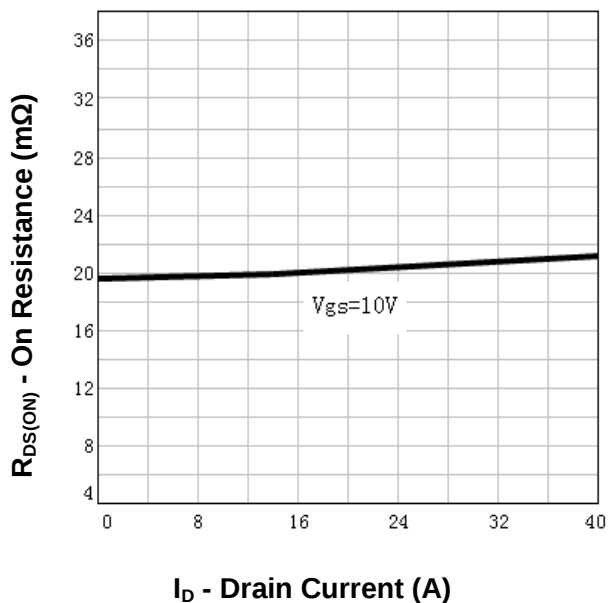


Typical Characteristics

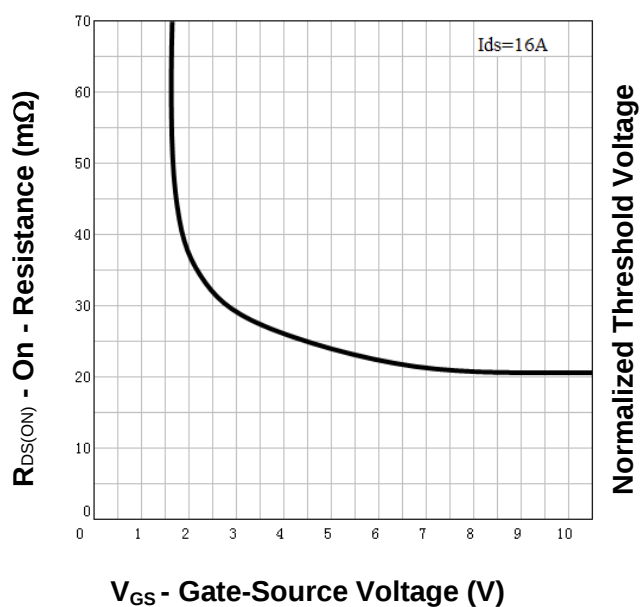
Output Characteristics



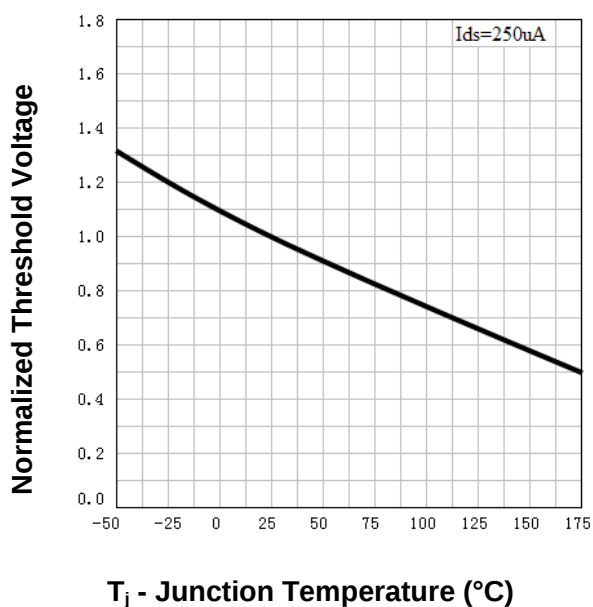
Drain-Source On Resistance



Drain-Source On Resistance

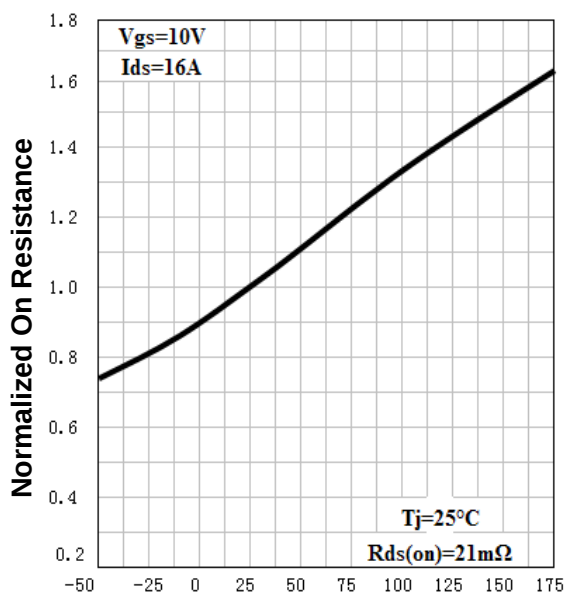


Gate Threshold Voltage



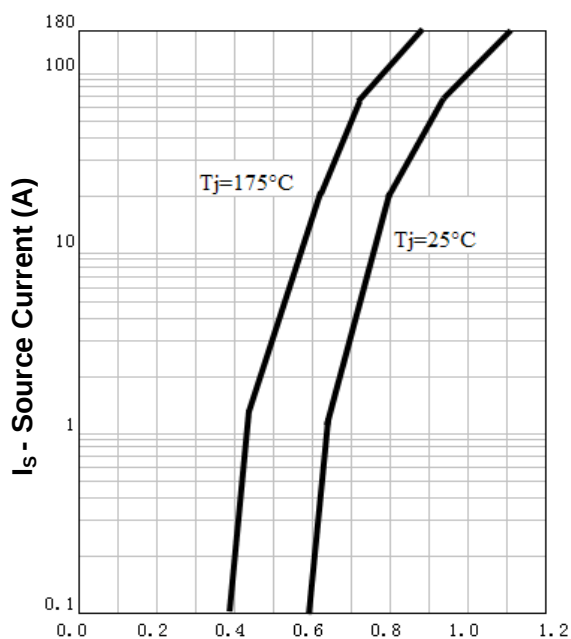
Typical Characteristics

Drain-Source On Resistance



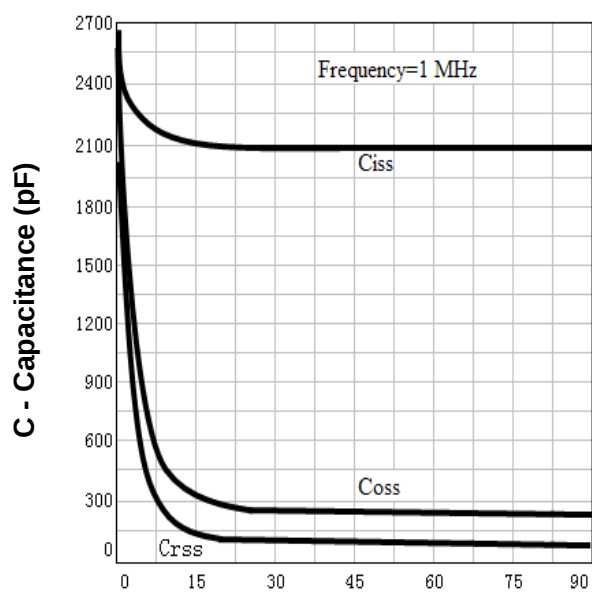
T_j - Junction Temperature ($^{\circ}\text{C}$)

Source-Drain Diode Forward



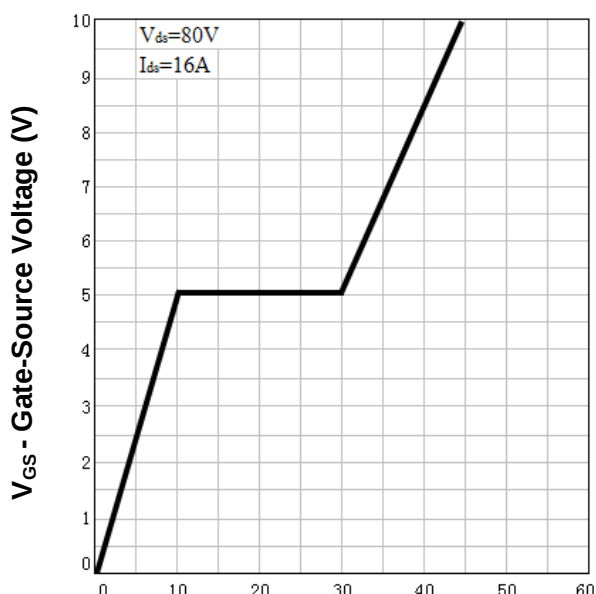
V_{SD} - Source-Drain Voltage (V)

Capacitance



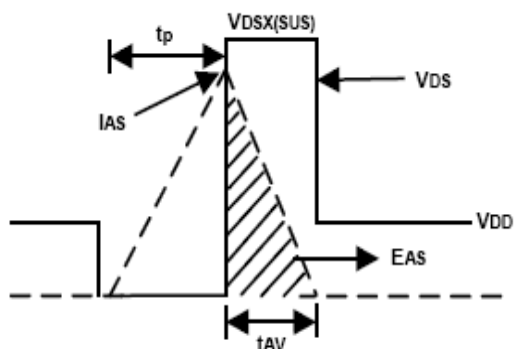
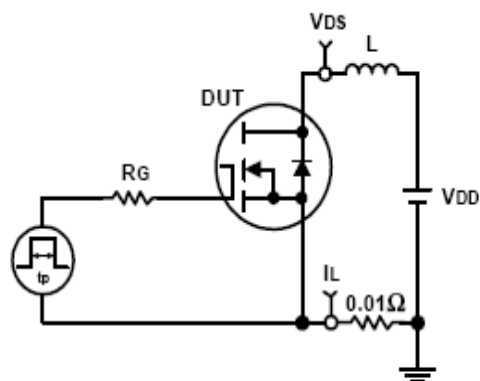
V_{DS} - Drain-Source Voltage (V)

Gate Charge

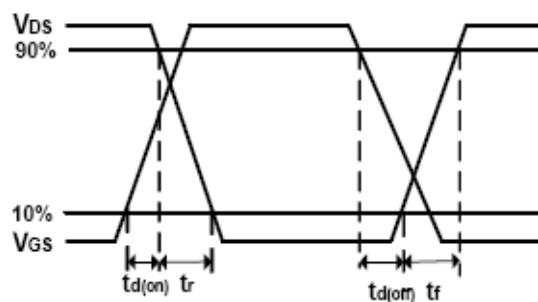
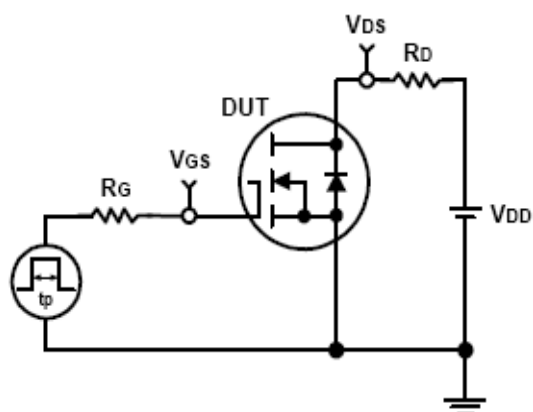


Q_G - Gate Charge (nC)

Avalanche Test Circuit and Waveforms



Switching Time Test Circuit and Waveforms

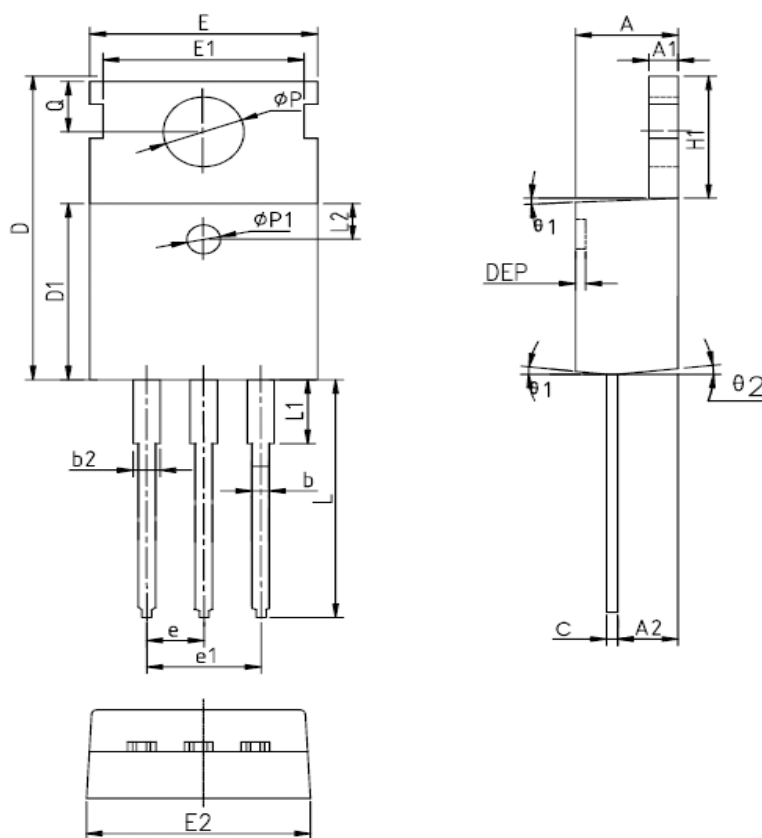


Ordering and Marking Information

Device	Marking	Package	Packaging	Quantity	Reel Size	Tape width
RU1H35R	RU1H35R	TO-220	Tube	50	-	-

Package Information

TO-220FB-3L



SYMBOL	MM			INCH			SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185	$\phi p1$	1.40	1.50	1.60	0.055	0.059	0.063
A1	1.27	1.30	1.33	0.050	0.051	0.052	e	2.54BSC			0.1BSC		
A2	2.35	2.40	2.50	0.093	0.094	0.098	e1	5.08BSC			0.2BSC		
b	0.77	-	0.90	0.030	-	0.035	H1	6.40	6.50	6.60	0.252	0.256	0.260
b2	1.23	-	1.36	0.048	-	0.054	L	12.75	-	13.17	0.502	-	0.519
C	0.48	0.50	0.52	0.019	0.020	0.021	L1	-	-	3.95	-	-	0.156
D	15.40	15.60	15.80	0.606	0.614	0.622	L2	2.50REF.			0.098REF.		
D1	9.00	9.10	9.20	0.354	0.358	0.362	ϕp	3.57	3.60	3.63	0.141	0.142	0.143
DEP	0.05	0.10	0.20	0.002	0.004	0.008	Q	2.73	2.80	2.87	0.107	0.110	0.113
E	9.70	9.90	10.10	0.382	0.389	0.398	$\theta 1$	5°	7°	9°	5°	7°	9°
E1	-	8.70	-	-	0.343	-	$\theta 2$	1°	3°	5°	1°	3°	5°
E2	9.80	10.00	10.20	0.386	0.394	0.401							

ALL DIMENSIONS REFER TO JEDEC STANDARD
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS

Customer Service

Worldwide Sales and Service:

Sales@ruichips.com

Technical Support:

Technical@ruichips.com

Investor Relations Contacts:

Investor@ruichips.com

Marcom Contact:

Marcom@ruichips.com

Editorial Contact:

Editorial@ruichips.com

HR Contact:

HR@ruichips.com

Legal Contact:

Legal@ruichips.com

Shen Zhen RUICHIPS Semiconductor CO., LTD

Room 501, the 5floor An Tong Industrial Building,
NO.207 Mei Hua Road Fu Tian Area Shen Zhen City, CHINA

TEL: (86-755) 8311-5334

FAX: (86-755) 8311-4278

E-mail: Sales-SZ@ruichips.com