RW1025G Revision History		
Version	**Date**	**Description**
V0.0	2014/06/30	First Edition
V0.1	2016/3/3	instruction and display data refresh are the most commonly used software techniques to improve EFT/ESD immunity. Registers in the instructions table and display data should be refreshed periodically in order to recover display content and function from corruption if EFT/ESD occurs. 0xE3H must be added to instruction refresh sequence. Add Type B 4-SPI application circuit

■ Features

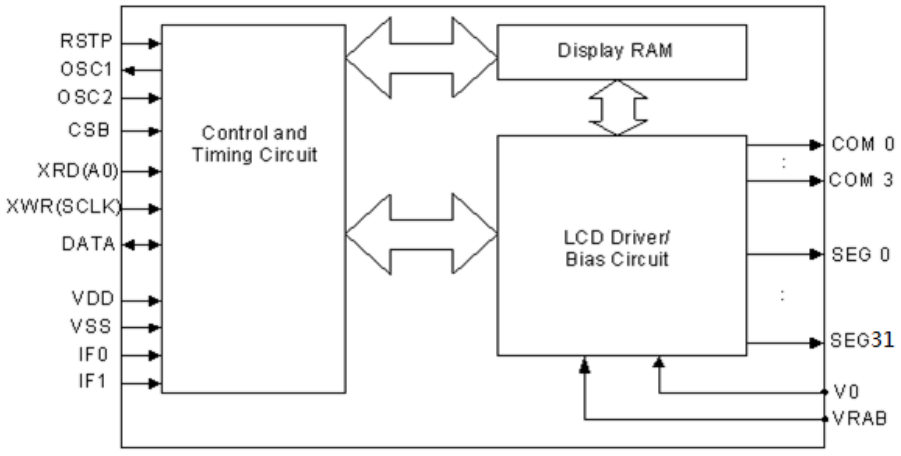
- Operating voltage: 2.4V~5.2V
- External resistor CR oscillator
- External 256k Hz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of static or 1/2 or 1/3 or 1/4 duty LCD applications
- Power down command reduces power consumption
- 32 x 4 LCD driver
- Built-in 32 x 4 bit display RAM
- IIC serial interface
- 3-line/4-line (type A & type B) serial interface (SPI)
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- R/W address auto increment
- VRAB pin for adjusting V0 operating voltage
- Available highest possible frame frequency to 200Hz

■ General Description

The RW1025G is a 128 patterns (32x4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the RW1025G makes it suitable for multiple LCD applications including LCD modules and display subsystems.

Only two or three or four lines are required for the serial interface between the host controller and the RW1025G.
The RW1025G contains a power down command to reduce power consumption.

■ Block Diagram

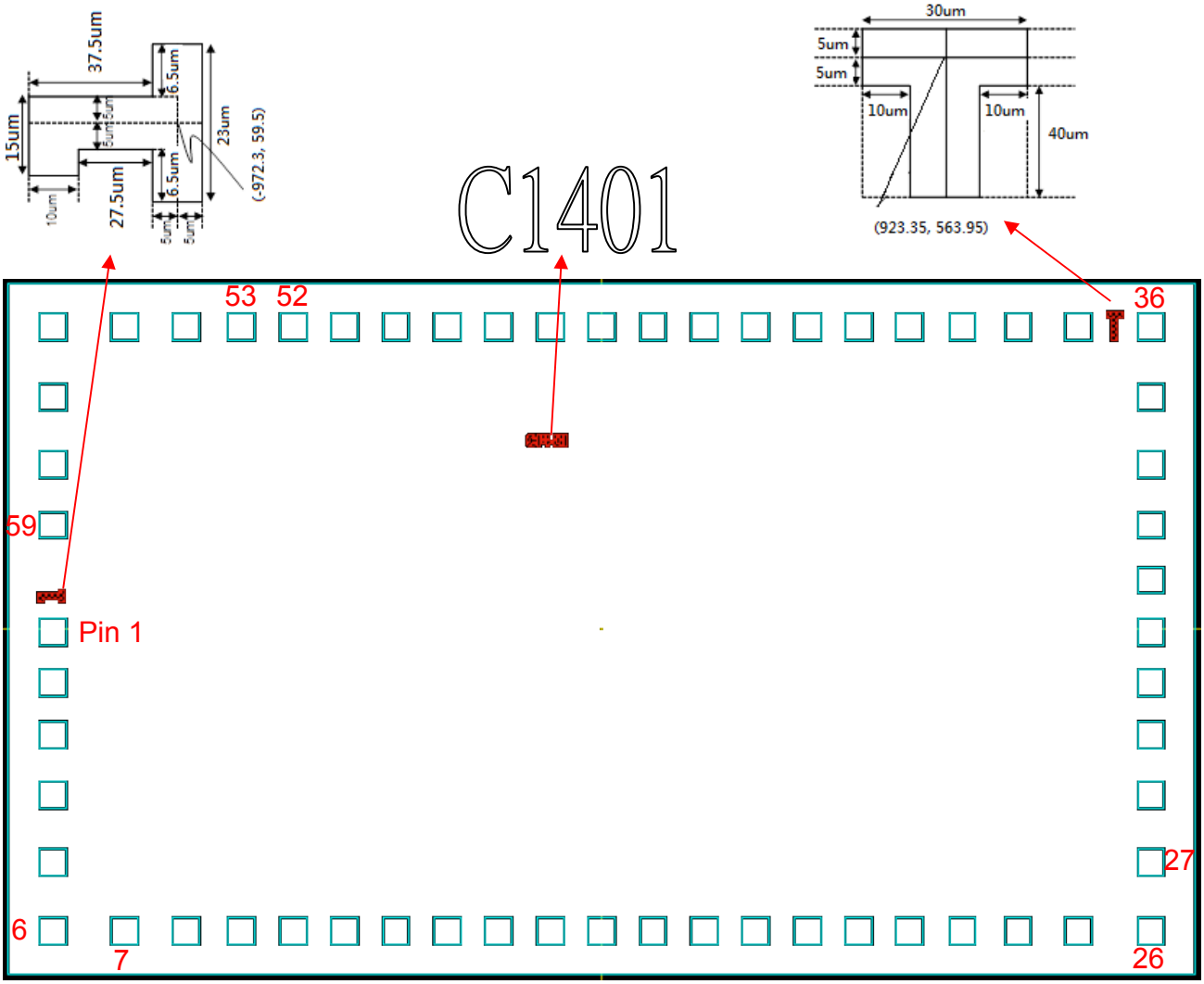


Note: CSB : Chip Selection
XWR,XRD,DATA:Serial Interface
COM0~COM3,SEG0~SEG31: LCD Outputs
IF1,IF0: Interface select pin

■ Pad Assignment

Chip size: 2135 x 1245 um
Bump Size: 48 x 48 um
Bump Pitch: 92.5~129.8 um
Bump Height: 15 um (Typ)
Chip thickness: 400 um

PAD 53~ PAD 59 is Dummy PAD



■ Pad Location

PAD No.	PAD NAME	COORDINATE		PAD No.	PAD NAME	COORDINATE	
		X	Y			X	Y
1	VDD	-988.5	-5.25	31	SEG[17]	988.5	-5.25
2	IF1	-988.5	-97.75	32	SEG[16]	988.5	87.25
3	IF0	-988.5	-190.25	33	SEG[15]	988.5	186.75
4	VSS1	-988.5	-299.75	34	SEG[14]	988.5	296.25
5	VSS2	-988.5	-419.25	35	SEG[13]	988.5	415.75
6	CSB	-988.5	-543.5	36	SEG[12]	988.5	543.5
7	XRD	-858.75	-543.5	37	SEG[11]	858.25	543.5
8	XWR	-749.25	-543.5	38	SEG[10]	748.75	543.5
9	DATA	-649.75	-543.5	39	SEG[9]	649.25	543.5
10	OSC2	-555.25	-543.5	40	SEG[8]	554.75	543.5
11	OSC1	-462.75	-543.5	41	SEG[7]	462.25	543.5
12	RSTP	-370.25	-543.5	42	SEG[6]	369.75	543.5
13	COM[0]	-277.75	-543.5	43	SEG[5]	277.25	543.5
14	COM[1]	-185.25	-543.5	44	SEG[4]	184.75	543.5
15	COM[2]	-92.75	-543.5	45	SEG[3]	92.25	543.5
16	COM[3]	-0.25	-543.5	46	SEG[2]	-0.25	543.5
17	SEG[31]	92.25	-543.5	47	SEG[1]	-92.75	543.5
18	SEG[30]	184.75	-543.5	48	SEG[0]	-185.25	543.5
19	SEG[29]	277.25	-543.5	49	VRAB	-277.75	543.5
20	SEG[28]	369.75	-543.5	50	V2	-370.25	543.5
21	SEG[27]	462.25	-543.5	51	V1	-462.75	543.5
22	SEG[26]	554.75	-543.5	52	V0	-555.25	543.5
23	SEG[25]	649.25	-543.5	53	Dummy	-649.25	543.5
24	SEG[24]	748.75	-543.5	54	Dummy	-748.75	543.5
25	SEG[23]	858.25	-543.5	55	Dummy	-858.25	543.5
26	SEG[22]	988.5	-543.5	56	Dummy	-988.5	543.5
27	SEG[21]	988.5	-419.25	57	Dummy	-988.5	415.75
28	SEG[20]	988.5	-299.75	58	Dummy	-988.5	296.25
29	SEG[19]	988.5	-190.25	59	Dummy	-988.5	186.75
30	SEG[18]	988.5	-97.75				

■ Pad Description

Pad	I/O	Function
CSB	I	Chip selection input for 3-SPI, 4-SPI with pull-high resistor. When CSB is at logic high, the data and command read from or written to the RW1025G are disabled. The serial interface circuit is also reset. But if CSB is at logic low level and is input to the CSB pad, the data and command transmission between the host controller and the RW1025G are all enabled.
XRD(A0)	I	READ clock input for 4-SPI (type B) with pull-high resistor. Data in the RAM of RW1025G are clocked out on the falling edge of the XRD signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data. A0 pin for 4-SPI (type A) serial interface. A0=1: DATA A0=0: Command
XWR(SCLK)	I	WRITE clock input for 4-SPI (type B) with pull-high resistor. Data on the DATA line are latched into the RW1025G on the rising edge of the XWR signal. Serial clock input (SCLK) pin for 3-SPI, 4-SPI (type A), and IIC interface.
DATA	I/O	Serial data input/output with pull-high resistor.
VSS1	-	Ground power supply for Digital Circuit
VSS2	-	Ground power supply for Analog Circuit
OSC1	I	The OSC1 and OSC2 pads are connected to a external resistor if an RC oscillator is selected. If the system clock comes from an external clock source, the external clock source should be connected to the OSC1 pad.
OSC2	O	
V0	I	LCD power input.
VDD	-	Positive power supply.
V1,V2	-	Bias voltage level for LCD driving. These voltages must satisfy the following: **VDD ≥ V0 ≥ V1 ≥ V2 ≥ VSS**
COM0-COM3	O	LCD common output.
SEG0-SEG31	O	LCD segment output.
RSTP	I	Reset pin with pull-up resistor, Initialized by setting RSTP to "L". Reset operation is performing at RSTP signal level.
VRAB	I	LCD voltage adjusting pin. Applies voltage between V0 and VSS using a split resistor.
IF1,IF0	I	Interface selection pins IF1,IF0 (0 , 0) : IIC Interface (0 , 1) : 3-line Interface (1 , 0) : 4-line Interface (Type A) (1 , 1) : 4-line Interface (Type B compatible HT1621)

■ Absolute Maximum Ratings

Supply Voltage .....VSS-0.3V to VSS +5.5V
Storage Temperature.....-50°C to +125°C
Input Voltage.....VSS-0.3V to VDD+0.3V
Operating Temperature.....-30°C to +85°C

Note: These are stress ratings only. Stresses exceeding the range specified under Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

➢ D.C. Characteristics (Ta=25°C)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	-	-	2.4	-	5.2	V
I_{DD1}	Operating Current	3V	No load/LCD ON On-chip RC oscillation	-	150	200	μA
		5V		-	300	600	μA
I_{DD3}	Operating Current	3V	No load/LCD ON external clock source	-	100	200	μA
		5V		-	200	400	μA
I_{STB}	Standby Current	3V	No load, Power down mode	-	0.1	5	μA
		5V		-	0.3	10	μA
V_{IL}	Input Low Voltage	3V	DATA, XWR,CSB,XRD	0	-	0.6	V
		5V		0	-	1.0	V
V_{IH}	Input High Voltage	3V	DATA, XWR,CSB,XRD	2.4	-	3.0	V
		5V		4	-	5.0	V
I_{OL1}	DATA	3V	V_{OL}=0.3V	0.5	1.2	-	mA
		5V	V_{OL}=0.5V	1.3	2.6	-	mA
I_{OH1}	DATA	3V	V_{OH}=2.7V	-0.4	-0.8	-	mA
		5V	V_{OH}=4.5V	-0.9	-1.8	-	mA
I_{OL2}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	150	-	μA
		5V	V_{OL}=0.5V	150	250	-	μA
I_{OH2}	LCD Common Source Current	3V	V_{OH}=2.7V	-80	-120	-	μA
		5V	V_{OH}=4.5V	-120	-200	-	μA
I_{OL3}	LCD Segment Sink Current	3V	V_{OL}=0.3V	60	120	-	μA
		5V	V_{OL}=0.5V	120	200	-	μA
I_{OH3}	LCD Segment Source Current	3V	V_{OH}=2.7V	-40	-70	-	μA
		5V	V_{OH}=4.5V	-70	-100	-	μA
R_{PH}	Pull-high Resistance	3V	DATA, XWR,CSB,XRD	60	120	200	kΩ
		5V		30	60	100	kΩ

➢ A.C. Characteristics (Ta=25 °C)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		VDD	Conditions				
fSYS1	System Clock	-	On-chip RC Oscillation **RF OSC=62KΩ**	-	256	-	kHz
fSYS2	System Clock	-	External clock source	-	256	-	kHz
fLCD	LCD Clock	-	On-chip RC Oscillation	-	fSYS1/1024	-	Hz
		-	External clock source	-	fSYS2/1024	-	Hz
tCOM	LCD Common Period	-	n: Number of COM	-	n/fLCD	-	s
fCLK1	Serial Data Clock(XWR pin)	3V	Duty cycle 50%	4	-	150	kHz
		5V		4	-	300	kHz
fCLK2	Serial Data Clock(XRD pin)	3V	Duty cycle 50%	-	-	75	kHz
		5V		-	-	150	kHz
tCS	Serial Interface Reset Pulse Width(Figure 3)	-	CSB	-	250	-	ns
tCLK	XWR,XRD Input Pulse Width (Figure 1)	3V	Write mode	3.34	-	125	µs
			Read mode	6.67	-	-	
		5V	Write mode	1.67	-	125	µs
			Read mode	3.34	-	-	
tr,tf	Rise/Fall Time Serial Data Clock Width (Figure 1)	-	-	-	120	-	ns
tSU	Setup Time for DATA to XWR,XRD Clock Width (Figure 2)	-	-	-	120	-	ns
th	Hold Time for DATA to XWR,XRD Clock Width (Figure 2)	-	-	-	120	-	ns
tSU1	Setup Time for CSB to XWR,XRD Clock Width (Figure 3)	-	-	-	100	-	ns
th1	Hold Time for CSB to XWR,XRD Clock Width (Figure 3)	-	-	-	100	-	ns

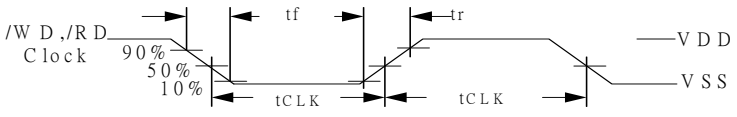


Figure 1

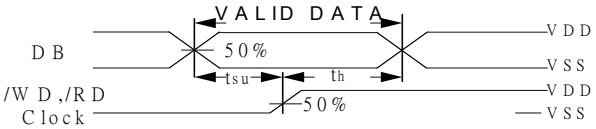


Figure 2

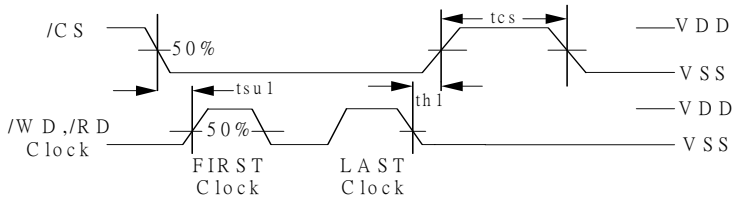
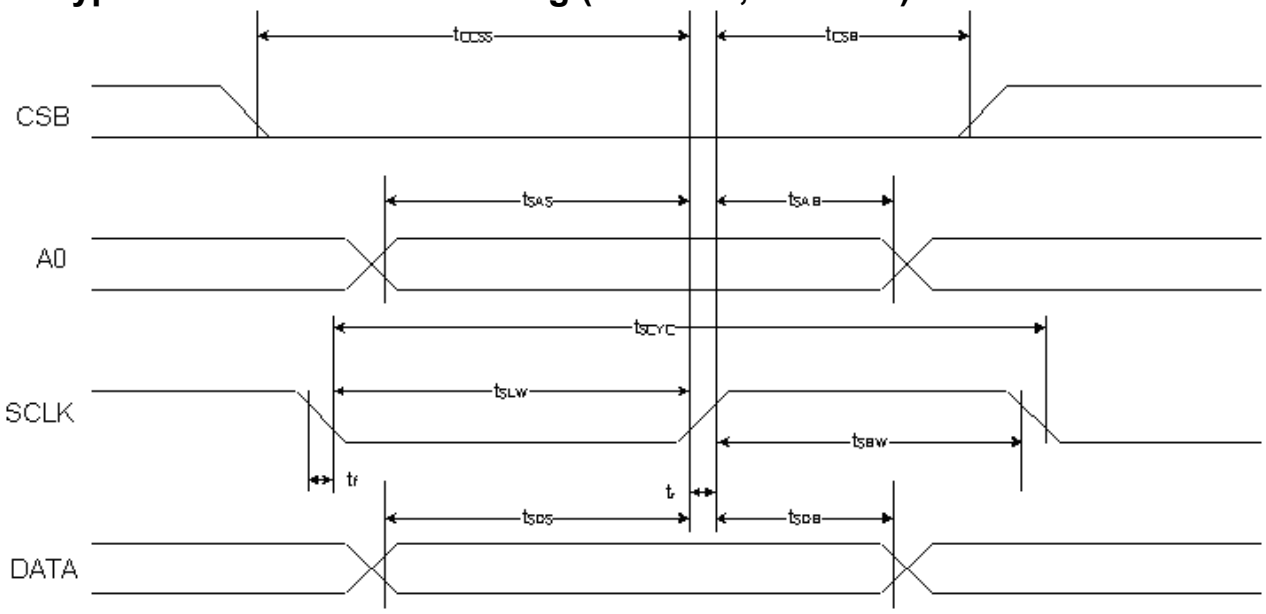


Figure 3

■ Type A Serial Interface Timing (IF0=VSS,IF1=VDD)



RF=68K (VDD = 3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCLK	Tscyc		240	—	ns
SCL "H" pulse width		Tshw		120	—	
SCL "L" pulse width		TSLW		120	—	
Address setup time	A0	TSAS		0	—	
Address hold time		Tsah		0	—	
Data setup time	DATA	Tsds		90	—	
Data hold time		TSDH		0	—	
CS-SCL time	CS	Tcss		100	—	
CS-SCL time		Tcsh		100	—	

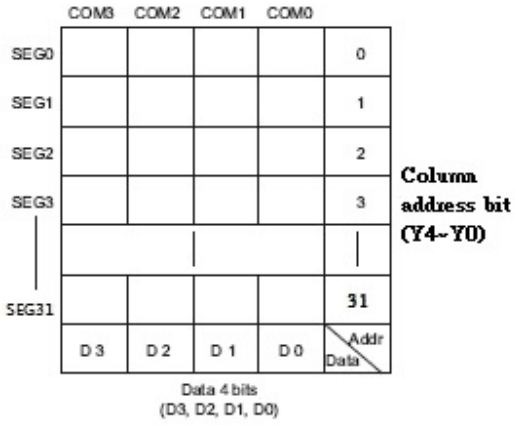
RF=68K (VDD = 5.0V, Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCLK	Tscyc		160	—	ns
SCL "H" pulse width		Tshw		80	—	
SCL "L" pulse width		TSLW		80	—	
Address setup time	A0	TSAS		0	—	
Address hold time		Tsah		0	—	
Data setup time	DATA	Tsds		60	—	
Data hold time		TSDH		0	—	
CS-SCL time	CS	Tcss		60	—	
CS-SCL time		Tcsh		60	—	

■ Functional Description

➢ Display Memory RAM

The static display memory (RAM) is organized into 32x4 bits and stores the displayed data. The contents of the RAM data are directly mapped to the contents of the LCD driver. The following is a mapping from the RAM to the LCD pattern:



RAM Mapping

➢ System Oscillator

The RW1025G system clock is used to generate the LCD driving clock. The source of the clock may be from an external-resistor RC oscillator (256 kHz), or an external 256 kHz clock by the S/W setting. The configuration of the system oscillator is as shown.
After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the external-resistor RC oscillator. Once the system clock stops, the LCD display will become blank.
The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The external clock source can be applied to connect of 256 kHz to the OSC1 pin. In this case, the system fails to enter the power down mode. At the initial system power on, the RW1025G is at the SYS DIS state.

➢ LCD Driver

The RW1025G is a 144 (32x4) pattern LCD driver.
It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the RW1025G suitable for various LCD applications.
The LCD driving clock is derived from the system clock. The value of the driving clock is always 256 kHz even when it is at an external-resistor RC oscillator frequency, or an external frequency.

The LCD OFF command turns the LCD display off by disabling the LCD bias generator.
The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator.
The BIAS and COM are the LCD panel related commands. Using the LCD related commands; the RW1025G can be compatible with most types of LCD panels.
The LCD corresponding commands are summarized in the following tables.

➢ Display command

	A0	D7	D6	D5	D4	D3	D2	D1	D0
1st Byte →	0	1	1	1	1	0	1	0	0
2nd Byte →		-	-	-	-	SHL	ADC	REV	All on

This register can select the scan direction of the COM output terminal.
SHL=0: Normal
SHL=1: Reverse

This register can reverse the correspondence between the display RAM data column address and the segment driver output.
ADC=0: Normal
ADC=1: Reverse

This register can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.
REV=0: Normal (RAM data "H")
REV=1: Reverse (RAM data "L")

This register makes it possible to force all display points ON regardless of the content of the display data RAM.
All on=0: Normal display mode
All on=1: Display all point ON

➢ Set static Display

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	0	0	1	STA

The static LCD drive mode is used when a single backplane is provided in the LCD.

STA=1; static display on

STA=0; normal display

➢ Reset

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	0	0	0	0

This register initializes the column address, the Mode select, the SYS DIS, the RC 256K, the analog off, display command, the set static display.

OSC OFF
LCD OFF
Duty: 1/4
Bias: 1/2
Set column address: Y4~Y0=0
Mode select: EXT=0
Analog command: REGOFF=0, FOLOFF=0
Display command: SHL=0, ADC=0, REV=0, All on=0
Set static display: STA=0

➢ Analog command

	A0	D7	D6	D5	D4	D3	D2	D1	D0
1st Byte →	0	1	1	1	1	0	1	0	0
2nd Byte →		-	-	REGOFF	FOLOFF	1	0	1	1

This register sets the power supply circuit functions.

Regulator circuit ON/OFF control bit:
REGOFF=0; Regulator on
REGOFF=1; Regulator off

Follower circuit ON/OFF control bit:
FOLOFF=0; Follower on
FOLOFF=1; Follower off

■ Command Summary for 4-line (type A IF0,IF1=1,0), 3-line, and IIC interface

Instruction of RW1025G	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXT=0 or 1										
Mode Set	0	1	1	1	1	1	1	0	EXT	set EXT mode

EXT=0										
Instruction	**A0**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**	**Description**
Set column (segment)address	0	0	1	0	Y4	Y3	Y2	Y1	Y0	Set Display RAM column address in column address register *valid for Type A 3-4SPI,IIC only
Write display data	1	Write data								Write data to Display memory RAM
Select DUTY & Bias	0	0	0	1	0	DU1	DU0	0	Bias	Set LCD Duty & Bias DU1,DU0 0 0 : 1/2 Duty 0 1 : 1/3 Duty 1 0 : 1/4 Duty Bias=1 : 1/3 bias Bias=0 : 1/2 bias
RC 256K	0	0	0	0	1	0	1	X	X	System clock source, on-chip RC oscillator
RC 256K	0	0	0	0	1	1	0	X	X	System clock source, on-chip RC oscillator
EXT 256K	0	0	0	0	1	1	1	0	0	System clock source, external clock source
SYS DIS	0	0	0	0	0	0	0	0	0	Turn off both oscillator and LCD bias
SYS EN	0	0	0	0	0	0	0	0	1	Turn on system oscillator
LCDOFF	0	0	0	0	0	0	0	1	0	Turn off LCD bias
LCDON	0	0	0	0	0	0	0	1	1	Turn on LCD bias
Reserved instruction	0	1	1	1	0	0	0	1	1	Reserved for the in wafer probing test

EXT=1										
Instruction	**A0**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**	**Description**
Display COMMAND (Double Command)	0	1	1	1	1	0	1	0	1	display control command SHL: Com output scan direction ADC: SEG output correspondence REV: reverse display ALLON: all point on display
	0	-	-	-	-	SHL	ADC	REV	ALLON	
Set Static display	0	1	1	1	1	0	0	1	STA	STA=0:normal display STA=1 :static display on
Reset	0	1	1	1	1	0	0	0	0	Software Reset
ANALOG COMMAND (Double Command)	0	1	1	1	1	0	1	0	0	Analog control command FOLOFF =1 , follower off FOLOFF =0 , follower on REGOFF = 1 , regulator off REGOFF = 0 , regulator on
	0	-	-	REGOFF	FOLOFF	1	0	1	1	

■ Command Summary for 4-line serial interface (type B) IF0,IF1=1,1

EXT=1 or 0

Instruction	ID	Command Code	Data/command mode	Description	power on initial value
Mode Select	**100**	1111-110a-X	C	a=0 : EXT=0 a=1 : EXT=1	0

EXT=0

Instruction	ID	Command Code	Data/command mode	Description	power on initial value
Read display data	**110**	0A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
Write display data	**101**	0A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	**101**	0A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	**100**	0000-0000-X	C	Turn off both oscillator and LCD bias	yes
SYS EN	**100**	0000-0001-X	C	Turn on system oscillator	
LCDOFF	**100**	0000-0010-X	C	Turn off LCD bias	yes
LCDON	**100**	0000-0011-X	C	Turn on LCD bias	
RC 256K	**100**	0001-01XX-X	C	System clock source, on-chip RC oscillator	
RC 256K	**100**	0001-10XX-X	C	System clock source, on-chip RC oscillator	yes
EXT 256K	**100**	0001-11XX-X	C	System clock source, external clock source	
BIAS 1/2	**100**	0010-abX0-X	C	LCD 1/2 bias option ab = 00 : 2 commons option ab = 01 : 3 common option ab = 10 : 4 common option	
BIAS 1/3	**100**	0010-abX1-X	C	LCD 1/3 bias option ab = 00 : 2 commons option ab = 01 : 3 common option ab = 10 : 4 common option	
Reversed instruction	**100**	1110-0011-X	C	Reserved for the in wafer probing test	

EXT=1

Instruction	ID	Command Code	Data/command mode	Function	power on initial value
Analog off	**100**	1111-0100-X XXab-1011-X	C	a=1, regulator off b=1, follower off	00
Display COMMAND	**100**	1111-0101-X	C	display control command a=SHL: Com output scan direction b=ADC: SEG output correspondence c=REV: reverse display d=ALLON: all point on display	0000
	100	XXXX-abcd-X	C		
Set Static display	**100**	1111-001a-X	C	a=1 :static display on	off
Reset	**100**	1111-0000-X	C	Software Reset	

Note: X: Don't care;A5~ A0: RAM addresses;D3~D0: RAM data

All the bold forms, namely 1 1 0, 1 0 1, and 1 0 0, are mode commands. Of these, 1 0 0 indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the RW1025G after system reset.

■ Improving EFT/ESD immunity by using software techniques

Instruction and display data refresh are the most commonly used software techniques to improve EFT/ESD immunity. Registers in the instructions table and display data should be refreshed periodically in order to recover display content and function from corruption if EFT/ESD occurs. 0xE3H must be added to instruction refresh sequence.

※EFT/ESD refresh Command Summary for 4-SPI (type A IF0,IF1=1,0), 3-SPI and IIC interface

EXT=0										
Instruction	**A0**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**	**Description**
EFT/ESD command	0	1	1	1	0	0	0	1	1	Add this command into refresh sequence periodically for better EFT/ESD performance

※EFT/ESD refresh Command Summary for 4-SPI (type B IF0, IF1=1,1)

EXT=0				
Instruction	**ID**	**Command Code**	**Data/command mode**	**Description**
EFT/ESD command	**100**	**1110-0011-X**	**C**	Add this command into refresh sequence periodically for better EFT/ESD performance

➢ Command Format for 4-SPI (Type B)

The RW1025G can be configured by the S/W setting. There are two mode commands for 4-line interface (Type B) to configure the RW1025G resources and to transfer the LCD display data. The configuration mode of the RW1025G is called command mode, and its command mode ID is 1 0 0. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

Operating	Mode	ID
Read	Data	110
Write	Data	101
Read-Modify-Write	Data	101
Command	Command	100

The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely 1 0 0, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the CSB pin should be set to “1” and the previous operation mode will be reset also. Once the CSB pin returns to “0” a new operation mode ID should be issued first.

➢ Interfacing

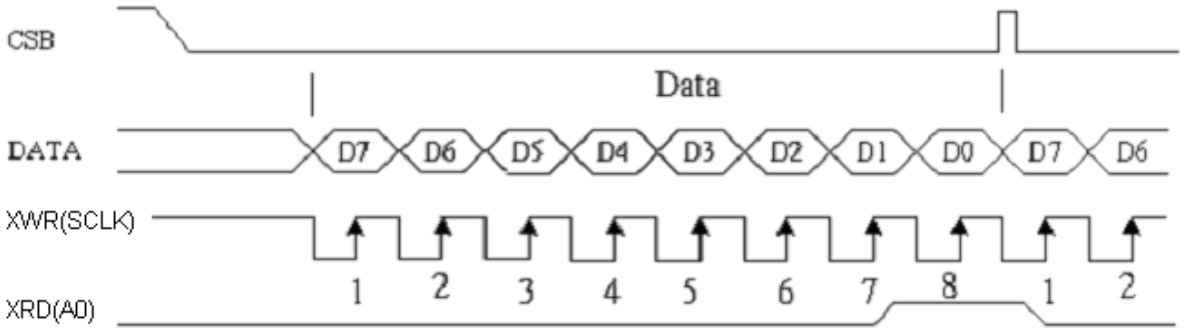
Only 2/3/4 lines are required to interface with the RW1025G. The CSB line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the RW1025G. If the CSB pin is set to 1, the data and command issued between the host controller and the RW1025G are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the RW1025G. The DATA line is the serial data input /output line.

Data to be read (Only available for Type B 4-line Interface) or written or commands to be written have to be passed through the DATA line. The RD line is the READ (or A0) clock input. Data in the RAM are clocked out on the falling edge of the RD signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the XRD signal. The XWR line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the RW1025G on the rising edge of the XWR signal.

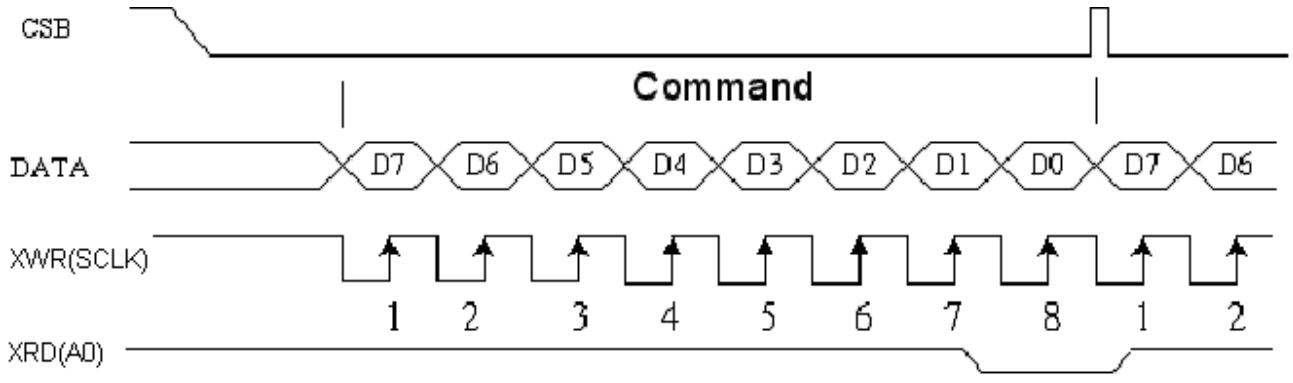
■ Interface Timing Diagrams

(1) 4-line Serial Interface (type A, IF0=0, IF1=1)

When entering data (parameters): **A0= HIGH,** A0 should be kept at high period of the clock pulse when the rising edge of the 8th SCLK is arrived.

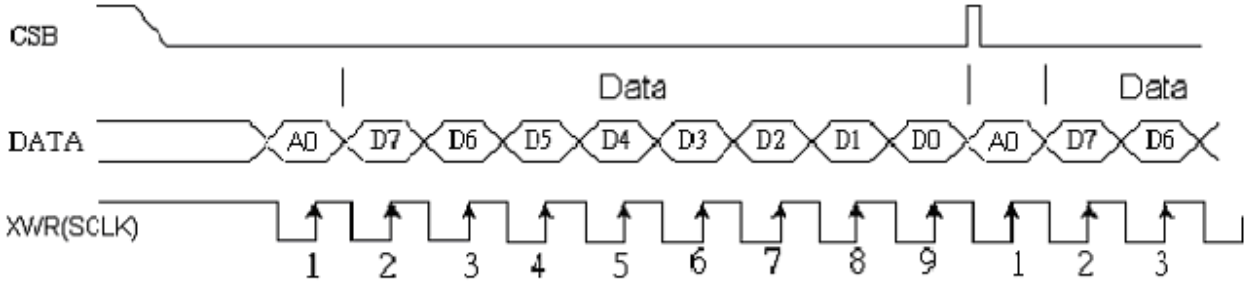


When entering command: **A0= LOW**, A0 should be kept at low period of the clock pulse when the rising edge of the 8th SCLK is arrived.

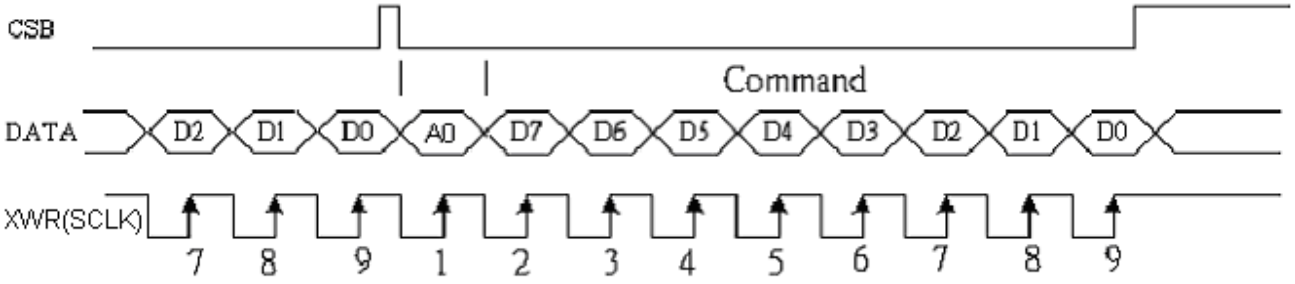


(2) 3-line Serial Interface (IF0=1,IF1=0)

When entering **data** (parameters): **A0 = HIGH** at the rising edge of the 1st SCLK.



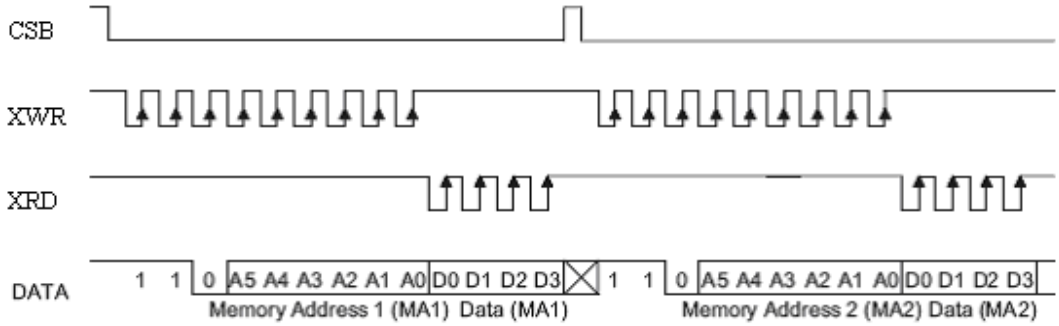
When entering **command**: **A0 = LOW** at the rising edge of the 1st SCLK



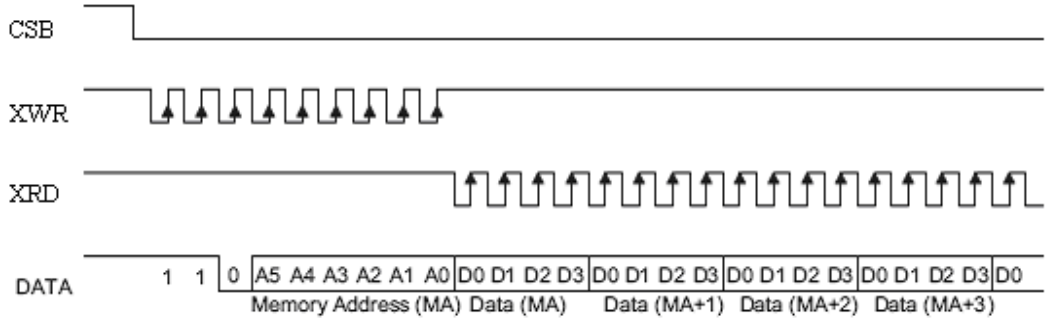
- If CSB is caused to HIGH before 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set CSB at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.
- When executing the command command/Data, set CSB to HIGH after writing the last address (after starting the 9th pulse in case of 9-bit serial input or after starting the 8th pulse in case of 8-bit serial input).

(3) 4-line Serial Interface (type B , IF0=1 , IF1=1)

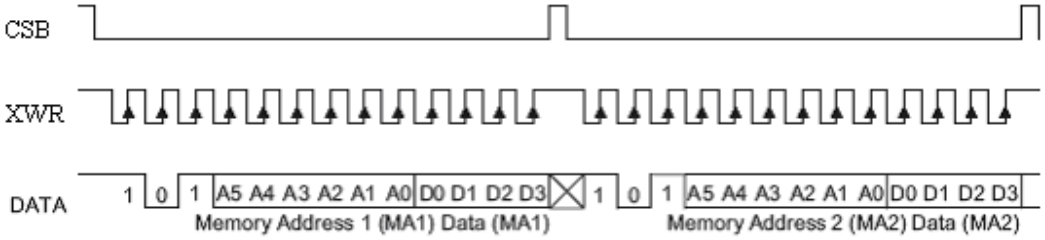
READ Mode (Command Code: 1 1 0)



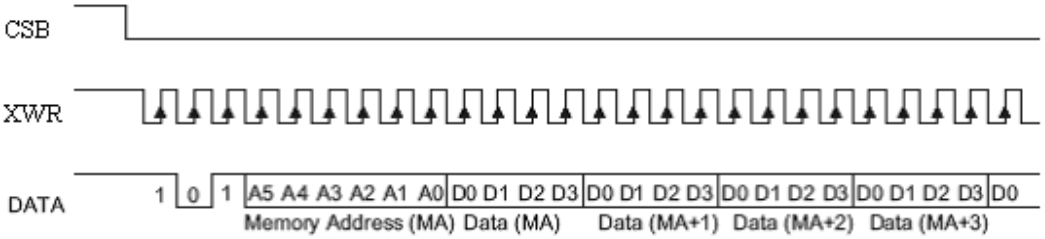
READ Mode (Successive Address Reading)



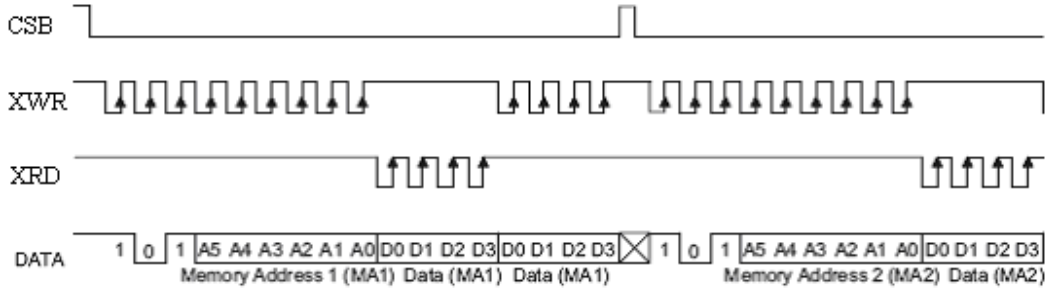
WRITE Mode (Command Code: 1 0 1)



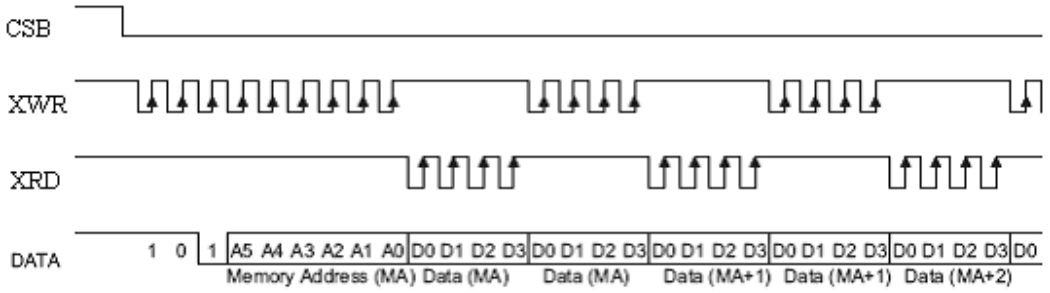
WRITE Mode (Successive Address Writing)



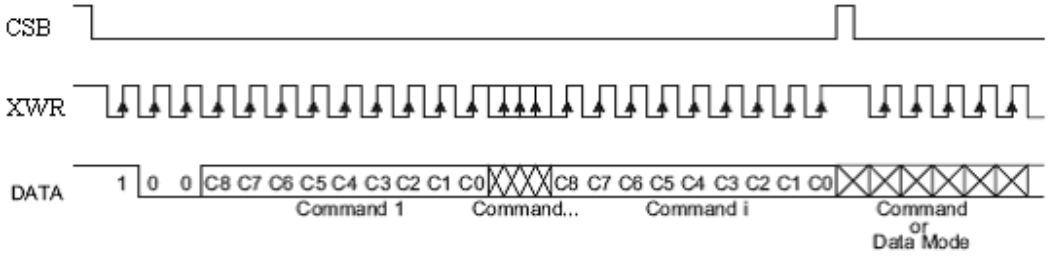
Read-Modify-Write Mode (Command Code: 1 0 1)



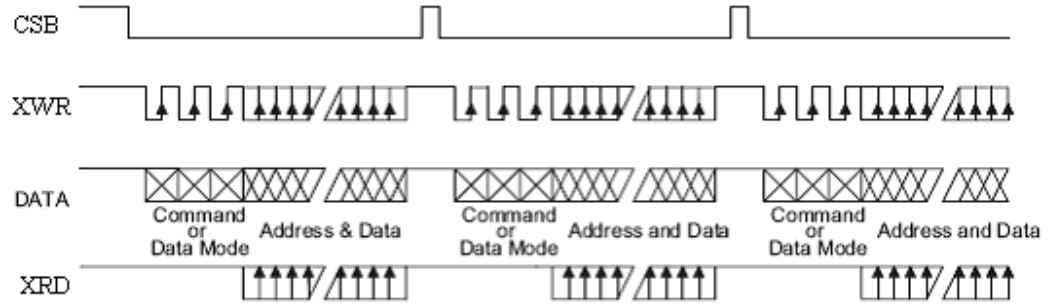
Read-Modify-Write Mode (Successive Address Accessing)



Command Mode (Command Mode: 1 0 0)



Mode (Data and Command Mode)



Note: It is recommended that controller should read in the data from the DATA line between the rising edge of XRD line and the falling edge of the next XRD line.

(4) IIC Interface (IF0=0, IF1=0)

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.
The IIC Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (DATA) and a Serial Clock line XWR (SCLK). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

➢ BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the DATA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure. 4

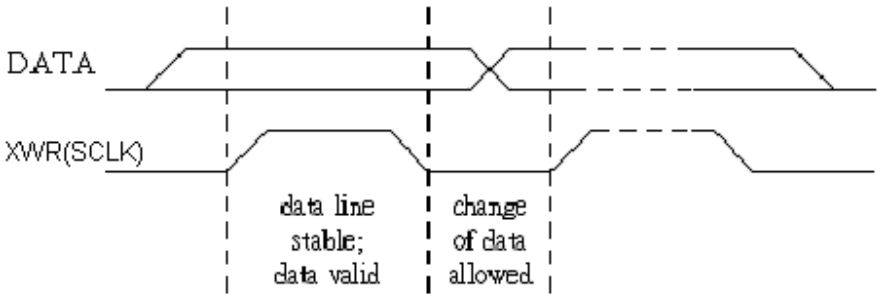


Figure.4

➢ START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure.5

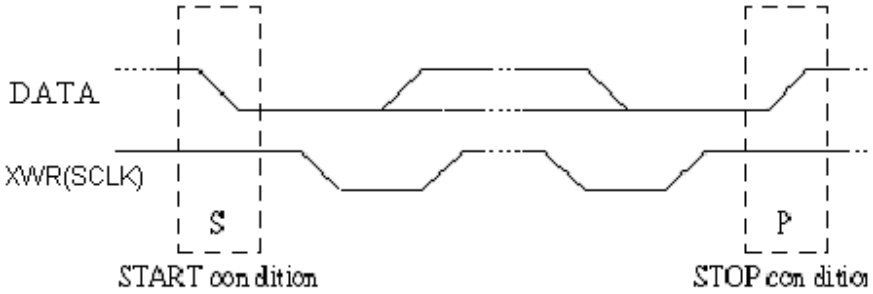


Figure 5. Definition of START and STOP conditions

·Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
· Slave: the device addressed by a master
· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
· Synchronization: procedure to synchronize the clock signals of two or more devices.

➢ ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the DATA line during the acknowledge clock pulse, so that the DATA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the IIC Interface is illustrated in Fig.6

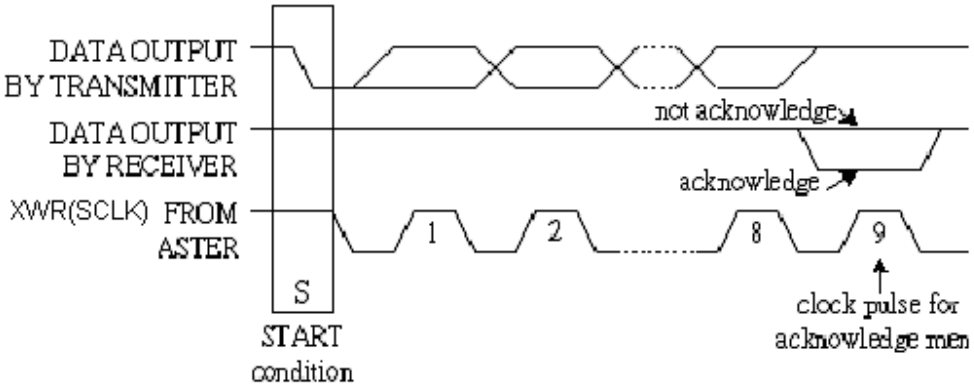


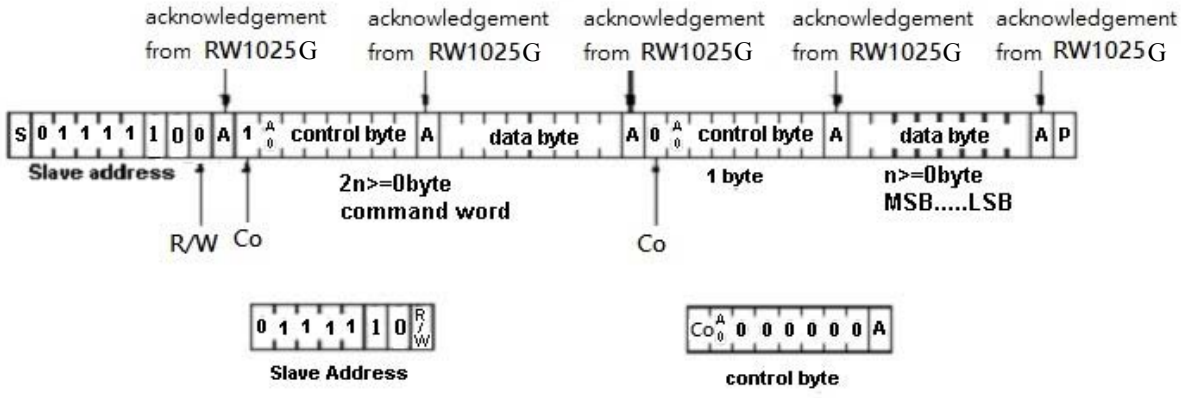
Fig 6. Acknowledgement on the 2-line Interface

➢ IIC Interface protocol

The RW1025G supports command, data write addressed slaves on the bus.
Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first.
The slave address (0111110) is reserved for the RW1025G.

The IIC Interface protocol is illustrated in Fig.7.

The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and A0, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended RW1025G device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC INTERFACE-bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.



R/W always "0".RW1025G can only be slave receiver

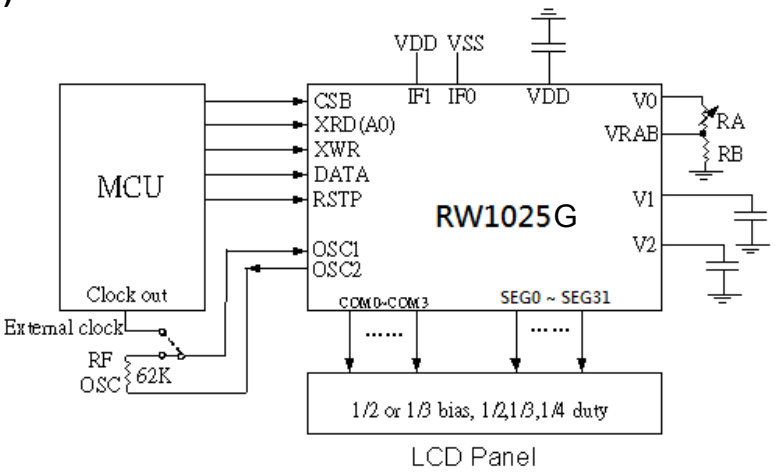
Fig 7. Acknowledgement on the 2-line Interface

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

A0	0	Write command
	1	Write data

■ Application Circuits

(1) Host Controller with an RW1025G Display System (using Internal V0 Regulator) for 4-SPI (Type A)

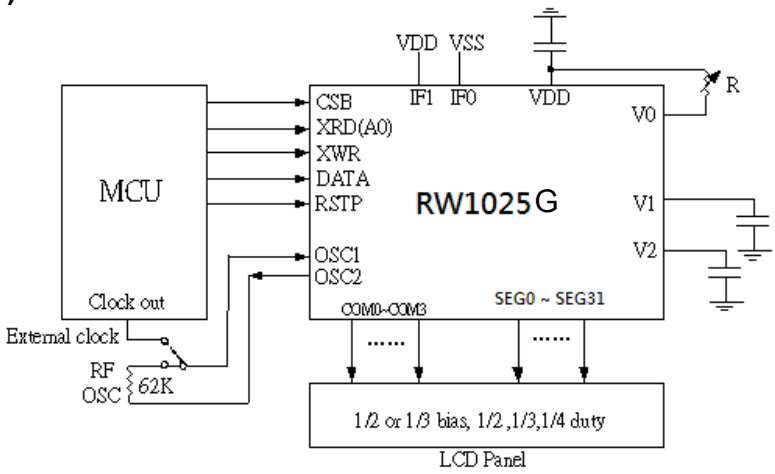


V0 = (1 + Ra/Rb) * 0.5*VDD

V1、V2 capacitor :0.1uF – 1uF

*** Note: Please keep VDD ≥ V0 ≥ V1 ≥ V2 ≥VSS**

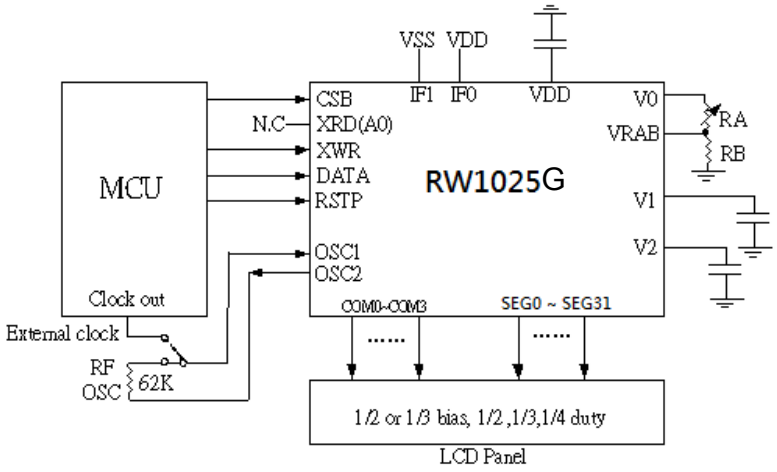
(2) Host Controller with an RW1025G Display System (using external V0 power input) for 4-SPI (Type A)



V1、V2 capacitor :0.1uF – 1uF

*** Note: Please keep VDD ≥ V0 ≥ V1 ≥ V2 ≥VSS**

(3) Host Controller with an RW1025G Display System (using internal V0 regulator) for 3-SPI

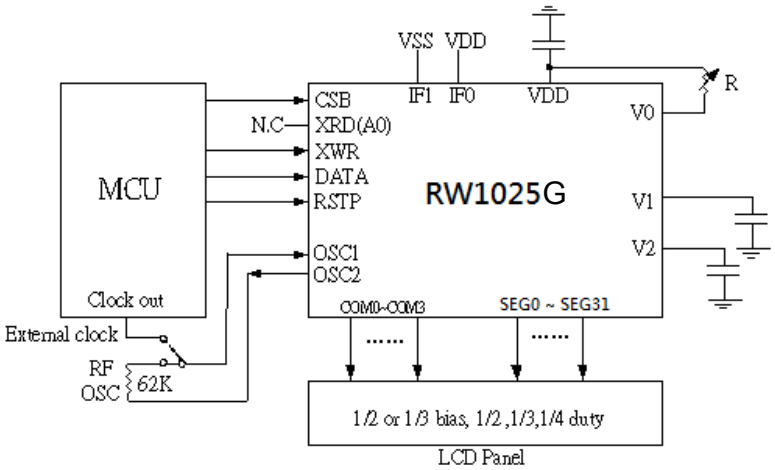


V0 = (1 + Ra/Rb) * 0.5*VDD

V1、V2 capacitor :0.1uF – 1uF

*** Note: Please keep VDD ≥ V0 ≥ V1 ≥ V2 ≥VSS**

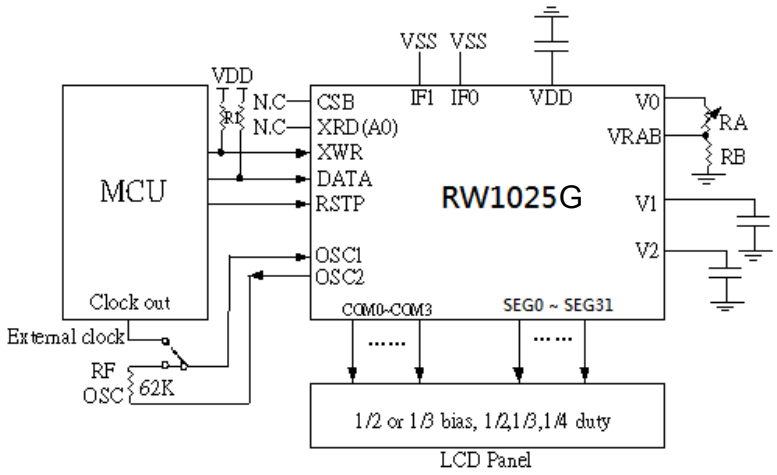
(4) Host Controller with an RW1025G Display System (use external V0 power input) for 3-SPI



V1、V2 capacitor :0.1uF – 1uF

*** Note: Please keep VDD ≥ V0 ≥ V1 ≥ V2 ≥VSS**

(5) Host Controller with an RW1025G Display System (using internal V0 regulator) for IIC



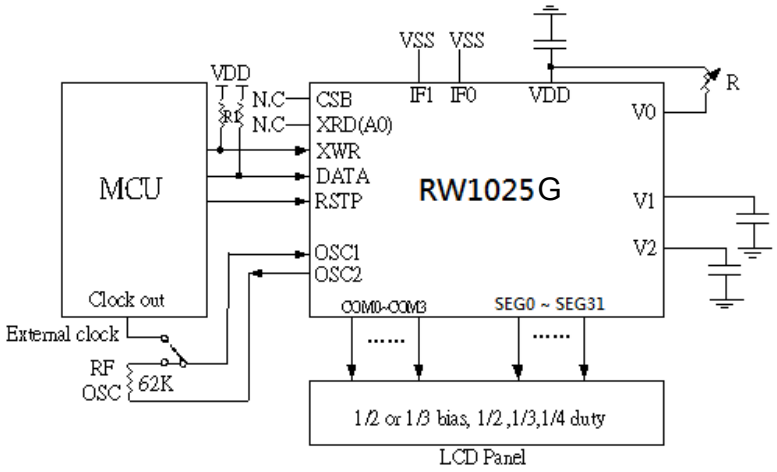
V0= (1 + Ra/Rb) * 0.5*VDD

R1 resistor about: 1K~2.2K

V1、V2 capacitor :0.1uF – 1uF

*** Note: Please keep VDD ≥ V0 ≥ V1 ≥ V2 ≥VSS**

(6) Host Controller with an RW1025G Display System (use external V0 power input) for IIC

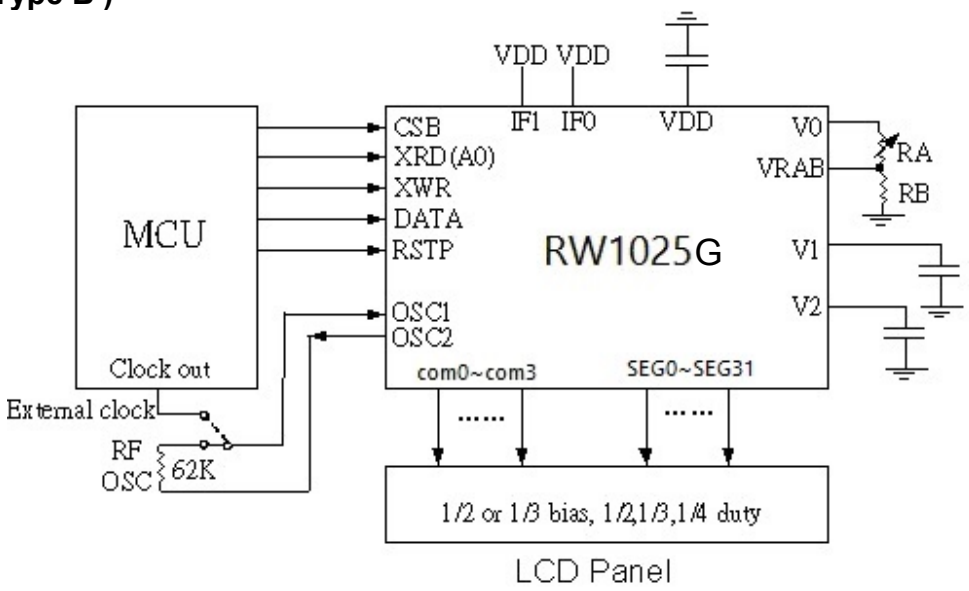


R1 resistor about: 1K~2.2K

V1、V2 capacitor :0.1uF – 1uF

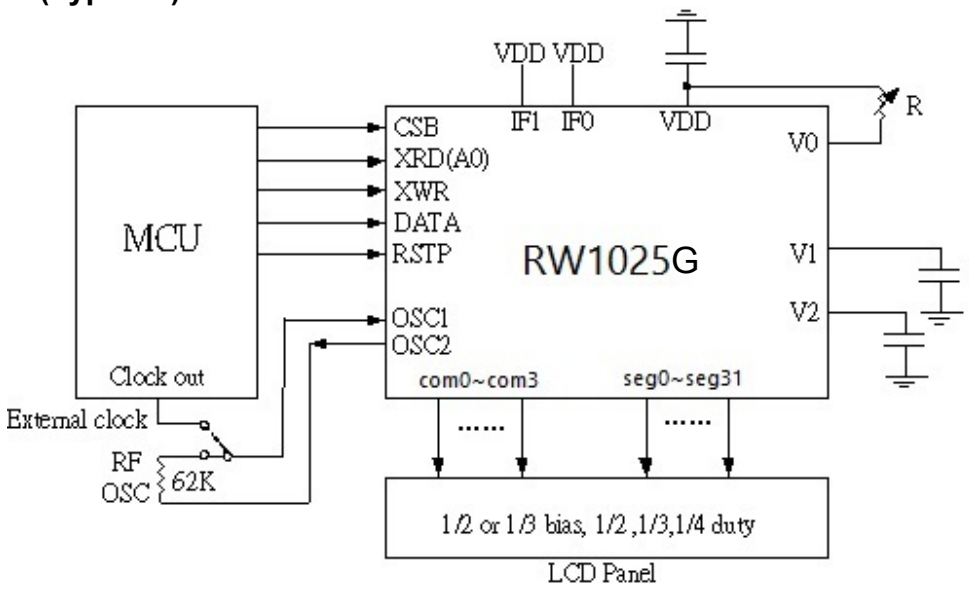
*** Note: Please keep VDD ≥ V0 ≥ V1 ≥ V2 ≥VSS**

(7) Host Controller with an RW1025G Display System (using Internal V0 Regulator) for 4-SPI (Type B)



V0= (1 + Ra/Rb) * 0.5*VDD
R1 resistor about: 1K~2.2K
V1、V2 capacitor :0.1uF – 1uF
*** Note: Please keep VDD ≥ V0 ≥ V1 ≥ V2 ≥VSS**

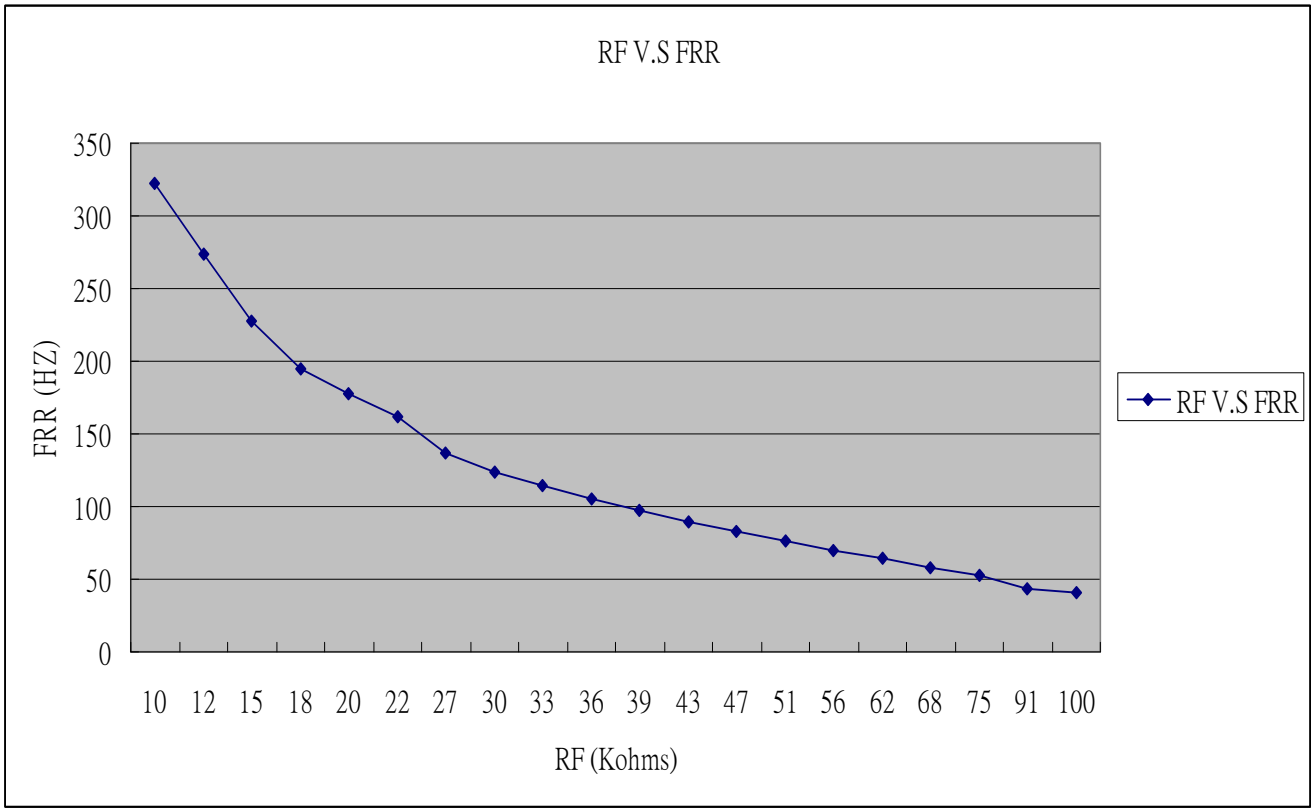
(8) Host Controller with an RW1025G Display System (using external V0 power input) for 4-SPI (Type B)



R1 resistor about: 1K~2.2K
V1、V2 capacitor :0.1uF – 1uF
*** Note: Please keep VDD ≥ V0 ≥ V1 ≥ V2 ≥VSS**

■ RF OSC V.S Frame Frequency

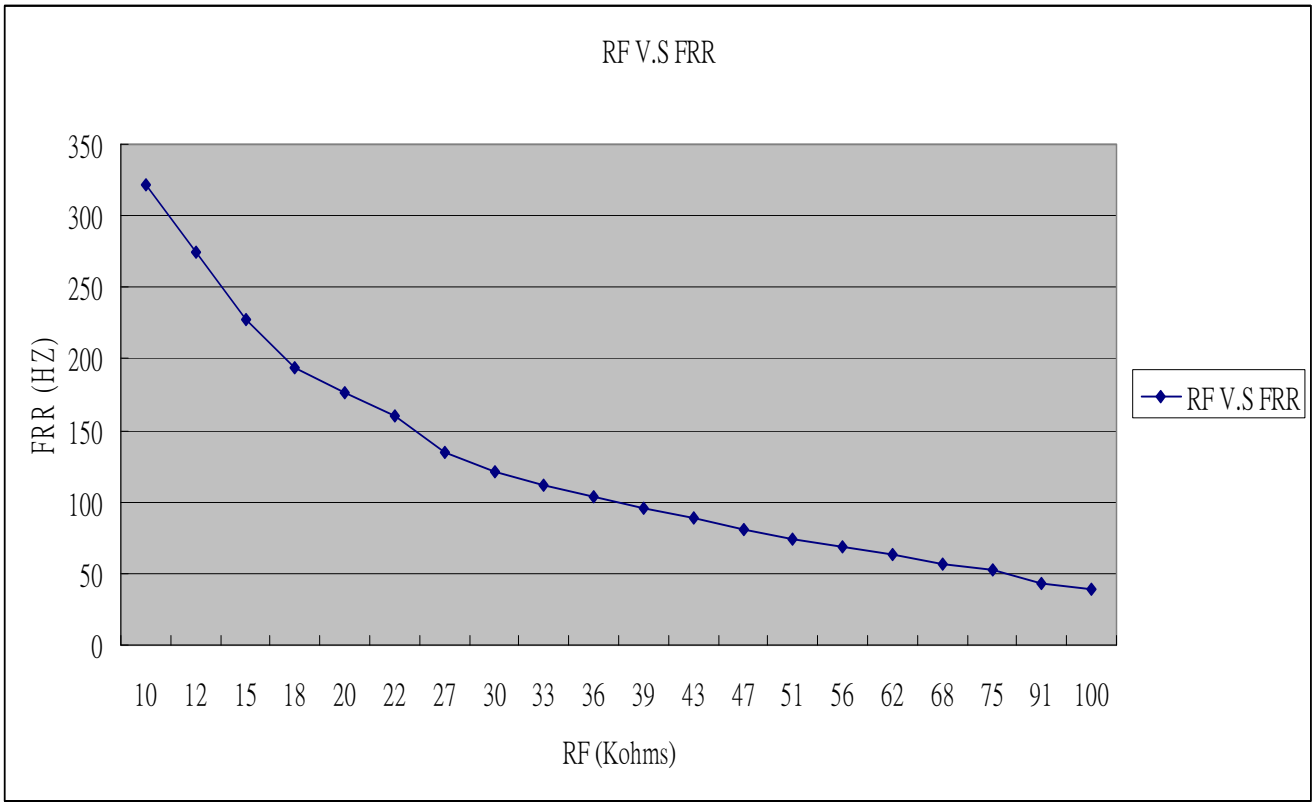
(VDD=3.3V)



(VDD=3.3V, Ta=25 °C) (+/- 10%)

RF	OSC (KHz)	FRR (Hz)	RF	OSC (KHz)	FRR (Hz)	RF	OSC (KHz)	FRR (Hz)	RF	OSC (KHz)	FRR (Hz)
10K	1.28M	322	27K	546	137	47K	338	83	91K	180	44
12K	1.1	274	30K	498	124	51K	309	76	100K	166	41
15K	909	227	33K	463	114	56K	286	70			
18K	775	195	36K	424	105	62K	258	64			
20K	709	177	39K	397	98	68K	237	58			
22K	654	162	43K	365	90	75K	216	53			

(VDD=5.0V)



(VDD=5.0V, Ta=25 °C) (+/- 10%)

RF	OSC (KHz)	FRR (Hz)	RF	OSC (KHz)	FRR (Hz)	RF	OSC (KHz)	FRR (Hz)	RF	OSC (KHz)	FRR (Hz)
10K	1.28M	322	27K	546	134	47K	338	81	91K	180	43
12K	1.1	274	30K	498	121	51K	309	74	100K	166	39
15K	909	227	33K	463	112	56K	286	69			
18K	775	194	36K	424	103	62K	258	63			
20K	709	176	39K	397	95	68K	237	56			
22K	654	160	43K	365	89	75K	216	52			