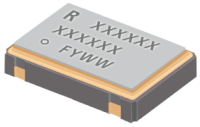
RXO5032M

SMD Clock Oscillator

High Performance XO in 5 x 3.2 mm Surface Mount package



Product description

The RXO5032M offers ultra low RMS phase jitter in a small 5 x 3.2 mm SMD package (including a low profile 1mm height option for CMOS products). Available in hundreds of industry standard frequencies from 1MHz to 200MHz, as well as for custom frequency development.

Applications

- Base stations
- Communications
- Consumer
- DSL/ADSL
- Ethernet
- Wi-Fi
- WiMAX/W-LAN

Features

- Ultra Low Jitter 0.05 to 0.3 ps integrated 12 kHz to 20 MHz
- Excellent temperature stability
- CMOS, LVPECL, LVDS, or HCSL output options
- Wide frequency range
- Low power differential outputs
- Small form factor

Specifications

1.0 SPECIFICATION REFERENCES

Line	Parameter	Description
1.1	Model Description	RXO5032M XO
1.2	Reference Number	
1.3	Rakon Part Number	

2.0 FREQUENCY CHARACTERISTICS

Line	Parameter	Test Condition	Value	Unit
2.1	Frequency		1 to 200	MHz
2.2	Operating Temperature Range	Operable -40 to 85°C	-10 to 70	°C
2.3	Frequency Stability	Including Temperature range, Supply variation, Load variation and 10 years aging at 25°C	±30 to 50	ppm
2.4	Temperature Stability	Temperature range only	±10 to 20	ppm
2.5	Frequency Aging	First year	±3	ppm

3.0 POWER SUPPLY

Line	Parameter	Test Condition	Value	Unit
3.1	Supply Voltage (VDD)	With a tolerance of ±10%	3.3	V
3.2	Supply Voltage (VDD)	With a tolerance of ±5%	2.5	V
3.3	Supply Current	For LVCMOS (To be specified based on frequency and voltage)	6 to 40	mA
3.4	Supply Current	For LVPECL/LVDS	65 max	mA
3.5	Supply Voltage (VDD)	With a tolerance of ±10%	5	V

4.0 OUTPUT CHARACTERISTICS - LVCMOS

Line	Parameter	Test Condition	Value	Unit
4.1	Output Voltage (Vol)		10 max	%VDD
4.2	Output Voltage (Voh)		90 min	%VDD
4.3	Output load		15	pF
4.4	Duty Cycle	@ 50% VDD	40 to 60	%
4.5	Rise Time / Fall Time	80%/20% (To be specified based on frequency and voltage)	1 to 10	ns
4.6	RMS Phase Jitter	Integrated 12kHz to 20MHz	0.05 to 0.3	ps
4.7	Startup Time		10 max	ms

5.0 OUTPUT CHARACTERISTIC - LVPECL

Line	Parameter	Test Condition	Value	Unit
5.1	Output Voltage (Vol)	50Ω nominal load. (VDD - 1.6V) max.		
5.2	Output Voltage (Voh)	50Ω nominal load. (VDD - 1.03V) min.		
5.3	Duty Cycle	@ VDD-1.3 V	45 to 55	%
5.4	Rise Time / Fall Time	80%/20%	1 max	ns
5.5	RMS Phase Jitter	Integrated 12kHz to 20MHz	0.05 to 0.3	ps
5.6	Startup Time		10 max	ms

6.0 OUTPUT CHARACTERISTICS - LVDS

Line	Parameter	Test Condition	Value	Unit
6.1	Differential Output: Voltage Swing (Vod)		350	mV
6.2	Duty Cycle	Measured at 1.25 V	45 to 55	%
6.3	Rise Time / Fall Time	RL = 100 Ω / CL = 10 pF	1 max	ns
6.4	RMS Phase Jitter	Integrated 12kHz to 20MHz	0.05 to 0.3	ps
6.5	Startup Time		10 max	ms

7.0 PIN CONNECTIONS - 4 PIN PACKAGE

Line	Parameter	Description
7.1	Pin 1	E/D* or NC
7.2	Pin 2	GND
7.3	Pin 3	OUTPUT
7.4	Pin 4	VDD
7.5	* Output Enabled	>70% of VDD on E/D pin, or E/D pin left open (connected to internal pull-up resistor)
7.6	* Output Disabled	<30% of VDD on E/D pin, or E/D pin to GND

8.0 PIN CONNECTIONS - 6 PIN PACKAGE

Line	Parameter	Description
8.1	Pin 1	E/D* or NC
8.2	Pin 2	E/D* or NC
8.3	Pin 3	GND
8.4	Pin 4	OUTPUT
8.5	Pin 5	COMPLIMENTARY OUTPUT (LVPECL/LVDS only), or E/D*, or N/C
8.6	Pin 6	VDD
8.7	* Output Enabled	>70% of VDD on E/D, or E/D pin left open (connected to internal pull-up resistor)
8.8	* Output Disabled	<30% of VDD on E/D, or E/D pin to GND

9.0 PACKAGE DETAIL

Line	Parameter	Description
9.1	Package type	G45, or G4L, or G65, or F
9.2	Top line	[R ######] Part identifier
9.3	Middle line	[######] Part information
9.4	Bottom line	[o FYWW] Pin 1, Manufacturing code, Year code* and Week code**
9.5	* Year code	A = 2010, B = 2011, C = 2012, D = 2013, ... Z = 2035
9.6	** Week Code	WW = 01 = Week of first Monday of the year

10.0 ENVIRONMENTAL SPECIFICATION

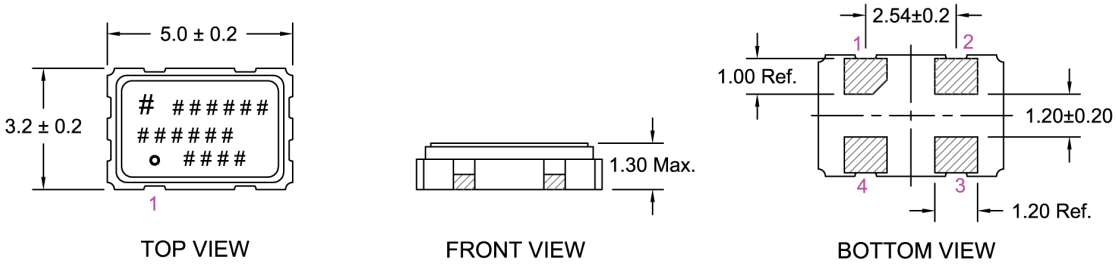
Line	Parameter	Description
10.1	Mechanical Shock	MIL-STD-883, Method 2002
10.2	Storage Temperature Range	-55 to 125 °C
10.3	Humidity	After 48 hours at 85 °C±2 °C 85 % relative humidity non-condensing
10.4	Thermal Shock	MIL-STD-883, Method 1011
10.5	Vibration	MIL-STD-883, Method 2007
10.6	Gross and Fine Leak	MIL-STD-883, Method 1014
10.7	RoHS Compliant	Yes

11.0 MANUFACTURING INFORMATION

Line	Parameter	Description
11.1	Packaging Description	Tape and Reel. Standard packing quantity is 1000 per reel (CAT029), or 2000 per reel (CAT687)
11.2	Reflow	Solder reflow process as per attached profile

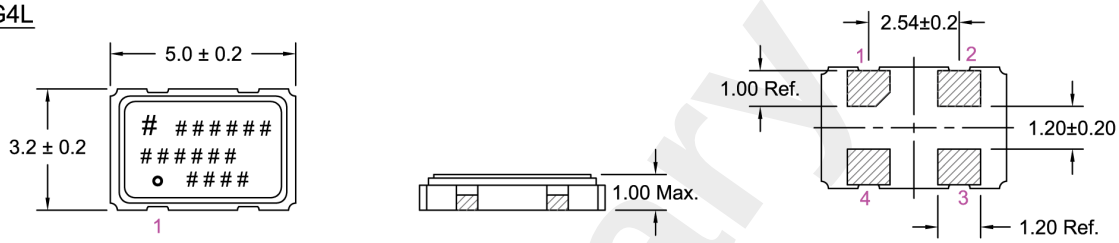
Drawing Name: XO 5032 4-Pin Model Drawing

PACKAGE G45



TOP VIEW | FRONT VIEW | BOTTOM VIEW

PACKAGE G4L

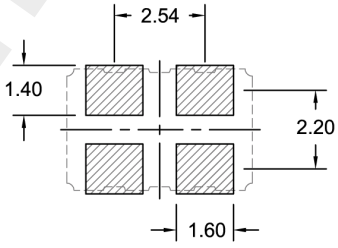


TOP VIEW | FRONT VIEW | BOTTOM VIEW

NOTE : 1. PIN CONNECTIONS ARE DETAILED IN THE SPECIFICATION.
2. MARKING INFORMATION IS DETAILED IN THE SPECIFICATION.

RECOMMENDED PAD LAYOUT - Top View

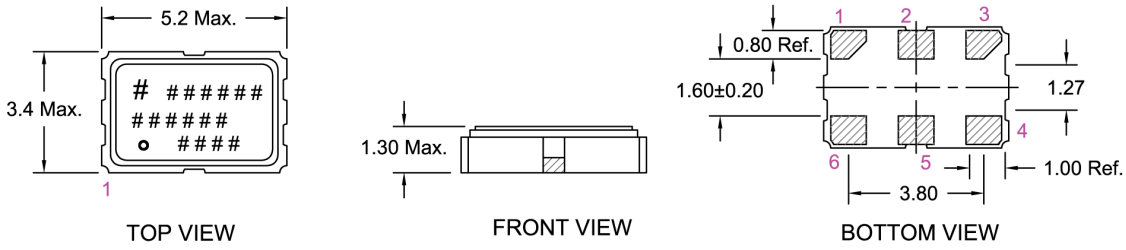
PACKAGE G45 AND G4L



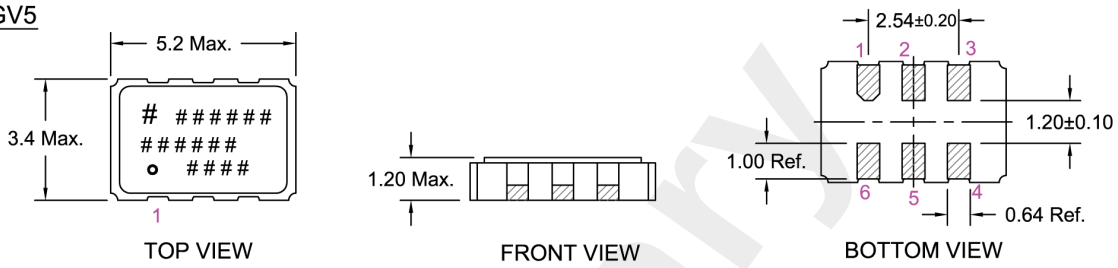
TITLE: XO 5032 4-PIN MODEL	FILENAME: CAT686	TOLERANCES:
RELATED DRAWINGS:	REVISION: A	XX =
	DATE: 01-May-12	X.X = ±0.15
	SCALE: 5 : 1	X.XX = ±0.10
	Millimetres	X.XXX =
		X° =
		Hole =

Drawing Name: XO/VCXO 5032 6-Pin Model Drawing

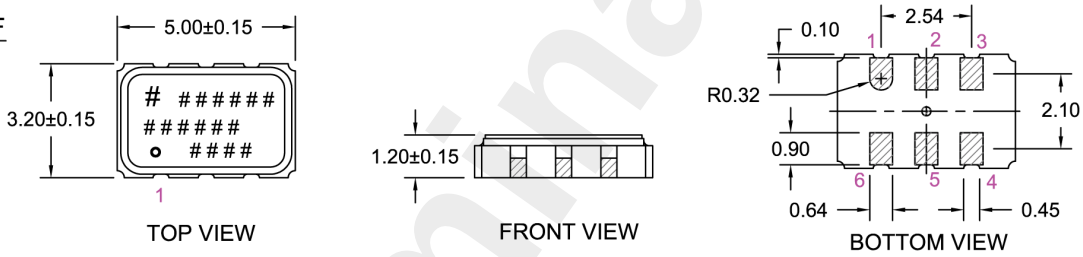
PACKAGE G65



PACKAGE GV5



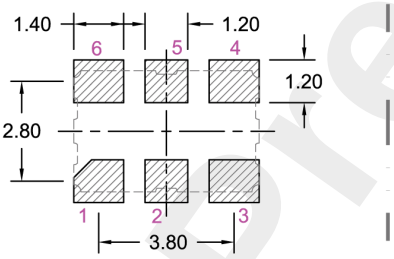
PACKAGE F



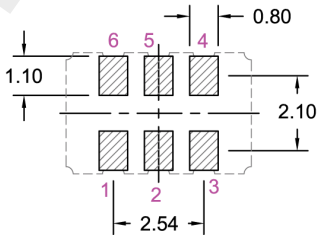
NOTE :
1. PIN CONNECTIONS ARE DETAILED IN THE SPECIFICATION.
2. MARKING INFORMATION IS DETAILED IN THE SPECIFICATION.

RECOMMENDED PAD LAYOUT - Top View

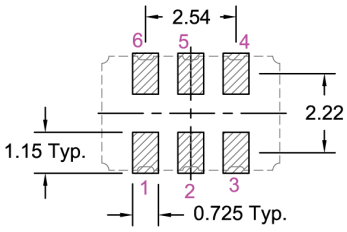
PACKAGE G65



PACKAGE GV5



PACKAGE F



TITLE: XO/VCXO 5032 6-PIN MODEL	FILENAME: CAT026	TOLERANCES:	
RELATED DRAWINGS:	REVISION: C	XX	=
	DATE: 01-May-12	X.X	= ±0.15
	SCALE: 5 : 1	X.XX	= ±0.10
	Millimetres	X.XXX	=
		X°	=
		Hole	=

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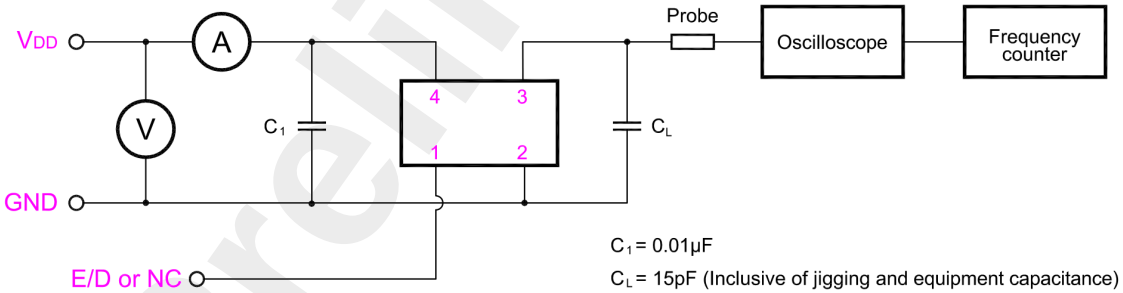
Drawing Name: XO 4 Pin Series Test Circuit

CMOS/LVCMOS TEST CIRCUIT



C_1 = 0.01µF

C_L = 15pF (Inclusive of jigging and equipment capacitance)

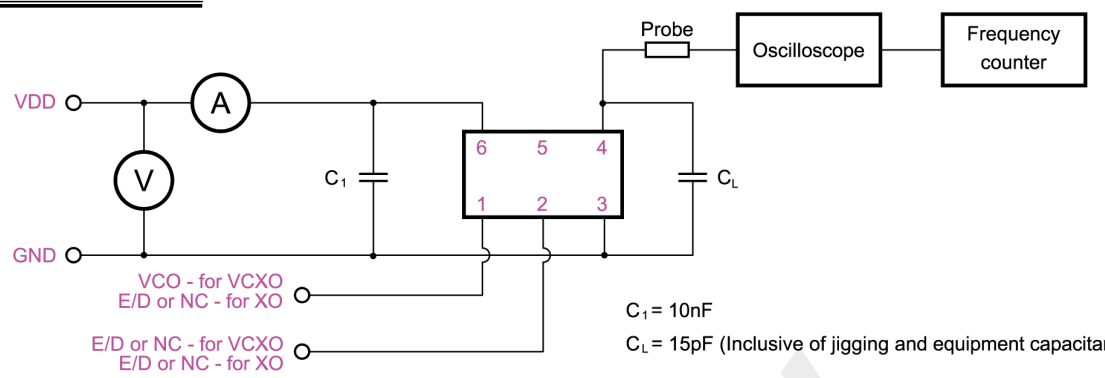
NOTE:

THIS SERIES HAS NO BY PASS CAPACITOR. WE RECOMMEND OUR CUSTOMER USE CAPACITOR 0.01µF BETWEEN V_{DD} AND GND.

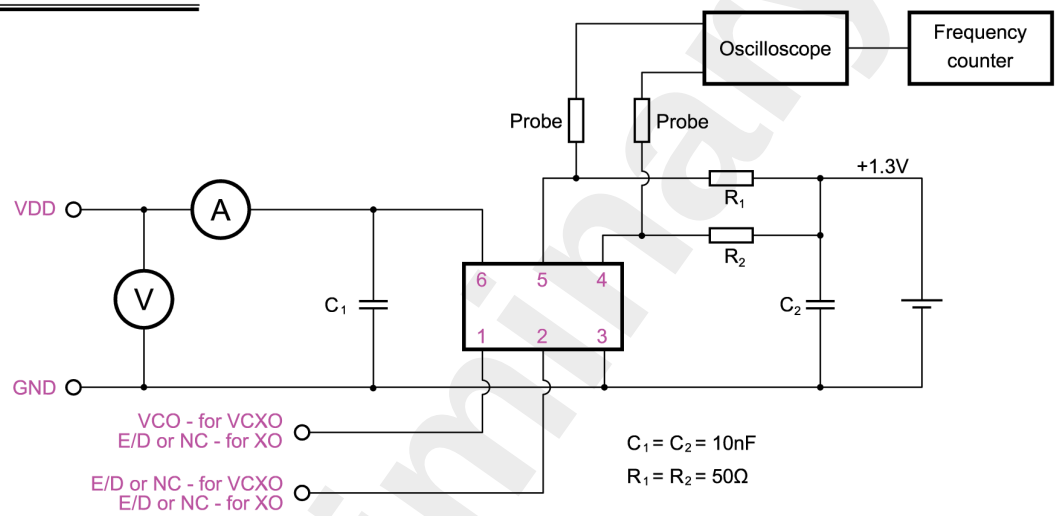
TITLE: XO 4 PIN TEST CIRCUIT	FILENAME: CAT616
RELATED DRAWINGS:	REVISION: C
	DATE: 03 May-12
	SCALE: NTS
	Millimetres

Drawing Name: XO/VCXO 6 Pin Series Test Circuit

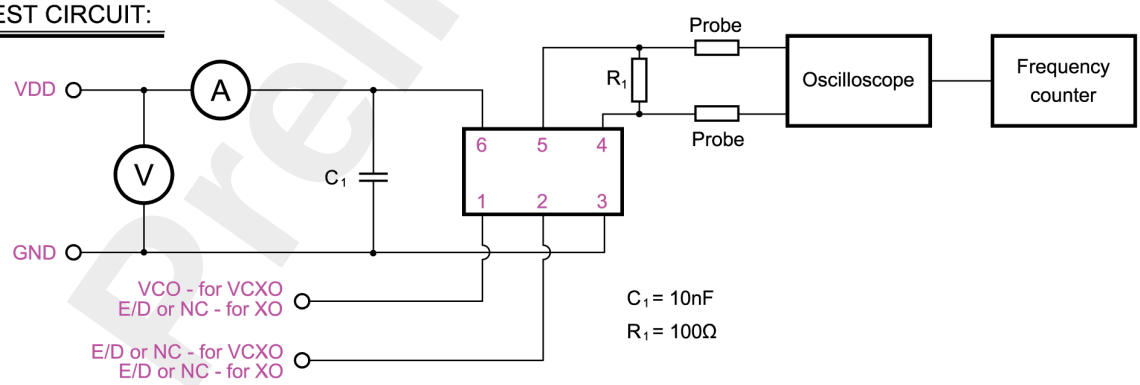
LVCMOS TEST CIRCUIT:



LVPECL TEST CIRCUIT:



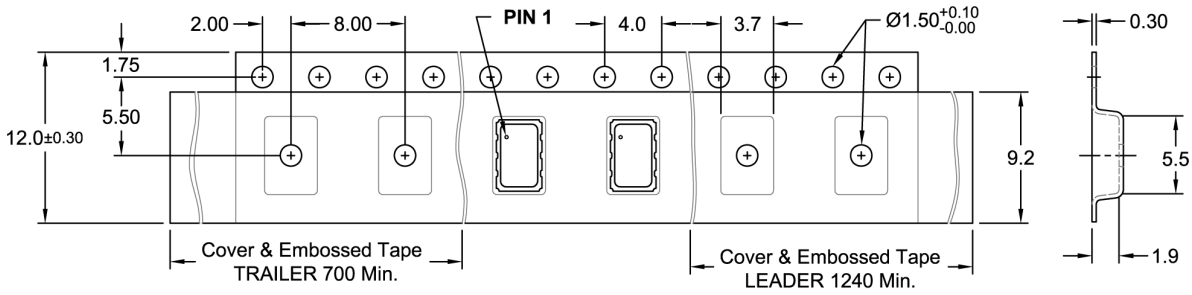
LVDS TEST CIRCUIT:



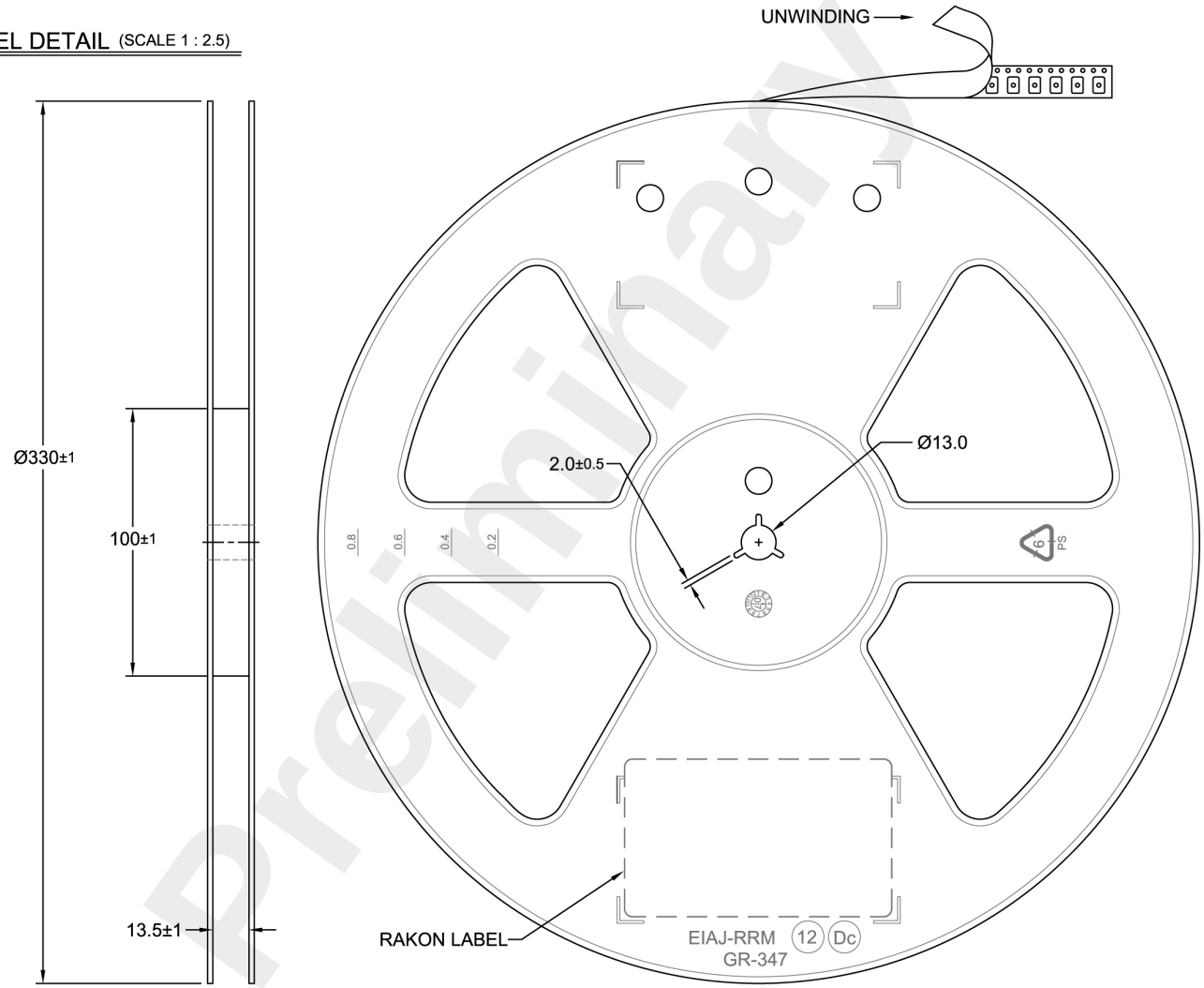
TITLE: XO/VCXO 6 PIN SERIES TEST CIRCUIT	FILENAME: CAT088
RELATED DRAWINGS:	REVISION: F
	DATE: 03-May-12
	SCALE: 1 : 1
	Millimetres

Drawing Name: XO/VCXO5032 F Series Tape & Reel

TAPE DETAIL (SCALE 2 : 1)



REEL DETAIL (SCALE 1 : 2.5)



TITLE: XO / VCXO 5032 F SERIES TAPE & REEL	FILENAME: CAT029	TOLERANCES:
RELATED DRAWINGS:	REVISION: B	XX =
	DATE: 14-Oct-11	X.X = ±0.1
	SCALE: 2 : 1	X.XX = ±0.05
	Millimetres	X.XXX =
		X° =
		Hole =

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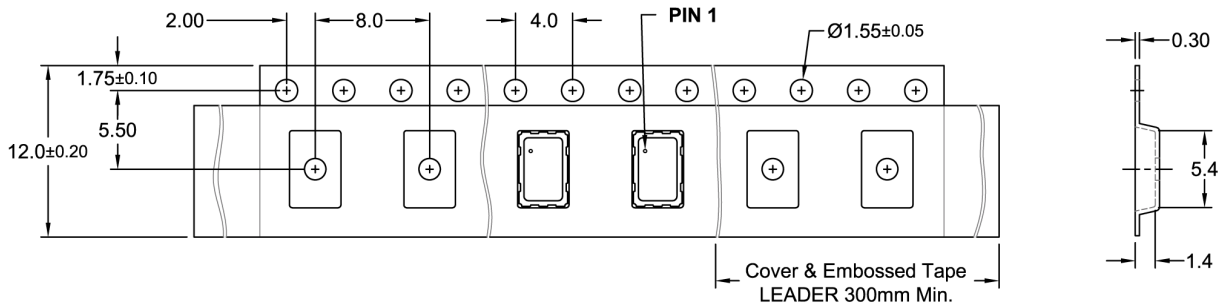
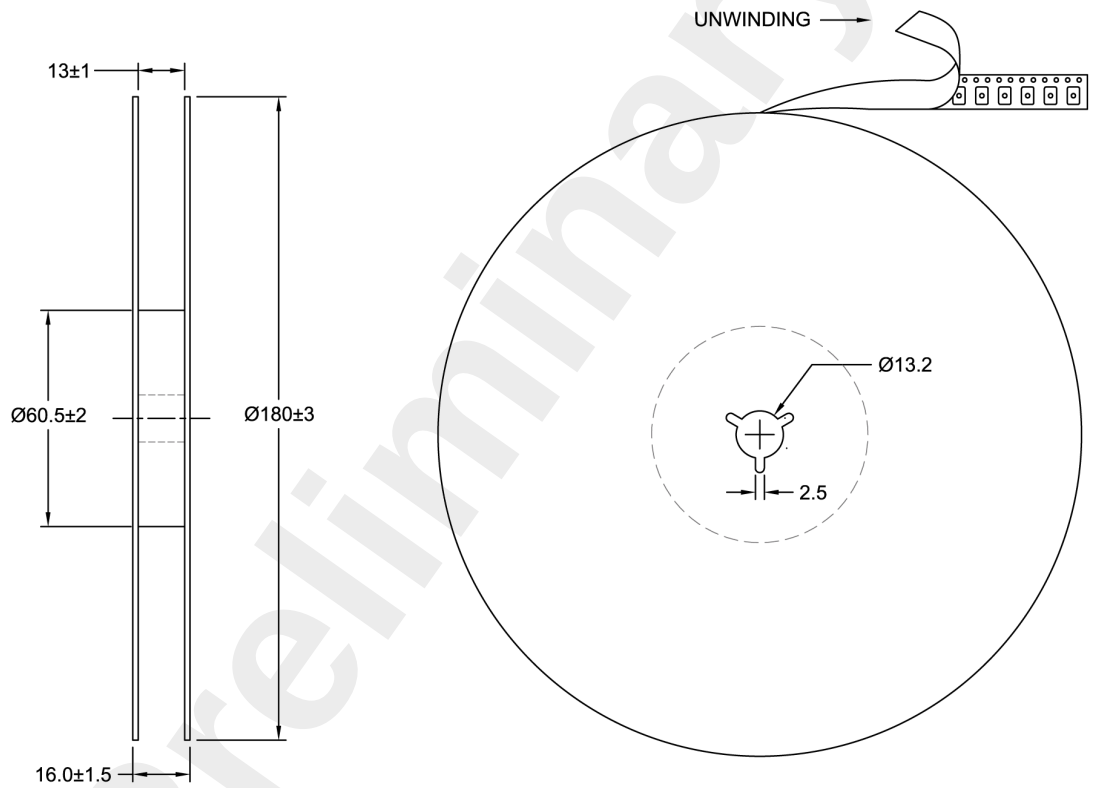
Drawing Name: XO/VCXO 5032 G Tape & Reel

TAPE DETAIL (SCALE 2 : 1)



REEL DETAIL (SCALE 1 : 2.5)



TITLE: XO / VCXO 5032 G TAPE & REEL	FILENAME: CAT687	TOLERANCES:	
RELATED DRAWINGS:	REVISION: A	XX =	
	DATE: 03-Apr-12	X.X = ±0.1	
	SCALE: 2 : 1	X.XX = ±0.05	
	Millimetres	X.XXX =	
		X° =	
		Hole =	

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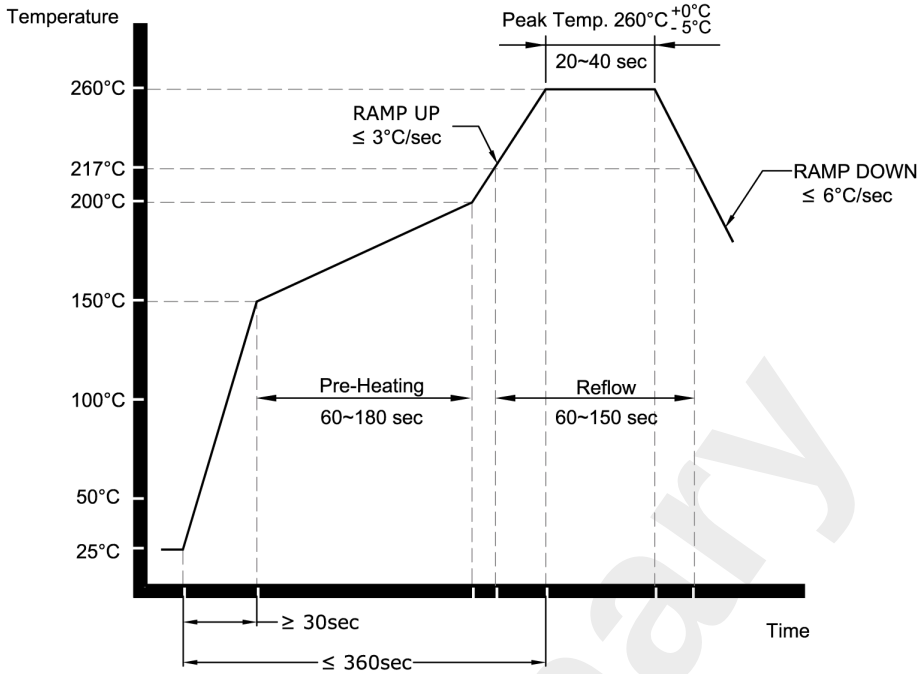
Drawing Name: Pb-Free Reflow



NOTE:
The product has been tested to withstand the Reflow Profile shown. The Reflow Profile used to solder Rakon products is determined by the solder paste Manufacturer's specification. It is recommended that the Reflow Profile used does not exceed the one shown above.

TITLE: Pb-FREE REFLOW	FILENAME: CAT541
RELATED DRAWINGS:	REVISION: B
	DATE: 05-Sep-11
	SCALE: NTS
	Millimetres