![iWave — Embedding Intelligence]

System On Module RainboW-G17M-Q7
Cyclone V SoC Qseven Module

iWave Systems launching world's first Altera's Cyclone V SX SoC FPGA based Qseven compatible module for the increased system performance requirements. The Dual ARM Cortex A9 core with the FPGA allows greater flexibility for the system designers and helps to lower the system cost and power consumption. The improved logic integration with integrated high speed transceivers and hard memory controllers provides increased bandwidth capacity which is ideal for cost-sensitive high end applications.

APPLICATIONS: Industrial Automation, Smart Energy Systems, Video Surveillance, Defense & Aerospace

iW-RainboW-G17M-Q7 HIGHLIGHTS

ARM Cortex A9 Dual core CPU integrated with FPGA with up to 110K LEs

Enhanced with integrated transceivers and hard memory controller

Readily available FPGA IP cores for integration

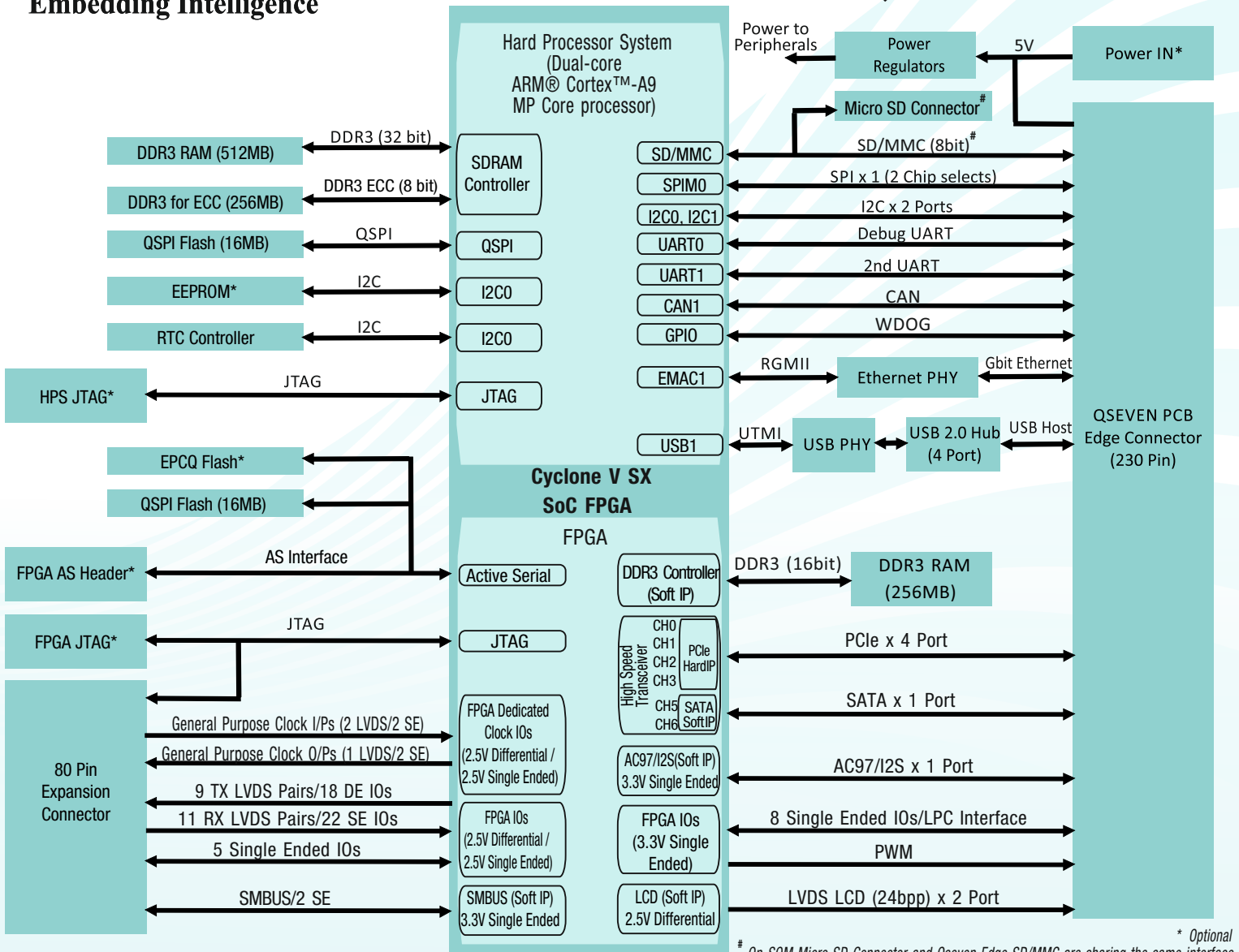R2.0 Qseven compatible module

SPECIFICATIONS

CPU:	
Altera's Cyclone V SX SoC FPGA	
• Integrated Dual core ARM Cortex-A9 Hard Processor System(HPS)	
• FPGA with upto 110K LEs	

Memory:
512MB DDR3 with ECC for HPS
16MB QSPI Flash
On-SOM Micro SD Connector [#]
256MB DDR3 for FPGA
EPCQ Flash* / QSPI Flash for FPGA
EEPROM*

On Board Peripherals Support:
JTAG Header for FPGA*
JTAG Header for HPS*
DIP Switch for boot settings
RTC controller

80 Pin Expansion Connector:
FPGA IOs (Up to 45 Single Ended IOs - SE IOs)
9 TX LVDS Pairs / 18 SE IOs
11 RX LVDS Pairs / 22 SE IOs
5 Single Ended IOs

FPGA Dedicated Clock IOs:
General Purpose Clock Inputs (2 LVDS/2 SE)
General Purpose Clock Outputs (1 LVDS/2 SE)

Others:
SMBUS / 2 SE IOs
FPGA JTAG

Qseven PCB Edge Connector Interfaces:
From HPS:
Gigabit Ethernet - 1 Port (On-SOM PHY)
USB 2.0 Host - 4 Ports (On-SOM HUB)
CAN - 1 Port
SD/MMC (8 bit) [#]
WDOG - 1 Port
I2C - 2 Ports
SPI - 1 Port
Debug UART - 1 Port
2nd UART - 1 Port
Other Control IOs - Through HPS
From FPGA[+]:
LVDS LCD - 2 Ports (FPGA Soft IP)/ 23 SE IOs
AC97/I2S Audio (FPGA Soft IP)/ 5 SE IOs
PWM
FPGA IOs - 8 SE IOs
From FPGA High Speed Transceivers[+]:
PCIe Gen1 x 4 Lane
SATA (FPGA Soft IP)
Form Factor:
70mm x 70mm Qseven Specification 2.0
Power Input:
5V DC
Operating Temperature:
-40°C to +85°C Industrial
Operating System:
WEC7, Linux

* Optional

[#] On-SOM Micro SD Connector and Qseven Edge SD/MMC are sharing the same interface

[+] If the FPGA interfaces available in the Qseven edge are not used for Qseven compliance requirement, same interface pins can be used for custom Industrial/networking interface requirements.

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CYCLONE V SoC Qseven SOM BLOCK DIAGRAM

Block diagram showing:

- Hard Processor System (Dual-core ARM® Cortex™-A9 MP Core processor)
- DDR3 RAM (512MB) — DDR3 (32 bit) — SDRAM Controller
- DDR3 for ECC (256MB) — DDR3 ECC (8 bit)
- QSPI Flash (16MB) — QSPI — QSPI
- EEPROM* — I2C — I2C0
- RTC Controller — I2C — I2C0
- HPS JTAG* — JTAG — JTAG
- Power Regulators — 5V — Power IN*
- Power to Peripherals
- Micro SD Connector#
- SD/MMC — SD/MMC (8bit)#
- SPIM0 — SPI x 1 (2 Chip selects)
- I2C0, I2C1 — I2C x 2 Ports
- UART0 — Debug UART
- UART1 — 2nd UART
- CAN1 — CAN
- GPIO — WDOG
- EMAC1 — RGMII — Ethernet PHY — Gbit Ethernet
- USB1 — UTMI — USB PHY — USB 2.0 Hub (4 Port) — USB Host
- QSEVEN PCB Edge Connector (230 Pin)

Cyclone V SX SoC FPGA

FPGA:
- EPCQ Flash* — AS Interface — Active Serial
- QSPI Flash (16MB)
- FPGA AS Header*
- FPGA JTAG* — JTAG — JTAG
- DDR3 Controller (Soft IP) — DDR3 (16bit) — DDR3 RAM (256MB)
- High Speed Transceiver: CH0 CH1 CH2 CH3 — PCIe HardIP — PCIe x 4 Port; CH5 CH6 — SATA SoftIP — SATA x 1 Port
- 80 Pin Expansion Connector
  - General Purpose Clock I/Ps (2 LVDS/2 SE)
  - General Purpose Clock O/Ps (1 LVDS/2 SE) — FPGA Dedicated Clock IOs (2.5V Differential / 2.5V Single Ended)
  - 9 TX LVDS Pairs/18 DE IOs
  - 11 RX LVDS Pairs/22 SE IOs — FPGA IOs (2.5V Differential / 2.5V Single Ended)
  - 5 Single Ended IOs
  - SMBUS/2 SE — SMBUS (Soft IP) 3.3V Single Ended
- AC97/I2S(Soft IP) 3.3V Single Ended — AC97/I2S x 1 Port
- FPGA IOs (3.3V Single Ended) — 8 Single Ended IOs/LPC Interface; PWM
- LCD (Soft IP) 2.5V Differential — LVDS LCD (24bpp) x 2 Port

* Optional
 # On-SOM Micro SD Connector and Qseven Edge SD/MMC are sharing the same interface

OS Support

WEC7
Linux

Deliverables

Cyclone V SoC Qseven Module
Board Support Package
User Manual

Optional Kits

RainboW-G7D-Q7
(Generic Qseven Development Kit)

Custom Development

BSP Development/OS Porting
Custom RTL Logic Development
Custom SOM/Carrier Development
Custom Application/GUI Development
Design Review and Support

iWave Systems Technologies, established in 1999, focuses on Product Engineering Services involving Embedded Hardware, Software & FPGA. The company designs and develops cutting edge products and solutions. iWave has been an innovator in the development of highly integrated, high performance, low power and low cost System On Modules and Development Platforms. iWave's expertise has brought out multiple SOMs based on ARM, Freescale, Altera, Intel Atom, Marvell and TI Processors.

iWave Systems has won the confidence of its customers over the years by being a reliable partner in developing innovative products. Our engineers combine outstanding System design experience to deliver Quality Solutions. iWave specializes across Industrial, Automotive and Medical domains. We support our customers by being time efficient, which in turn helps our customers accelerate time to market their products. iWave is a Windows embedded Silver partner and a winner of the Partner Excellence Award.

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*Optional items not included in the standard deliverables

Ordering the Cyclone V SoC Qseven SOM
The board can be ordered online from the iWave Website
http://www.iwavesystems.com/webforms

IW-G17M-Q7-8R-R1.0